Digital Predistortion (DPD) Algorithm For 5G Applications

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Abstract

The wireless networks of upcoming fifth generation (5G) promises connection speeds and data rates that are one hundred times faster than the existing networks and much improved signal and connection quality. As there is the development of wireless communication systems, the requirement of Power Amplifier's linearity is hard. The Radio Frequency (RF) power amplifiers that are operating with wideband signals such as WCDMA that is used in UMTS leads to the generation of out-of-band emissions which are referred as "Spectral regrowth". To improve PA efficiency and linearity, this paper uses Digital Predistortion technique. This paper of DPD in combination with power amplifier using Memory Polynomial Algorithm is designed in the MATLAB/SIMULINK. The designed algorithm was tested with against various test cases and it was observed with high non-linearity and the good performance is seen for the order of 4 and 5 of the memory polynomial and non-linearity coefficients having linear output. Hence by using Memory Polynomial DPD in this paper the output of the previous input and present input is obtained. The advantage of DPD is having a linear power amplifier with less distortion and high non-linearity.

Full Text

Due to technical limitations, full-text HTML conversion of this manuscript could not be completed. However, the manuscript can be downloaded and accessed as a PDF.

Figures

Figure 1

Generic Predistortion Scheme

Figure 2

Block diagram of Power Amplifier

(b) Subsystem model of Bandlimited Source

(c) Subsystem model of PA reference

Figure 3

(a) illustrates the main Simulink Power Amplifier model which have the two subsystem models Bandlimited Source and PA reference model fig (b) refers to the bandlimited sources model and fig (c) refers to the PA reference model.

Figure 4

(a) Simulation result of Power Amplifier with Saleh Model (b) Simulation result of Power Amplifier with Rapp Model (c) Simulation result of Power Amplifier with Ghorbani Model

Figure 5

Basic block diagram of Digital Predistortion (DPD)

Figure 6

Simulink model of Digital Predistortion

Figure 7

Predistortion by Indirect Learning Architecture

Figure 8

Simulink Model of Adaptive Digital Predistortion

Figure 9

(a) Simulink model of Memory Polynomial DPD (b) Subsystem model of Delay tapped lines of fig (a)

Figure 10

(a) Simulink subsystem model of Dpd_Coef from fig 8 (b) Simulink subsystem model of dpd_compute from 10(a) (estimation algorithm model)

Figure 11

Simulation result of Power Amplifier With DPD

Figure 12

Simulation result of Real and Imaginary coefficients of DPD