A Fresh Design of Power Effective Adapted Vedic Multiplier for Modern Digital Signal Processors

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Abstract

The Multiply Accumulate (MAC) unit constructed using antiquated Vedic mathematical practice and the efficiency of the vertical and transversely of Vedic approach for multiplication, which gives a distinction in genuine cycle of Multiplier itself. Vedic-Mathematics is depend on 16-Sutras, in that Urdhva-Triyakbhyam (UT) more productive one. It literally means vertical and cross wise operations. It eliminates unwanted multiplication and allows the parallel creation of partial products and addition steps. The adders are utilized to append the partial-product generated in the Vedic mathematics methodology to drops the combinational lag. MAC is an essential unit in the digital signal processors, to show the characters like speed, power as well as area. Hence, finer multiplier plans are to increase the order of the system. The Modified sum product algorithm based Vedic multiplier is one such promising solution. It has a rapid multiplication process and reaches a less calculation complexity above its traditional multiplier. Array multiplier, Baugh-Wooley multiplier, Wallace-tree multiplier and Vedic multiplier were created in the existing work. In proposed work Vedic multiplier, using modified sum product algorithm was designed. The structure design coded in verilog and parameter analysis was done in Xilinx. The parameters like delay as well as power were compare between existing and proposed. When comparing with different multiplier with our proposed work delay get reduced. Comparing with existing multiplier the proposed 4x4 Vedic multiplier have 49.12% reduction in delay. Comparing with existing multiplier the proposed Vedic 4x4 multiplier have 42.51% reduction in power.

Introduction

VLSI implies that Very Large Scale Integration, is the way of engendering an IC that is Integrated Circuit by which blending a great many semiconductors into a solo chip [1]. It is used in PC for microprocessor, digital camera and an electronic circuit which might consists of a CPU refers to Control processing Unit, ROM indicated as Read Only memory, RAM indicated as Random Access Memory, and other glue logic. VLSI lets IC designers add all of these into one single chip [2].

VLSI has been fully surrounded for the lifetime, but which has side consequences of approach in the world of computers, there has been a substantial proliferation of implemented that can be used to sketch the VLSI circuits. Moore's law certifies that the quantity of semiconductors created in a chip is multiplied. By considering this, the capacity of an IC increased, with regard to computation power, usage of accessible area with yield. The focal point of VLSI is to diminish region, force and speed up the performance [3]. The following are the parameter considered while dealing with VLSI circuit. Delay in VLSI is time trigger on any pin or net of interest and change in signal level of the same or other pin. For example for delay, once there is change in input pin the period needed by the cell to swap the signal level of output pin which is called ads cell delay and the time taken by the signal on the net to trade from low to high or vice-versa is known as net delay [4]. Delay calculation is done by taking of the gate delay of a unique logic gate moreover the wires added to it. While taking the static timing it evaluated the delays of whole paths.

This is the another parameter of VLSI which has managed the high performed frequency because that has increased in utilization of power including two issues, the first is devices drain batteries faster and the second is heat dissipation rises. The need for design of low power is for battery lifetime and reliability [5-7]. There are different of power among that static power consumed even when chip is quiescent. In Digital Signal Processor (DSP), the Multiplier is one of the basic functional unit and electronics circuit.

The goals of multiplier are High speed along with low power utilization. In common, multiplier use “add and shift” algorithm [8]. In digital multiplier there are special types of multiplier namely Array multiplier, Baugh-Wooley Multiplier, Booth multiplier, Wallace-tree multiplier, Dadda multiplier, and Vedic Multiplier. The primary method used to layout the typical multiplication algorithm such as Array Techniques, Booth's Technique, Shift & Add Techniques and many more techniques. The existing method shows a novel methodology in wherein multiplier segment is executing by use of antiquated Vedic Mathematics [9]. Vedic Multiplier is one of the traditional and ancient one that focus on being fast and low power. The effective elementary activity in arithmetic processes is Multiplication. A portion of the persistently utilized Computation- Intensive Arithmetic Functions (CIAF) are Multiplication-based activities together with Multiply Accumulate (MAC), and inner product. These are at present utilized in various Digital signal Processing (DSP) utilizations like Fast Fourier Transform (FFT), filtering, convolution, and microprocessors in its ALU module. Therefore, clearly, there is a requirement for a high performance multiplier. At present, the order of revolution flow in a DSP chip determination is subject on multiplication time, which is immobile, the controlling. Due to expanding of computer and signal processing utilization, the attention of excessive speed processing has been expanding gigantically. Design of regular and simple structure that multiplier should have increase speed, reduce area and reduce power [10].

The multipliers are mainly correlated with respect to delay. In real-time signal along with image processing applications, the computation performance is the principle to achieve the desired execution [11]. Among that, this is one of the good keys of arithmetic operations is multiplication along with the improvement of a high performance multiplier. Optimizing the power and delay are vital part for numerous implementations [12]. This work introduces different multiplier architectures. The Vedic multiplication is derived from 16-Vedic sutras. This sutra tells about natural ways of solving mathematical problem. The Urdhva-Triyakbhyam sutra is more efficient and relevant to all cases, among these 16 Vedic Sutras [13]. It means vertically along with crosswise. Partial product are produced concurrently which itself lower the delay and produced this method rapid.

Figure 1.1 shows that multiplication method for Vedic multiplier. Examine the number A and B whereas A=a2.a1.a0 as well as B=b2.b1.b0. Result of multiplication = c4s4s3s2s1s0.

In continuation of the paper, existing system is discussed in section 2, followed by in section 3 is about the proposed system, section 4 is about the result as well as discussion, and finally section 5 is about the conclusion of the work carried in this paper.

Existing Design Structures

In the case of an existing system, they have compared various types of multiplier like Wallace multiplier, Baugh Wooley multiplier, and Array multiplier. In addition, for reducing power they have used the Power gating technique and gate-level optimization technique and coding in VHDL. Moreover, by using these three multiplier areas, power and speed are simulated by using the software modelsim6.5e and in Xilinx ISE and finally, the values are analysed.

2.1 ARRAY MULTIPLIER

Array multiplier is the conventional design. It is suitable for VLSI appliance because it has a high level of solidarity. It is applied for the amplification of two numerical digits by an arrangement of both half adders and full adders. In the place of production of partial products involves AND of multiplier and multiplicands bit. Parallel array multiplier is extensively to get high-performance speed, and consumes high power.

The multiplication involves an input wave, a central wave, and an output wave. The RTL schematic for the array multiplier is given in Fig 2.1 and schematic diagram of Array multiplier is given in Fig 2.2. Here multiplier, there are two binary digits, simultaneously X, Y is a, b bits. Figure 2.3 structure of array multiplier in that way we are taking two four- bit number and multiply with multiplicand.

2.2 WALLACE TREE MULTIPLIER

Using a variant of long multiplication method, the two numbers are multiplied by three-stage procedure. The bit amount is developed by the 2 × 2 bit matrices. Estimation of bit products equal to the estimation of row. The row summed by a faster adder and final output generated by a ripple carry adder. Figure 2.4 RTL schematic for Wallace tree multiplier. Figure 2.5 shows a diagram of the Variant of the long multiplication multiplier. The three stages of operations. 1) By multiplying the multiplier and multiplicand, product is developed bit by bit. 2) Grouping up the partial products. 3) Final output generated by using adders [14]. The developed area's last product is summed up, it takes less time, and the speed of the multiplier is greater. Figure 2.6 shows the structure of the Wallace tree multiplier in that first stage is responsible to develop the partial products. In the second stage, partial products are grouped. Then in the last stage generated area products are added together.

2.3 BAUGH WOOLEY MULTIPLIER

In the two's complement high-performance multiplier, the opposing sign transfers to the final [15]. Figure 2.7 shows the RTL schematic for 2's complements high-performance multiplier.

The schematic diagram of the Baugh Wooley multiplier shown in Fig.2.8 and the Baugh Wooley multiplier structure given in Fig.2.9. In first stage, excluding the highest significant bit other than all partial product rows are inverted. In the second stage, one can be added to the Mth column; in the third stage, most significant it is reversed.

2.4 LOW POWER DESIGN TECHNIQUES

Power gating techniques applied in IC, to reduce the power by terminating the current block. Gate level optimization techniques carries three types that is logic resizing, transition rate buffering and pin swapping. For optimizing the slew rate and leakage as well as dynamic current logic rescaling approach is used [16]. Accurate switching which leads to a correct sizing process. In transition rate buffering thin out dynamic power by shifting the time delay. Pin swapping is a kind of shifting technique and taken place on lower load values.

By comparing the above-mentioned multiplier, the output parameters were verified. Number of gates used and total power were given more attention. Power consumption and delay value are decreased.

2.5 LIMITATION

By comparing the different kind of multiplier, the power consumption of array multiplier was high when compared to other multiplier. Gate count and adder count are high when compare to other multiplier so it occupy more area in array multiplier. In Baugh Wooley multiplier the operation speed is very much high when compared to array multiplier but delay and power consumption are very less [17-20]. Whereas in Wallace multiplier speed is high and power consumption is high when compared to Baugh Wooley multiplier. Delay is little bit increased.

Proposed Design Structure

The overview of our proposed idea is to reduce power and delay for Vedic multiplier by using Modified sum product algorithm and code in Verilog. In addition, that are implemented in Xilinx. Finally, delay and power are compared to the existing one.

3.1 4X4 VEDIC MULTIPLIER

In the projected work, MAC unit is one of the key processes widely used in DSP application modules. Multiplier is the vital module of Modified sum product algorithm [21]. It dispenses with undesirable multiplication steps, follows a quick multiplication procedure, and accomplishes an altogether less calculation unpredictability over its conservative equivalent [22]. The Vedic multiplier uses top down approach, where more modest squares can be utilized to plan greater one. Antique Indian method of computing mathematical operations are the core of Vedic mathematics as well as Vedic multipliers [23]. The projected work is given in the Fig.3.1. This work was simulated in Xilinx and compared all the parameters.

3.2 VEDIC MULTIPLIER BASED ON MODIFIED SUM PRODUCT ALGORITHM

In this figure 3.2 shows that pictorial representation of the multiplier. In first step, we have to multiplier the A0 and B0 that will store in S0. Then in second step, we have cross multiply A0.B1 and A1.B0 that will added and stored in C0S0. Then third stage we have multiplier A1.B1 and add C0 that will stored in COUT S2.

3.3 CALCULATION DETAILS

Figure 3.3 shows that example calculation of proposed work in that step one we have to vertically multiply 2 and 5 we get result as 10 and pre carry is zero. In second step, we have cross multiply 1 and 5, 1, and 2 then add the multiplied value is 7 then the precarry generated from the first step is 1 the result is 8. The final step is vertically multiply 1 and 1 value is 1 precarry from previous step is 0 the result is 1. The result we have to take last bit of each stage and write it together. Figure 4.4 RTL schematic for projected multiplier.

The projected 4x4 Vedic multiplier is shown in Fig 3.6. In that four Vedic 2x2 multiplier (Figure 3.5) used and last stage, we have to add result by using adder. Input data (a, b) sent to the 4x4 multiplier we get output in p. The result was verified by the simulation output. The parameters are comparing with existing system.

Results And Discussion

In Xilinx ISE (Integrated Software Environment), design suite that allows taking design plan entry between Xilinx programming devices. In that control and operations of design done by design entry, synthesis, implementation, verification [24]. In design entry, we can generate source files based on objectives and create top – level module file using HDL such as Verilog, VHDL or using schematic. After design entry, synthesis can run during this Verilog design input given for implementation [25]. Next to run the implementation that convert the Verilog code into the report format. During simulation input are given to the respect port and get the simulated output. After the design is successfully defined, perform behavioural simulation, run implementation with the Xilinx implementation tools.

The overview of simulation result shows that the output for array multiplier, Wallace multiplier, Baugh Wooley multiplier and proposed 4x4 Vedic multiplier and its output are taken from Xilinx. The different types of input are given to the values and the correct outputs are taken.

4.1 EXISTING ARRAY MULTIPLIER

The conventional array multiplier’s simulation output is given in Fig 4.1. Here, for example, the input a, b given 0000, 0101 and it produces an output of p as 00000000.

4.2 EXISTING WALLACE TREE MULTIPLIER

Fig 4.2 shows that simulation output of existing Wallace tree multiplier. Here, for example, the input a, b given 0101, 0100 and it produces an output of p as 00010100.

4.3 EXISTING BAUGH WOOLEY MULTIPLIER

Figure 4.3 shows that simulation output of existing Baugh Wooley multiplier. Here, for example, the input a, b given 0111, 0011 and it produces an output of p as 00010101.

4.4 EXISTING 4x4VEDIC MULTIPLIER

Figure 4.4 shows that simulation output of existing Vedic multiplier. Here, for example, the input a, b given 1000, 1000 and it produces an output of p as 01000000.

4.5 PROPOSED 4x4 VEDIC MULTIPLIER

Figure 4.5 shows that simulation output of proposed Vedic multiplier. Here, for example, the input a, b given 1000, 0010 and it produces an output of p as 00001000.

4.6 DELAY ANALYSIS

Table 4.1 Delay analysis of 2x2 Vedic multiplier and 4x4 Vedic multiplier

DESIGN	DELAY (ns)
EXISTING (2x2)	7.858
PROPOSED (2x2)	6.376
EXISTING (4x4)	15.378
PROPOSED (4x4)	7.824

Table 4.1 shows the delay of existing multiplier and proposed Vedic multiplier. From this delay has been analysed with existing and proposed circuit.

4.7 POWER ANALYSIS

Table 4.2 Power analysis of 2x2 multiplier and 4x4 Vedic multiplier

DESIGN	POWER (mW)
EXISTING (2x2)	195.43
PROPOSED (2x2)	81.53
EXISTING (4x4)	339.98
PROPOSED (4x4)	195.43

Table 4.2 shows the power of existing multiplier and proposed Vedic multiplier. From this power has been analysed with existing and proposed circuit.

From this the result are taken for both existing and proposed multiplier and outputs are taken. From the analysis of delay, the execution time was decreased when compared to the existing system. From the analysis the delay get reduced 49.12 % when compare to existing system. From the analysis the power get reduced 42.51 %when compare to existing system.

Conclusion

A 4bit MAC unit make use of Vedic multiplier with modified sum product algorithm was constructed. It was formed on Urdhva-Triyakbhyam technique which is programmed using HDL and the synthesis was supported by Xilinx. It was noticed to possess that power get reduced along with optimization in circuit delay and area. The MAC module established with the projected multiplier can be utilized in DSP application for better performance. Thus, the delay of advised Vedic multiplier is lesser while using modified sum product algorithm when compare to existing Vedic multiplier. When comparing with different multiplier with our proposed work delay get reduced. Comparing with existing multiplier the proposed 4x4 Vedic multiplier have 49.12 %reduction in delay. Comparing with existing multiplier the proposed Vedic 4x4 multiplier have 42.51 % reduction in power.

Declarations

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Conflicts of interest/Competing interests

The authors whose names are listed immediately certify that they have NO affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript.

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References

[1] Kashik, Vikas, and Himanshi Saini. "A Review on Comparative Performance Analysis of Different Digital Multipliers." Advances in Computational Sciences and Technology 10.5 (2017): 1257-1272.

[2] Bhattacharjee, Abhishek, and Anindya Sen. "Compare efficiency of different multipliers using Verilog simulation & modify an efficient multiplier." Int J Latest Technol in EngManag Appl Sci (IJLTEMAS) 6.3 (2017).

[3] Patel, Sujit Kumar, and Subodh Kumar Singhal. "Area–delay and energy efficient multi-operand binary tree adder." IET Circuits, Devices & Systems 14.5 (2020): 586-593.

[4] Sakellariou, Panagiotis, and Vassilis Paliouras. "Application-specific low-power multipliers." IEEE Transactions on Computers 65.10 (2016): 2973-2985.

[5] Jaya, Eppili, and K. Rao. "Power, area and delay comparision of different multipliers." Int.J. Sci. Eng. Technol. Res 5.6 (2016): 2093-2100.

[6] Wairya, Subodh, Rajendra Kumar Nagaria, and Sudarshan Tiwari. "Performance analysis of high speed hybrid CMOS full adder circuits for low voltage VLSI design." VLSI Design 2012.

[7] Akhter, Shamim, and Saurabh Chaturvedi. "Modified binary multiplier circuit based on Vedic mathematics." 2019 6th International Conference on Signal Processing and Integrated Networks (SPIN). IEEE, 2019.

[8] Eshack, Ansiya, and S. Krishnakumar. "Implementation of Pipelined Low Power Vedic Multiplier." 2018 2nd International Conference on Trends in Electronics and Informatics (ICOEI). IEEE, 2018 .

[9] Hanuman, C. R. S., and J. Kamala. "Hardware implementation of 24-bit vedic multiplier in 32-bit floating-point divider." 2018 4th International Conference on Electrical, Electronics and System Engineering (ICEESE). IEEE, 2018.

[10] Dalmia, Preyesh, et al. "Novel high speed vedic multiplier proposal incorporating adder based on quaternary signed digit number system." 2018 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID). IEEE, 2018.

[11] Deshmukh, Prashant R., and Jitendra S. Edle. "Development of Concurrent Architecture of Vedic Multiplier." 2018 Fourth International Conference on Computing Communication Control and Automation (ICCUBEA). IEEE, 2018.

[12] Ram, G. Challa, et al. "VLSI architecture for delay efficient 32-bit multiplier using vedic mathematic sutras." 2016 IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT). IEEE, 2016.

[13] Liu, Weiqiang, et al. "Design and analysis of approximate redundant binary multipliers." IEEE Transactions on Computers 68.6 (2018): 804-819.

[14] Patel, Sujit Kumar, and Subodh Kumar Singhal. "Area–delay and energy efficient multi-operand binary tree adder." IET Circuits, Devices & Systems 14.5 (2020): 586-593.

[15] Perri, Stefania, et al. "Parallel architecture of power-of-two multipliers for FPGAs." IET Circuits, Devices & Systems 14.3 (2020): 381-389.

[16] Hussain, Inamul, and Saurabh Chaudhury. "Fast and High-Performing 1-Bit Full Adder Circuit Based on Input Switching Activity Patterns and Gate Diffusion Input Technique." Circuits, Systems, and Signal Processing (2020): 1-26.

[17] Petrović, Predrag Bosko. "New current-mode RMS-to-DC converters and four-quadrant multiplier/divider based on VDTA." IET Circuits, Devices & Systems (2020).

[18] Bandi, Vijaya Lakshmi, Prathima Gamini, and Balla Sai Harshith. "Performance Analysis of Dadda Multiplier Using Modified Full Adder." International journal of innovative research in computer and communication engineering 6.2.

[19] Kadu, Rakesh K., and Dattatraya S. Adane. "A Novel Efficient Hardware Implementation of Elliptic Curve Cryptography Scalar Multiplication using Vedic Multiplier." International Journal of Simulation–Systems, Science & Technology 19.6 (2018).

[20] Abdul-Hadi, Alaa Mohammed, and Firas Ghanim Tawfeeq. "Performance Evaluation of Scalar Multiplication in Elliptic Curve Cryptography Implementation using Different Multipliers Over Binary Field GF (2233)." Journal of Engineering 26.9 (2020): 45-64.

[21] Kadu, Rakesh K., and Dattatraya S. Adane. "Hardware Implementation of Efficient Elliptic Curve Scalar Multiplication using Vedic Multiplier." International Journal of Communication Networks and Information Security 11.2 (2019): 270-277.

[22] Sebastian, Alen, et al. "Design and Implementation of an Efficient Dadda Multiplier Using Novel Compressors and Fast Adder." 2020 International Symposium on Devices, Circuits and Systems (ISDCS). IEEE, 2020.

[23] Vamsi, Akella Srinivasa Krishna, and S. R. Ramesh. "An efficient design of 16 bit mac unit using vedic mathematics." 2019 International Conference on Communication and Signal Processing (ICCSP). IEEE, 2019.

[24] Eshack, Ansiya, and S. Krishnakumar. "Design of Low-Power Vedic Multipliers Using Pipelining Technology." Proceedings of the Third International Conference on Computational Intelligence and Informatics. Springer, Singapore, 2020.

[25] Krishna, Aki Vamsi, S. Deepthi, and M. Nirmala Devi. "Design of 32—Bit MAC Unit Using Vedic Multiplier and XOR Logic." Proceedings of International Conference on Recent Trends in Machine Learning, IoT, Smart Cities and Applications. Springer, Singapore, 2021.

Figures

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Figure 1

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