High resolution mutated dynamic precision power gated comparator for 9-bit SAR ADC

T. Thamaraimanalan (t.thamaraimanalan@gmail.com)
Sri Eshwar College of Engineering

C. Venkatesan
HKBK College of Engineering

Research Article

Keywords: Analog to Digital converter (ADC), Precision Comparator, Successive Approximation Register (SAR), Low Power, High Resolution

Posted Date: August 23rd, 2022

DOI: https://doi.org/10.21203/rs.3.rs-1961847/v1

High resolution mutated dynamic precision power gated comparator for 9-bit SAR ADC

T.Thamaraimanalan[1], C.Venkatesan[2]

[1]Department of Electronics and Communication Engineering, Sri Eshwar College of Engineering, Coimbatore, Tamilnadu, India.

[2]Department of Electronics and Communication Engineering, HKBK College of Engineering, Bangalore, Karnataka, India.

Corresponding author: t.thamaraimanalan@gmail.com

Abstract

Comparator design is a major challenge during the implementation of high resolution SAR ADCs. In this research, a mutated dynamic power gated comparator is designed to achieve the SAR ADC with ultra-low power and enhanced gain. The proposed power gated comparator is designed using 45nm CMOS technology, and it is tested at 3.3V and 5V. High speed and low power are achieved through transistor sizing and power gating techniques. Mismatch of transistors, the offset value is appropriately calculated using the input resistance of the differential amplifier and trans conductance. Also, the offset cancellation and digital calibration techniques are included in the design to enhance the precision, and to improve the performance of ADCs. For the proposed comparator, phase margin, gain, ICMR, power consumption, offset voltage, slew rate, load capacitance, propagation delay, kickback noise, and settling time are compared with the conventional comparator. The proposed design consumes only 4.2mW while operating at 5V and 1.5mW when the input voltage is 3.3V. The effective resolution of the SAR ADC is observed as 8.2 bit with the proposed power gated comparator.

Keywords: Analog to Digital converter (ADC), Precision Comparator, Successive Approximation Register (SAR), Low Power, High Resolution.

1. INTRODUCTION

The advancement of Integrated Circuits (ICs) is due to the advancement in CMOS technology. As a result, digital signal processing simulations will become more popular. Analog-to-digital converters (ADCs) are standard devices in all ICs that convert an analog signal to a digital signal. The few common ADC types are, flash ADC, SAR ADC, delta-sigma ADC, dual-slope ADC, and pipeline ADC. In operational amplifier architecture, the SAR ADC has a power efficiency benefit over conventional ADC architectures. SAR ADCs are extensively used and account for a distinct set of benefits like the power consumption is lower, with rising resolution and time delay in the conditions of output data, and smaller in size as a major benefit. DAC, comparator, preamplifier circuit, decision circuit are the vital components in SAR ADCs. In terms of clock control, MSB to LSB, the converter finishes the conversion using the successive comparison conditions. However, in the case of SAR logic control, DAC output signal and sampling signals are assessed by a comparator, generating the result as feedback to DAC. The performance specifications for the comparator are managed by the offset voltage, speed, resolution, kickback noise, power consumption, and resolution, towards a crucial impact for the complete ADC functionality [1,2].

Comparators are broadly classified into two groups such as static and dynamic comparators. Static comparators are amplifier-based comparators and dynamic comparators are comparators clock-based comparators. Because of their rapid turning speed and zero static power dissipation, dynamic comparators are commonly preferred over static comparators. Dynamic comparators, on the other hand, have a larger voltage offset and kickback noise, which limits SAR ADC resolution. The comparator is the most power-hungry part of the ADC. As a result, the ADC's power usage must be reduced. As a result, a precise and accurate comparator is essential for a good amplifier [3]. Always there exists a tradeoff between size and speed in CMOS devices. Large size transistors are used to increase the speed of the comparator and to balance the drop of supply voltage, but it requires more power and area [4,5].

In this research work, a mutated dynamic comparator is designed to achieve high resolution of SAR ADC with low power consumption. To obtain a large speed at low power, a different ratio in transistor sizing is used, which leads to a mismatch of transistors and the offset value would be higher than the requisite gaps. The offset cancellation and digital calibration techniques are essential in offering the offset, and towards enhancing the precision and improving the performance conditions for ADCs. Low power can be achieved through the power gating technique and leakage power has also been reduced. The transconductance of the device is reduced by changing the transistor size during its fabrication [6].

This paper describes a mutated dynamic comparator architecture that achieves excellent resolution while consuming minimum power. As a result, the comparator can be used in a SAR ADC with 9-bit synchronisation. The rest of this paper is laid out as follows. Section 2 describes the comparator's and SAR ADC's related work. The comparator's design configuration for SAR ADC is described in Section 3. The proposed comparator and other SAR ADC building components are presented in Section 4. The simulation results and description of the proposed precision comparator design are presented in Section 5. The research work is concluded in Section 6.

2. LITERATURE WORK

Design and implementation of a low-power 1V, 77.26μW 6-bit SAR ADC in Cadence 90nm CMOS process for biomedical application is depicted in [7]. The proposed comparator consumes low power with the medium speed in the SAR ADCs. ADC with a 6-bit resolution is developed with the help of a sample-and-hold (S/H) circuit, analog comparator, and 6-bit SAR logic unit. According to the simulation results, the circuit consumes 77.26W at sampling frequencies up to 1MHz. The SQNR is 37.34 dB and the ENOB is 5.91 dB when the offset voltage is zero [8].

A low-power 10-bit SAR ADC with variable threshold technique for biomedical applications is introduced in [9]. The ADC described in this work uses two low-power design strategies by set and reset phase. A two-way switch on a single side scaling for switching the digital-to-analog converter (DAC) is used. A transmission gate is involved for reducing the leakage power. The comparator's delay time is significantly reduced by cascading amplifiers.

A hybrid comparator for high-resolution SAR ADC is discussed in [10, 21]. A 14-bit SAR ADC employing two dynamic comparators is proposed. Low-power comparators use

automatic noise reduction techniques to make good decisions about LSBs. This SAR conversion for two-speed monotonic design and differential threshold voltage is introduced. At the transistor level, 40nm CMOS technology is used for partial implementation and simulation. ADC uses the sampling operation and the frequency is 1.6 MS/s, with an SNDR of 81 dB and SFDR of 97 dB.

An 11-bit single-ended SAR ADC with an inverter-based comparator for design automation is proposed in [11]. From an analog-to-digital converter, this research presents a low-power single-ended SAR ADC in which the analog active circuit comparator is replaced with a digital circuit based on inverters. Voltage fluctuation at the inverters is unaffected by the ADC offset since the SAR ADC only has one comparator. Leakage current is reduced as the threshold voltage is applied using the set and reset method.

Low power and low noise edge race comparator for SAR ADCs are designed in [12, 17]. This article proposes a comparator is called edge race comparator (ERC). Differential clamping is accomplished by generating two propagating edges. The distance between two inverter loops is measured at both sides and the two edges come into contact with each other. The proposed comparator produces less noise, low power and does not necessitate a high voltage. Noise, energy consumption, delays that vary with the input voltage are cost-effective methods. The measurement results from an ADC designed in a conventional 40-nm CMOS process reveal that the comparator energy at the LSB is decreased by 7.5 times, and the ADC sampling rate is enhanced by 3.85 times.

The design of low power and improved T latch comparator for SAR ADC is described in [13]. Dynamic comparator architecture is designed with latch type voltage sense amplifier (SA) comparator, for evaluation. As a result, this research proposes a novel modified latch-type voltage SA comparator with lower delay, power consumption, and a short delay. In a 0.18 m CMOS process, the suggested dynamic comparator is built and simulated. At a 1.5 V power supply and 200 MHz clock frequency, simulation findings reveal that it only consumes 138 pW.

A two-step ADC with a continuous-time SAR is proposed in [14, 15]. In the research, a two-step dynamic comparator is designed. The first step involves the dynamic-differential-pair (DDP) method, the second step uses CMOS capacitors and Dynamic Source Follower (DSF). The performance of the device is improved with an increase in leakage power.

Inverting amplifier-based ultra-low power low offset current comparator is discussed in [16,20]. In this proposed method an identical inverting amplifier is introduced to produce the low-input offset current in a comparator. The power consumption is reduced by compromising the area of the design. Technology scaling curtails the output conductance, output voltage swing, so the DC gain decreases. Transistors are drafted with large sizes to increase the speed of the comparator. ICMR is crucial in the design of the comparator. The system-driven transistors techniques, supply boosting methods, and dual-oxide process advice is used for low supply designs. The cancellation of offsets, overdrive recovery, PSRR, and power consumption are the major challenges in comparator design. Because the decision of logic 0 and logic 1 should be switched fast for data converters. The comparator must be developed with high accuracy and provide a high slew rate and gain. [18,19].

3. COMPARATOR DESIGN CONFIGURATIONS FOR SAR ADC

Comparator is the analog part in the system, and often a restricting part in the plan of rapid information transformation frameworks due to constraints of precision, power consumption limitations, and correlation speed conditions. The sampled analog voltage could manage because of the positive terminal for comparator and DAC output, which could address in terms of the negative terminal for the comparator.

In the instances of signal emergence for DAC blocks being higher than that of the other input factors, the comparator delivers output in the form of logic 0 in the instances of being true, or logic 1 as standard. Comparative levels might vary depending on the conversion cycle level changes. There are two different configurations of comparators as single-ended architecture and differential configuration are designed.

Deployment of a comprehensive range of differential comparators is more effective than the deployment of single-ended architecture, in addressing the requirement of managing power supply rejections and disrupting the common mode noise characteristics. Profoundly, the differential comparator constitutes three blocks namely SR latch, differential input stage, and regenerative CMOS flip-flops as depicted in Figure 1.

The input stage is the differential stage, which is the composition of the M_1 and M_2 range of transistors. The input stage has the scope of the biasing stage, wherein current mirrors M_{13} and M_3 are composed. Here, the current mirror has been designed for maintaining the ratio of 1:2 in the case of M_{13} and M_3. CMOS flip-flop section comprises N-Channel and P-channel range of flip-flops, whereas M_4 and M_5 develop an N-Channel, M_6, and M_7 forming P-channel range. M_{12} conducts a setting switch, while the M_{10} and M_{11} function in the form of pre-charging transistors.

The architecture supports recharging the positive supply voltage level conditions, while the M_8 and M_9 are reliant for managing the N-Channel flip-flop and P Channel flip-flop in the instances of initial generation and the resetting phase. There are two non-overlapping clocks $\varphi 1$ and $\varphi 2$.

The operation of the comparators can classify into three key states in the form of resetting states, first regeneration state, and final regeneration state. In the instances of the setting State, clock CLK1 (φ_1) can be seen as higher, when it gets connected to the N-channel flip-flop towards managing the pre-charge conditions to the ground levels. In such intervals, the flow of current in the range of M_{12} turns to reset of earlier logic applications. Lowered range CLK2 (φ_2) connects at such instance to the pre-charging transistors to enable positive supply voltage levels from P and Q, which can define as P-channel flip-flops. During the conditions of resetting, N-Channel flip-flops have positioned at ground state, and P-channel flip-flop gets linked to the power supply that is positively termed as V_{dd} levels.

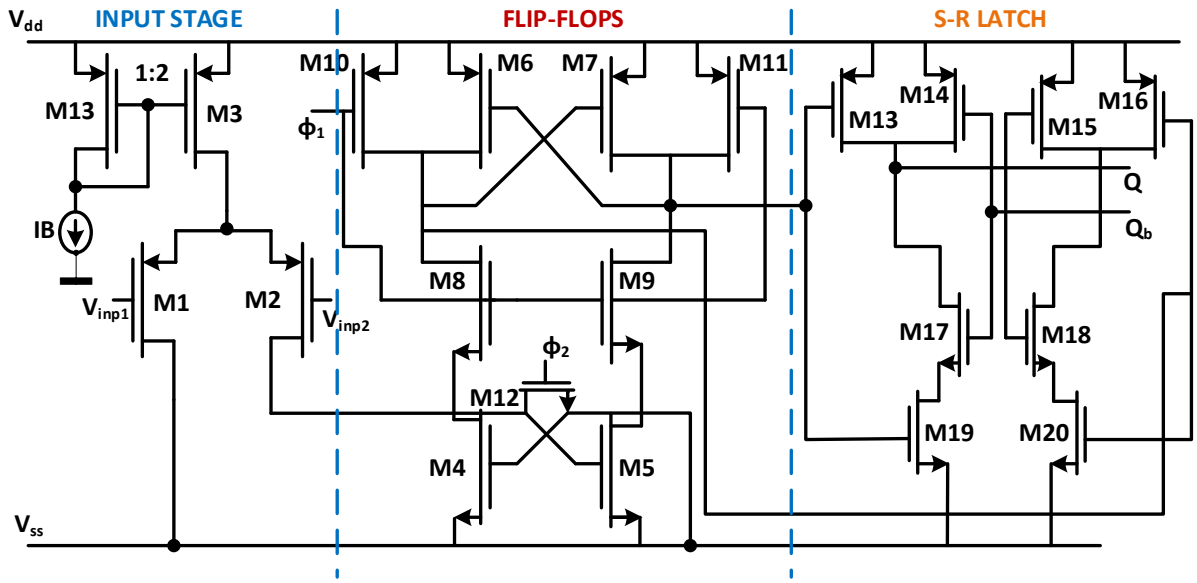

Figure 1: Schematic of fully differential comparator

Here, the initial level regeneration state takes place in the instance of CLKs reaching the higher logic levels and CLK1 attains the low logic levels. The phase of such a transition has 90°, termed as the first regeneration state; wherein there is a significant rise in the regeneration speed. It also supports reducing the conditions of the offset voltage. Because of the last regeneration state, the CLK2 becomes higher and it requires M_8 and M_9 for connecting to P-channel flip-flop and N-Channel flip-flop. Following SR latch, a state is driven over the comprehensive complimentary digital output levels across the last regenerative models, which rests in a similar stage of addressing the forthcoming resetting model for further stages of comparison as stated in Equation (1).

$$Offset\ voltage, V_{off} = V_{off1} + \left[\frac{gm_4}{gm_1}\right] V_{off2} \quad (1)$$

where,

$$V_{off1} = \text{ offset value of the input transistor pairs}$$

$$\left[\frac{gm_4}{gm_1}\right] V_{off2} = \text{offset value of the N} - \text{ channel flip} - \text{flop}$$

Transistor element ratios have been designed for managing the mobility property of PMOS, wherein the consideration is about designing the current partition, which is executed based on the smaller outputs for a small range of voltage conditions.

4. PROPOSED MUTATED DYNAMIC PRECISION POWER GATED COMPARATOR DESIGN

The proposed design is to achieve high response time with reduced power consumption. This circuit is a three-stage comparator based on pre-amplification to improve the performance. The proposed precision comparator circuit is shown in Figure 2. M_1 and M_2 transistors sizes will optimize by calculating the input resistance of the differential amplifier and trans conductance.

The conversion speed is increased by maintaining the channel length stable, but it causes unwanted offset voltage. Stage-1 gain is improved by changing the widths of M_3 and M_4 analogous to the M_2 and M_3 widths. Power gated transistors are introduced to reduce the static power consumption of the proposed comparator when the device is idle. Output currents of this stage for the applied input voltages are calculated using Equations (2) and (3).

$$i_{0+} = \frac{g_m}{2}(v_+ - v_-) + \frac{I_{ss}}{2} = I_{ss} - i_{0-} \tag{2}$$

$$g_m = g_{m1} = g_{m2} \tag{3}$$

Where,

$$i_{0+}\ and\ i_{0-} = output\ currents\ of\ stage\ 1$$

$$g_m = transconductance$$

$$v_+\ and\ v_- = input\ voltages$$

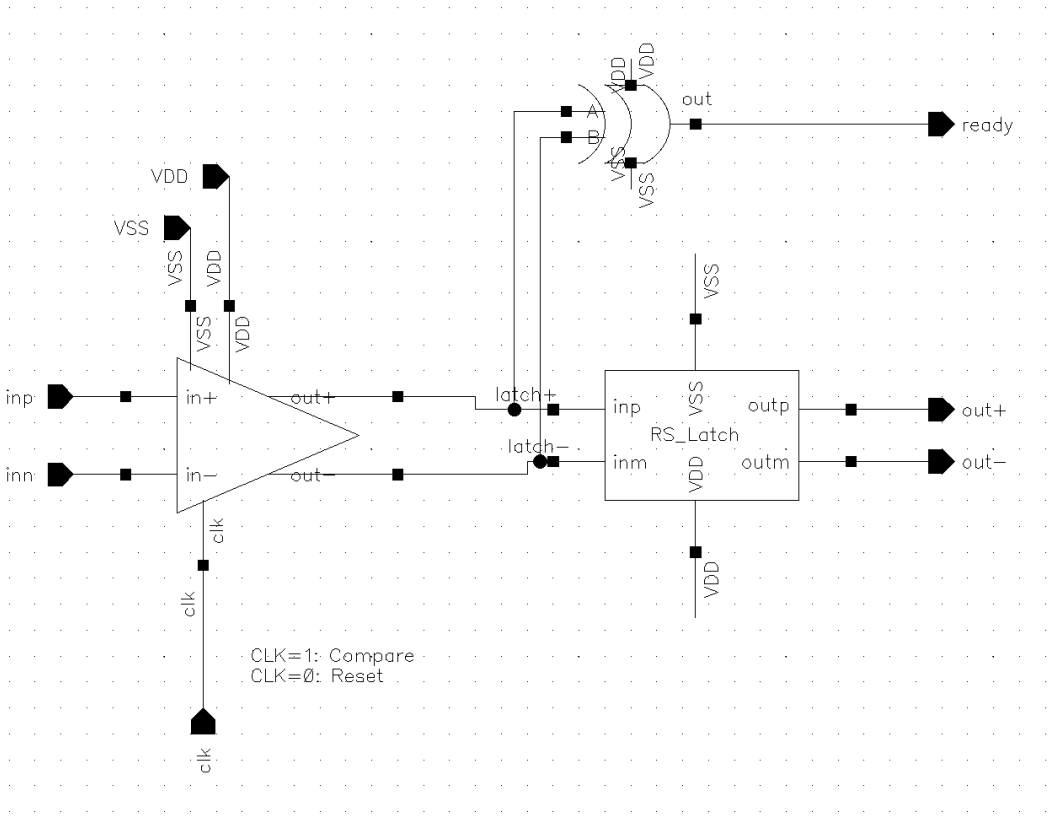

Figure 2: Proposed precision comparator design

Stage-1: The preamplifier stage, which is made with the transistors M_1 to M_6, is laid out in Figure 3. The two inputs voltages $v_+\ and\ v_-$ are applied to the input stage and the output currents $i_{0+}\ and\ i_{0-}$ are transferred to the next stage. M_1 and M_2 transistors have the same trans conductance, but when the input of the transistor varies, it produces two different currents.

The gain of the preamplifier is very small for a large increase of W/L as given below in Equation (4), (5), and (6).

$$|A_v| = \frac{g_{m1}}{g_{m3}} - \frac{g_{m2}}{g_{m4}} \tag{4}$$

$$F_{3db} = \frac{f_{GBW}}{|A_v|} \tag{5}$$

$$G_m = \sqrt{2k_p \left(\frac{W}{L}\right) I_D} \tag{6}$$

$$where, k_p = \frac{\mu_p C_{ox}}{2}$$

The main preamplifier design parameters are gain and bandwidth. To achieve higher gain W/L should be decreased, hence $|V_{GS} - V_{TP}|$ need to be increased and lower the common-mode voltage at the output nodes. M_5 and M_6 are included to improve current in M_1 and M_2 so that the gain increases at the square root of the difference of current in M_1 and M_2 given as in Equation (7).

$$A_v = \frac{g_{m1}}{g_{m2}} - \sqrt{1 + \frac{I_5}{I_3}} \tag{7}$$

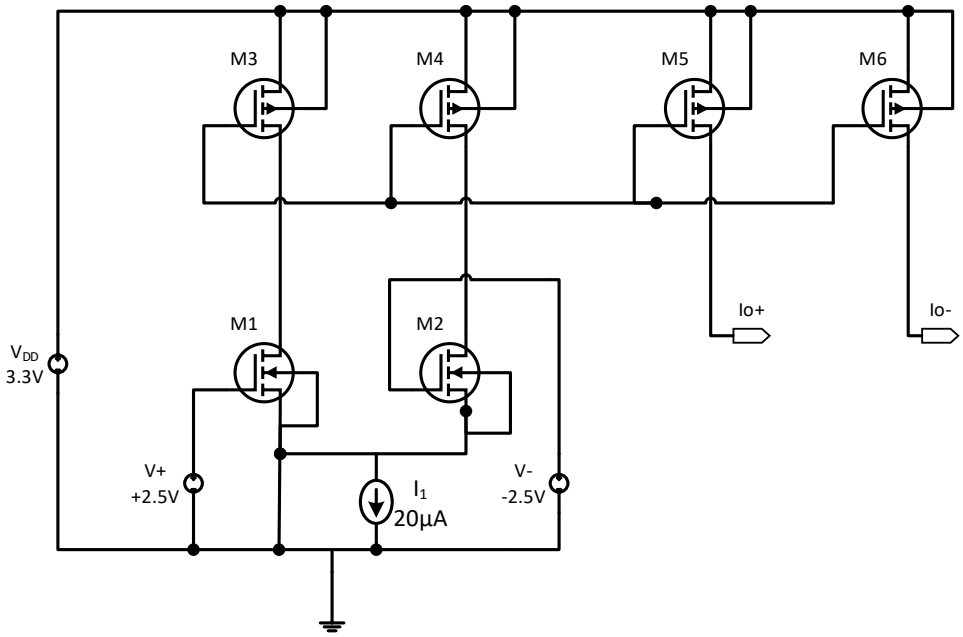

Figure 3: Preamplifier circuit of the proposed comparator

Stage-2: The transistors M_7-M_{10} and M_{19} form the decision circuit, as shown in Figure 4, which makes the decision. The decision of the output logic can be decided based on differentiating mV levels of output voltages V0+ and V0-. The gain in the circuit can be enhanced with positive feedback of M_8 and M_9, and noise on the signal has been removed by arrangement with hysteresis.

The preamplifier output is implemented to the decision circuit via M_5 and M_6 to provide isolation between the latch output and output of the preamplifier. A rapid change in yield of

latch could disseminate by the drain gate capacitance of M_1 and M_2, and it results in kickback noise.

Therefore $\Delta V_0 < V_{OH} - V_{OL}$

To curtail the propagation delay

i) The time required to reach $V_{OH} - V_{OL}$ can be decreased by utilizing a large input for a latch.

ii) Decrease the latch time constant.

Due to applying a reasonably large value ΔV_0 for rapid response. The propagation delay and latch time constant of the preamplifier are expressed using Equations (8) and (9) respectively.

The propagation delay is

$$t_p = Z_L ln \frac{V_{OH} - V_{OL}}{2\Delta V_0} \tag{8}$$

Where latch time constant

$$Z_L = 0.6 C_{ox} \sqrt{\frac{W L^3 I_D}{2K_p}} \tag{9}$$

When, $i_{0+} \gg i_{0-}$, causes $V_{GS} > V_{TH}$ of M_7 and M_9, hence the transistors M_7 and M_9 turned ON, since $V_{GS} < V_{TH}$ of M_{10} and M_8, pushes them in OFF state and it is shown using Equation (10), (11), and (12).

Assume that,

$$\beta_{m7} = \beta_{m10} = \beta_A \tag{10}$$

$$\beta_{m8} = \beta_{m9} = \beta_B \tag{11}$$

Under these conditions, $v_{o-} \approx 0V$ and v_{o+} is given by,

$$v_{o+} = \sqrt{\frac{2i_{0+}}{\beta_A}} + V_{THN} \tag{12}$$

When i_{0-} starts to increase and i_{0+} starts to decrease (i.e.,$i_{0-} \gg i_{0+}$), the switching occurs when $V_{DS}(M_8) = V_{TH}(M_9)$, M_7 covers the way to M_8 for the usage of the current, thus reducing the $V_{DS}(M_7)$ and as a result, M_9 turned off. Presuming the maximal value of v_{o+} or v_{o-} is equivalent to $2V_{THN}$, then M_8 and M_9 operate under steady-state circumstances, either in triode or cut-off regions.

Circumstantially, the voltage across M_9 gets to V_{THN}, and thus M_9 enters the saturation region, in the instance of current through M_9 as given in Equation 13.

$$i_{0-} = \frac{\beta_B}{2}(v_{o+} - v_{THN})^2 = \frac{\beta_B}{\beta_A} i_{0+} \tag{13}$$

The switching happens at the point wherein M_9 is off, and M_8 is on.

If $\beta_A = \beta_B$ and $i_{0-} = i_{0+}$ accordingly, switching recurs. Unequal βs cause the hysteresis of a comparator. The relation between $i_{0-}\ and\ i_{0+}$ is stated in Equation 14.

$$i_{0+} = \frac{\beta_B}{\beta_A} i_{0+} \tag{14}$$

The switching point voltages are given by Equation (15) and (16):

$$V_{SPH} = v_+ - v_- = \frac{I_{SS}\frac{\beta_B}{\beta_A} - 1}{g_m \frac{\beta_B}{\beta_A} - 1}\ for\ \beta_B \geq \beta_A \tag{15}$$

$$V_{SPL} = -V_{SPH} \tag{16}$$

Where, V_{SPL} = switching point low voltage and V_{SPH} = switching point high voltage.

Figure 4 represents the combination of both preamplifier and decision stages with transistors M_1 to M_{11}. The positive voltage is swept from 0V to 5V, and the reference voltage is set at 2.5 volts. Before 2.5V, the positive output voltage is at logic 0, and after 2.5V the positive output logic is at logic 1.

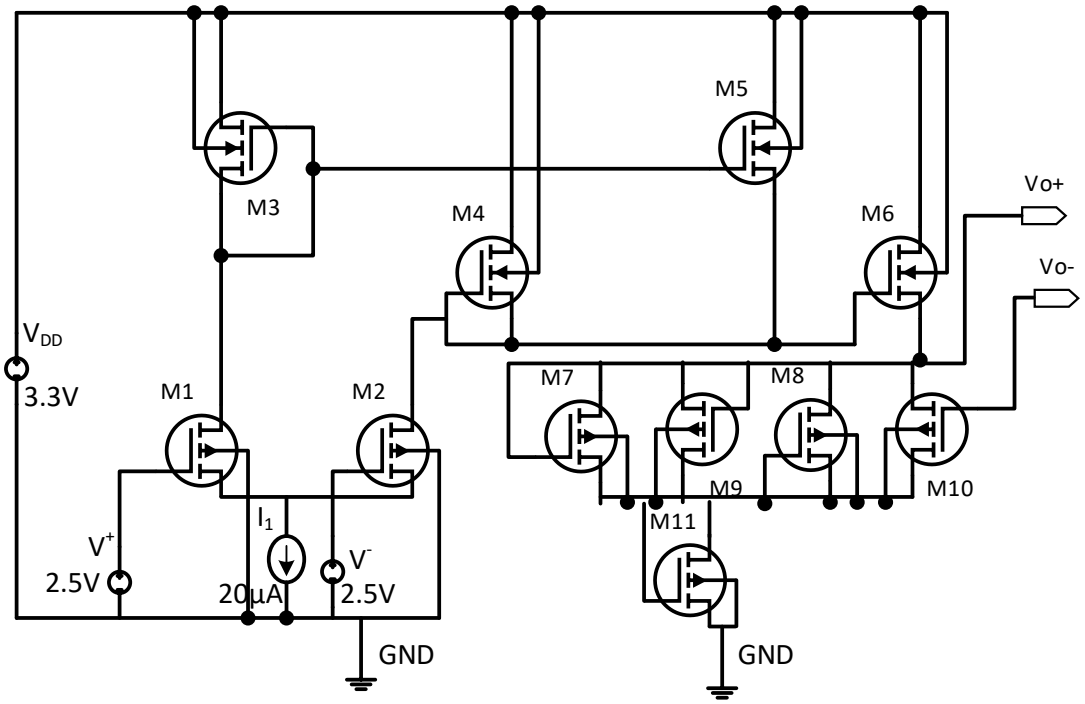

Figure 4: Preamplifier and decision circuit of the proposed circuit

Stage-3: Output buffer is the final stage of a comparator design. It acquires a differential signal from the decision circuit and converts it into a logic level (0V or 5V) without limitations of slew rate. The output buffer comprised of transistors M_{12} to M_{19} is shown in Figure 6. Transistor M_{11} is attached in sequence with decision circuits to raise the mean potential and to avoid the problem of interfacing the decision circuit to the output buffer. By adjusting the aspect ratio of

M_{11}, the decision circuit output can enhance by the amount of V_{THN}. Output buffer converts the output of DC into a logic value.

The overall comparator gain is computed by multiplying the gain of the preamplifier and the gain of the decision circuit. The gain of the inverter after the latch is not integral to overall gain, as the decision circuit starts full logic levels. Additional inverters are required to drive the capacitive load. Figure 5 represents the buffer stage of the complete 3.3V CMOS comparator.

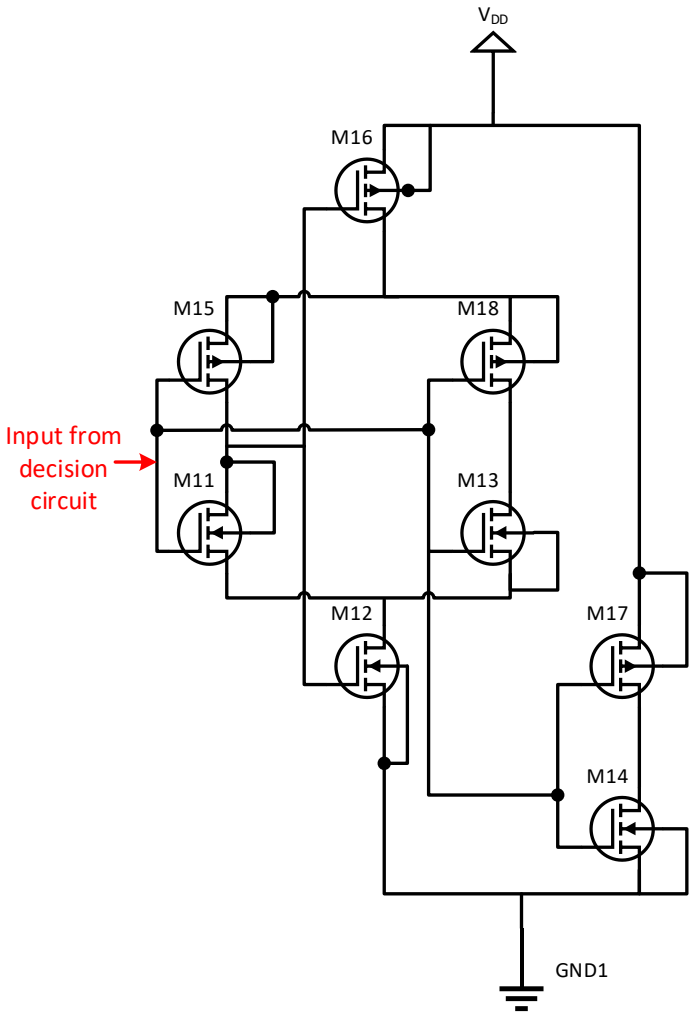

Figure 5: Decision circuit connection to the output buffer

5. RESULTS AND DISCUSSION

5.1 Sample and hold circuit

With a CMOS transmission gate and a sampling capacitor, a simple sample and hold circuit is designed. A dummy switch is placed to prevent charge injection errors. The charge injection from the sampling switch is absorbed by the fake switch, which is operated by an inverted clock. By attaching a buffer to the end of the sample and hold circuit, DNL and INL can be reduced, resulting in a superior ADC design. The results of the sample and hold circuit simulation are shown in Figure 6.

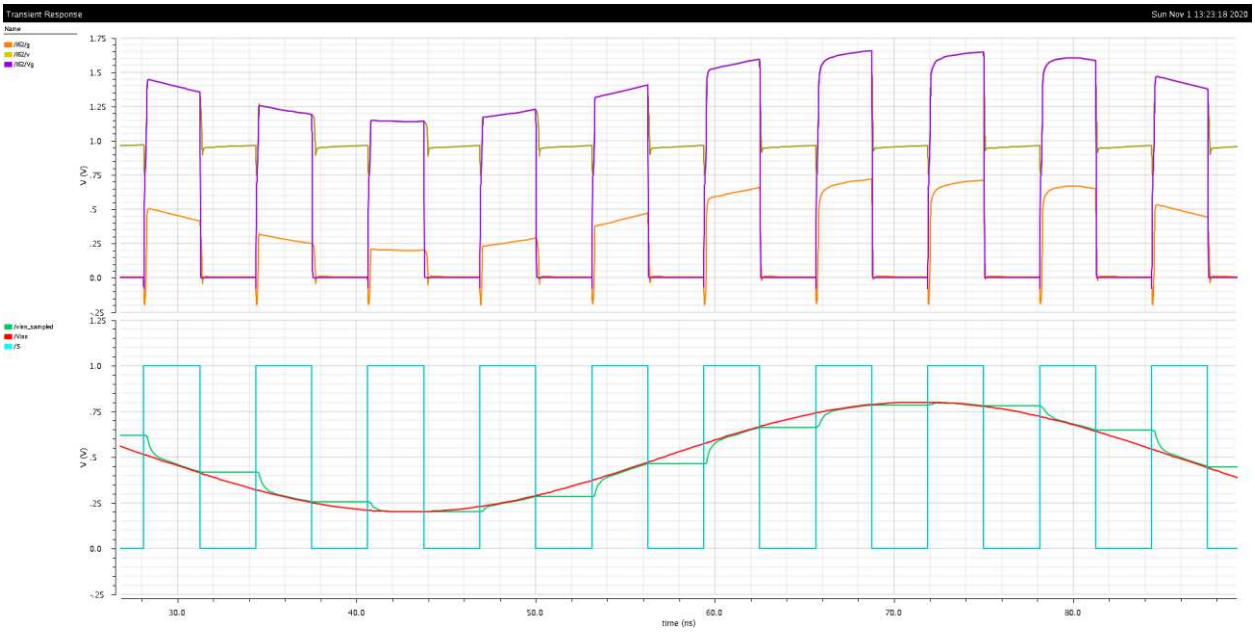

Figure 6: Simulation result of the sample and hold circuit

5.2 Transient analysis of the proposed comparator

The schematic structure of the proposed power gated comparator is shown in Figure 7. Transient analysis for the proposed comparator is obtained at 40mV and 250MHz frequency. $V+$ input, and $V-$ is fixed at a voltage of 900mV. An input voltage pulse of a width of 100ns is fed to both V_{inp} and V_{inn}. Pulse amplitude is varied from 0 to 5V at V_{inp} and 5 to 0V at V_{inn}.

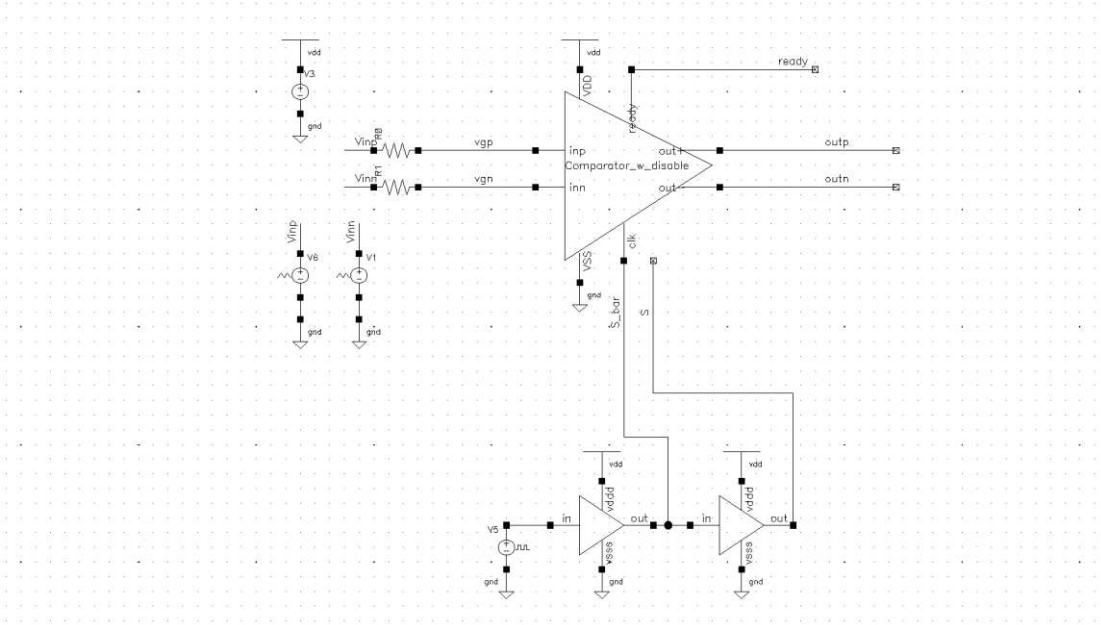

Figure 7: Schematic diagram of the proposed power gated comparator

The transient analysis of DAC using 45nm technology is given in Figure 8. If $(V+) > (V-)$, the output results in logic-1 otherwise the output is logic-0. The period for both the pulses is applied as 200ns. The transient analysis of DAC using 45nm technology is given in Figure 9.

Corner analysis is performed for 45 process corners to find slew rate variation and the results for voltage variations from 10V/ µs to 15V/µs are shown in Figure 9.

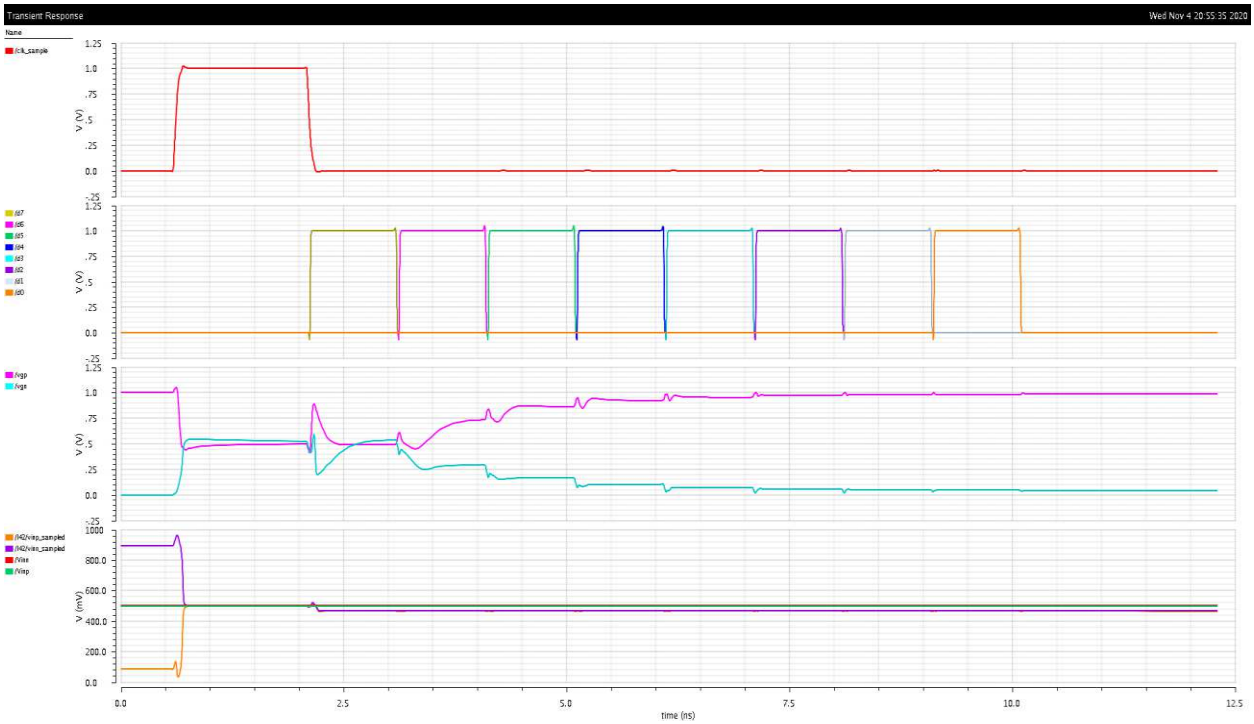

Figure 8: Transient analysis of DAC at 5V using 45nm technology

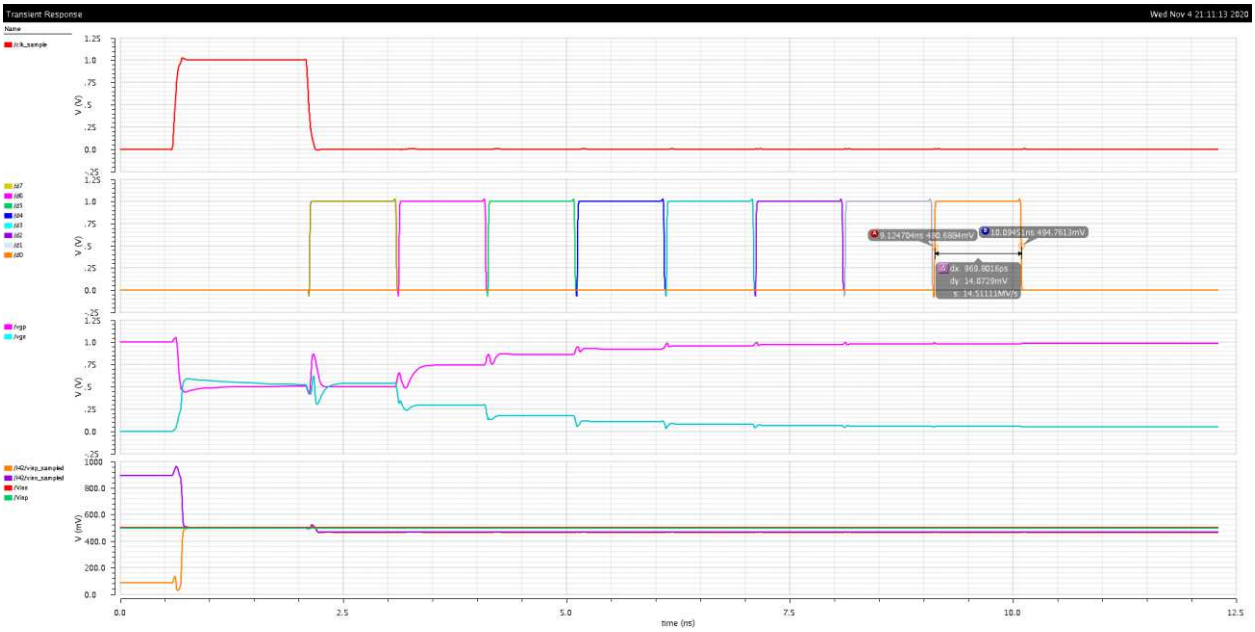

Figure 9: Transient analysis of DAC at 3.3V using 45nm technology

The simulated results of a 3.3V comparator are shown in Table 1.

Table 1: Simulation results of the proposed comparator at 3.3V

S.No.	Parameter	Specifications	Proposed 3.3V comparator
1	Technology (μm)	0.45	0.45
2	Supply Voltage (V)	3.3- 5	3.3
3	Gain (dB)	8.24	11.04
4	Phase margin (deg)	>60	74.63
5	Input Offset Voltage (mV)	<20	10
6	ICMR Range (3.3 V)	0.9-3	0.7-3.1
7	Slew Rate (V/μS)	>5	12
8	Power consumption (mW)	<10	4.5
9	Load Capacitance (pF)	>2	2
10	Settling Time (pS)	<200	120

5.3 Simulation results of a proposed comparator at 5V

A 5V CMOS comparator designed using cadence 45nm technology is exhibited in Figure 10. The input voltage can be varied from 0V to 5V. If the input voltage is less than the reference voltage, the output is set to logic 0; otherwise, the output is set to logic 1. The design is to meet power dissipation less than 1.5mW, offset voltage more than 8.4mV, and slew rate more than 4.68V/μS.

The static power dissipation of the circuit is reduced by implementing M_{15} transistor. The transistor acts as a power gated transistor with a control input ϕ. Whenever the circuit is not in use, the control input is set to logic 0 to keep the circuit idle. The control input should change to logic 1, to make use of the circuit. The DC transient response of the proposed power gated comparator is obtained through simulation with the process parameter of 5V at 27° C.

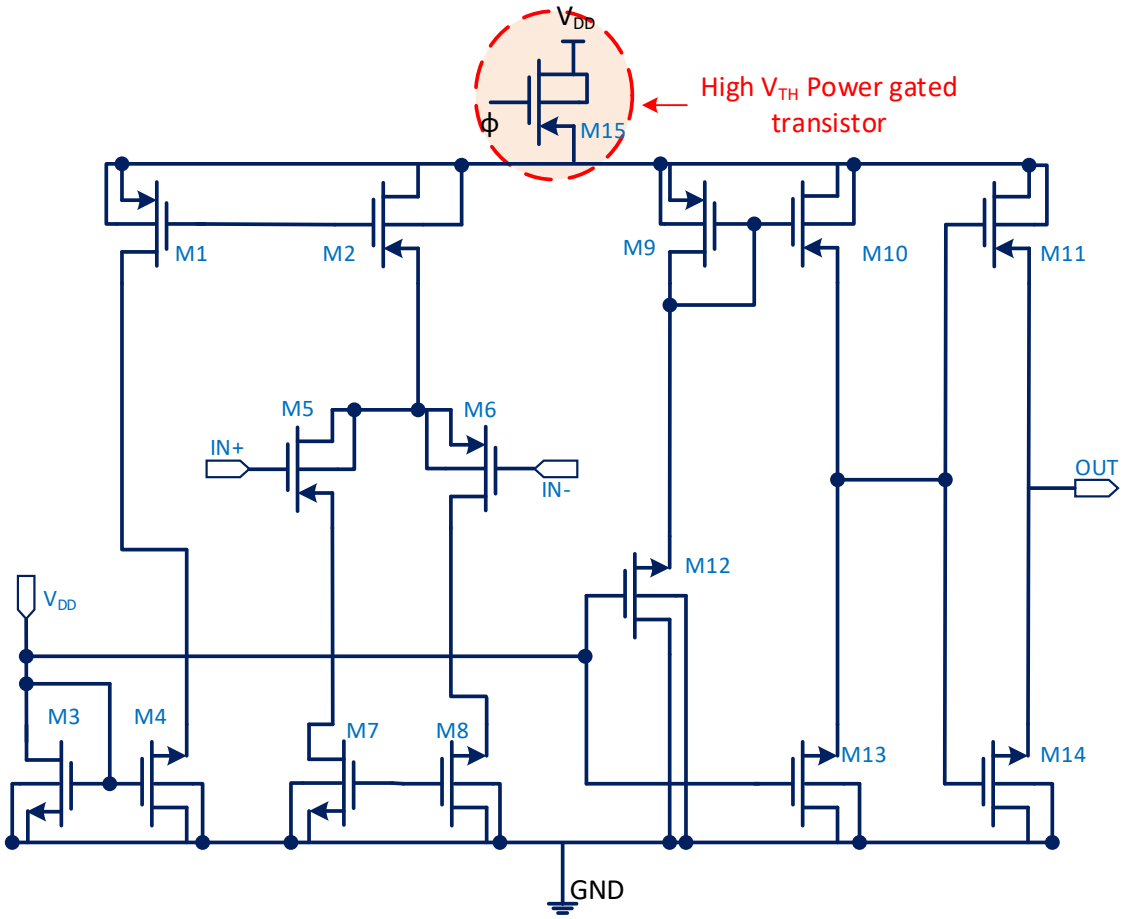

Figure 10: Proposed dynamic comparator design in cadence environment

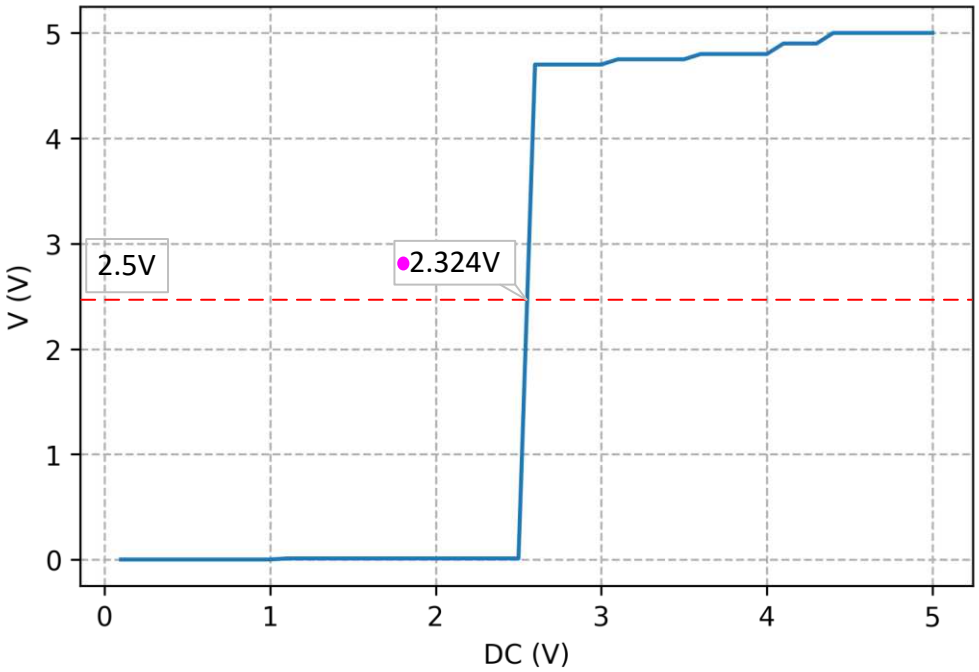

Figure 11: DC offset voltage characteristics of the proposed comparator

A DC drift of voltage is shown in Figure 11 at output providing a voltage of 2.324 mV at 2.5 V input.

5.4 DC analysis test setup and simulation

The DC analysis is used to identify node voltages, loop voltages, branch currents, and operating point. Approximately the offset value is measured as 18mV. The voltage sweep is from 2.49 to 2.50V, with an interval of 0.005V. The 45 corners DC analysis is shown in Figure 12. The corner analysis is carried out in cadence using ADE GXL and tested for 45 corners. Here the circuit is tested at temperature, process, and voltage (PVT) for its efficiency. DC analysis is done with sweep voltage from 2.49V to 2.50V with a step of 0.005V.

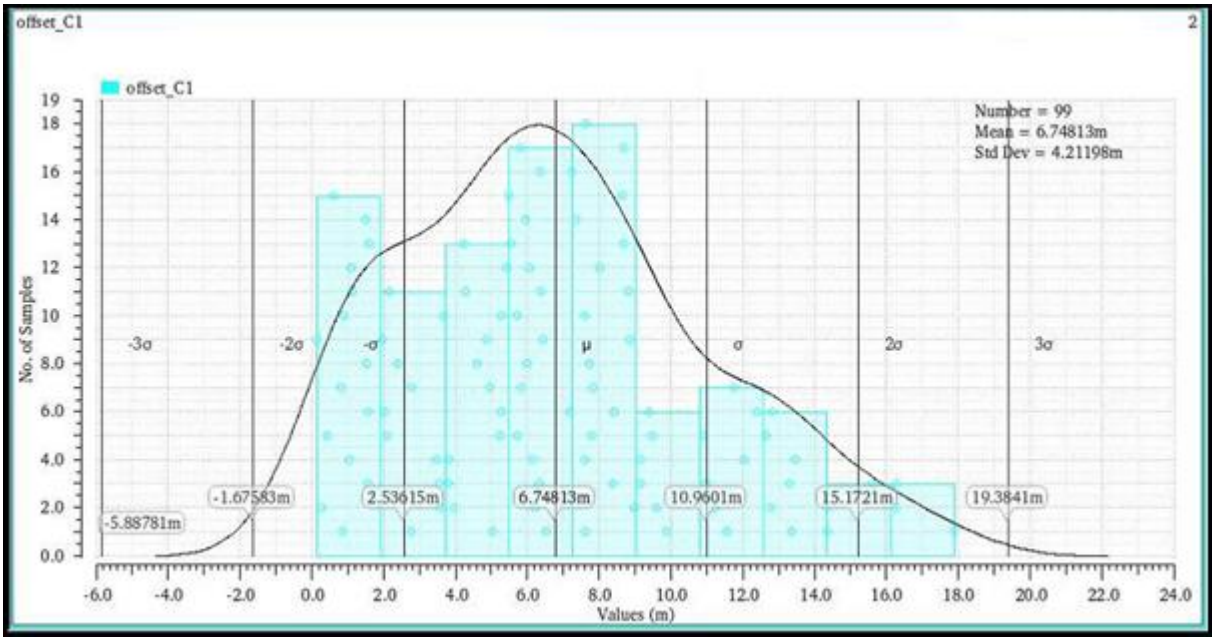

Figure 12: 45 Corners DC analysis using Monte Carlo simulation

The PVT, V (10% of 5V, i.e. 4.5V, 5V, and 5.5 V) and T (Temp = -40˚C, 27˚C, and 125˚C) corner analysis have been done using cadence ADE GXL at 45 different corners. The minimum offset has been observed as 5mV, and the maximum offset is 9mV. Monte Carlo analysis is done for 100 samples. From Figure 14 it is found that the mean and standard deviation is 6.74 mV and 4.2 mV respectively.

5.5 Transient response of the proposed comparator

Figures 13 and 14 display the transient response of the proposed comparator using 45nm technology. Through this, the frequency response of the comparator is evaluated i.e. gain and phase margins. After finding the biasing points, For AC analysis, a well-behaving AC input signal is applied to the circuit. Speed and accuracy are the key parameters of a comparator for ADC and DAC. DC analysis and transient analysis are done to obtain the slew rate and offset.

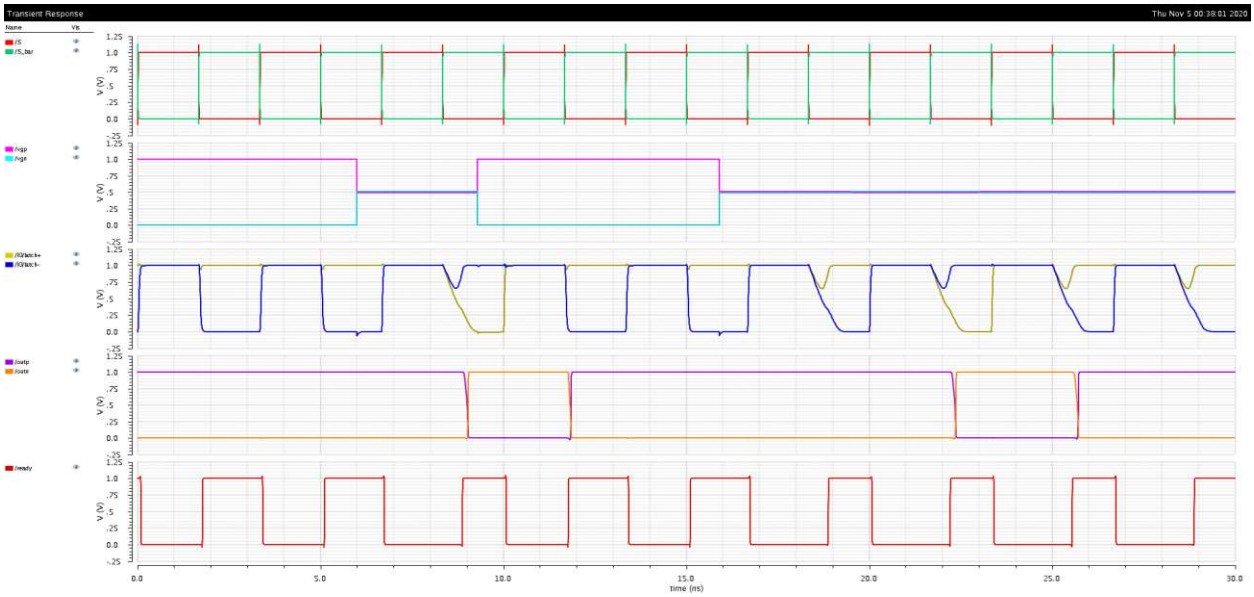

Figure 13: Transient response of the proposed comparator at 5V using 45nm technology

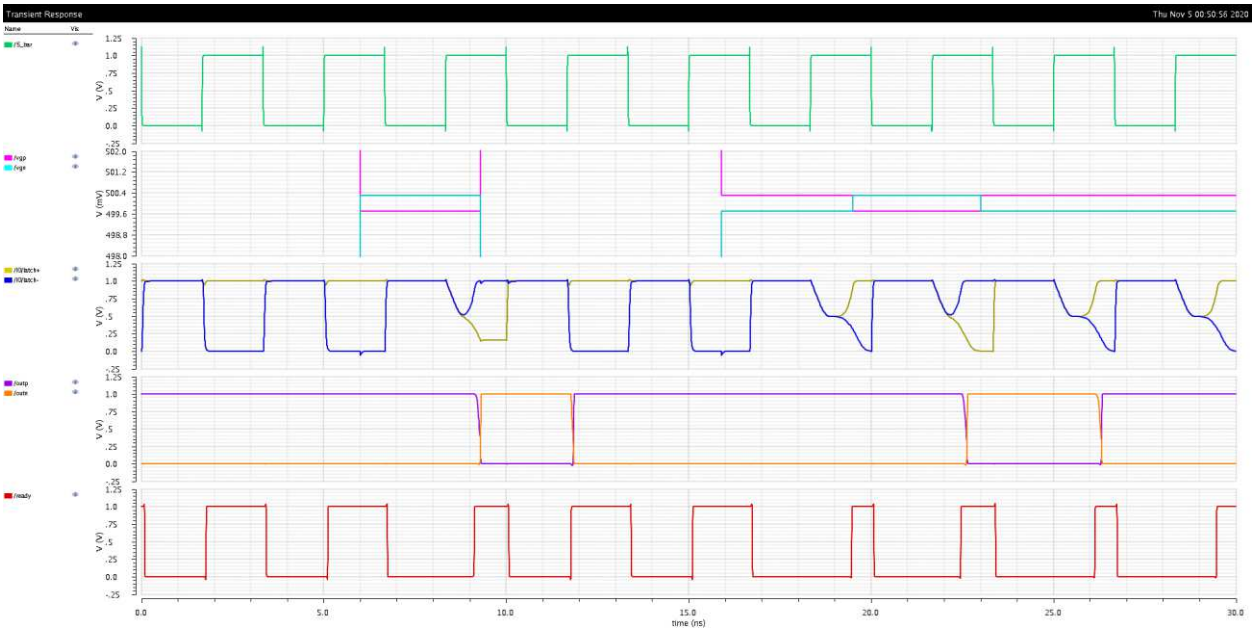

Figure 14: Transient response of the proposed comparator at 3.3V using 45nm technology

5.6 Frequency response of the proposed comparator

After DC analysis, the offset because of mismatch needs to be found. From the simulation results, the gain margin is found as 22.22 dB. However, for a comparator, the gain margin is not the required specification. The phase margin is an important parameter. The frequency response of the mutated dynamic power gated comparator is given in Figure 15. The obtained phase margin is 96° and the unity-gain bandwidth is 12 MHz.

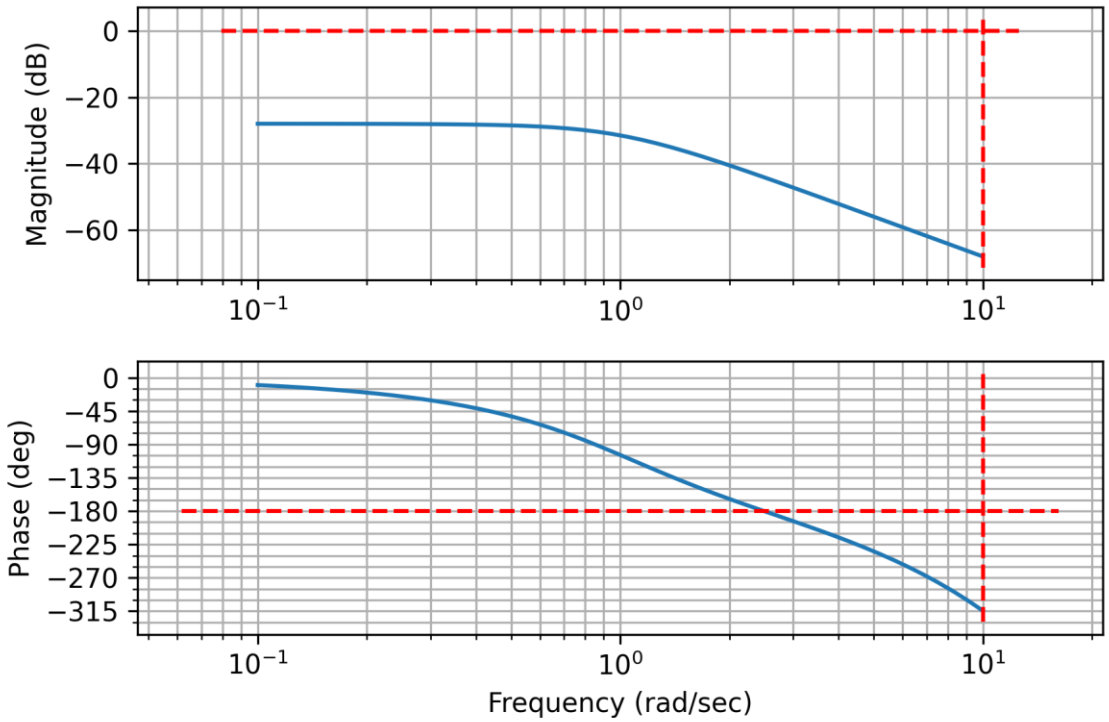

Figure 15: Frequency response of the mutated dynamic power gated comparator

Figures 16 and 17 display the schematic diagram of the proposed SAR ADC in the Cadence environment and Test bench creation for the simulation of the proposed SAR using a power gated comparator. Figure 18 shows the final simulation result of the proposed SAR ADC.

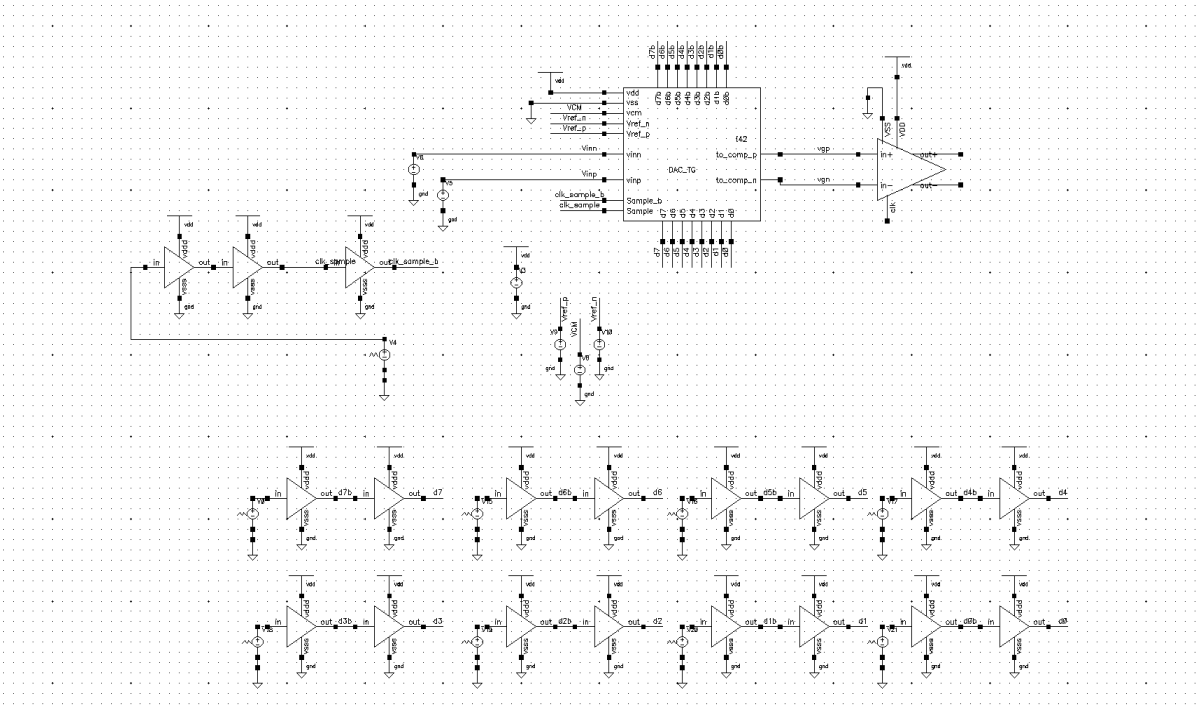

Figure 16: Schematic diagram of the proposed SAR ADC in Cadence environment

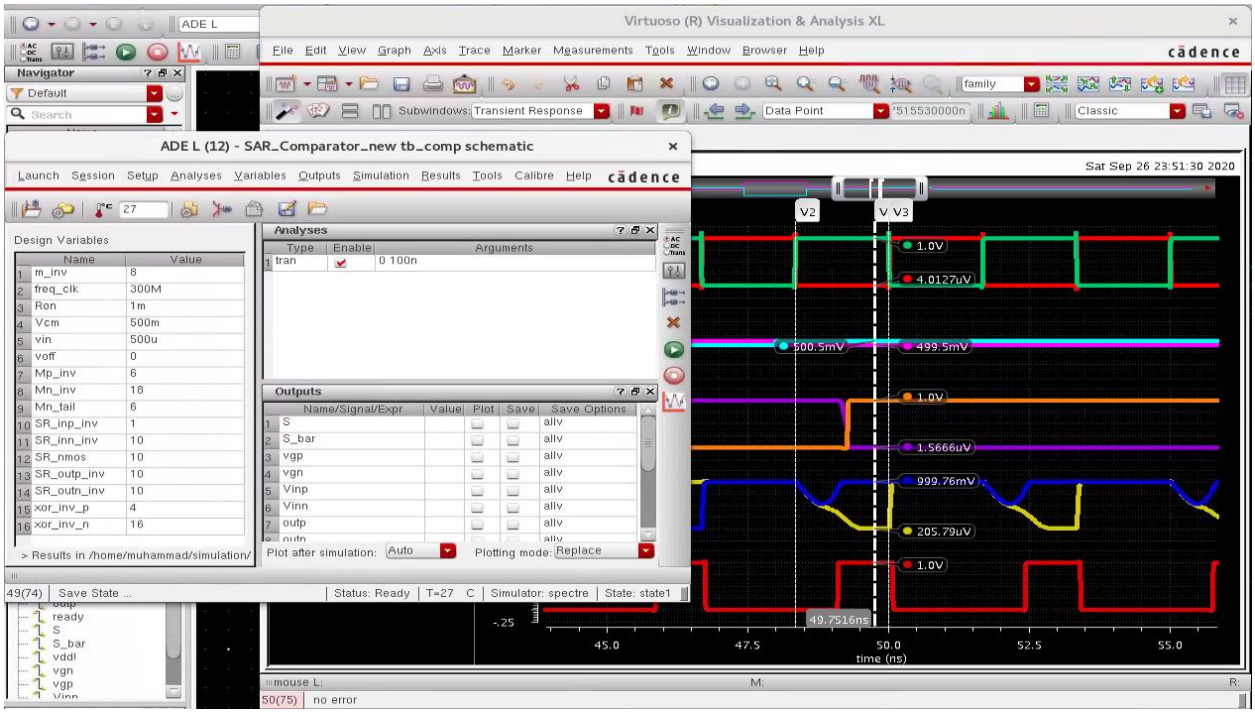

Figure 17: Test bench creation for the simulation of proposed SAR

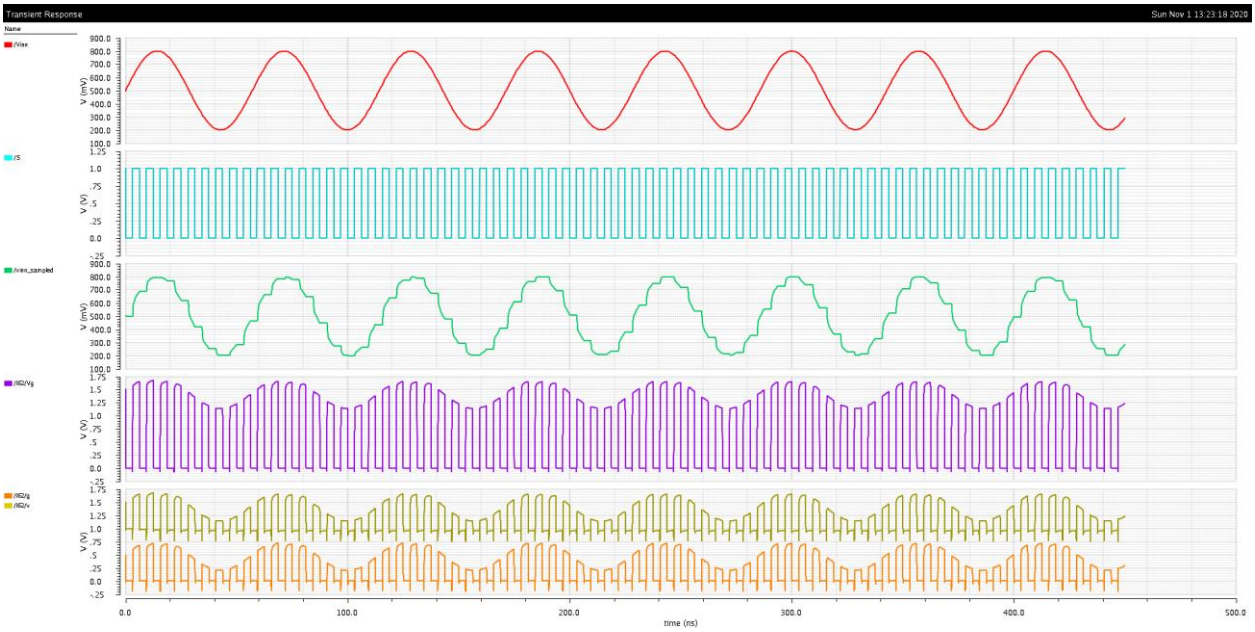

Figure 18: Cadence simulation result of the proposed SAR ADC

5.7 Post layout simulation of the proposed comparator

The Comparator layout is represented in Figure 19. Differential pair is carefully designed because all the offset has been generated from them. The layout area is 7500 μm^2, which is less than 2% of the latest design in this technology.

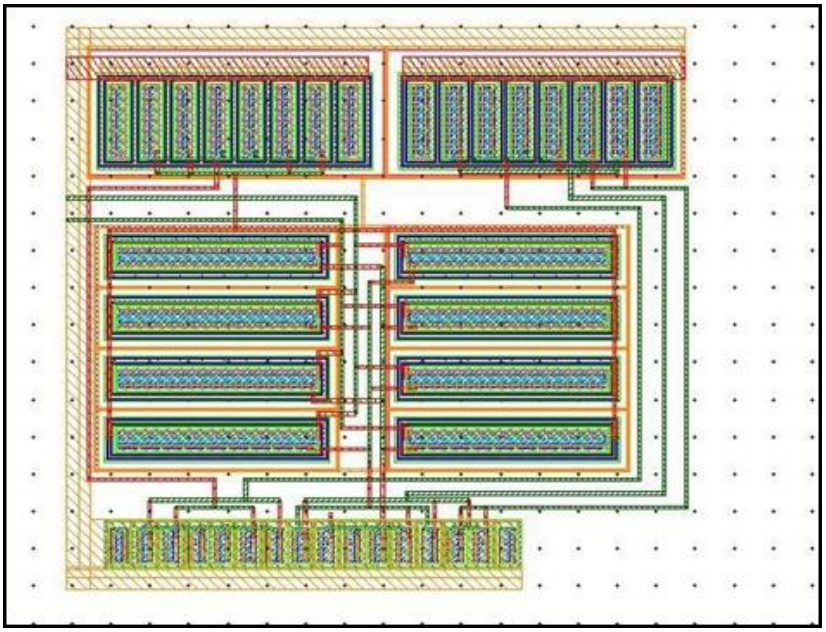

Figure 19: Layout of proposed 9-bit SAR ADC

All simulations were run on a 45nm CMOS technology cadence analogue design environment (ADE). All circuits are functionally verified using Cadence spectra and virtuoso tools. The suggested SAR ADC's power consumption, area, delay, and other factors are all measured and compared to traditional logic circuits. The overall performance of the SAR ADC has increased as a result of the simulation results, and it may be beneficial in future biomedical applications. When the input voltage is 5V, Table 2 illustrates the simulation results of the proposed comparator. Table 3 compares the proposed comparator's performance to that of other traditional comparators.

Table 2: Simulation results of the proposed comparator at 5V

S.No.	Parameter	Specifications	Proposed 5V comparator
1	Technology (µm)	0.45	0.45
2	Supply Voltage (V)	3.3- 5	5
3	Gain (dB)	8.24	12.22
4	Phase margin (deg)	>60	83.5841
5	Input Offset Voltage (mV)	<20	8.4
6	ICMR Range (5 V)	1.2-4.5	0.8-4.74
7	Slew Rate (V/µS)	>5	15
8	Power consumption (mW)	<10	1.5
9	Load Capacitance (pF)	>2	2
10	Settling Time (pS)	<200	178

Table 3: Performance comparison table of different comparators

S.No.	Parameters	Proposed comparator at 5V	Proposed comparator at 3.3V	Babayan-Mashhadi & Lotfi, [3]	Shen et al., [14]	Shesharaman & Kittur [15]	Suriyavejwongs et al., [16]	Dubey & Nagaria [6]	Yewale [20]
1	Technology (µm)	0.45	0.45	0.90	0.90	0.45	0.45	1.8	1.8
2	Supply Voltage (V)	5	3.3	5	3.3	3.3	5	5	5
3	Gain (dB)	12.22	11.04	-	-	-	-	-	-
4	Phase margin (deg)	83.58	74.63	-	-	-	-	-	-
5	Input Offset Voltage (mV)	8.4	10	24	16	50	8.27	21.9	7.99
6	ICMR Range (V)	0.8-4.74	0.7-3.1	0.65-1.48	0-2.5	0-3	0-1.2	0-1.65	0-1.8
7	Slew Rate (V/µS)	15	12	9.14	11.35	14.72	17.87	33	
8	Power consumption (mW)	1.5	4.5	8	21.3	25.66	11.5	18.2	10.2
9	Load Capacitance (pF)	2	2	1	5	5	1.72	1.11	1.49
10	Settling Time (pS)	178	120	-	-	-	-	-	-

5. CONCLUSION

An ultra-low power 3.3V and 5V comparator are designed using 45nm CMOS technology. Simulations are performed through process corners and Monte-Carlo analysis for the supply voltage 3.3V ±10% and 5V ±10% with temperature variations ranging from -40°C to +125°C. The results represent that the design consumes 1.5mW of total power with an offset voltage of 8.4mV along with a slew rate of 14.68V/µS, which can be used in ADCs for high speed and accurate comparison. The noise present in the input and clock pulse is suppressed by the output stage latch present in the differential amplifier. Maximum power and minimum power consumed by the proposed comparator with the supply voltage 3.3V are 70.07mW and 63.63mW respectively. Maximum power and minimum power consumed by the proposed comparator with the operating voltage 5V are 81.94mW and 78.84mW respectively. The maximum gain obtained is 80.8 dB and the minimum gain is observed as 68.8 dB for 3.3V and 5 V respectively.

CONFLICTS OF INTEREST

The authors declare that there are no conflicts of interest regarding the publication of this paper.

DATA AVAILABILITY

All the data underlying results are available as a part of this article and no additional source of data are necessary.

AUTHORS CONTRIBUTION

Author 1 contributed towards conceptualization, conceived and designed the analysis, contributed to perform analysis. Author 1 and 2 together contributed towards result validation and writing original article.

REFERENCES

[1] AlMarashli, A., Anders, J., & Ortmanns, M. (2016). A hybrid comparator for high resolution SAR ADC. *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*. https://doi.org/10.1109/iscas.2016.7527424

[2] Ay, S. U. (2010). A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS. *Analog Integrated Circuits and Signal Processing*, *66*(2), 213–221. https://doi.org/10.1007/s10470-010-9515-3

[3] Babayan-Mashhadi, S., & Lotfi, R. (2014). Analysis and design of a low-voltage low-power double-tail comparator. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *22*(2), 343–352. https://doi.org/10.1109/tvlsi.2013.2241799

[4] Banik, S., Rasel, M. M. H., Mahmud, T., & Hasanuzzaman, M. (2020). Design and implementation of a low-power 1V, 77.26µw 6-bit SAR ADC in Cadence 90nm CMOS process for biomedical application. *2020 IEEE Region 10 Symposium (TENSYMP)*. https://doi.org/10.1109/tensymp50017.2020.9230608

[5] Choi, M., & Abidi, A. A. (2001). A 6 B 1.3 gsample/S A/D converter in 0.35 µm CMOS. *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177)*. https://doi.org/10.1109/isscc.2001.912571

[6] Dubey, A. K., & Nagaria, R. K. (2018). Optimization for offset and kickback-noise in novel CMOS double-tail dynamic comparator: A low-power, high-speed design approach using bulk-driven load. *Microelectronics Journal*, *78*, 1–10. https://doi.org/10.1016/j.mejo.2018.05.006

[7] JEN, G.-W., & LIN, W.-L. (2016). An 11-bit single-ended SAR ADC with an inverter-based comparator for Design Automation. *IEICE Transactions on Electronics*, *E99.C*(12), 1331–1334. https://doi.org/10.1587/transele.e99.c.1331

[8] Jun He, Sanyi Zhan, Degang Chen, & Geiger, R. L. (2009). Analyses of static and dynamic random offset voltages in dynamic comparators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *56*(5), 911–919. https://doi.org/10.1109/tcsi.2009.2015207

[9] Le, H. P., Zayegh, A., & Singh, J. (2003). Performance analysis of optimised CMOS comparator. *Electronics Letters*, *39*(11), 833. https://doi.org/10.1049/el:20030546

[10] Mandrumaka, K. K., & Noorbasha, F. (2019). A low power 10 bit SAR ADC with variable threshold technique for biomedical applications. *SN Applied Sciences*, *1*(8). https://doi.org/10.1007/s42452-019-0940-3

[11] Mehra, K., Sharma, T., & Somal, S. (2021). Performance analysis on low-power, low-offset, high-speed comparator for high-speed ADCA Review. *Intelligent Communication and Automation Systems*, 99–112. https://doi.org/10.1201/9781003104599-7

[12] Mesgarani, A., Alam, M. N., Nelson, F. Z., & Ay, S. U. (2010). Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS. *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*. https://doi.org/10.1109/mwscas.2010.5548658

[13] Sharuddin, I., & Lee, L. (2014). Design of low power and improved Tlatch comparator for SAR ADC. *2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*. https://doi.org/10.1109/apccas.2014.7032860

[14] Shen, L., Sun, N., Shen, Y., Li, Z., Shi, W., Tang, X., Li, S., Zhao, W., Zhang, M., & Zhu, Z. (2019). A two-step ADC with a continuous-time SAR-based first stage. *IEEE Journal of Solid-State Circuits*, *54*(12), 3375–3385. https://doi.org/10.1109/jssc.2019.2933951

[15] Shesharaman, K. N., & Kittur, H. M. (2012). A 180nm CMOS low power latched comparator for NMR applications. *IET Chennai 3rd International Conference on Sustainable Energy and Intelligent Systems (SEISCON 2012)*. https://doi.org/10.1049/cp.2012.2240

[16] Suriyavejwongs, P., Leelarasmee, E., Pora, W., & Tontisirin, S. (2017). Inverting amplifier based ultra low power low offset current comparator. *2017 International Electrical Engineering Congress (IEECON)*. https://doi.org/10.1109/ieecon.2017.8075910

[17] Thamaraimanalan, T., & Sampath, P. (2019). A low power fuzzy logic based variable resolution ADC for wireless ECG Monitoring Systems. *Cognitive Systems Research*, *57*, 236–245. https://doi.org/10.1016/j.cogsys.2018.10.033

[18] Thamaraimanalan, T., & Sampath, P. (2019). Leakage power reduction in deep submicron VLSI circuits using delay-based power gating. *National Academy Science Letters*, *43*(3), 229–232. https://doi.org/10.1007/s40009-019-00848-4

[19] Xu, W., & Chen, H. (2014). Designing a precision comparator for 10-bit synchronization SAR ADC. *2014 International Conference on Anti-Counterfeiting, Security and Identification (ASID)*. https://doi.org/10.1109/icasid.2014.7064965

[20] Yewale, S. (2012). Design of low power and high speed CMOS comparator for a/D converter application. *Wireless Engineering and Technology*, *03*(02), 90–95. https://doi.org/10.4236/wet.2012.32015

[21] Zhuang, H., Tong, C., Peng, X., & Tang, H. (2020). Low-power, low-noise edge-race comparator for SAR adcs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *28*(12), 2699–2707. https://doi.org/10.1109/tvlsi.2020.3021680