Aligned carbon nanotube integrated circuit downsizing toward a sub-10 nm node

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Abstract

Transistors on aligned semiconducting carbon nanotubes (A-CNTs) have been considered a promising substitute for mainstream Si transistors to extend integrated circuit (IC) technology owing to their potential advantages of easy miniaturization and high energy efficiency, but whether A-CNT FETs can be scalably fabricated with ultrascaled whole dimensions while maintaining high performance remains questionable. Here, we explore the whole size scaling down potential of A-CNT transistors and demonstrate the possibility of implementing such small-geometry transistors in ultra-large-scale ICs that consist of billions of transistors. A-CNT transistors with a contacted gate pitch (CGP) of 175 nm have been achieved by simultaneously scaling the gate length and the contact length, and exhibit an on-current of 2.24 mA/μm and a peak transconductance of 1.64 mS/μm, surpassing silicon 45 nm node transistors in terms of both size and electronic performance. A static random-access memory (SRAM) cell has been built using six A-CNT transistors in an area of 0.967 μm2, which is comparable to the commercial silicon 90 nm technology node and is the smallest SRAM cell based on non-Si semiconductors. Furthermore, a full-contact structure is introduced between the metal and A-CNTs to achieve a contact resistance as low as 90 Ω·μm and to reduce the dependence on the contact length. A-CNT transistors downsized to a CGP of 55 nm (corresponding to the silicon 10 nm technology node) have been demonstrated to outperform 10 nm Si MOS transistors in terms of carrier mobility and Fermi velocity, indicating the tremendous potential of A-CNT transistors in high-performance digital ICs of sub 10 nm nodes.

Full Text

Development of integrated circuits (ICs) has been accomplished by downsizing silicon complementary metal-oxide-semiconductor (CMOS) transistors to improve the performance, integration density and parallel operation capability and simultaneously decrease the power consumption and cost. As sub-5 nm node Si CMOS technology is used for commercially available ultra-large-scale ICs (ULSICs), the downsizing of Si transistors is reaching the limit set by the power dissipation, cost and even physics [1]. Emerging IC technologies with novelties in materials, device structures/mechanisms, and system architectures have been intensively explored in academia and industry to meet the ever-increasing computing demands [2-5]. One of the most promising methods is to use semiconductors with an ultrathin body and a high carrier mobility as active channels to construct field-effect transistors (FETs) with a better scaling down property and higher performance than Si transistors, which provides significant improvement in performance and integration density for future digital IC applications [6-8]. Therefore, tremendous FETs and simple ICs have been demonstrated with one-dimensional (1D) materials, such as semiconducting nanowires and carbon nanotubes (CNTs), and two-dimensional (2D) materials, such as transition metal dichalcogenides (TMDs) and black phosphorus (BP) [3,9-17]. Among these new semiconductors, semiconducting CNTs have attracted long-term and tremendous attention owing to their unique geometric configuration and outstanding electronic properties [18-20]. High and symmetric performance CMOS FETs have been demonstrated with individual CNTs through a doping-free process down to a sub-10 nm gate length [21] and have shown excellent scaling down behavior and extraordinary

electronic performance surpassing that of silicon CMOS transistors, indicating the great potential of CNT electronics in future digital ICs. However, these advantages were only demonstrated for individual-CNT-based transistors [22-24], which cannot be scalably fabricated as building blocks for ULSIs. The recent improvements in the semiconducting purity and alignment of CNT materials enable scalable fabrication of CNT transistors [16,25-30], and FETs with practical performance comparable to that of Si transistors have been fabricated with scaled gate length (L_g) from aligned semiconducting CNTs (A-CNTs) [13,14,16]. However, fabricated with a large contact length (L_{con}, usually above 200 nm) [14,16], the contacted gate pitch (CGP), a key featured dimension reflecting the integration density of transistors in one generation [31], of these devices is too large to promise the scaling potential of CNT electronics. A-CNT FETs with a 40 nm footprint have been reported by using end-bonded contact with L_{con} down to 10 nm [15,32], but the transistors are based on a back-gated structure, and there is no obvious performance advantage with respect to the corresponding Si p-type FETs. Furthermore, various ICs, including modern microprocessors consisting of more than 14,000 transistors, have been realized [17,33-41], but the low performance and large circuit area induced by the large CGP of CNT FETs completely deviate from the predicted advantages of CNT electronics. In each generation of Si CMOS technology, the area of a six-transistor (6T) static random-access memory (SRAM) cell has also been used as an important figure-of-merit to benchmark practical integration density [42]. The reported area of CNT-based SRAM cells thus far is in the range of 2,000 to 100,000 μm^2 [26,43], which is at least 2,000 times larger than that of 90 nm node Si CMOS technology (1 μm^2) [44]. Since a combination of high performance and ultrascaled whole size is necessary for transistors to construct modern digital ICs, whether A-CNT FETs can be scalably fabricated with ultrascaled whole dimensions while maintaining high performance remains questionable, which is also a common problem existing for all low-dimensional semiconductor-based FETs. Exploring the performance advantage over mainstream IC technology under a constrained CGP to draw up an available roadmap for industrial development of A-CNT transistors and digital ICs is highly desirable.

In this work, we explore the possibility of implementing high-performance and small-geometry A-CNT FETs in ULSIs that consist of billions of transistors. A-CNT FETs with a small CGP and high performance are explored to target the 45 nm to 90 nm node Si technology. A-CNT 6-T SRAM cells are placed within an area of 1 μm^2, which is comparable to the commercial silicon 90 nm technology node and is the smallest SRAM cell based on non-Si semiconductors. We also scale down L_{con} through a full-contact structure between the metal and A-CNTs and explore the feasibility and potential of sub-10 nm node A-CNT transistors.

The CGP, defined as the smallest possible distance between gates of adjacent transistors, is used to characterize the integration density in Si CMOS technology nodes [31] and is also known as the contacted poly pitch (CPP). As shown in Figure 1a, the CGP of a transistor equals the sum of L_g, L_{con}, and two times the spacer length (L_{sp}) and is a more accurate figure-of-merit than L_g to reflect the true scaling capability [42]. Therefore, the whole downsizing of transistors in ICs involves shrinking not only L_g but also L_{con}, which affects the contact resistance (R_c) but is usually ignored by many scientific studies [13,14,16,40]. Top-

gated FETs with scaled CGP were fabricated on an A-CNT monolayer with a density of approximately 300 CNT/μm and a diameter distribution of 1.514 ± 0.076 nm (see the transmission electron microscopy (TEM) and scanning electron microscopy (SEM) images in Fig. 1b) to form good ohmic contacts [45,46]. Typical FETs with a CGP of 175 nm (see the SEM image in Fig. 1c) were achieved with an L_{con} of 80 nm, an L_{sp} of 5 nm (actually the thickness of the gate insulator) and an L_g of 85 nm, corresponding to the CGP of 90 nm (260 nm) to 45 nm (160 nm) nodes in Si CMOS technologies. With Pd as source/drain contacts, the transistors present p-type field-effect characteristics (Fig. 1d and e) with high performance, including a current on/off ratio (I_{on}/I_{off}) of 10^5, a subthreshold swing (SS) of 178 mV/dec and a threshold voltage (V_{th}) of -0.67 V at a low bias (V_{ds} = -0.1 V), a saturation current (I_{on}) of 2.24 mA/μm (V_{ds} = -0.8 V) and a peak transconductance g_m of 1.64 mS/μm (see Figure S1 in the Supplementary Information). Notably, the FET still exhibits good ohmic contact with a total resistance of 240 Ω·μm (V_{gs} = -2.2 V) even when L_{con} is scaled down to 80 nm. As a direct comparison, an adjacent FET (see Figure S1 in the Supplementary Information) with longer L_{con} (200 nm) presented improved I_{on} (2.79 mA/μm) and g_m (2.06 mS/μm) and a lower total resistance of 220 Ω·μm (V_{gs} = -2.2 V). Therefore, the 175 nm CGP A-CNT FET outperforms the silicon 45 nm technology node (CGP = 160 nm) in terms of I_{on} and g_m, demonstrating the performance superiority of CNT-based electronics at similar integration densities. However, the SS is as high as 178 mV/dec in the A-CNT FET and is much larger than that of commercial Si MOS FETs (<80 mV/dec). The high SS mainly originates from the disorder in the CNT array and the high density of interface states in the gate stack. Tubes in the high-density A-CNT array easily stack onto each other during the fabrication process, which destroys the monolayer nature of A-CNTs and leads to nanotube pitch variations (Figure S2 in the Supplementary Information). The stacking will severely degrade the gate efficiency owing to the intertube electrostatic screening effect. Moreover, a density of interface states as high as 10^{13} $cm^{-2}eV^{-1}$ (see Figure S3 in the Supplementary Information) lowers not only the on-state performance but also the switching-off property [16,47]. Future improvements, such as keeping the monolayer morphology in the fabrication process and lowering the interface state density in the gate stack, are expected to greatly lower the SS to an ideal value and further improve the performance of A-CNT FETs while maintaining a small CGP, which will provide promising building blocks for high-speed ULSIs.

In mainstream Si technology, the area of an SRAM cell is generally used as an important figure-of-merit to benchmark the integration density of a certain technology node [44,48-56]. We designed and fabricated scaled SRAM cells consisting of six whole-size-scaled p-type A-CNT FETs (see the circuit diagram and layout in Figure 2a-b and Figure S4). The SRAM cells consisting of six A-CNT FETs with a CGP of 420 nm (see Fig. S4 in the Supplementary Information, L_{con} = 250 nm, L_g = 150 nm) present a total area of 8.58 μm^2, which is similar to that (5.59 μm^2) of the silicon 0.18 μm technology node [50]. With scaling of the A-CNT FETs to a CGP of 175 nm, the area of the 6T-SRAM cells is scaled down to 0.976 μm^2, as shown in Fig. 2b, while maintaining a normal function at V_{dd} = 1.0 V, as shown in Fig. 2c and 2d. Significantly, this is the first demonstration of SRAM cells with a total area below 1 μm^2 based on all non-Si semiconductor technology, even without complex multilayer back-end interconnects, indicating the

downsizing advantage of CNT electronics. The main advantage of A-CNT FET technology in terms of integration density originates from the isolation region. Specifically, Si CMOS technology at 130-45 nm nodes employs shallow trench isolation (STI) with a pitch of approximately 200 nm [44,51,52], while a simple isolation method, such as cutting the CNT array, is adequate in A-CNT FET technology, which leads to a significantly smaller isolation region. If the 175 nm CGP A-CNT FETs demonstrated here are defined as a generation technology node (90 nm) for CNT electronics, then the key pitch comparison between the CNT 90 nm node and 3 generations (130 nm, 90 nm and 45 nm) of Si technology is shown in Fig. 2e and f. The CNT 90 nm node technology corresponds to the Si 0.13 μm technology node in terms of L_g (70 nm), to the Si 90 nm node in terms of the SRAM cell total area (~1 μm^2), and to the Si 45 nm node in terms of the CGP (160 nm) but exceeds all of them in performance owing to the intrinsic advantage of the material. Although they exhibit the same SRAM cell area as and a higher integration density than the silicon 90 nm technology node, the 90 nm node CNT FETs have a larger L_g (85 nm vs. 50 nm), indicating a relaxed manufacturing accuracy requirement in CNT electronics at the same node. As a result, the 175 nm CGP A-CNT FET technology can comprehensively outperform the Si 90 nm node technology in terms of both integration density and performance. If CNT CMOS FET technology is developed and incorporated with a mature back-end copper interconnect process, then the 175 nm CGP A-CNT FET technology will be comparable to or even exceed the Si 45 nm node technology in terms of both the integration density and performance.

Realization of A-CNT/metal contact with both low contact resistance and small size is necessary for whole downsizing of A-CNT transistors, especially down to a 50 nm CGP (sub 10 nm node). Two kinds of contact structures are widely used in low-dimensional semiconductor FETs, *i.e.*, side contact and end contact (named end-bonded contact or edge contact) [57]. The side-contact structure is widely used and adopted by our above transistors since this structure is easy to fabricate. However, its contact resistance strongly depends on the contact length [58,59]. The end-contact structure is almost independent of the contact length but suffers from high contact resistance and complicated processes, including high-temperature annealing [15,32]. Here, we utilized a full-contact structure to realize high-quality and small-size contact in A-CNT FETs (Figure 3a). The transfer length method (TLM) was used to extract the contact length (L_{con})-dependent contact resistance (R_c) of the two kinds of contact structures from top-gated A-CNT FETs. Specifically, a group of top-gated A-CNT FETs with a fixed L_{con} but various L_g from several tens to hundreds of nm were fabricated (see the SEM image in Fig. 3b) and used to retrieve the contact resistance for this fixed L_{con} (see the details in Methods and the measured electronic performances of all FETs in Figures S5 and S6 in the Supplementary Information). Typical transfer characteristics of the two groups of A-CNT FETs with side contact (L_{con} of 80 nm) and full contact (L_{con} of 30 nm) are shown in Fig. 3c and 3d, respectively, both indicating high-performance p-type FET characteristics as well as a current on/off ratio up to 10^5. The L_g-dependent R_{tot} data were then retrieved from the FETs with side- and full-contact structures for various L_{con} values, as shown in Fig. 3e and 3f, respectively. The R_{tot} values of full-contact FETs are obviously lower than those of side-contact FETs at the same drain and gate bias (Fig. 3g), which benefits from the lower R_c

originating from the use of the full-contact structure (Fig.3h). Notably, the full-contact structure presents comprehensively lower and weaker L_{con}-dependent contact resistance than the side-contact structure since the transfer length is 60 nm and 80 nm for full and side contacts, respectively (see Figure S7 in the Supplementary Information). By adopting the full-contact structure, the R_c of A-CNT FETs can be lowered to 163 Ω·μm and maintained at approximately 200 Ω·μm even at an L_{con} scaled down to 30 nm, which lays the foundation for whole size miniaturization of high-performance A-CNT FETs. The full-contact structure combines the carrier injection mechanism of side contact and end contact, *i.e.*, the carriers can be injected from the metal to CNTs at the side (length-dependent) and at the edge (length-independent). Therefore, the full-contact A-CNT/metal junction exhibits lower contact resistance than the side-contact or end-contact junctions while maintaining a weaker contact length dependence[57]. Furthermore, the full-contact A-CNT FET-based ICs present advantages in whole downsizing over Si CMOS ICs arising from the small isolation region, as shown in Fig. 3a. Compared with STI, which requires a complex process and a large area cost [60], the isolation between CNT FETs only requires one-step oxygen plasma etching to remove unwanted CNTs in the isolation area.

We further scaled the gate length down to 30 nm to explore the CGP scaling down potential of full-contact A-CNT FETs. Figure 4a demonstrates that the isolation spacing between two FETs can be scaled to 32 nm, which is much smaller than the STI region (~200 nm) in Si ICs [44,51,52]. The A-CNT FETs with scaled L_g while maintaining a long contact length (L_{con} of 200 nm, as shown in Fig. 4a) exhibit E-mode p-type behavior (V_{th} = -0.34 V at V_{ds} = -0.1 V) with an on/off ratio of ~10^3 at a V_{ds} of -0.7 V (Fig. 4b). A minimum total resistance R_{tot} as low as 186 Ω·μm (Fig. 4c and Figure S8 in the Supplementary Information) was achieved, indicating that R_c is lowered to approximately 90 Ω·μm, benefitting from the 200 nm L_{con} full contacts. More importantly, the FET presents high performance, including peak g_m of 2.69 mS/μm and I_{on} of 3.31 mA/μm (Fig. 4c and Fig. S8 in the Supplementary Information) at a drain-to-source bias of -0.7 V, which represents the record performance thus far for CNT-based FETs [13,14,16]. Since the 30 nm gate length A-CNT FETs have a higher current driving capability at smaller V_{ds} than the 10 nm node (L_g = 18 nm) Si transistors (Fig. 4c), there is sufficient room for performance compromise to realize a 10 nm node (~ 54 nm CGP) CNT FET with a 30 nm L_g through scaling of the contact length. L_{con} was then aggressively shrunk to 15 nm while keeping a 30 nm L_g, and then, the FETs were designed with a CGP of 55 nm (L_{sp}=5 nm). The as-fabricated A-CNT FET (see the SEM image and cross-sectional TEM image in Fig. 4d) exhibits an as-fabricated L_g of 35 nm and an as-fabricated actual L_{con} of approximately 20 nm (16 nm/27 nm for the source/drain) owing to process variations, indicating a practical minimum CGP of 61 nm. The transistor presents high performance (Fig. 4e and Fig. S8 in the Supplementary Information), including an I_{on} of 2.43 mA/μm and a g_m of 2.45 mS/μm at a V_{ds} of -0.8 V, which is still comparable to that of the 10 nm node Si PMOS FET [56], although slightly lower than that of the 200 nm contact length transistor in Fig. 4b. However, fabrication of sub-55 nm CGP A-CNT FETs with both small gate length and full-contact length requires a double self-aligned (self-aligned gate

and self-aligned contact) process, as proposed in Fig. S9 (see the detailed in the Supplementary Information).

To estimate the latent capacity of A-CNT FETs as a promising candidate for Si transistors in digital ICs, we benchmarked the performance of A-CNT FETs with that of silicon CMOS transistors at various CGPs (as shown in Figure 5a and Figures S10 and S11 in the Supplementary Information). At CGPs larger than 160 nm (corresponding to a 90 nm node), the A-CNT FETs present much higher I_{on} and g_m than the Si transistors. The performance advantage of A-CNT FETs over Si MOS FETs reaches the maximum value at the 90 nm node since a sufficiently long contact length can be used in A-CNT FETs, indicating that the 90 nm node is the most worthwhile technology node for the application of CNT ICs at the current stage. Shrinking the A-CNT FETs to generations below 45 nm requires a novel contact structure to scale the contact length and CGP while maintaining high performance. By introducing full contacts instead of side contacts, the CGP of A-CNT FETs has been demonstrated to be scaled down to approximately 61 nm (at L_g=30 nm, limited by the accuracy of e-beam lithography and the thickness of the gate oxide), with performance superior to that of the corresponding node Si transistors. In principle, the CGP can be further scaled to below 40 nm by scaling L_g down to approximately 15 nm, which will contribute to the performance increase. Therefore, with downsizing to a sub-10 nm node (CGP < 50 nm), A-CNT FETs with current material and device technologies will retain an obvious performance advantage over commercial Si technology, indicating the great potential of CNT electronics for digital ICs. The performance advantage of A-CNT transistors mainly originates from the high carrier mobility and Fermi velocity in the A-CNT array, as shown in Fig. S13 and Fig. 5b. The effective carrier mobility retrieved from our A-CNT FETs reaches 1500 cm^2/Vs at an L_g of 3 μm and 500 cm^2/Vs even at an L_g of 30 nm (see Figure S12 in the Supplementary Information) and is at least four times higher than the electron/hole mobility of Si transistors at any gate length [5,61,62]. The A-CNT FETs have a much higher injection velocity (see the details in Method and Figure S13 in the Supplementary Information) than the Si transistors (either NMOS or PMOS) at any gate length. Furthermore, the injection velocity in A-CNT FETs increases with scaling down of L_g following an inversely proportional relation even to an L_g of 30 nm, which indicates that the performance advantage over Si transistors will further increase at the sub-10 nm node [63]. Notably, although the injection velocity in 30 nm L_g A-CNT FETs reaches 1.1×10^7 cm/s, it is still lower than that (3×10^7 cm/s) in individual-CNT-based FETs [62], indicating that there is great room to improve the performance of A-CNT FETs.

Off-state current I_{off} is one of the metrics of most concern for transistors, as it directly affects the statistical power dissipation in digital ICs and requires more attention in A-CNT FETs, which are subject to gate-induced drain leakage (GIDL) [64,65] mainly owing to the small bandgap of CNTs. We compared A-CNT FETs with commercial Si FETs from the 130 nm to 32 nm node in the I_{on}-I_{off} representation (Fig. 5c). The 175 nm CGP A-CNT FETs in this work show an obvious advantage in terms of I_{on} versus I_{off} over Si PMOS FETs, *i.e.*, achieving higher I_{on} than Si transistors under the same I_{off}, which verifies the advantage of the energy-delay product of CNT transistors. As L_g is scaled down to 30

nm, the I_{off} of A-CNT FETs drastically increases owing to GIDL, and some structural improvements are required to lower the field strength of the drain to suppress I_{off} [65-69].

In summary, we explore the whole size scaling down potential of A-CNT FETs and demonstrate scaled A-CNT FETs with a CGP of 175 nm and 6-T SRAM cells within an area of 1 μm^2. Furthermore, a full-contact structure is introduced to lower the contact resistance, reduce the contact length, and enable the A-CNT FETs to shrink to a CGP below 50 nm (corresponding to a 10 nm technology node) while outperforming 10 nm Si PMOS transistors owing to the higher carrier mobility and Fermi velocity. The performance advantage provides the A-CNT FETs with more room for the trade-off between the gate length and contact length for whole downsizing, indicating the tremendous potential of A-CNT transistors in high-performance digital ICs containing tens of billions of transistors. However, several challenges remain for CNT transistor applications in digital ICs. First, n-type FETs should be developed with performance and CGP matching those of p-type FETs to constitute CMOS technology. Second, a high-quality gate dielectric with an ultrathin equivalent oxide thickness (EOT) and a low interface state density should be realized on A-CNTs to further improve the gate efficiency, which is predicted to improve the performance and lower the SS. Finally, a well-designed device structure at the drain side is necessary to suppress GIDL and lower the static power dissipation.

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Declarations

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Author contributions:

Z. Z. and L. M. P. proposed and supervised the project. Y. L. fabricated the scaled A-CNT FETs and 6T-SRAM cells. Y. L. and Y. C. characterized the devices and 6T-SRAM cells. L. X. extracted the mobility and injection velocity of the CNTs using the VS model. S. D. and C. J. performed the TEM characterizations. C. L. and Q. H. helped characterize the devices. Y. L., Y. C., Z. Z., and L. M. P. analyzed the data and wrote the manuscript. All authors discussed the results and commented on the manuscript.

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Competing financial interests:

The authors declare no competing financial interests.

Data availability:

The data that support the plots within this paper are available from the corresponding author upon reasonable request.

Figures

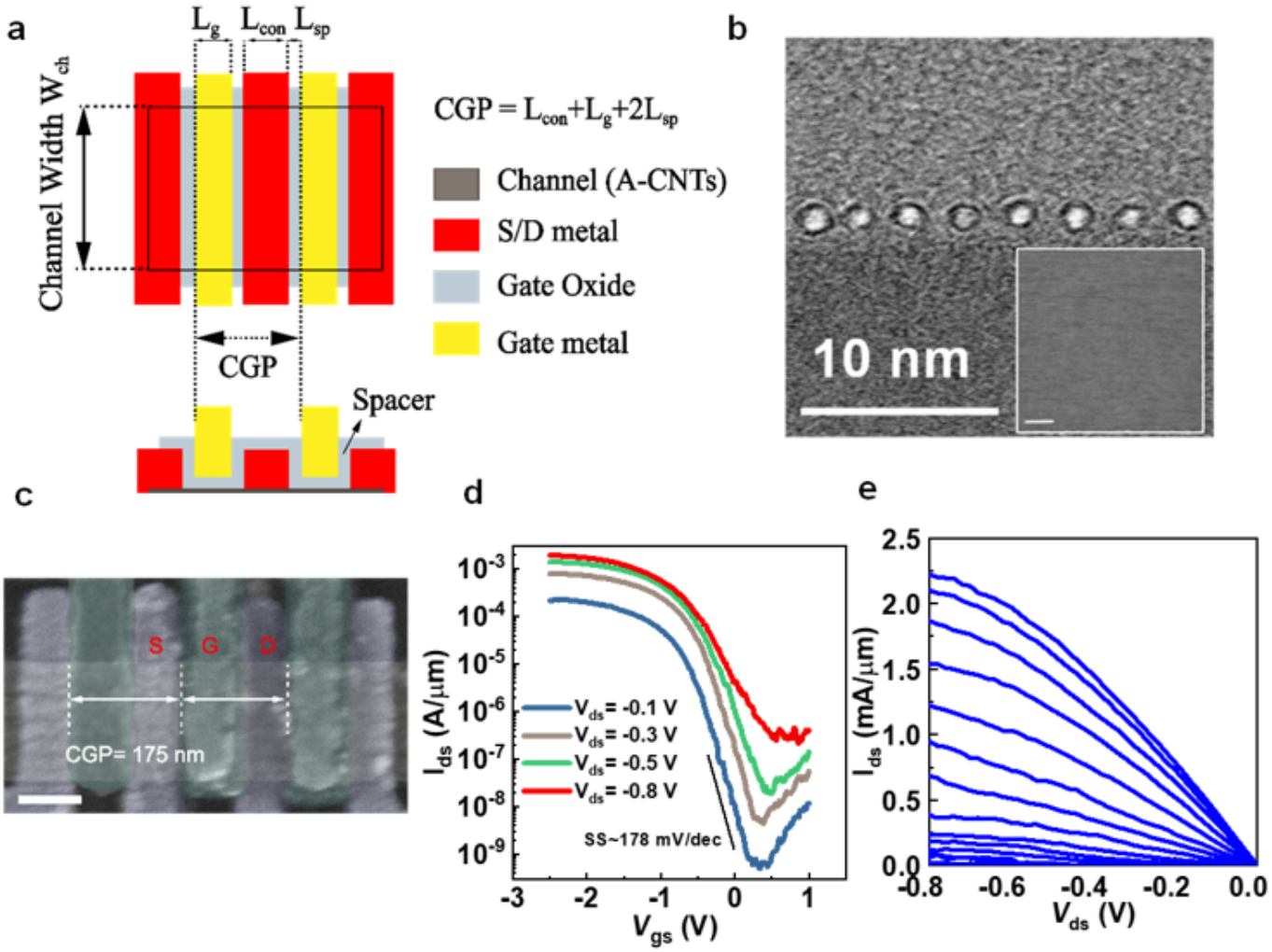

Figure 1

CGP scaling of top-gated A-CNT FETs for a 90 nm node. a, Schematic of CGP scaling. L_{con}, L_g, L_{sp} and W_{ch} represent the device contact length, gate length, spacer length and channel width, respectively. To scale the CGP, L_{con}, L_g, and L_{sp} must be simultaneously reduced. **b,** TEM image of the cross section of A-CNTs. The inset shows an SEM image of the same film. Scale bar for the inset: 500 nm. **c,** False-color SEM image of three top-gated A-CNT FETs in series with shared source/drain contacts. A CGP of 175 nm is achieved with an L_{con} of 80 nm and an L_g of 85 nm. Scale bar: 100 nm. **d, e,** Transfer characteristics (d) and output characteristics (e) of the top-gated A-CNT FET with a CGP of 175 nm. V_{gs} is varied from -2.2 V to 3.0 V with a step of 0.4 V from top to bottom.

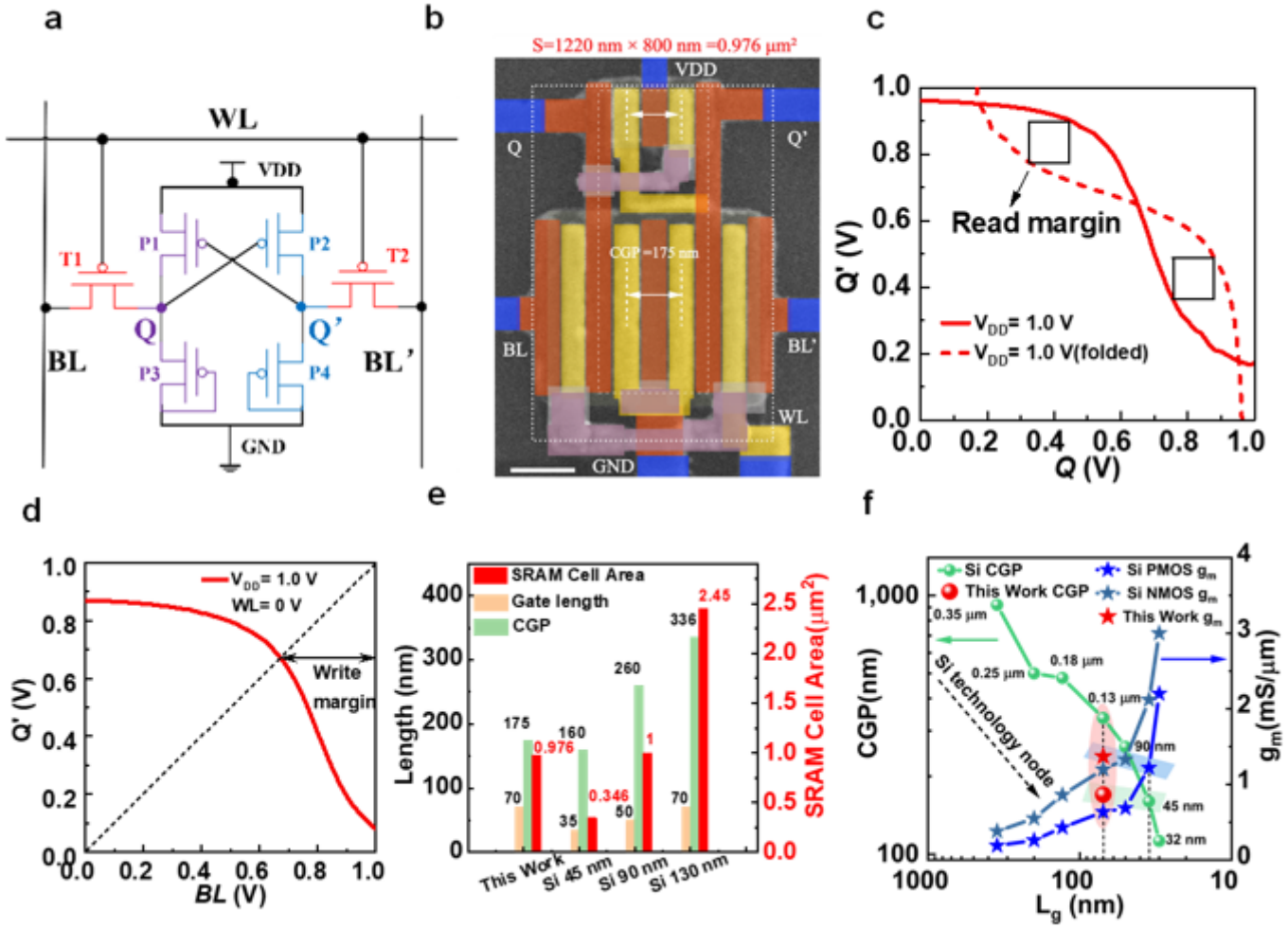

Figure 2

Ultrascaled 6T-SRAM cell based on 90 nm node A-CNT FETs. a, Circuit diagram of the 6T-SRAM cell based on A-CNT FETs. **b,** False-color SEM image of a representative 6T-SRAM cell with a CGP of 175 nm and an area of 0.976 μm^2 for the 90 nm CNT technology node. Scale bar: 200 nm. **c,** Read margin characterization of the 6T-SRAM cell in b. **d,** Write margin characterization of the 6T-SRAM cell in b. **e,** Benchmarking the ultrascaled A-CNT 6T-SRAM cell in b with silicon 130 nm , 90 nm and 45 nm technology nodes for gate length, CGP and SRAM cell area. **f,** Comparison of state-of-the-art CNT technology reported in this work with silicon technology (0.35 μm [48], 0.25 μm [49], 0.18 μm [50], 0.13 μm [51], 90 nm [44], 45 nm [52], 32 nm [53], 22 nm [54], 14 nm [55], and 10 nm [56]). Both the CGP and g_m are benchmarked for various L_g.

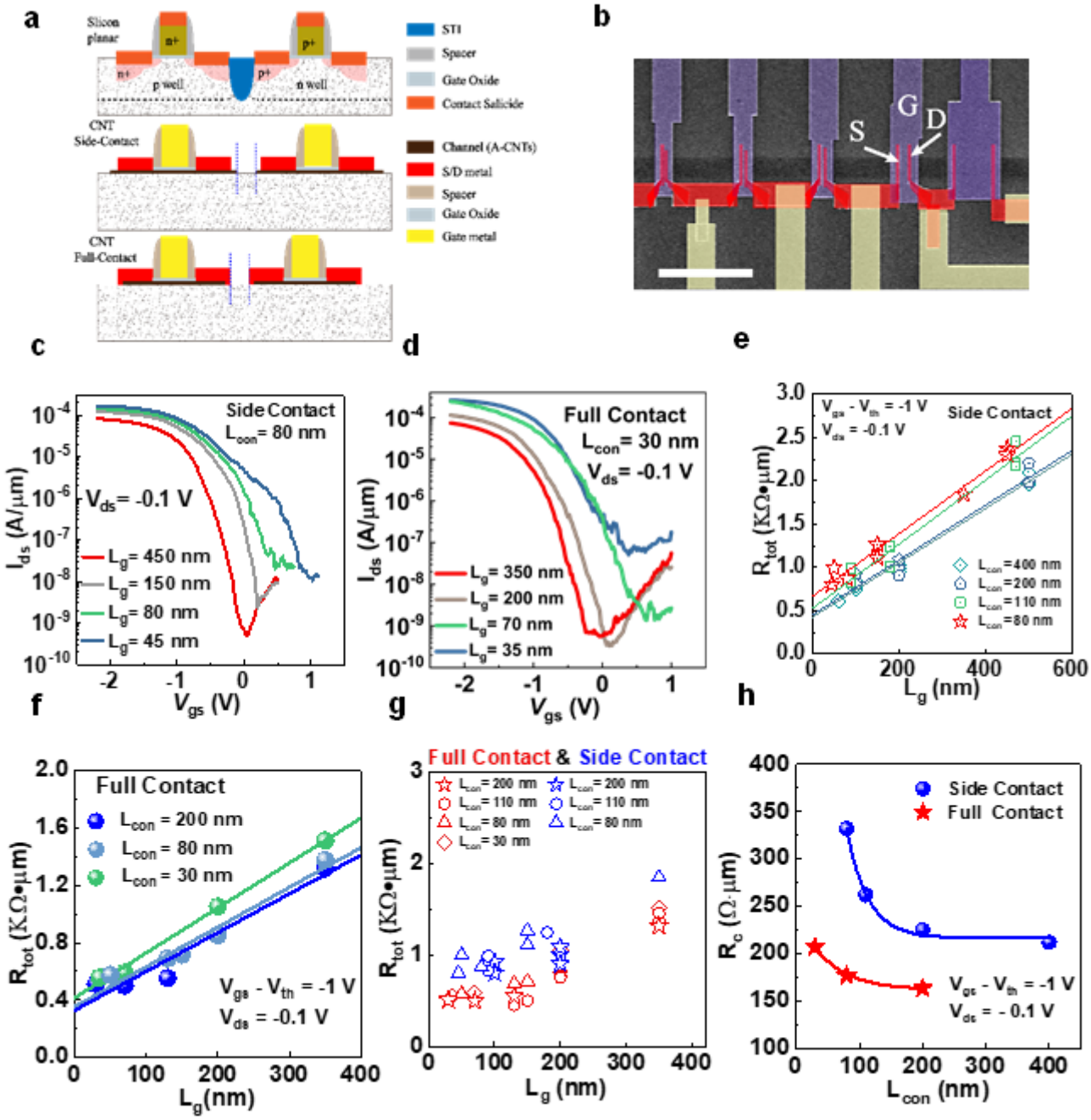

Figure 3

Contact length scaling down in A-CNT FETs. a, Schematics of the silicon planar structure, CNT side-contact structure, and CNT full-contact structure. **b,** False-color SEM image of the TLM test structure to extract R_c. Four A-CNT FETs with L_g ranging from 500 nm to 45 nm are used for each L_{con}. Scale bar: 5 μm. **c,** Transfer characteristics of A-CNT FETs with the conventional side-contact structure and an L_{con} of 80 nm. **d,** Transfer characteristics of A-CNT FETs with the full-contact structure and an L_{con} of 30 nm. **e,** R_{tot} versus L_g for A-CNT FETs with the side-contact structure. The lines represent linear fitting of R_{tot} versus L_g, and the intercept is twice the value of R_c. **f,** R_{tot} versus L_g for A-CNT FETs with the full-contact structure. The lines represent linear fitting of R_{tot} versus L_g, and the intercept is twice the value of R_c. **g,**

R_{tot} for A-CNT FETs with various L_g and L_{con} and the side-contact structure (blue) or full-contact structure (red). **h,** R_c versus L_{con} for both the side-contact structure (blue) and full-contact structure (red).

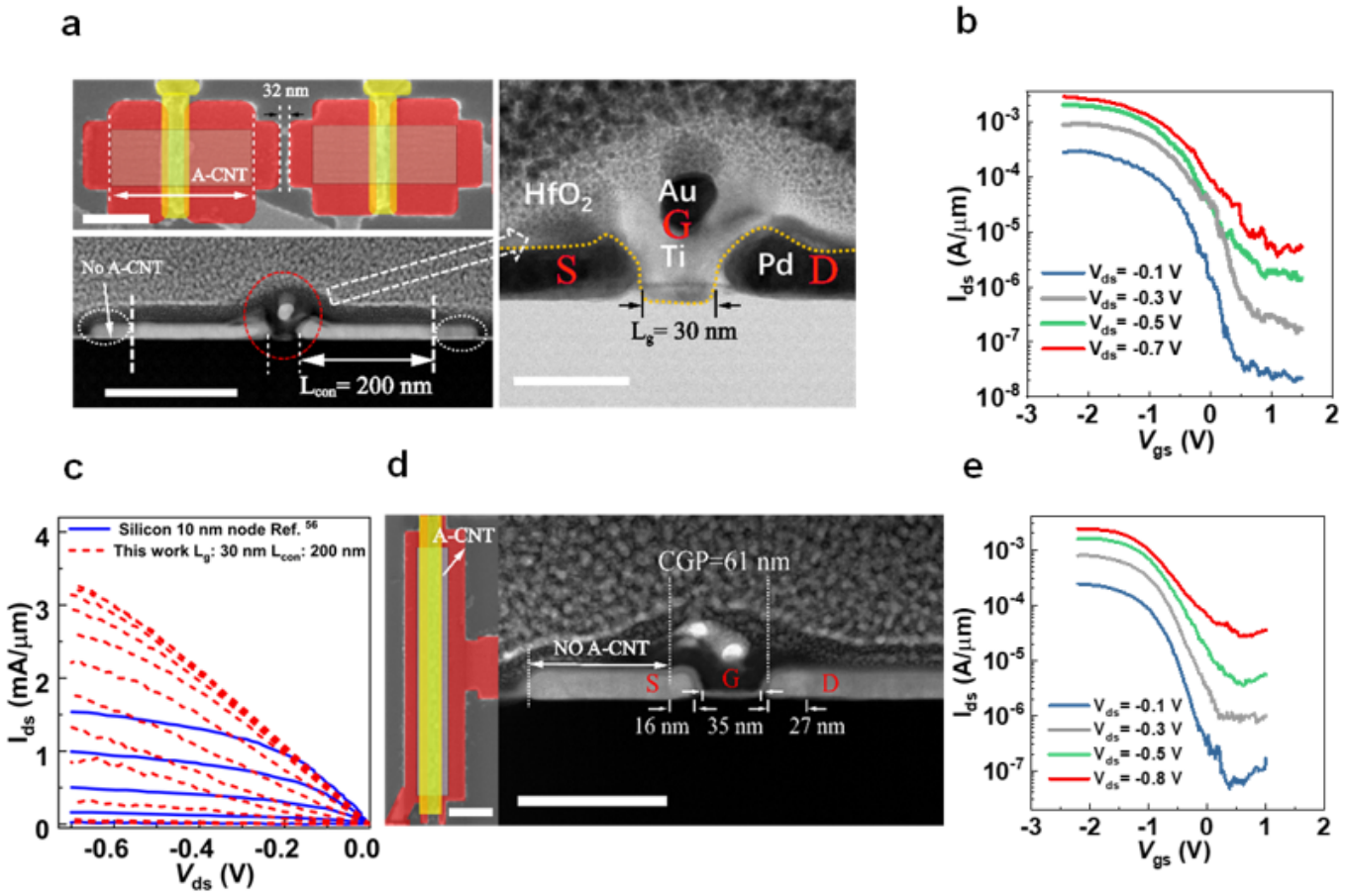

Figure 4

A-CNT FET downsizing toward a sub-10 nm node. a, SEM and cross-sectional TEM images of two adjacent A-CNT FETs. The two FETs have an L_g of 30 nm and an L_{con} of 200 nm, and the isolation space between them is 32 nm. Scale bar of the SEM image: 200 nm; of the left TEM image: 200 nm; of the right TEM image: 50 nm. **b,** Transfer characteristics of representative top-gated A-CNT FETs in a. **c,** Output characteristics of the A-CNT FET in b and comparison with the silicon PMOS FET of the 10 nm technology node. **d,** SEM and cross-sectional TEM image of an ultrascaled A-CNT FET with a CGP of 61 nm, an L_g of 35 nm and an L_{con} of 16 nm. Scale bar of the SEM image: 200 nm; of the TEM image: 100 nm. **e,** Transfer characteristics of the same device as in d.

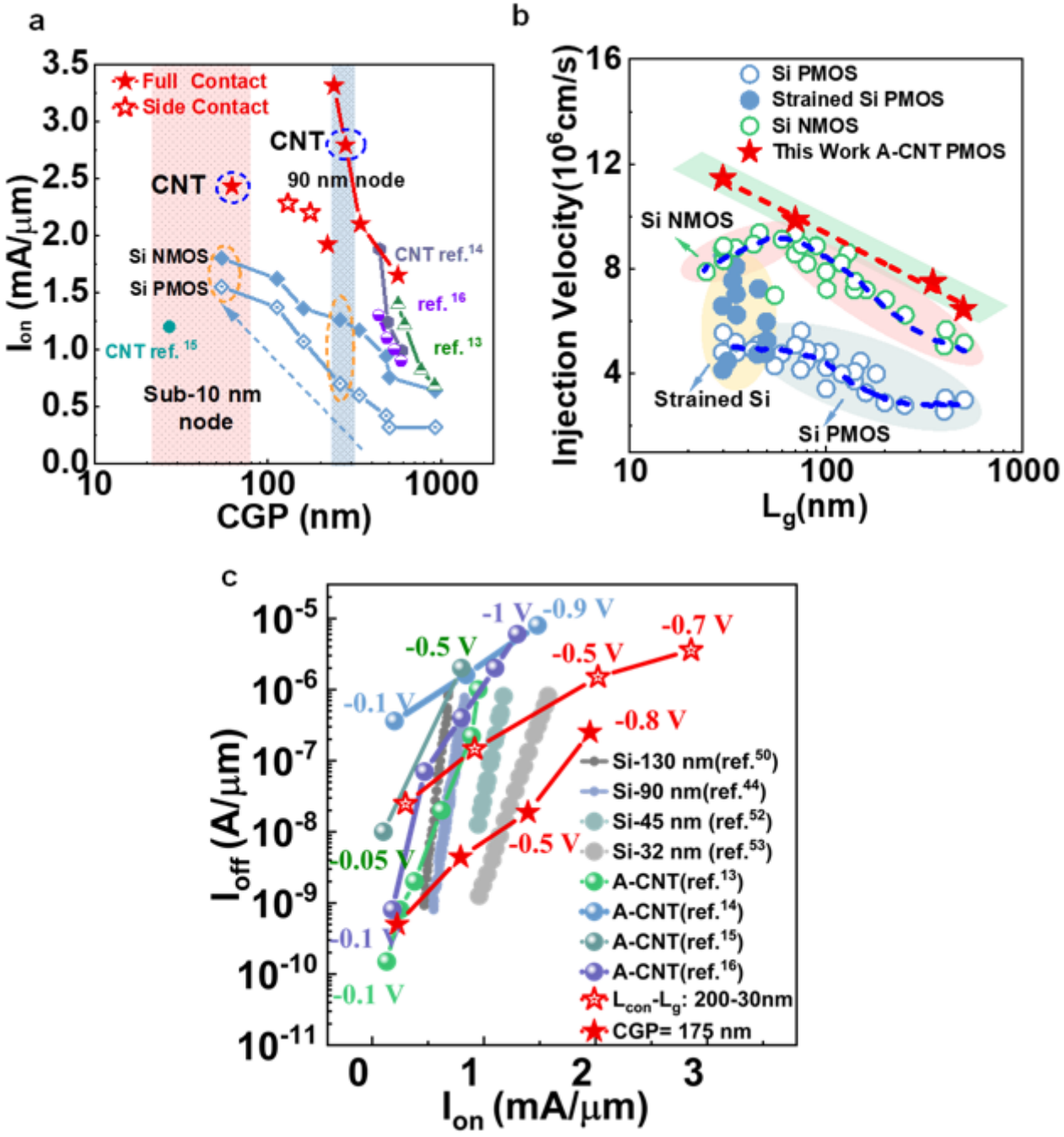

Figure 5

Benchmarking A-CNT FETs. a, Comparison of I_{on} at various CGP for A-CNT FETs in this work with that for other reported A-CNT FETs and silicon technology. **b,** Benchmarking the injection velocity of the aligned CNT arrays (all extracted by the VS model for CNT FETs) with that of Si FETs. **c,** Comparison of I_{on} versus I_{off} at different V_{ds} (increasing from left to right) for A-CNT FETs in this work with that for other reported A-CNT FETs and silicon technology. Note that here, I_{on} is the maximum on-current at the highest gate overdrive and I_{off} is the minimum off-current.

Supplementary Files

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