

# Efficient and Compact SR-flip Flop Optical Memory Based Photonic Crystals Platform

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## Research Article

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# Abstract

The paper presents a different type of designing methods and operational improvements of the optical logic memory SR-flip flop (SR-FF). The proposed optical memory SR-FF is based on two optical NOR logic gates which use two-dimension (2D) photonic crystal (PhC) with a square lattice of silicon (Si) dielectric rods. The structure has a switching time in only a few Picoseconds with little power input and very little power loss. The proposed optical memory SR-FF has a small dimension  $38 \times 22 \mu\text{m}^2$  which makes it one of the best optimized and most practical structures to be used in all photonic integrated circuits (PICs). The ultra-compact size enables the possibility of multiple devices to be embedded in a single PIC chip.

## 1 Introduction

The optical memory SR-FF is a fundamental technology for transparent fiber optical signal processing and the networks based on the optical mode. Recently, optical memories have been designed based on PhCs which are a periodical arrangement of dielectric materials. The PhCs are attractive optical materials for controlling and manipulating light flow that affects the motion of photons<sup>[4]</sup>. The light waves could not propagate through the PhC for some frequency ranges, this frequency ranges are called forbidden band gaps. Inspired by the references<sup>[4, 5, 6, 7, 8, 9, 10, 11, 12, 13]</sup>, the optical memory SR-FF has been proposed. The optical memory SR-FF is founded on optical NOR gates which composed of optical T-type switches, PhC ring resonators (PhCRRs), and a set of waveguides with optical power drivers Y-splitters. The proposed waveguides and Y-splitters are not standard another design based on a 2D-PhC slab in a silicon-on-insulator (SOI) material is used. Due to the Q-factor and the compact size, the proposed SR-FF has a switching time in only a few Picoseconds and little power input of 150 mW. The transmitted data will have remained in the optical domain without the need for the optical-electrical-optical (OEO) conversions<sup>[1]</sup>. The proposed SR-FF has output time response equal to 1.2ps with high switching rate up to 133GHz by comparing that in references<sup>[4, 14, 21]</sup>, which reaches up to 50, 44, and 100GHz respectively. Furthermore, the proposed SR-FF can keep its previous state with a small dimension  $38 \times 22 \mu\text{m}^2$  by comparing that in references<sup>[14, 21]</sup>, which use a structure dimension  $30 \times 30 \mu\text{m}^2$ . The remaining paper was arranged as follows, the considered PhC was explained in Sect. 2. The NOR optical gate design was explained in Sect. 3. The proposed optical memory SR-FF was introduced in Sect. 4. The results were discussed in Sect. 5. Finally, the fabrication efficacy was explained in Sect. 6.

## 2 Photonic Crystal Platform

The particular platform of interest here is the 2D-PhC slab as shown in Fig. 1(a). The 2D-PhC square lattice is made up of Si arranged in the air<sup>[20]</sup>. The radius of the Si rods ( $r_a$ ) is equal to  $0.2a$  in which ( $a$ ) is the lattice constant and set to 630 nm. The electric permittivity of the dielectric Si rods in the PhC platform is taken by,  $\epsilon_{(r)} = 11.492$  with refractive index  $n = 3.39$ . Figure. 1(b) shows the calculated band structure for the considered 2D-PhC platform. It can be observed from the figure that the bandgap lies in

the normalized frequency ( $\omega a/2\pi c$ ) for regions ( $0.29 \leq a/\lambda \leq 0.42$ ) and ( $0.725 \leq a/\lambda \leq 0.74$ ) where  $\lambda$  is the wavelength per primitive cell.

### 3 All-optical Mode Nor Gate

The optical NOR gate based on 2D-PhC has been formed by utilizing two optical T-shaped switches which composed of PhCRRs with T-type waveguides [11]. The proposed PhCRRs and T-type waveguides are formed by forming defects in the 2D-PhC structure in x-direction and y-direction as shown in Fig. 2. At the corners of the proposed PhCRRs, there are four extra Si rods with a radius of  $0.3a$  that were added in blue color to avoid the light wave back reflection.

Furthermore, the other four extra Si rods were also added with a radius of  $0.1a$  in green color within the PhCRR as shown in Fig. 2. It can be used to improve the interaction of wave and material within the PhCRR and for increasing the Q-factor which has a direct impact and effective contribution for the energy stored inside the proposed PhCRR. Additionally, the switch uses three ports, input port 'A' and pump port 'C' with forwarding transmission output port 'B'. Figure 3(a) describes the output power at port B when port C is OFF. In case of applying an optical signal at C (port C is ON), as a result of the optical power from port C nearby PhCRR, the optical signal from port A could not propagate to reach port B for some normalized frequency ranges which lie from  $a/\lambda = 0.392$  to  $a/\lambda = 0.398$  as shown in Fig. 3(b).

The proposed logic NOR gate is based on 2D-PhC of  $32 \times 16$  Si rods in the air with refractive index  $n = 3.39$  as shown in Fig. 4. The refractive index of the structure works at the wavelength of 1600 nm or 1580 nm. The optical NOR gate whole size is equal to  $21 \times 12 \mu\text{m}^2$ .

The optical NOR gate has been proposed using two cascade optical T-shaped switches with the same material and the same lattice constant radius. These two optical T-shaped switches were created with three ports, the first port is the 'BIAS' port which lies between 'C' and 'Q'. It has been created by eliminating a complete line of Si rods in the x-direction to propagate the data signal. The other two input control ports 'A' and 'B' were originated by eliminating twelve rods in y-direction for each in order to connect the logic input ports with the PhCRRs as shown in Fig. 4.

The optical wave at  $\lambda = 1600$  nm enters the structure from port C and the output status of the NOR gate will be controlled via A and B ports. The port Q is in OFF state when one or both logic inputs A and B are in ON state ( $A$  and/or  $B = 1$ ) as shown in Fig. 5 (a), (b), and (c) otherwise port Q turns ON as shown in Fig. 5(d). In other words, there is no output optical signal at port Q when one or both of PhC ring resonators are activated which controlled by input ports A and B. Table 1 expresses the truth table of the NOR gate in all-optical mode.

### 4 All-optical Mode Sr-ff

In [electronics](#), The SR-FF is one of the essential parts of the sequent logic circuits. SR-FF is a one-bit bistable memory device which has two stable states in which the data can be stored either binary 0 or binary 1 [12]. SR-FF can be also designed by cross-coupling of two NOR gates as shown in Fig.6. The SR-FF includes two inputs set (**S**) and reset (**R**) with two outputs (**Q**) and (**Q**). It has two stable states one is allocated to logic 0 values, the other is allocated to logic 1. By applying logic 1 to the **S** input the output **Q** is set to logic 1, returning the **S** to a low does not affect the output **Q** which stays set to logic 1. By applying logic 1 to the **R** input the output **Q** is reset to logic 0, returning the **R** input to a low does not affect the output **Q** which stays reset to the logic 0. By altering the inputs logic states to a low it can be observed that after SET or RESET states the output **Q** remembers its previous state. Table 2 summarizes the truth table for the logic SR-FF states.

Based on the principle of the sequent logic SR-FF circuit Fig. 6, the structure of the optical NOR gate Fig. 4, and the PhC platform bandgap diagram Fig. 1 the proposed optical memory SR-FF was composed as shown in Fig. 7. It can be observed from the figure that the proposed structure includes two input ports, **SET** and **RESET** with extra input bias ports **I<sub>1</sub>** and **I<sub>2</sub>**, and two output ports, **Q** and **Q**. The optical SR-FF consists of two optical NOR logic gates using four PhCRRs (PC-MRR1, PCMRR2, PC-MRR3, and PC-MRR4) and optical T-shaped waveguides connected to two Y-splitters. The optical power from waveguides is being split by optical PhC Y-splitters. The PhC power splitter transmission efficiency is 94 % with a splitting ratio of 50:50. The power from the waveguide is split into two identical halves through the splitter with the power of 47 % per halve from the power outflow of the main waveguide [9]. The quality of optical bends and junctions are very important during designing the PhC power splitter. The main waveguide channel **Y<sub>1</sub>** divides the optical signal from the bias port '**I<sub>1</sub>**' into two channels (**Y<sub>1A</sub>** and **Y<sub>1B</sub>**) **Y<sub>1A</sub>** transfer the optical signal toward port **Q** and **Y<sub>1B</sub>** is defined as feedback for NOR<sub>2</sub> while **Y<sub>2</sub>** divides the optical signal from the bias port '**I<sub>2</sub>**' into two channels (**Y<sub>2A</sub>** and **Y<sub>2B</sub>**) **Y<sub>2A</sub>** transfer the optical signal toward port **Q** and **Y<sub>2B</sub>** is defined as feedback for NOR<sub>1</sub> as shown Fig. 7. The operational wavelength for optical ports '**I<sub>1</sub>**' and SET '**S**' is  $\lambda_1=1600\text{nm}$ , while the operational wavelength for optical ports '**I<sub>2</sub>**' and RESET '**R**' is  $\lambda_2=1580\text{nm}$ .

## 5 Simulation Of Optical Sr-ff

This device includes two optical waves with different wavelengths. The normalized resonant frequencies of the structure is equal  $a/\lambda_1 = 0.3937$  for ports '**I<sub>1</sub>**' and Set '**S**' while equal  $a/\lambda_2 = 0.3987$  for ports '**I<sub>2</sub>**' and Reset '**R**'. The optical input power for each input port at the active state is equal to  $P_{in} \cong 150\text{mW}$  as shown in Fig. 10(a). The optical input power is spread equally through the activated input ports. The proposed optical SR-FF has mainly four states and one undefined state. For investigating the proposed SR-FF operations, Table 3 main status were simulated sequentially as follows:

- a. **Case 1** (Set case): If port SET (**S**) is at ON state (**S**=1) and port RESET (**R**) is at OFF state (**R**=0), due to the optical power from **S** port which near to the PC-MRR<sub>4</sub>, the value of the optical power from **I<sub>2</sub>** will be shifted to the resonant value of the PC-MRR<sub>3</sub>. The high Q-factor allows the light wave to be

localized within the PC-MRR<sub>3</sub> and to be confined by the total internal reflection and Bragg's reflection [11] in a lateral direction as shown in Fig. 8(a). Furthermore, the I<sub>1</sub> signal will propagate through waveguide Y<sub>1</sub> then passing through the Y<sub>1</sub> splitter which divides the wave power into two identical halves through two channels Y<sub>1A</sub> and Y<sub>1B</sub>. The optical power from channel Y<sub>1A</sub> will travel toward port Q output so port Q=1, while the power through the channel Y<sub>1B</sub> will keep the power signal localized inside the PC-MRR<sub>3</sub> as feedback for the second NOR<sub>2</sub> gate input as shown in Fig. 8(a). At port Q the output power will equal to 160 mW as demonstrates in Fig. 9(a) in green.

- b. **Case 2** (No change case): If port S is changed its state to S=0 and port R has remained as R=0, the optical 'I<sub>1</sub>' signal will be passed through channel Y<sub>1A</sub> to the output port 'Q', so Q remains as Q=1 with output power ≈150 mW as shown in Fig. 9(a) in blue. Due to the energy stored inside PC-MRR<sub>3</sub>, the optical 'I<sub>2</sub>' signal will still be prevented from passing through waveguide Y<sub>2</sub>, and Q will have remained as Q=0. Thus how SR-FF will keep its previous state (memorized its previous state), regardless of the change of S status as shown in Fig. 8(b).
- c. **Case 3** (Reset case): If port R is at ON state (R=1) and port S is at OFF state (S=0), due to the optical power from R port which near to the PC-MRR<sub>1</sub>, the value of the optical power from I<sub>1</sub> will be shifted to the resonant value of the PC-MRR<sub>2</sub>. This allows the light wave to be localized within the PC-MRR<sub>2</sub> and to be confined by the total internal reflection and Bragg's reflection in a lateral direction as shown in 8(c). Due to the destructive interferences from PC-MRR<sub>2</sub> through Y<sub>2B</sub>, the energy stored inside PC-MRR<sub>3</sub> will be lost. Furthermore, the I<sub>2</sub> signal will propagate through waveguide Y<sub>2</sub> then passing through Y<sub>2</sub>-splitter which divides the wave power into two identical halves through two channels Y<sub>2A</sub> and Y<sub>2B</sub>. The optical power from channel Y<sub>2A</sub> will travel toward port Q output so port Q=1, while the power through the channel Y<sub>2B</sub> will keep the power signal localized inside the PC-MRR<sub>2</sub> as feedback for the second NOR<sub>1</sub> gate input as shown in Fig. 8(c). At port Q The output power will equal 130 mW as demonstrates in Fig. 9(b) in green.
- d. **Case 4** (No change case): If port R is changed its state to R=0 and port S has remained at OFF state S=0, the optical 'I<sub>2</sub>' signal will be passed through channel Y<sub>2A</sub> to the output port 'Q', so Q remains as Q=1 with output power ≈90 mW as shown in Fig. 9(b) in blue. Due to the energy stored inside PC-MRR<sub>3</sub>, the optical 'I<sub>1</sub>' signal will be prevented from passing through waveguide Y<sub>1</sub>, and Q will have remained as Q=0 (the previous state is memorized) as shown in Fig. 8(d).

According to Fig. 9, it can be observed that the output power does not approach a constant value but it oscillates. Furthermore, the contrast ratio for the output power logic 0 (P<sub>0</sub>) and logic 1 (P<sub>1</sub>) is obtained as follows, P<sub>0</sub> is between 0 to 30 mW while P<sub>1</sub> is between 50 to 160 mW as summarized in Fig. 10(b). The truth table of the optical SR-FF at different states and the power contrast ratio is summarized in Table 3.

Figure. 11(a) summarizes the timing diagram for a sequence of events that were presented in Table 3. The simulation shows that by altering the SR-FF inputs state, the output rise time (t<sub>r</sub>) and the fall time (t<sub>f</sub>)

response for the proposed SR-FF memory is equal to 3ps and 1ps respectively as shown in Fig. 11(b). Additionally, the output time response is equal to 1.2ps with a switching rate reaches up to 133 GHz.

The ultra-confinement of light and the light-matter interaction brings the advantage of ultra-efficient to the proposed SR-FF optical memory. The proposed structure of optical SR-FF can be simply adjusted into D, T, and JK Flip flops by utilizing a group of logic gates in all-optical mode [6].

## 6 Feasibility Of Fabricating The Optical Sr-ff

Inspired by references, [15, 22], the proposed SR-FF can be fabricated by using low refractive index materials such as SiNx, SiOx, and polymers. The polymer layer pile can be implemented to reduce the out-of-plane scattering and increase efficiency. The implementation of the polymer layer pile between silicon rods reduces the lateral index contrast where the effective refractive index in the polymer pile is higher than the refractive index of air. The SR-FF waveguides are suspended in air in order to improve confinement in the vertical direction and symmetry properties of the structure [22].

## 7 Comparison

Table 4 shows the comparison between the proposed structure and the previous reverted structures. It can be observed from the table that Notomi *et al.* [14] forming the RS-FF with a switching rate of 44 GHz. Abbasi *et al.* [4] proposed RS-FF, with a switching rate of 50 GHz, which employed two nonlinear cavities with an elliptical core. Moniem [21] proposed the RS-FF based NOR gates which included four T-shaped nonlinear resonant rings with switching frequency 100 GHz. The proposed RS-FF has used four PhCRRs and two different wavelengths with a switching rate of 133 GHz. Finally, Table 4 shows that, the proposed optical memory SR-FF has a small dimension with switching time in only a few Picoseconds. The ultra-compact size gives the advantage of high transmission efficiencies and low power input with very little power loss. Furthermore, SR-FF can keep the previous states regardless of the input states which makes it one of the best optimized and most practical structures to be used in the PICs.

## 8 Conclusion

In this paper, the proposed optical SR-FF was designed by using a square array of dielectric with a dimension of  $38 \times 22 \mu\text{m}^2$  and lattice constant equal to 630 nm. Due to the small dimension, the proposed SR-FF can be embedded in the photonic integrated circuits. Additionally, the proposed SR-FF has a high time response that reaches up to 1.2ps with a switching rate equal to 133 GHz which would raise the efficiency of the optical data processing rate. The proposed SR-FF is utilizing the proposed PhCRRs and T-type waveguides which increase the Q-factor and reduce the out-of-plane scattering. The simulation is derived by applying two methods, (PWE) for calculating PBG and (FDTD) for solving Maxwell's equations. Finally, the proposed SR-FF can be used in the future to accelerate optical computing operations and optical signal processing. Furthermore, the data will remain in the optical mode without the need for OEO conversions, which would help for pushing forward the efficiency of the optical mode devices.

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## Tables

**Table 1. The truth table of the optical NOR gate at different input states.**

BIAS 'C'	Input port 'A'	Input port 'B'	Out port 'Q'
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

**Table 2. The truth table of SR-FF at different input states.**

SET	RESET	Q	$\bar{Q}$	state
1	0	1	0	SET
0	1	0	1	RESET
0	0	previous state	previous state	No Change
1	1	!	!	Undefined state

Table 3. The truth table of optical SR-FF at different input states with the power contrast ratio.

BIAS ( $I_1, I_2$ )/power(mW)		SET/power(mW)		RESET/power(mW)		Q/power(mW)		$\bar{Q}$ /power(mW)	
Logic	power(mW)	Logic	power(mW)	Logic	power(mW)	Logic	power(mW)	Logic	power(mW)
1	150	1	150	0	19	1	160	0	0 to 30
1	150	0	19	0	19	1	150 (memorized state)	0	0 to 30
1	150	0	19	1	150	0	0 to 30	1	130
1	150	0	19	0	19	0	0 to 30	1	90 (memorized state)
1	150	1	150	1	150	0	0 to 30	0	0 to 30

Table 4. The comparison between the proposed structure and the previous reverted structures.

Design	Input Power	Switching rate	Dimensions	Previous state
Abbasi <i>et al</i> [4]	50 mW	50 GHz	30x30 $\mu\text{m}^2$	Can't keep its previous state when inputs are inactive
Notomi <i>et al</i> [14]	50 mW	44 GHz	18x12 $\mu\text{m}^2$	Can't keep its previous state when inputs are inactive
Moniem [21]	50 mW	$\cong$ 100 GHz	30x30 $\mu\text{m}^2$	Keep its previous state by using output feedbacks
The proposed structure	150 mW	$\cong$ 133 GHz	38x22 $\mu\text{m}^2$	Keep its previous states when inputs are inactive by using the energy stored inside the PhCRRs

## Figures

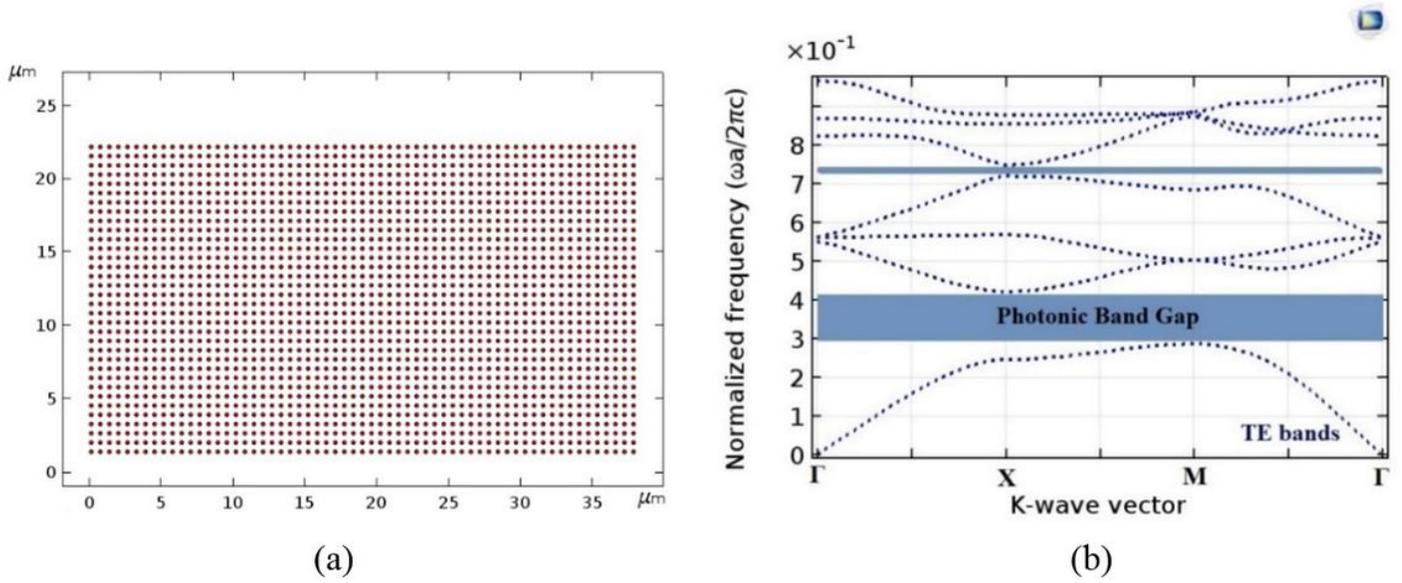


Figure 1

(a) the proposed PhC platform, (b) PhC band structure diagram.

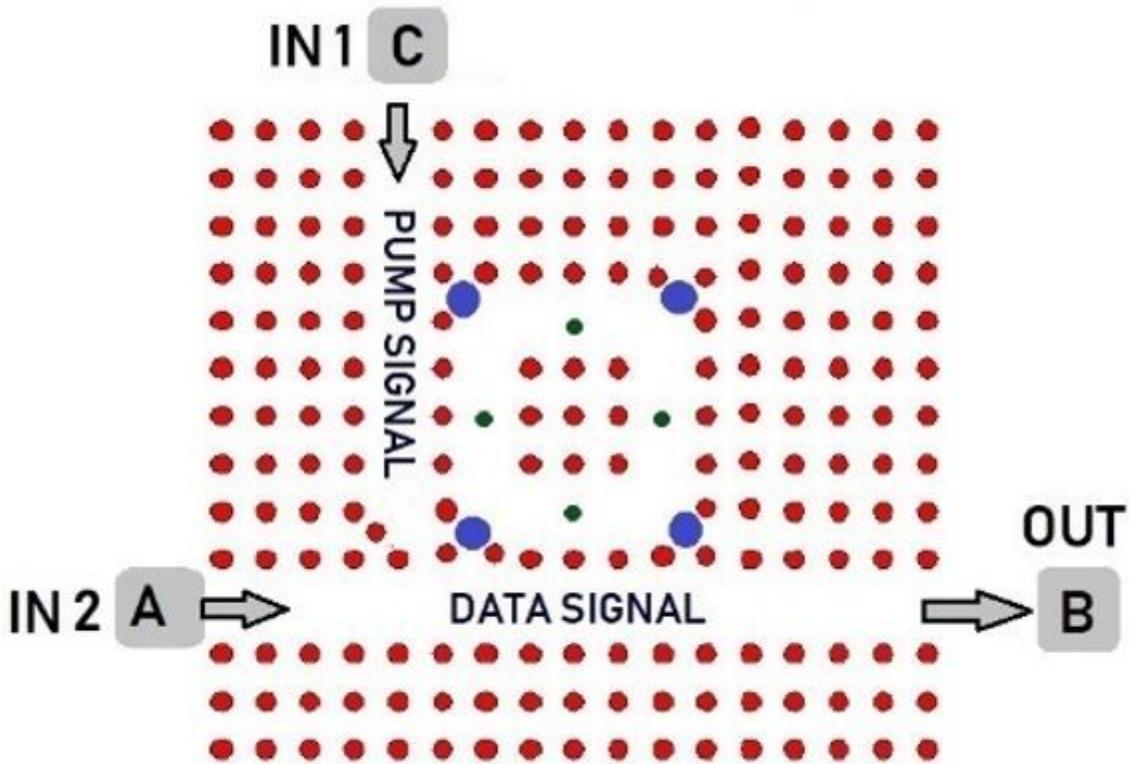
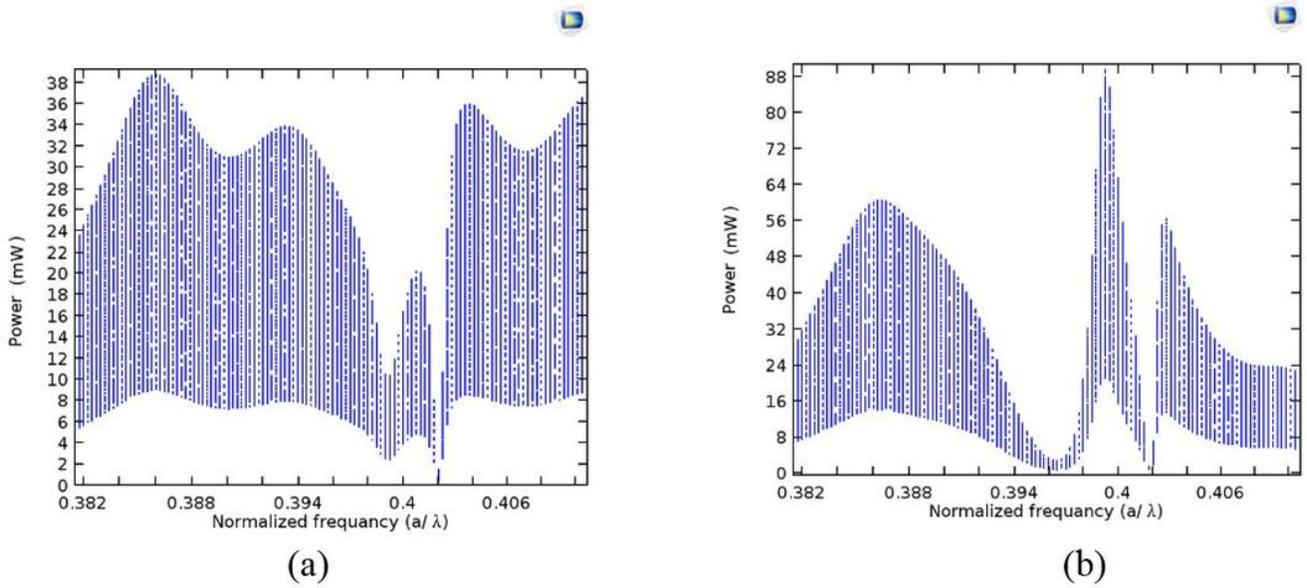


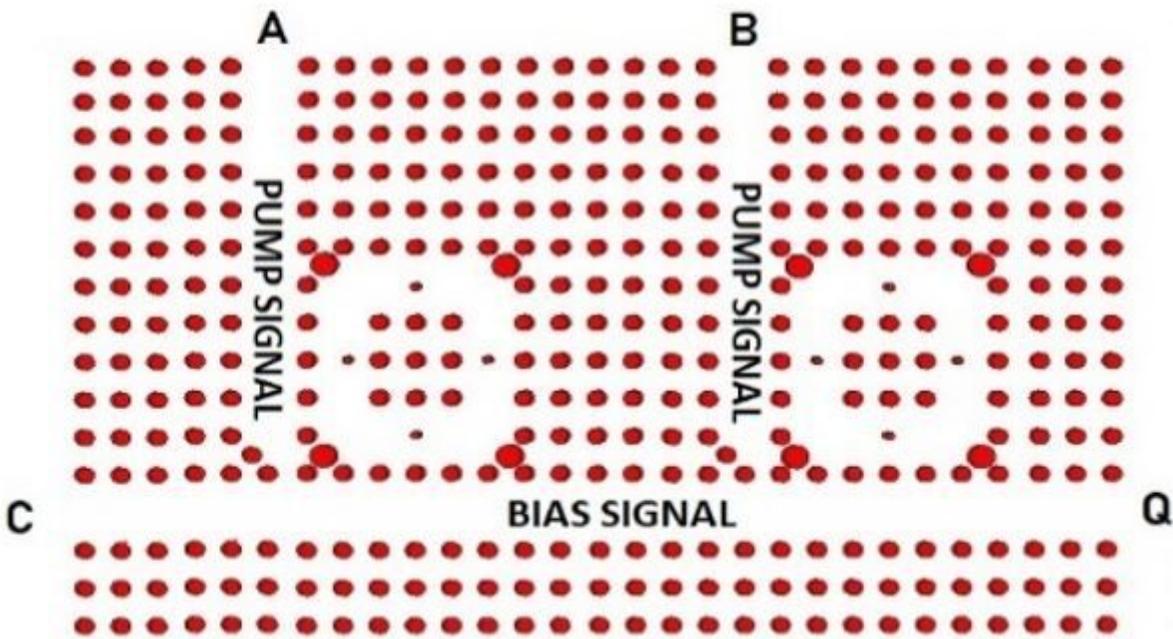
Figure 2

The proposed optical T-switch based on PhCRR.



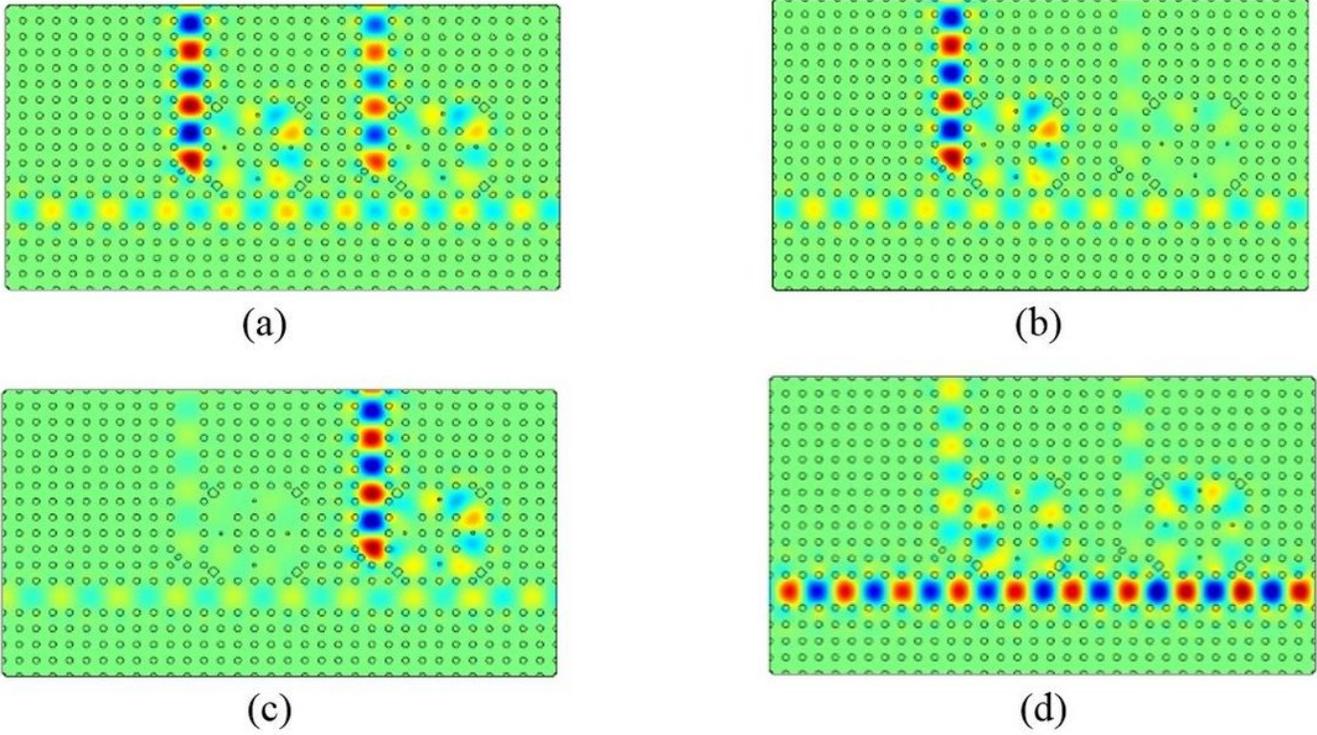
**Figure 3**

The proposed T-switch Transmission spectra at port B (a) when port C is OFF, (b) when port C is ON.



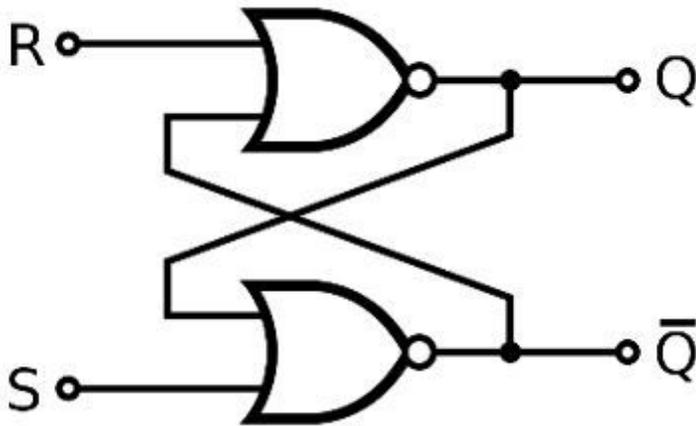
**Figure 4**

The proposed optical logic NOR gate.



**Figure 5**

NOR gate electric field pattern when the normalized frequency is equal to  $a/\lambda=0.3937$ , (a), (b), and (c) when logic inputs A and/or B are ON, (d) when logic inputs A and B are off.



**Figure 6**

The logic circuit diagram of SR-FF.

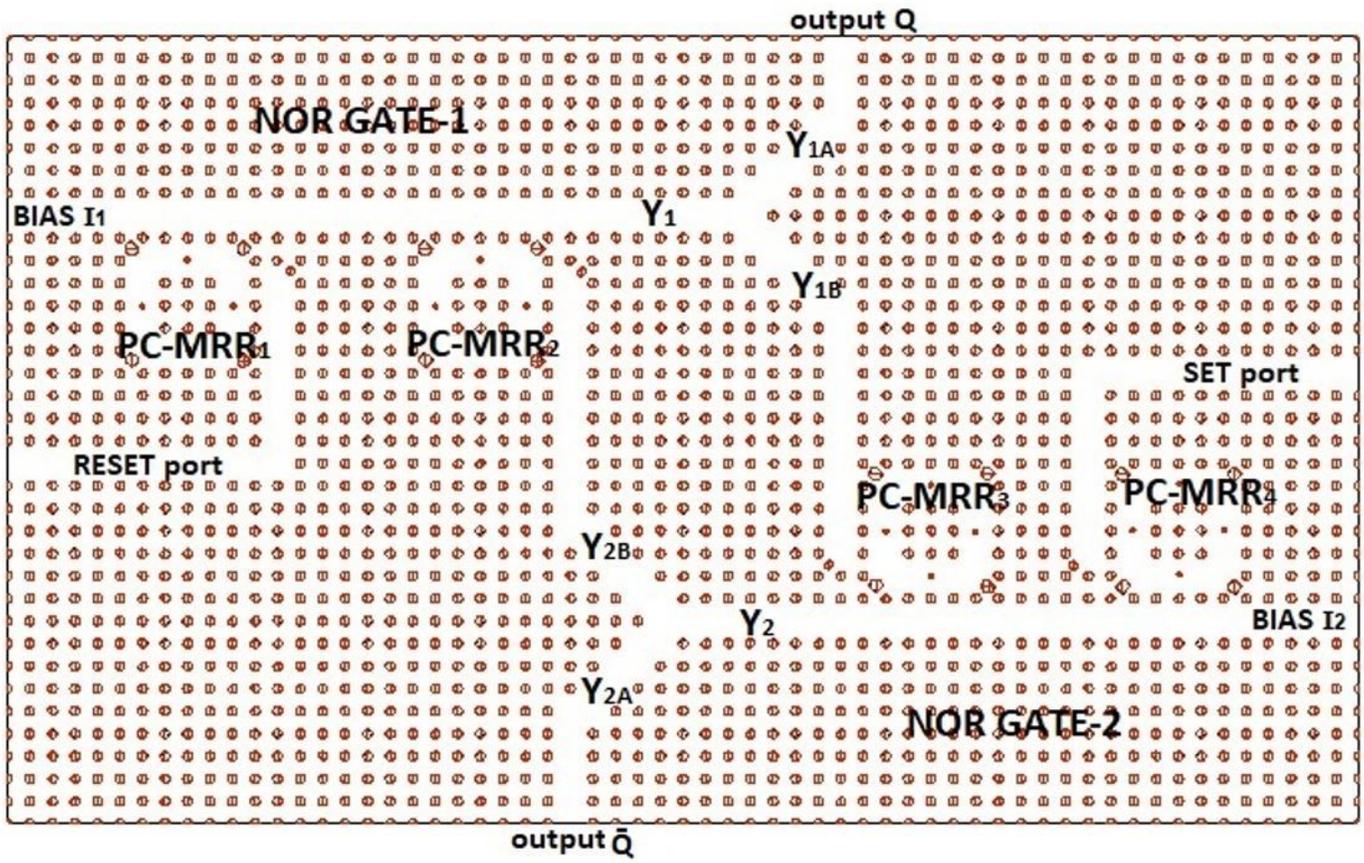
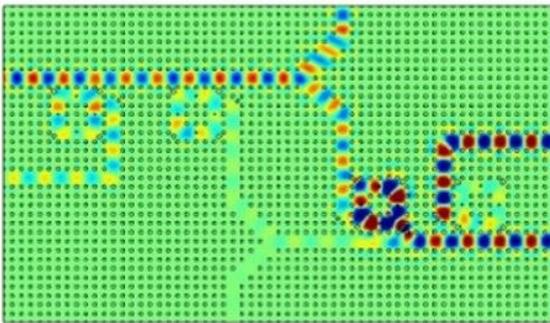
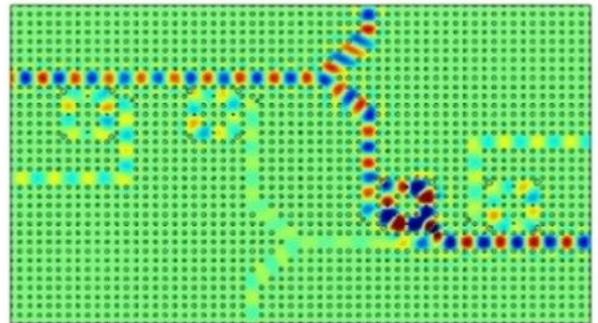


Figure 7

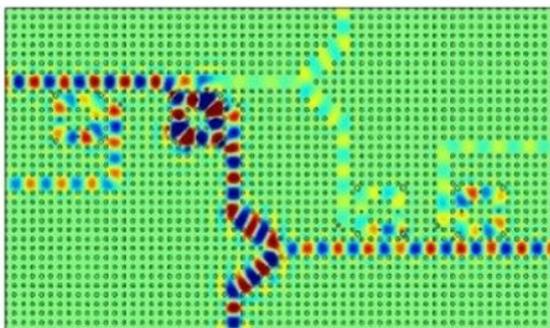
The proposed structure of optical SR-FF based on 2D-PhC.



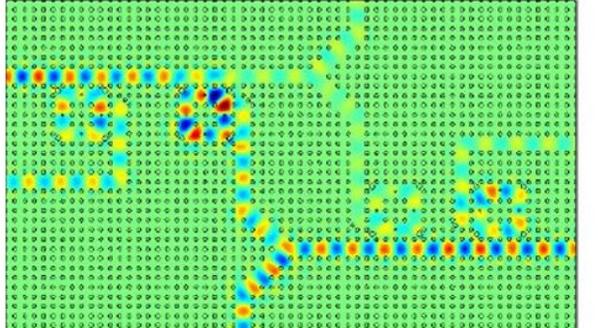
(a)



(b)



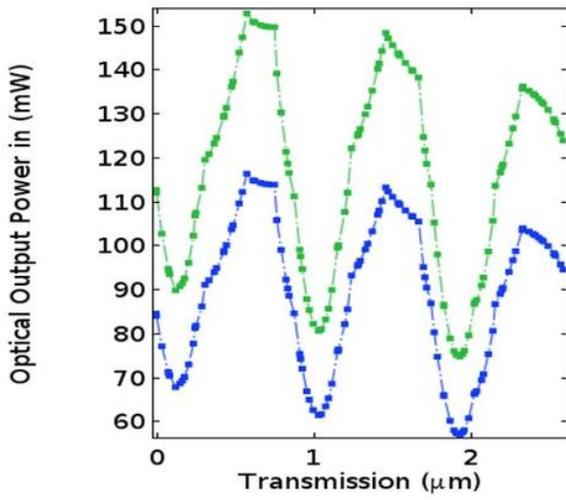
(b)



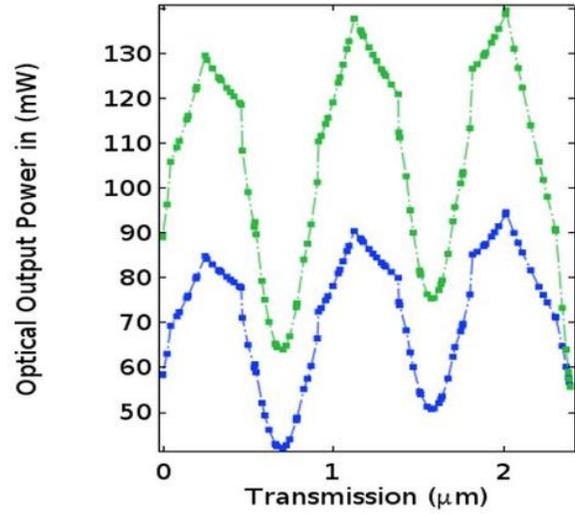
(d)

**Figure 8**

All-optical mode SR-FF electric field pattern, (a) Set state, (b) no change after Set state, (c) Reset state, and (d) no change after Reset state.



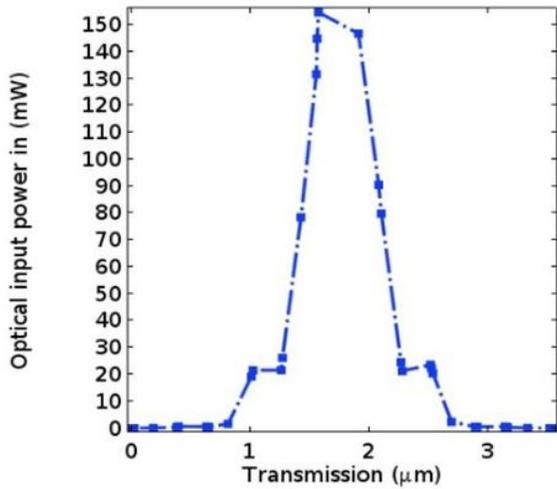
(a)



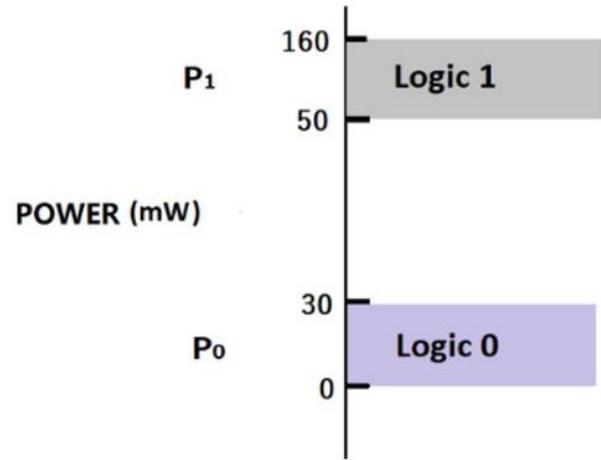
(b)

**Figure 9**

The optical output power (a) at port 'Q', (b) at port 'Q'.



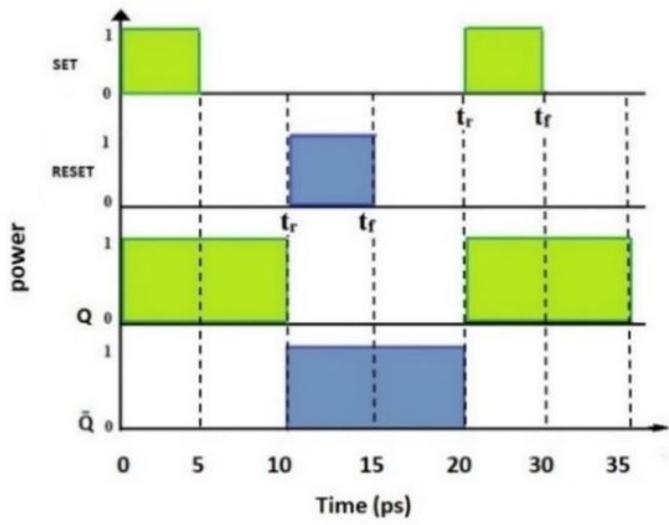
(a)



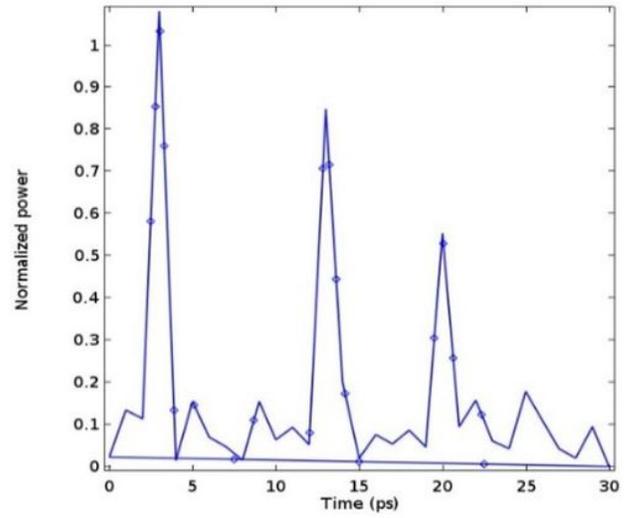
(b)

**Figure 10**

(a) input power for different ports, (b) the power ratio between the logic-0 and logic-1.



(a)



(b)

Figure 11

(a) The timing diagram for different SR-FF states, (b) the time response graph.