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Research Article

Keywords: ATOPs, thin-films, amorphous, VBD, AC-DC conversion, GaN

Posted Date: February 16th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-221354/v1

Amorphous thin-film oxide power devices operating beyond bulk single-crystal silicon limit

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Power devices (PD) are ubiquitous elements of the modern electronics industry that must satisfy the rigorous and diverse demands for robust power conversion systems that are essential for emerging technologies including Internet of Things (IoT), mobile electronics, and wearable devices. However, conventional PDs based on "bulk" and "single-crystal" semiconductors require high temperature (>1000°C) fabrication processing and a thick (typically a few tens to 100 μm) drift layer[1], thereby preventing their applications to compact devices[2], where PDs must be fabricated on a heat sensitive and flexible substrate. Here we report next-generation PDs based on "thin-films" of "amorphous" oxide semiconductors with the performance exceeding the silicon limit (a theoretical limit for a PD based on bulk

single-crystal silicon[3]). The breakthrough was achieved by the creation of an ideal Schottky interface without Fermi-level pinning at the interface, resulting in low specific on-resistance $R_{on,sp}$ (<1×10^{-4} Ωcm^2) and high breakdown voltage V_{BD} (~100 V). To demonstrate the unprecedented capability of the amorphous thin-film oxide power devices (ATOPs), we successfully fabricated a prototype on a flexible polyimide film, which is not compatible with the fabrication process of bulk single-crystal devices. The ATOP will play a central role in the development of next generation advanced technologies where devices require large area fabrication on flexible substrates and three-dimensional integration.

A power device (PD) is a general term for semiconductor on/off control elements, such as diodes and transistors for energy conversion (e.g. AC-DC conversion). Two important characteristics for designing PDs are specific on-resistance ($R_{on,sp}$) and breakdown voltage (V_{BD}). According to these parameters, the numerical factor related to the efficiency of power conversion, which is critical for PDs, is represented by the figure of merit (FOM) according to the following relationship[1,4]:

$$\mathrm{FOM} = V_{BD}^2/R_{on,sp} \quad (1),$$

which shows that a PD with low energy loss requires a large FOM value. Recently, application of materials such as gallium-nitride (GaN) and silicon-carbide (SiC) are being developed to replace single-crystal silicon (Si) because they are expected to exhibit higher FOM than Si[1,18]. However, PDs fabricated using these materials still suffer from fundamental constraints associated with "bulk" and "single-crystalline" materials that restrict the flexibility of designing devices (Fig. 1 bottom panel)[1,18,26]. Therefore, PDs based on "amorphous" and "thin-film" materials mitigate both of these problems and enable the fabrication of flexible devices using low temperature processes (Fig. 1 top panel). Although there have not been any reports of applications to date, amorphous oxide semiconductors (AOS) typically based on indium-gallium-zinc-oxide (InGaZnO)[5,6] are candidates for producing PDs because Schottky barrier diodes (SBDs) with low $R_{on,sp}$[7-10] and high V_{BD}[11,12] have been reported for these materials, with the high potential of achieving high FOM.

Results and discussion

To demonstrate the potential of amorphous thin-film oxide power devices (ATOPs), we first fabricated SBD structures to assess the basic performance of PDs with a view to realizing high FOM. Notably, in order to improve FOM, both low $R_{on,sp}$ and high V_{BD}

have to be achieved at the same time in spite of the trade-off between them[1]. In conventional AOS-SBD, the surfaces of Schottky electrodes of palladium (Pd) are oxidized with UV ozone treatment to improve the Schottky interface for lower $R_{on,sp}$ and higher V_{BD}[11,12]. With this approach, however, it is difficult to achieve high FOM because of a thin ~1 nm oxide layer on the Pd surface, resulting in insufficient Schottky interfaces which have relatively high resistance up to ~1×10^{-3} Ωcm^2 and low V_{BD} up to -16 V[11]. To resolve this problem, we used a much thicker palladium-oxide (PdO) layer and succeeded in forming PdO layers with arbitrary thicknesses by introducing oxygen-added sputtering, which has not been applied to AOS-SBD so far. As shown in Fig. 2a and b, a 40 nm-thick PdO layer drastically improved V_{BD} compared to AOS-SBD without PdO (Supplementary Fig. 1a, Supplementary Table 1a). Although the PdO layer led to an increase in $R_{on,sp}$ because of an additional contact resistance, we found that an insertion of a Pd/Titanium(Ti) layer under the PdO layer circumvented this issue, maintaining low $R_{on,sp}$ (Supplementary Fig. 1a, Supplementary Table 1a). Furthermore, we also developed a new method to control the drift layer thickness d, which is an important parameter as described later to maximize FOM for ATOPs. In contrast to conventional methods[13], which cannot produce uniform layers with the thicknesses larger than 50 nm, our method enables the formation of uniform layers up to ~1000 nm (Supplementary Fig. 2a-c) by adding water vapour during the sputtering (see Method). Accordingly, we succeeded in producing an SBD with V_{BD} that varied linearly with d (Supplementary Fig. 6, Supplementary Table 1a). Such an optimized SBD was also confirmed to have an ideal Schottky barrier without pinning[14,15] as shown in Fig. 2c and d.

The schematic illustration of ATOP that we fabricated based on InGaZnO-SBD is shown in Fig. 3a with the current density-voltage (J-V) dependence on the thickness of each layer and the area of top electrode. The characteristics of the device according to the Schottky theory[16] were determined from -5 V to +0.5 V in both forward and reverse directions and were independent of the drift layer thickness and the electrode size. This ATOP exhibited a superior SBD performance with a rectification ratio of over 10^{14}, a diode ideal factor (n) of approximately 1.1, and a Schottky barrier height (V_b) of 1.2 eV in the forward direction (Supplementary Table 1a). It should be noted that ATOP with 100 nm and 200 nm of d exhibited $R_{on,sp}$ <10^{-4} Ωcm^2 (Fig. 3b), which is difficult to realize even with a single-crystal semiconductor PD[17,18]. In the reverse direction, on the other hand, a flat thermionic emission current characteristic[19] was observed with less than 10^{-9} Acm^{-2} even under high electric fields before breakdown, which is also challenging even for a single-crystal SBD. The FOMs obtained for these ATOPs are comparable or even higher than theoretical values of single-crystal silicon[17,18,20], as shown in Fig. 3b.

To clarify the performance limit of ATOP with respect to $R_{on,sp}$ and V_{BD}, we first focused on $R_{on,sp}$. For a typical single-crystal PD based on drift conduction, $R_{on,sp}$ is given by $d/\mu nq$[1], where μ, n and q correspond to mobility, carrier density and elementary charge, respectively. It is important to notice that ATOP has a low $R_{on,sp}$ irrespective of the low μ (~10 $cm^2V^{-1}s^{-1}$; ~1/100 compared to Si in Fig. 1c) of AOSs. Therefore, we constructed a forward conduction model through the ATOP in Fig. 3c and d. As shown in the inset of Fig. 3d, the resistance of an SBD can be regarded as consisting of the two components with the diode at the Schottky interface and the resistance of the drift layer[1]. Notably the latter component is more important for PD design because it is common for a wide range of semiconductor elements. We confirmed that the diode component obeys the relationship based on the common thermionic emission theory through a Schottky contact[16] (Equation (1) in Method). As for the resistance of the drift layer, our new model (Equation (24) in Method) based on the space-charge limited current (SCLC) model[21,22] with a modification to account for AOS characteristics was found to be applied. It should be noted that the resistance model for the drift layer is not based on conventional drift conduction with single-crystal semiconductors, but on the SCLC conduction, which is current behaviour for the injection of external carriers into substances with low carrier density such as insulators. In the case of ideal solid insulators, the current density is given by $J_{SCLC,\ Std.} = 9\varepsilon\mu V^2/8d^3$ where ε is a dielectric constant; $J_{SCLC,\ Std.}$ is inversely proportional to the cube of d and proportional to the square of the divided voltage V to the drift layer. The characteristics according to the model (Equation (1), (3), (24) in Method) were experimentally confirmed in Fig. 3c and also for each temperature and thickness (Supplementary Fig. 3). Furthermore, in the region for applied voltage over 2 V, the resistance of the drift layer was confirmed to obey the ideal SCLC model of $J_{SCLC,\ Std.}$ (Supplementary Fig. 4a and b) described above. This behaviour can be ascribed to the reduced effect of trap levels[23] in the band-gap occupied by electrons supplied from top electrodes (Supplementary Fig. 4c). Figure 3d shows the simplified band diagram in the forward direction of the InGaZnO-SBD for applied voltages of 0 V and 3 V. This diagram shows that the diode component is dominant up to the built-in voltage V_{bi} of ~1.2 V (Fig. 3d left panel) and the SCLC conduction in the drift layer becomes dominant for higher applied voltages (Fig. 3d right panel). Since the ideal SCLC takes place for the low resistance region for applied voltages higher than 2 V in the case of an ATOP (Supplementary Fig. 4d), the $R_{on,sp}$ of ATOP can be approximated as follows:

$$R_{on,sp.} = \frac{dV}{dJ} \sim \frac{4d^3}{9\varepsilon\mu V} \qquad (2)$$

This equation shows that small d with large V leads to low $R_{on,sp}$. In the case of ATOP, d

is ~1/10 smaller than that of bulk single-crystal Si PD, achieving surprisingly low $R_{on,sp}$ (<10^{-4} Ωcm^2) in spite of low μ (~1/100), as shown in Supplementary Fig. 5a.

As for the V_{BD} that eliminates the effect of layer thickness, we focus on the breakdown electric field E_{BD}, which is a normalized value of V_{BD} divided by d. We found that the E_{BD} of all the devices we fabricated exhibited around 1 MVcm^{-1} (Supplementary Fig. 6, Supplementary Table 1a). While this value is already higher than that of single-crystal Si (~0.3 MVcm^{-1})[18], it is still lower than the expected value of approximately 3 MVcm^{-1} based on the critical breakdown field E_C[24]—intrinsic breakdown field determined by the properties of materials— estimated by the band-gap of InGaZnO, 3.2-3.3 eV (Supplementary Fig. 2f, Supplementary Table 1b). According to the capacitance-voltage (C-V) measurements and the depth profile of electric fields distribution in Fig. 3e and f (through Supplementary Fig. 7), respectively, it was confirmed that the local electric field concentrating at the PdO-InGaZnO interface (Fig. 3g) caused the breakdown with such a low electric field. It should be noted that the high electric field of 2.9-3.8 MVcm^{-1} in Fig. 3f, comparable to the estimated E_C values, was induced within 1 nm of the interface, resulting in the breakdown of the ATOPs. To achieve higher E_{BD}, an amorphous gallium-oxide (Ga_2O_3) layer having a wider band gap of 4.4 eV (Supplementary Fig. 1c and d, Supplementary Table 1b) was inserted between the PdO and InGaZnO layers. As the results shown in Supplementary Fig. 1c, the E_{BD} (~1.8 MVcm^{-1}) was improved to double that of a single PdO layer without sacrificing $R_{on,sp}$. This result demonstrates that E_{BD} can be improved close to E_C by optimizing the interface, showing that V_{BD} can be designed by the following equation (3) for ideal ATOP (Supplementary Fig. 5c):

$$V_{BD} \sim E_C \times d \qquad (3)$$

Accordingly, the FOM of ATOP can be described by the materials parameters as follows:

$$\mathrm{FOM} = V_{BD}^2/R_{on,sp} \sim 9\varepsilon\mu V E_c^{\,2}/4d \qquad (4)$$

Conclusions

The properties of the ATOPs fabricated in this study are summarized in Fig. 4a, comparing with conventional PDs. The theoretical limit of single-crystal Si can be estimated by FOM = $\varepsilon\mu E_c^{\,3}/4$ through materials parameters[1,4]. For the ATOP, on the other hand, a superior performance to single-crystal Si was confirmed for both experimental values and the theoretical limit estimated by equation (4). It is worth noting that the ATOP exhibits higher performance than GaN transistors[25], which have the advantage in lowering resistance, in the region with V_{BD} <100 V and $R_{on,sp}$ <10^{-4} Ωcm^2. This ultra-low resistance is one of the advantages of ATOP, which has almost no restriction on the type of substrate and is not significantly affected by the contact

resistance unlike that of the conventional PDs. Finally, we demonstrated the fabrication of devices on a flexible polyimide film (Fig. 4b-e), making most of the characteristics of ATOP that enables low temperature (≤300°C) sputtering on any type of substrate. ATOP has the potential to replace conventional bulk single-crystal PDs, thereby expanding the applications of PDs into new areas, where bulk single-crystal is intrinsically unable to reach.

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Acknowledgements:
We are grateful to N. Iwamuro, H. Tadano, H. Yano, R. Hasunuma and K. Yamabe (University of Tsukuba) for discussions about electrical characterization for power devices. We thank H. Tokairin, S. Ishii, A. Yao, Y. Harada and H. Kondo (Idemitsu Kosan Co., Ltd) for technical support of thin-film analysis and fabrication of flexible device. We

acknowledge A. Sandhu (The University of Electro-Communications) for helping with writing.

Contributions:

Y.T. conceived the idea for the study. E.K. designed the project. Y.T., E.K., and T.S. designed experiments and performed measurements. Y.N. prepared the samples by photolithography. Y.T. performed data analysis and developed the model. Y.T. wrote the first draft of the manuscript. Y.T. and E.K. drew the figures. T.S., G.I and G.Y. provided major revisions and verified the model. All authors read and commented on the manuscript.

Competing financial interests:

The authors declare no competing financial interests.

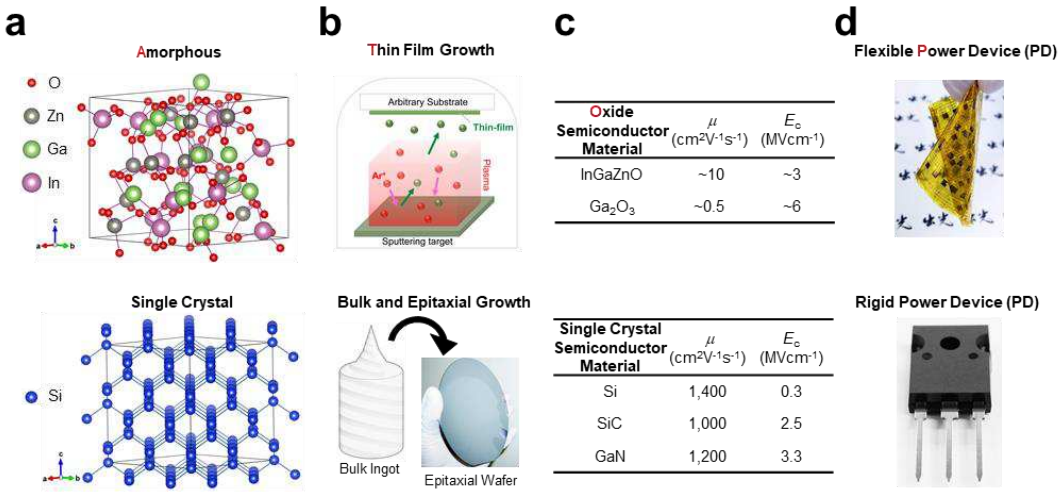


Fig. 1 | Concepts of amorphous thin-film oxide power device (ATOP, upper panel) compared with conventional bulk single crystal power device (PD, lower panel). a, Structures of amorphous indium-gallium-zinc-oxide (InGaZnO) and single crystal silicon (Si). **b,** Typical fabrication process of ATOP: thin-film growth on an arbitrary substrate by sputtering. That of the conventional PD: Bulk and epitaxial growth for bulk ingot and single-crystal semiconductor with the bulk substrate, respectively. **c,** Material parameters of measured mobility μ and estimated critical breakdown field E_C from measured bandgap for amorphous oxide semiconductor materials used in this work, and typical μ and E_C for conventional PD materials. **d,** PD structures of novel flexible ATOP and conventional rigid discrete.

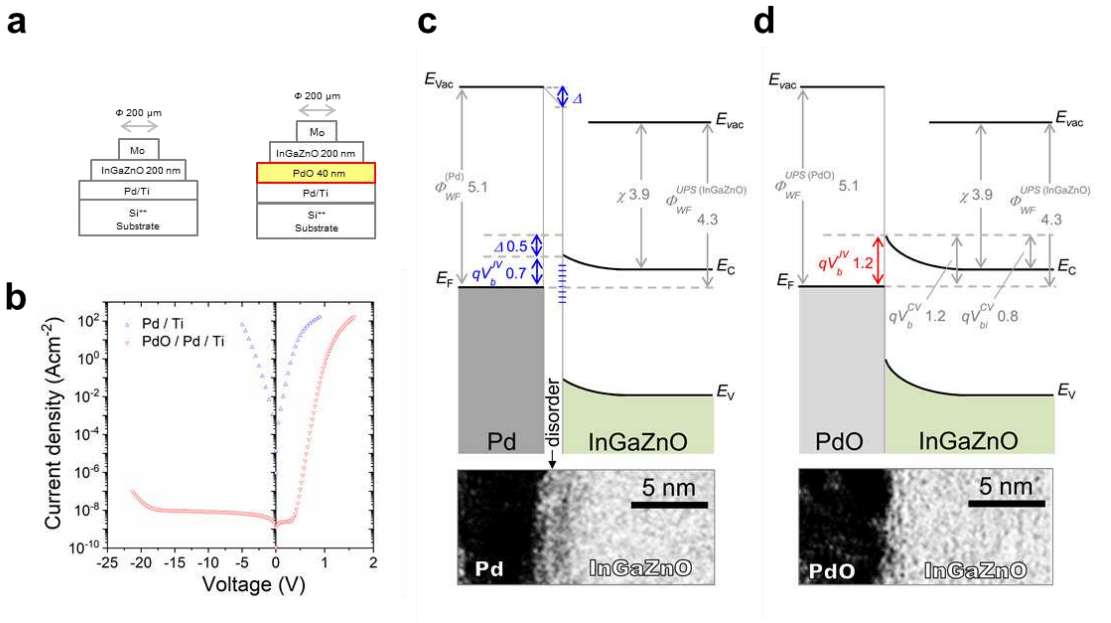
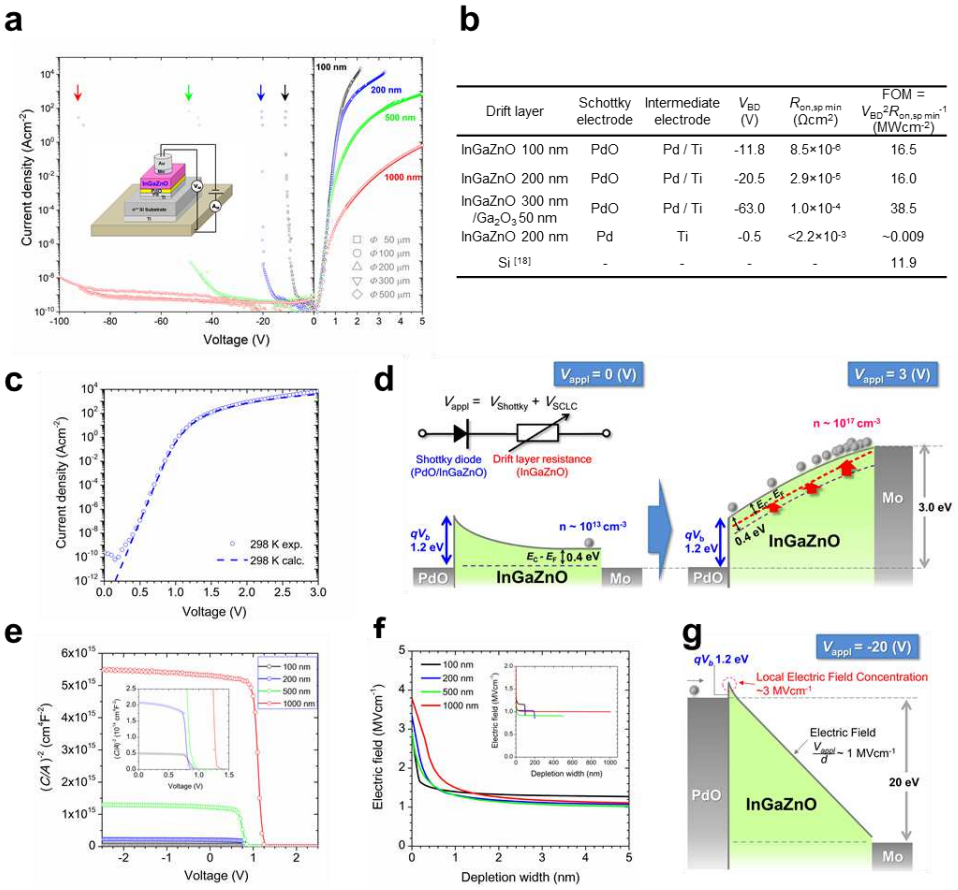


Fig. 2 | Schottky interface improved by palladium-oxide (PdO) layer for high breakdown voltage V_{BD}. a, Schematic images of Schottky barrier diode (SBD) structures with and without a PdO layer at the Schottky interface. **b,** Current density (J) – voltage (V) characteristics of before and after the optimization by PdO layer shown in (**a**). **c, d,** Band diagrams for the Schottky contact of Pd-InGaZnO and PdO-InGaZnO, respectively. The work function Φ_{WF}, Schottky barrier height V_b and built-in voltage V_{bi} were obtained from the results of UPS (from Supplementary Fig. 2e and Supplementary Table 1b), J-V (from Supplementary Table 1a) and Capacitance (C) – Voltage (V) (from Supplementary Table 1c) measurements, respectively. The semiconductor electronic affinity χ is determined by V_b^{CV}, V_{bi}^{CV} and $\Phi_{WF}^{(InGaZnO)}$. The interface dipole Δ is defined as $\Phi_{WF}^{(Metal)} - (J_b^{JV} + \chi)$. $\Delta = 0$ indicates no pinning effect at the Schottky interface: Pd-InGaZnO contact with pinning ($\Delta \neq 0$) and Pd-InGaZnO contact without pinning ($\Delta = 0$). Cross-sectional transmission electron microscope (TEM) images of the interface as shown in lower panel. The disordered interface, which can cause the pinning, is observed in (**c**).



Drift layer	Schottky electrode	Intermediate electrode	V_{BD} (V)	$R_{on,sp\ min}$ (Ωcm^2)	FOM = $V_{BD}^2 R_{on,sp\ min}^{-1}$ (MWcm^{-2})
InGaZnO 100 nm	PdO	Pd / Ti	-11.8	8.5×10^{-6}	16.5
InGaZnO 200 nm	PdO	Pd / Ti	-20.5	2.9×10^{-5}	16.0
InGaZnO 300 nm /Ga_2O_3 50 nm	PdO	Pd / Ti	-63.0	1.0×10^{-4}	38.5
InGaZnO 200 nm	Pd	Ti	-0.5	<2.2×10^{-3}	~0.009
Si [18]	-	-	-	-	11.9

Fig. 3 | Forward and reverse diode characteristics of ATOP. a, *J-V* characteristics of the ATOP with different drift layer thicknesses. The right and left sides show the forward and reverse characteristics with different scales in horizontal axes, respectively. The thicknesses and the sizes of Au/Mo top electrodes are indicated by different shapes and colours of each data point, respectively. The arrows indicate the breakdown voltage. **b,** Breakdown voltage V_{BD} and minimum specific on-resistance $R_{on,sp\ min}$ were obtained from *J-V* characteristics in (**a**). Figures-of-Merit (FOM) of power devices were calculated from V_{BD} and $R_{on,sp\ min}$. **c,** Forward characteristic of 200 nm SBD. The circles and the dashed line show the experimental data and the result of numerical calculation, respectively. The numerical calculation was performed on the basis of the new model taking account of the initial free carrier concentration n_0, using equation (24) in Method and fitting parameters with Supplementary Table 1d. **d,** Band diagrams for the forward characteristics in the 200 nm SBD. Left: Common Schottky operation at 0 V. Right: Dominant SCLC operation. The equivalent circuit at the top represents the Schottky-SCLC model with the diode component at the InGaZnO-PdO interface and variable resistance in the drift layer. **e** The calculated $(C/A)^{-2}$ (the capacitance(C) divided by the electrode area(A))– voltage(V) plots of the ATOPs in (**a**). **f,** Depth profile of electric fields distribution at the breakdown. **g,** Breakdown mechanism by the local electrical field concentration at the interface of InGaZnO-PdO at the breakdown voltage of 200 nm SBD.

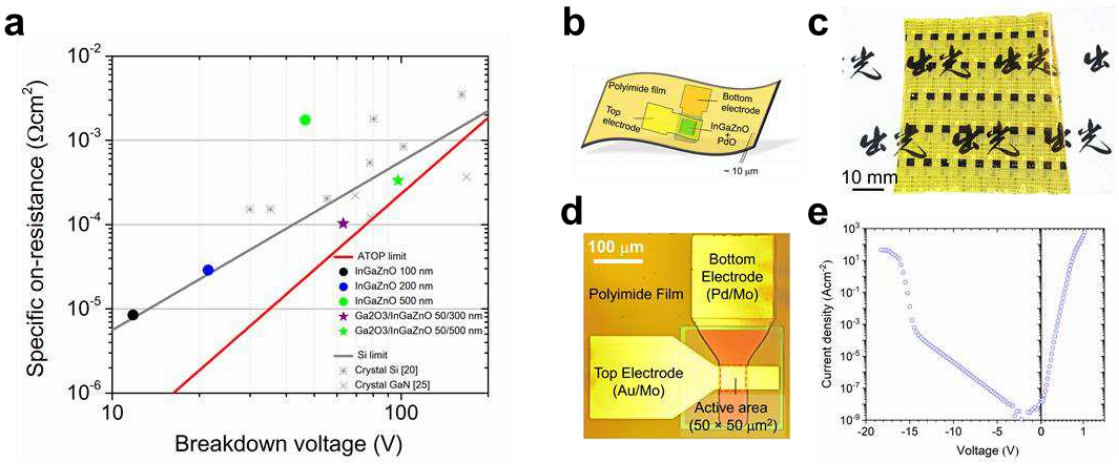


Fig. 4 | Figure-of-merits (FOM) for PDs and the demonstration of flexible ATOP. a, The relationship between breakdown voltage V_{BD} and on-specific resistance $R_{on,sp}$. The circles and the stars correspond to the present results of the single- and double-layer diodes, respectively. The asterisk and cross grey marks are taken from the references to Si and GaN single-crystal semiconductors, respectively. ATOP limit obtained from equation (4) with the parameters in Supplementary Fig. 5a and V at 5V. **b,** Schematic images of flexible ATOP (**c**) Photograph of ATOPs on polyimide film. **d,** Photograph of measured SBD on a flexible polyimide film with the optimized diode structure. **e,** J-V characteristics of SBD shown in (**d**).

Methods:

1. Device fabrication

Heavily doped n^{++} silicon (phosphorus doped, 1 mΩcm, 300 μm thick, Okmetic) was used as the substrate for the Schottky barrier diodes (SBDs). First, a 150 nm titanium (Ti) film was deposited on the backside of the silicon substrate by DC magnetron sputtering in argon (Ar) atmosphere at 0.5 Pa, as a backside electrode. Next, a 10 nm Ti and a 50 nm palladium (Pd) were deposited on the surface of the substrate under the same sputtering condition as both an adhesion layer and a contact resistance reducing layer. A 40 nm palladium-oxide (PdO) layer, which works as a Schottky electrode, was then deposited by DC magnetron sputtering in oxygen (O_2) atmosphere at 0.5 Pa. On the PdO layer, thin amorphous indium-gallium-zinc-oxide (InGaZnO) films with different thicknesses (*i.e.* 100 nm, 200 nm, 500 nm, and 1000 nm) were formed by DC magnetron sputtering of a InGaZnO ceramic target. During the sputtering, a 1% water vapour content (H_2O / Ar + H_2O) was introduced under the conditions of 0.5 Pa at room temperature. To form an amorphous gallium-oxide (Ga_2O_3) layer, Ga_2O_3 target was sputtered under the condition of 0.5 Pa and 1% partial pressure of O_2. All samples were then annealed at 300°C for 1 h in an air atmosphere. Finally, 150 nm Mo/ 500 nm gold (Au) was deposited as a top electrode by photolithography. We used different diameters of the electrodes ranging from 50 μm to 500 μm. To create a flexible device, ~10 μm polyimide film was spin-coated on a carrier glass wafer. Then, Mo/Pd layer was deposited as a bottom electrode. For the subsequent processes, the same processes described above were applied. Finally, flexible ATOP with 200nm InGaZnO is realized by peeling off the polyimide film from the carrier wafer.

2. Device evaluation

The current density-voltage (*J-V*) characteristics of the diodes were measured with a semiconductor parameter analyser (Agilent B1500 A). Current can be measured over a wide range (from 10^{-15} A to 1 A) owing to the several types of equipped SMUs (Source/Measure Unit) and ASU (atto-sense and switch unit). Capacitance-voltage (*C-V*) measurements were performed with an Agilent E4980A LCR meter under a frequency condition at 1 kHz. In both the *J-V* measurements and the *C-V* measurements including temperature dependence, the Ti backside electrode (the anodic electrode) was connected to the stage. Here, a Kelvin (4 probes/wire) connection was used to minimize the measurement error caused by parasitic resistance, that is the residual resistance of the connection cable and contact between the probe and electrode. For voltage measurement

and applied current, the two cathodic probes were connected to the top Au electrode of the device, while the two anode cables were connected to the stage. All measurements were performed in a black box with a semi-automatic probe station (Cascade Microtech PA200).

3. Diode analysis

(1) Forward characteristics

Current density J was defined as the current divided by the area of the top electrode. Basic transport properties of a Schottky junction are described by the following equations:

$$J = J_0\left[\exp\left(\frac{qV_{Schottky}}{nkT}\right)-1\right] \quad (1)$$

$$J_0 = A^{**}T^2\exp\left(\frac{-q\Phi_B}{kT}\right) \quad (2)$$

$$V_{Schottky} = V - V_{drift} \quad (3)$$

$$\Phi_B = -\frac{kT}{q}\ln\left(\frac{J_0}{A^{**}T^2}\right) \quad (4)$$

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln(J)}\right) \quad (5)$$

$$\ln\left(\frac{J_0}{T^2}\right) = \ln(A^{**}) - \frac{q\Phi_{B.M}}{kT} \quad (6)$$

where V_{Schottky} is the voltage applied to the Schottky interface, n is the ideality factor (n = 1 is the ideal value), Φ_B is the height of the Schottky barrier, k is the Boltzmann constant, q is the elementary charge, T is absolute temperature and V is the applied voltage to the device. Equation (2) shows the saturation current density J_0 and is equivalent to the intercept of ln$J$ in (1) [1]. Equation (3) shows the relationship between V_{Schottky}, V and V_{drift} (V_{drift} is the voltage distributed to the semiconductor drift layer) [2][3]. Equations (4) and (5) are derived from Equation (2) and (1), respectively. A^{**} is the effective

Richardson constant; the theoretical value for InGaZnO is 41 $Acm^{-2}K^{-2}$ (calculated from $m^* = 0.34\ m_e$) [4]. In this paper, Φ_B and n were calculated for $T = 298$ K and $A^{**} = 42$ $Acm^{-2}K^{-2}$. Φ_B and A^{**} were evaluated by the Richardson plot (Supplementary Fig. 8b). As shown in Equation (6), the mean barrier height $\Phi_{B.M}$, which is independent of A^{**} and T, is obtained by plotting J_0 against temperature T. Experimental results obtained with the 200 nm InGaZnO SBD was analysed according to Equation (6), resulting in $A^{**} = 42$ $Acm^{-2}K^{-2}$ and $\Phi_{B.M} = \Phi_B$.

(2) Reverse characteristics

Breakdown voltage V_{BD} is defined as the highest voltage that is recorded just before a current continuously exceeds 1 μA for more than three measurement points. In this study, it was found that the depletion width W_D is approximately the same as the film thickness d of the oxide semiconductor when a reverse voltage (negative bias) is applied (Supplementary Fig. 7a, Supplementary Table 1c). Therefore, it is reasonable to assume that the electric field is homogeneously distributed in the semiconductor drift layer. The breakdown strength E_{BD} was defined as the breakdown voltage V_{BD} divided by the film thickness d as the following form:

$$E_{BD} = \frac{V_{BD}}{d} \quad (7)$$

(3) CV measurements

From the measured capacitance of the diode C, the depletion width W_D at different voltages, the built-in voltage V_{bi}, and the charge density which contributes to the depletion layer N_{delp}, were obtained according to the following equations [1]:

$$W_D = \frac{\varepsilon_0 \varepsilon_r}{C} A \quad (8)$$

$$\frac{A^2}{C^2} = \left(\frac{2}{\varepsilon_0 \varepsilon_r N_{depl}} \right) \left(V_{bi} - V - \frac{kT}{q} \right) \quad (9)$$

where ε_r is the static dielectric constant of the semiconductor, ε_0 is the dielectric constant of a vacuum and A is the active area of the SBD. The Schottky barrier height $\Phi_{B,CV}$ can be calculated from the result of C-V measurements according to the following equation:

$$\Phi_{B,CV} = V_{bi} + \frac{kT}{q}\ln\left(\frac{N_c}{N_e}\right) \quad (10)$$

where N_C is the effective density of state in the conduction band. In the case of InGaZnO, N_C is 5.2 x 10^{18} cm^{-3} [5]. N_e is the free charge density, which can be experimentally obtained by Hall measurements.

(4) Power law

The forward *J-V* characteristics can be described as the following equation:

$$J = KV^m \quad (11)$$

where K is a constant and m is the power law index. By differentiating the logarithm of both sides of Equation (11), m is obtained the following equation:

$$m = \frac{d\log J}{d\log V} \quad (12)$$

Thus, m depends on V in the SCLC conduction according to the *J-V* relationship described as Equations (13) and (14). Based on this Equation (12), we discussed various conduction models (Equations (13), (14), and (24)) and the drift model ($J_{ohmic} = \mu nq\ V/\ d$) in Supplementary Fig. 4b.

(5) Existing SCLC model

The space charge limited current (SCLC) between two terminals forming Ohmic contacts can be explained by the Child's law for solids. In the simplest standard model, the relationship between current density $J_{SCLC,Std}$ and applied voltage V can be given as the following equation [6]:

$$J_{SCLC,Std.} = \frac{9\varepsilon\mu V^2}{8d^3} \quad (13)$$

where ε is the permittivity of the semiconductor, μ is the carrier mobility and d is the film thickness. When the carriers are affected by exponentially distributed traps (EDTs), the current changes according to the filling of traps below the quasi-Fermi level. Assuming the traps with an exponential energy distribution in the bandgap, the current $J_{SCLC,EDT}$ can be described by the following equation [7]:

$$J_{SCLC,EDT} = N_c \mu q \left(\frac{\varepsilon}{qN_t} \right)^l \left(\frac{l}{l+1} \right)^l \left(\frac{2l+1}{l+1} \right)^{l+1} \frac{V^{l+1}}{d^{2l+1}} \quad (14)$$

where N_c is the effective density of states, N_t is the total number of traps per unit volume. l is defined as $l = T_t / T$, where T_t is the characteristic temperature which determines the trap distribution. The validity of this model is supported by the result of deep-level transient spectroscopy (DLTS), which shows the distribution of the subgap states in the amorphous oxide semiconductor [8]. However, the effect of the free carrier concentration at the steady state was not considered in this model. Based on our model validation results, Equation (14) needs to be modified so as to include the effect of initial free carrier concentration. Therefore, referring to Reference [9], we expanded (14) to include the effect of the initial free carrier concentration.

(6) New SCLC model

We modified Equation (14) so as to include the effect of initial free carrier concentration n_0. According to the reference [9], the current considering $J_{SCLC,EDT,n0}$ can be described as follows:

$$J_{SCLC,EDT,n0} = q\mu n(x)E(x) = q\mu\left[n_0 + n_{i,f}(x)\right]E(x) \quad (15)$$

$$\frac{dE}{dx} = \frac{q}{\varepsilon} n_{inj}(x) = \frac{q}{\varepsilon}\left[n_{i,f}(x) + n_{i,t}(x)\right] \quad (16)$$

$$d = \int_0^d dx = \int_0^{E_d} \frac{dx}{dE} dE \quad (17)$$

$$V_{SCLC} = \int_0^d E(x)dx = \int_0^{E_d} E \frac{dx}{dE} dE \quad (18)$$

where $n(x)$ is the the carrier concentration contributing to conduction ($x = 0$ is the edge of the top electrode), $n_{i,f}(x)$ is the concentration of untrapped injected free carriers, $n_{i,t}(x)$ is the concentration of trapped injected carriers, and $n_{inj}(x)$ is the total concentration of injected carriers. Equations (15) and (16) show the drift current and Poisson's equation,

respectively. Equation (24) can be derived from Equations (15) and (16). Equations (17) and (18) show the boundary conditions. The diffusion current is not considered as its effect can be negligible in the present current region.

First, the exponential trap distribution $n_t(\varepsilon)$ is defined by the following equation:

$$n_t(\varepsilon) \equiv \frac{N_t}{kT_t} e^{(\varepsilon-\varepsilon_c)/kT_t} \quad (19)$$

where ε is the energy level of the trap states.

Using the Fermi-Dirac distribution as a step function, $n_{i,t}(x)$ can be written as shown in the following equation:

$$n_{i,t}(x) \equiv \int_{F_0}^{F(x)} n_t(\varepsilon)\, d\varepsilon = N_t \left[e^{(F(x)-\varepsilon_c)/kT_t} - e^{(F_0-\varepsilon_c)/kT_t} \right] \quad (20)$$

where F_0 is the Fermi level in thermal equilibrium. As the quasi-Fermi level $F(x)$ shows the depth dependence, the concentration of trapped injected electrons at a position x can be estimated from Equation (20). Since the concentration of the injected electrons is high near the cathode, the position of the quasi-Fermi level is also relatively closer to the conduction band in that region. To connect $n_{i,t}(x)$ with the concentration of total electrons that contribute to conduction, we rearrange Equation (20) by using the Boltzmann's distribution law:

$$n_{i,t}(x) = N_t \left[\left(\frac{n(x)}{N_c} \right)^{T/T_t} - \left(\frac{n_0}{N_c} \right)^{T/T_t} \right] \quad (21)$$

Equation (21) shows the trap distribution including the effect of the initial free carrier concentration. Based on Equation (21) and the Poisson's equation (16), the following equation can be derived:

$$\frac{dE}{dx} = \frac{q}{\varepsilon} n_{inj}(x) = \frac{q}{\varepsilon} \left\{ n(x) - n_0 + N_t \left[\left(\frac{n(x)}{N_c} \right)^{T/T_t} - \left(\frac{n_0}{N_c} \right)^{T/T_t} \right] \right\} \quad (22)$$

From Equations (15), Equation (22) can be written as

$$\frac{dE}{dx} = \frac{q}{\varepsilon}\left\{ \frac{J_{SCLC,EDT,n0}}{q\mu E(x)} - n_0 + N_t\left[\left(\frac{J_{SCLC,EDT,n0}}{q\mu E(x) N_c} \right)^{T/T_t} - \left(\frac{n_0}{N_c} \right)^{T/T_t} \right] \right\} \quad (23)$$

By integrating Equation (23), the voltage applied to the drift layer V_{SCLC} can be obtained, which represents a new SCLC model considering the effect of the initial free carrier concentration.

$$V_{SCLC} = \frac{\varepsilon}{q} \int_0^{E_d} \frac{E}{\frac{J_{SCLC,EDT,n0}}{q\mu E} - n_0 + N_t\left[\left(\frac{J_{SCLC,EDT,n0}}{q\mu E N_c} \right)^{T/T_t} - \left(\frac{n_0}{N_c} \right)^{T/T_t} \right]} dE \quad (24)$$

To determine E_d (a numerically calculated value), the boundary condition is written as follows:

$$d = \frac{\varepsilon}{q} \int_0^{E_d} \frac{1}{\frac{J_{SCLC,EDT,n0}}{q\mu E} - n_0 + N_t\left[\left(\frac{J_{SCLC,EDT,n0}}{q\mu E N_c} \right)^{T/T_t} - \left(\frac{n_0}{N_c} \right)^{T/T_t} \right]} dE \quad (25)$$

Here, $E(0)$ is set at 0. Note that Equations (24) and (25) must be calculated under the following conditions: $J_{SCLC,EDT,n0}$, $V_{SCLC} \geq 0$ and $E(x)$, $E_d \geq 0$. By using (24), it becomes possible to discuss the mechanism of EDT-type SCLC conduction, in which the concentration of free carriers at the steady state is considered.

To explain the experimentally-obtained J-V characteristics, we performed numerical calculations as the current density components of Equations (1) and (24) coincide with an intervening variable parameter of V_{SCLC}. In the new SCLC model described as Equation (24), we treated $J_{SCLC,EDT,n0}$ as an arbitrary input parameter. μ and n_0 are obtained through the Hall measurement. T_t and N_t are fitting parameters to obtain V_{SCLC} . The sample temperature was used for T, and ε was set at the converted value in the case of $\varepsilon_r = 16$ (determined from the C-V measurements). By verifying J in Equation (1) corresponding

to the arbitrary $J_{SCLC,EDT,n0}$ in Equation (24), comparison between the experimental results and the numerical calculation results can be possible. As J and $J_{SCLC,EDT,n0}$ should be the same value for the series circuit model as shown is Fig. 3d, V_{drift} in Equation (3) can be replaced by V_{SCLC} in Equation (24). Based on the results of the temperature dependence (Supplementary Fig. 8), Φ_B and n in Equation (1) are determined from Equations (4) and (5), respectively. Then, we can obtain J from Equation (1) through $V_{Schottky}$ as V-V_{SCLC}. In the case of $J = J_{SCLC,EDT,n0}$, the fitting parameter of T_t and N_t are correct.

(7) Estimation of E_c

The critical breakdown field E_c (the maximum electric field at the Schottky interface when the breakdown voltage V_{BD} is applied) can be estimated according to the relationship between the depletion layer width W_D and the charge concentration contributing to the depletion layer N_{depl} as shown in Equations (8) and (9). The calculations were performed with a model that considers the charge density distribution of a one-sided abrupt junction [10]. We assumed that the effect of minority carriers on the space charge formation is negligible. By using the depth profile of N_{depl} obtained from the C-V measurements, the field distribution in the film thickness direction can be calculated by the following equation:

$$\frac{dE}{dx} = -\frac{q}{\varepsilon} N_{depl} \quad (26)$$

As the reverse current is almost 0, Equation (26) can be written as the following form:

$$E(x) = -\frac{q}{\varepsilon}\int_0^x N_{depl}\, dx + E(0) \quad (27)$$

By integrating Equation (27), V can be described as

$$V = -\frac{q}{\varepsilon}\int_0^{W_D} \left(\int_0^x N_{depl}\, dx \right) dx + E(0) W_D \quad (28)$$

where $E(x)$ is the electric field intensity at a position x, and $E(0)$ is the electric field at the Schottky interface. W_D can be approximated to d as the depletion layer is formed through the whole diode even at 0 V. From the definition of E_c, $E(0)$ can be replaced by E_c when the breakdown voltage V_{BD} is applied. Then, Equation (28) can be written as the following form:

$$V_{BD} = -\frac{q}{\varepsilon}\int_0^{W_D}\left(\int_0^x N_{depl}\,dx\right)dx + E_C W_D \quad (29)$$

E_c can be estimated from Equation (29) by using the profiling of E as described in Equation (27). V_{BD} and the N_{depl} profile for W_D can be experimentally obtained from the J-V characteristics and the results of the C-V measurements. The resolution of this technique depends on the Debye screening length; that is, the length by the influence of the impurity concentration in the semiconductor. Thus, the resolution is better than 1 nm for $N_{depl} > 10^{19}$ cm^{-3} at the Schottky interface. [11],[12]

4. Characterization of thin film

Cross-sectional observation of the SBDs by transmission electron microscopy (TEM) was performed with a focused-ion-beam device (FB-2100, Hitachi) and TEM (JEM-2800, JEOL). TEM observations were performed at an accelerating voltage of 200 keV. X-ray diffraction (XRD) was performed with a Rigaku SmartLab system under a condition of 40 kV and 40 mA by using the Cu-Kα line (l.5406 Å). The same XRD system was also used to evaluate the crystallinity of the thin films: the grazing incident X-ray diffraction (GIXD, angle of incidence ω) and the conventional θ−2θ scan (XRD). The thin film samples were deposited on a quartz glass substrate for the XRD measurements and annealed at 300°C for 1 h before the measurement. The GIXD measurement was performed for a multilayer sample of PdO thin films to avoid the change in crystallinity by annealing on a different substrate. This analysis was also done in the multilayer condition of the actual diode structure to avoid transformation of the polycrystalline structure of the PdO during annealing on a different substrate.

To estimate the bandgap E_g, UV-VIS spectroscopy (V-370, JASCO) was performed for the thin film samples deposited on quartz glass substrates. The samples were annealed before the measurement. The work function Φ_{WF} was determined by using ultraviolet photoelectron spectroscopy (UPS) by focusing on the secondary electron cutoff. Monolayer thin films deposited on a Si substrate were used as samples. In the UPS measurements, monochromatized 7.7 eV photons from a D2 lamp were used, and a negative bias of 10 V was applied to the sample. A customized system equipped with a zero-dispersion type double monochromator and a 120 mm hemispherical analyser (PSP Vacuum Technology RESOLVE120) was used for the measurement.

Hall mobility μ_{Hall}, the free electron carrier concentration n_{Hall} and the specific electrical resistance ρ were obtained with a Hall measurement system (ResiTest 8400, TOYO

Corporation) by using an AC magnetic field. The measurements were performed with the Van der Pauw method at room temperature. Thin films deposited on quartz glass substrates (10 mm × 10 mm) were used as samples. The samples were annealed before the measurement, and indium electrodes were deposited on the 4 corners of the samples.

5. References

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Figures

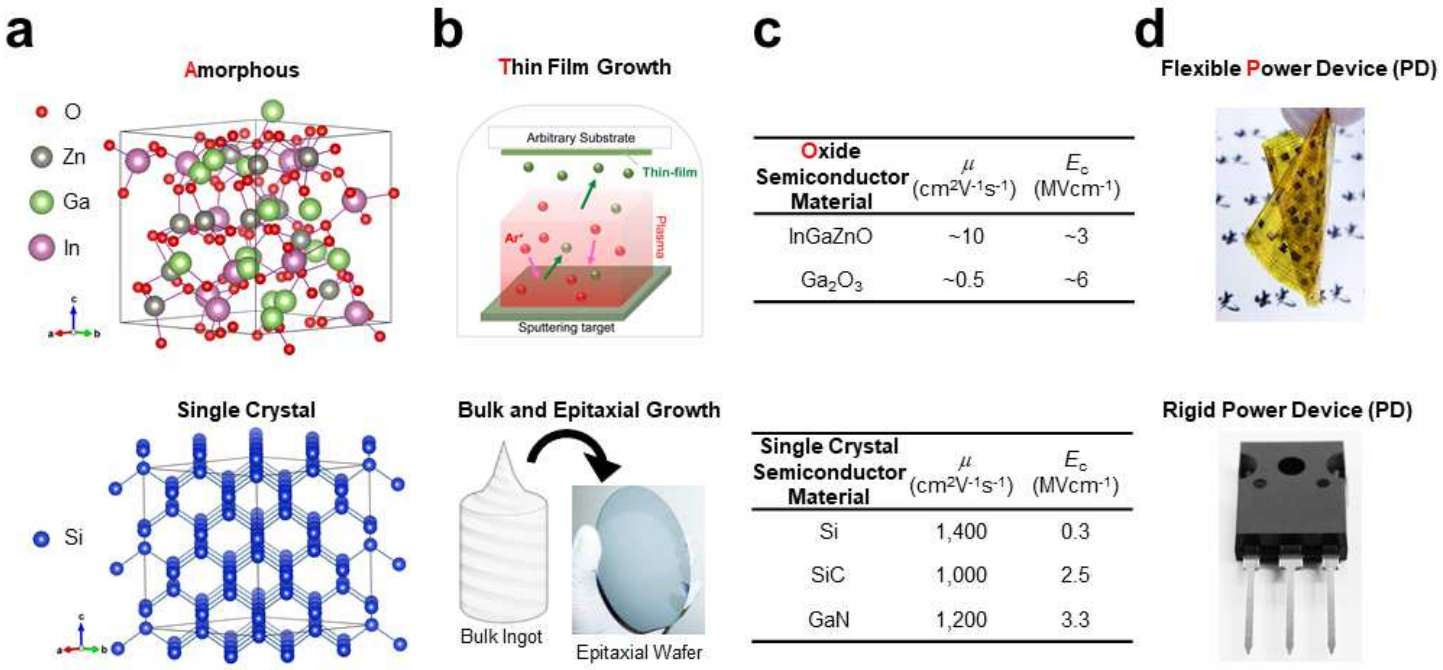


Figure 1

Concepts of amorphous thin-film oxide power device (ATOP, upper panel) compared with conventional bulk single crystal power device (PD, lower panel). a, Structures of amorphous indium-gallium-zinc-oxide (InGaZnO) and single crystal silicon (Si). b, Typical fabrication process of ATOP: thin-film growth on an arbitrary substrate by sputtering. That of the conventional PD: Bulk and epitaxial growth for bulk ingot and single-crystal semiconductor with the bulk substrate, respectively. c, Material parameters of measured mobility μ and estimated critical breakdown field EC from measured bandgap for amorphous oxide semiconductor materials used in this work, and typical μ and EC for conventional PD materials. d, PD structures of novel flexible ATOP and conventional rigid discrete.

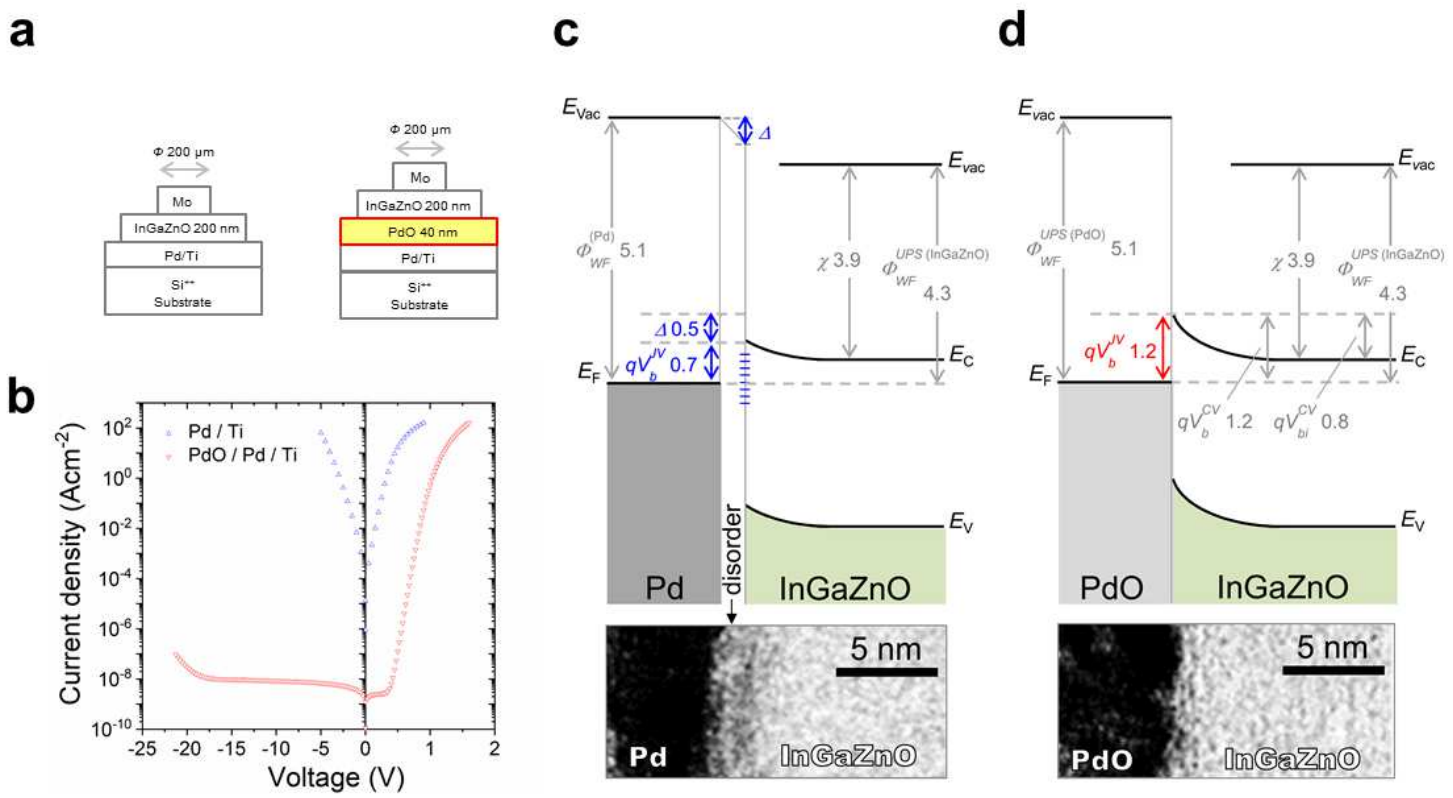
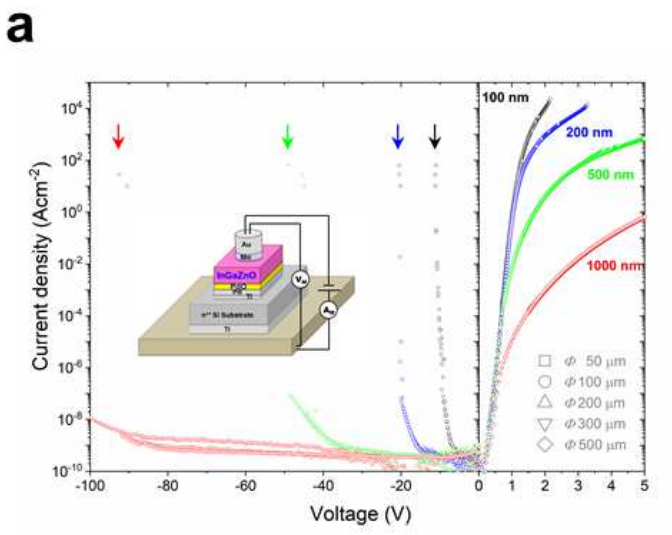


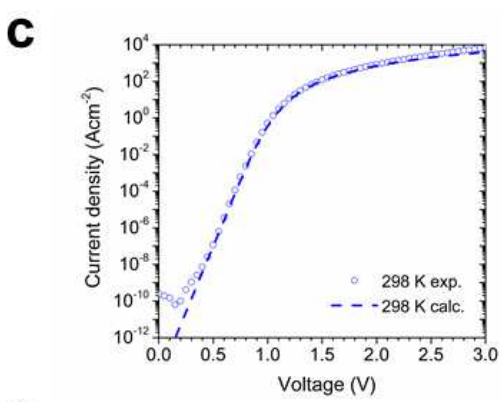
Figure 2

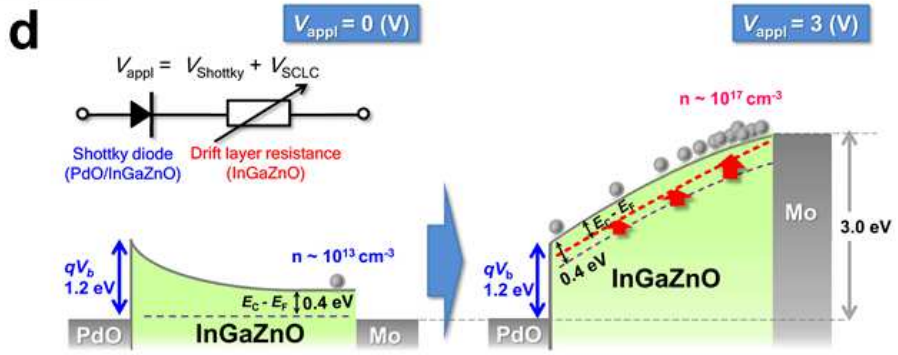
Schottky interface improved by palladium-oxide (PdO) layer for high breakdown voltage VBD. a, Schematic images of Schottky barrier diode (SBD) structures with and without a PdO layer at the Schottky interface. b, Current density (J) – voltage (V) characteristics of before and after the optimization by PdO layer shown in (a). c, d, Band diagrams for the Schottky contact of Pd-InGaZnO and PdO-InGaZnO, respectively. The work function ΦWF, Schottky barrier height Vb and built-in voltage Vbi were obtained from the results of UPS (from Supplementary Fig. 2e and Supplementary Table 1b), J-V (from Supplementary Table 1a) and Capacitance (C) – Voltage (V) (from Supplementary Table 1c) measurements, respectively. The semiconductor electronic affinity χ is determined by VbCV, VbiCV and ΦWF(InGaZnO). The interface dipole Δ is defined as ΦWF(Metal) – (JbJV + χ). Δ = 0 indicates no pinning effect at the Schottky interface: Pd-InGaZnO contact with pinning (Δ ≠ 0) and Pd-InGaZnO contact without pinning (Δ = 0). Cross-sectional transmission electron microscope (TEM) images of the interface as shown in lower panel. The disordered interface, which can cause the pinning, is observed in (c).

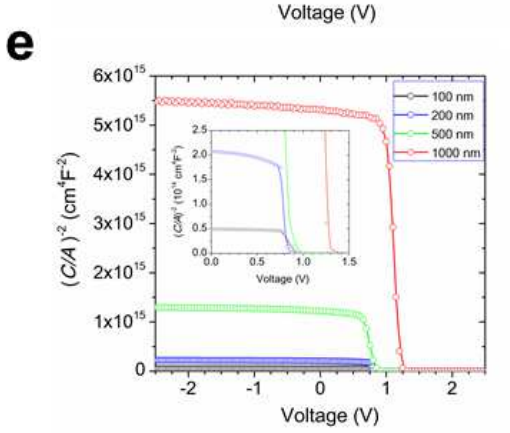


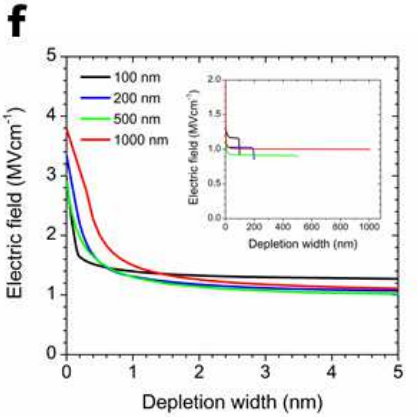
b

Drift layer	Schottky electrode	Intermediate electrode	V_{BD} (V)	$R_{on,sp\ min}$ (Ωcm^2)	FOM = $V_{BD}^2 R_{on,sp\ min}^{-1}$ ($MWcm^{-2}$)
InGaZnO 100 nm	PdO	Pd / Ti	-11.8	8.5×10^{-6}	16.5
InGaZnO 200 nm	PdO	Pd / Ti	-20.5	2.9×10^{-5}	16.0
InGaZnO 300 nm /Ga_2O_3 50 nm	PdO	Pd / Ti	-63.0	1.0×10^{-4}	38.5
InGaZnO 200 nm	Pd	Ti	-0.5	$<2.2\times10^{-3}$	~0.009
Si [18]	-	-	-	-	11.9









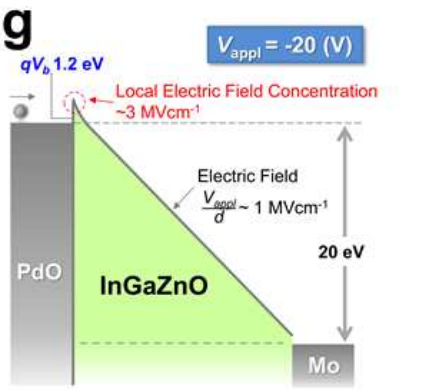


Figure 3

Forward and reverse diode characteristics of ATOP. a, J-V characteristics of the ATOP with different drift layer thicknesses. The right and left sides show the forward and reverse characteristics with different scales in horizontal axes, respectively. The thicknesses and the sizes of Au/Mo top electrodes are indicated by different shapes and colours of each data point, respectively. The arrows indicate the breakdown voltage. b, Breakdown voltage VBD and minimum specific on-resistance Ron,sp min were obtained from J-V characteristics in (a). Figures-of-Merit (FOM) of power devices were calculated from VBD and Ron,sp min. c, Forward characteristic of 200 nm SBD. The circles and the dashed line show the experimental data and the result of numerical calculation, respectively. The numerical calculation was performed on the basis of the new model taking account of the initial free carrier concentration n0, using equation (24) in Method and fitting parameters with Supplementary Table 1d. d, Band diagrams for the forward characteristics in the 200 nm SBD. Left: Common Schottky operation at 0 V. Right: Dominant SCLC

operation. The equivalent circuit at the top represents the Schottky-SCLC model with the diode component at the InGaZnO-PdO interface and variable resistance in the drift layer. e The calculated (C/A)-2 (the capacitance(C) divided by the electrode area(A))– voltage(V) plots of the ATOPs in (a). f, Depth profile of electric fields distribution at the breakdown. g, Breakdown mechanism by the local electrical field concentration at the interface of InGaZnO-PdO at the breakdown voltage of 200 nm SBD.

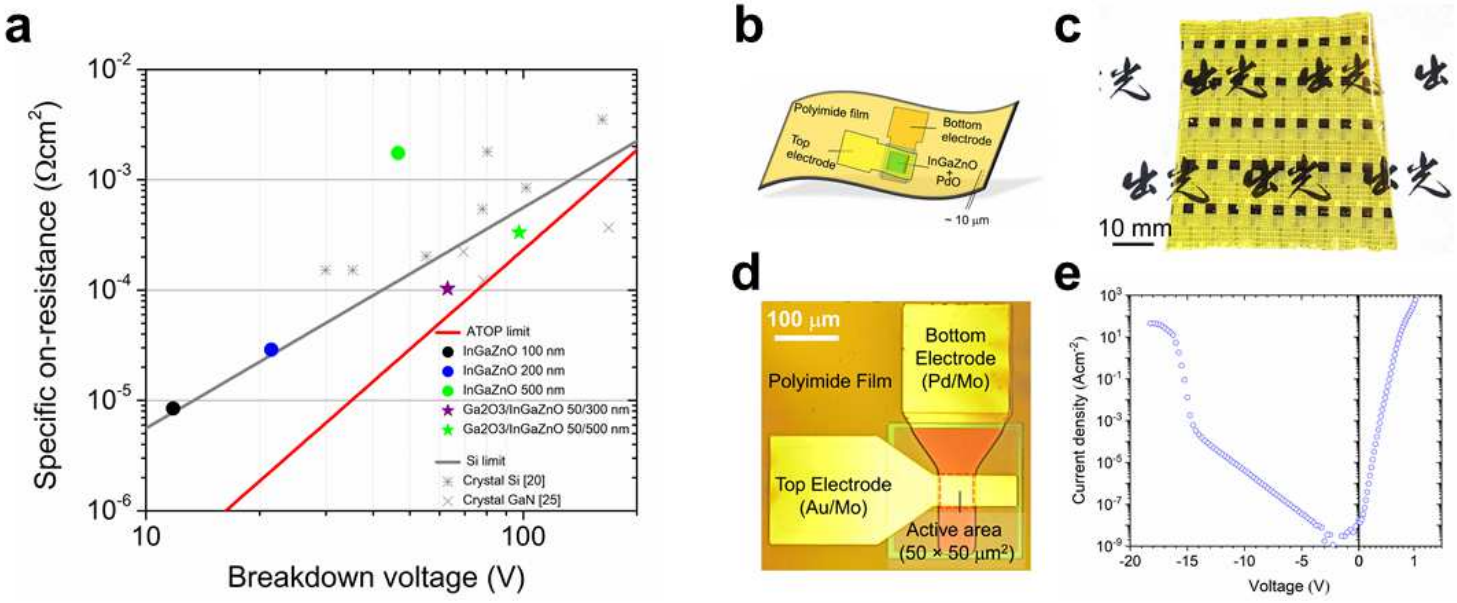


Figure 4

Figure-of-merits (FOM) for PDs and the demonstration of flexible ATOP. a, The relationship between breakdown voltage VBD and on-specific resistance Ron,sp. The circles and the stars correspond to the present results of the single- and double-layer diodes, respectively. The asterisk and cross grey marks are taken from the references to Si and GaN single-crystal semiconductors, respectively. ATOP limit obtained from equation (4) with the parameters in Supplementary Fig. 5a and V at 5V. b, Schematic images of flexible ATOP (c) Photograph of ATOPs on polyimide film. d, Photograph of measured SBD on a flexible polyimide film with the optimized diode structure. e, J-V characteristics of SBD shown in (d).

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