Effect of Negative Capacitance in Partially Ground Plane based SELBOX FET on Capacitance Matching and SCEs

Shalini Chaudhary (✉ 2019rec9066@mnit.ac.in)

MNIT Jaipur: Malaviya National Institute of Technology <https://orcid.org/0000-0001-6440-4782>

Basudha Dewan

MNIT Jaipur: Malaviya National Institute of Technology

Chitrakant Sahu

MNIT Jaipur: Malaviya National Institute of Technology

Menka Yadav

MNIT Jaipur: Malaviya National Institute of Technology

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Effect of Negative Capacitance in Partially Ground Plane based SELBOX FET on Capacitance Matching and SCEs

Design, Simulation and Performance Investigation

Shalini Chaudhary · Basudha Dewan · Chitrakant Sahu · Menka

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Abstract Here in, we investigated the impact of negative capacitance in PGP-SELBOX NCFET (partial ground plane on a selective buried oxide in negative capacitance FET) over FDSOI. The ferro-electric layer is placed in the gate stack of PGP-SELBOX NCFET to generate the negative capacitance phenomenon. Ferro-electric(FE) materials are similar to dielectric materials but differ in terms of their polarization properties. FE-HFO₂ is used as ferroelectric material due to its sufficient polarization rate with high dielectric capacitance and better reliability. The effect of ferro-electric material parameters like coercive field(E_c) and remnant polarization(P_R) on the capacitance matching of NCFET are analyzed. The simulation results reveal that the R_{PE} factor, which is the ratio of P_R to E_c , is closely related to better capacitance matching. In addition, the effect of variation in thickness of ferro-electric layer on the average sub-threshold swing(SS) is also explored. The relation between short channel effects (V_{th} rolloff and DIBL) and thickness of the ferro-electric (t_{fe}) for PGP-SELBOX NCFET is also analyzed. The simulation results clearly show that PGP-SELBOX NCFET is having reduced SCEs and 10^3 times better $\frac{I_{ON}}{I_{OFF}}$ ratio over FDSOI NCFET. For optimized value of ferro-electric parameters average SS for proposed device is found as 50 mV/decade at $t_{fe} = 5\text{nm}$ which is lesser than FDSOI NCFET (56 mV/decade).

Keywords Partial-ground-plane selective buried oxide (PGPSELBOX) · Ferroelectric material (FE) · Negative Capacitance (NC) · Drain induced barrier

rising (DIBR) or reverse DIBL · V_{th} roll off · SCEs (short channel effects) · Sub threshold swing(SS).

1 Introduction

In today's era, demand for low power devices at nano-scale level is continuously increasing. But with continuous scaling, issues related to gate control, leakage current and static power dissipation reached an unmanageable level and SS stuck at the fundamental thermal limit of 60 mV/dec, which is known as Boltzmann tyranny [1]. It is difficult to achieve low power consumption and high performance of the device due to this tyranny limit.

There are various concepts given to improve the SS. Based on current phenomenon, such as band to band tunneling in tunnel FET (TFET) [2,3] and impact ionization technique in impact ionization MOS (IMOS) [4] to improvise the SS below 60 mV/dec. The main disadvantage of TFET is that it could not address the issue of low ON current and its ambi polarity nature. IMOS too has drawback of operating at a very high voltage.

Due to these disadvantages of TFET and IMOS, the negative-capacitance FETs (NCFETs)[5] have draw much attention as a new type of steep switching device. The NCFETs can achieve steeper SS and higher I_{ON} . It is due to the amplification of the gate voltage by negative capacitance phenomenon obtained by integrating ferro-electric material in the gate stack of the traditional MOSFET [6–10]. Hence the lower value of SS is achieved.

However due to the continuous scaling of MOSFET ($< 65\text{nm}$), the performance is severely affected by short channel effects (SCEs). When length of the channel decreases, the control of the gate over the channel gets

reduced due to presence of SCEs like DIBL, V_{th} rolloff, mobility degradation and gate leakage current. A thin-film silicon-on-insulator (SOI) based MOSFET was introduced to overcome these SCEs. They are capable of performing at low power consumption and leakage power along with a steeper subthreshold slope [11,12]. But the main disadvantages associated with this are self heating and low breakdown voltage [13]. The self heating basically degrades the overall performance of the device and reliability too.

The self-heating problem is considerably reduced by using the silicon over partial BOX. One such example is the selective buried oxide (SELBOX) device [14,15]. This BOX is like a window which joins the active region of device with substrate and provides path for the dissipation of heat. So there is reduction in self heating during the achievement of high breakdown voltage. But issues with such structure is that the magnitude of short channel effects is higher in these devices. These short channel effects create many issues like increase in leakage current, increase in DIBL voltage, shift in threshold voltage with decreasing channel length, decrease in subthreshold slope and reliability issues like hot carrier effect [16].

To overcome the drawbacks of SELBOX structure, partial ground plane (PGP) is incorporated with SELBOX [17], due to which SCEs is reduced significantly. This also creates the scope of further scaling of the device. In this device, the BOX is made under the source and drain regions and another region is made under the channel region which worked like a window for this structure. The heavily doped PGPs is used under the SELBOX, which is placed along the edge of SELBOX and in line with the source/drain. This PGP type structure stops the electric field lines from reaching drain to source directly and minimize the coupling of field lines. Due to this, short channel effects like DIBL is reduced [18,19]. We have considered PGP in place of continuous ground plane because it increases the parasitic capacitance related to the source and drain and increases crosstalk. Hence for performing the NCFET operations, PGP-SELBOX as a baseline device is taken [17].

Fig. 1(a) shows comparison of the current characteristics of the FDSOI and PGP-SELBOX FET and we found that the I_{ON}/I_{OFF} is better in case of the PGP-SELBOX. Due to this high I_{ON}/I_{OFF} ratio and other advantages of PGP-SELBOX which are described above, we took this structure as baseline and did performance analysis by converting it into a NCFET. The doped hafnium oxide (FE-HFO₂) is used as FE material [20]. Because of the low dielectric constant (30) and high coercive field (1–2 MV/cm) of doped hafnium

oxide, we can easily incorporate it into current CMOS technology node.

Fig. 1 (a) Comparison in the current characteristics for FD-SOI and the PGP-SELBOX structure (b) Calibration plot of current characteristic with data in Ref [19]

Deliverables and Organization of this work

In this paper we propose a new geometrically negative capacitance FET which have a single gate and shows the performance like multigate FET. This proposed device uses the advantage of PGP-SELBOX FET and provide better FET design when it is combined with a ferro-electric layer in the gate stack for providing negative capacitance effect. When heavily doped ground plane is present then it prevents the electric field lines from reaching drain to source directly. With PGP, coupling of electric field lines is minimized which results in reduction of short channel effects like DIBL, SS, V_{th} roll off. This manuscript is organized as Section 2 in which the device architectural specifications and simulation methodology is discussed. In Section 3 the proposed device is mainly analyzed for capacitance matching in terms of ferro-electric material parameters and also discuss about short channel effects.

2 Device structure and simulation methodology

For preventing the complications related to parasitic capacitance and the short channel effects PGP-SELBOX technology is used, which is suitable for a baseline structure. Therefore the PGP-SELBOX structure with negative capacitance is analyzed in our work. The schematic of the investigated NCFETs and its corresponding capacitance model are shown in Fig. 2(b) and (c) respectively. In this work only n-channel structure is presented but the approach used in the simulation is equally valid for the p channel NCFET [6,21]. In Fig. 2 (c) the equivalent capacitance model of this structure is given and according to this, total capacitance of device is series combination of MOS capacitance (C_{MOS}) and ferro-electric capacitance (C_{fe}). C_{MOS} is the series combination of the oxide capacitance (C_{OX}) across oxide layer

Fig. 2 (a) Device parameter table of PGP-SELBOX NCFET structure (b) PGP-SELBOX NCFET device structure (c) Equivalent capacitance model of this structure (d) Process flow for simulation of the device

of baseline device and semiconductor(depletion) capacitance (C_s) of the baseline device. If we use the BOX structure then MOS capacitance is a series combination of capacitance of insulating layer, BOX layer and semiconductor. In Fig. 2(c), V_g is gate voltage across the NCFET structure and V_{MOS} is the mos voltage across the baseline device. The parameters values used in this structure are given Fig. 2(a). We used Equivalent oxide thickness(EOT) concept in place of the insulating layer of SiO₂ only and for that we have taken combination of HfO₂ with the thin layer of SiO₂ layer. Channel length(L_g) is taken as 30 nm and SELBOX length is also 30 nm. PGP is like a square box of dimension 10 nm.

There are two approaches to fabricate the NCFET. One is by directly integrating the ferro-electric material on the oxide layer in the gate stack like Metal ferro-electric insulator semiconductor (MFIS) and other one is the use of metallic layer in the gate stack before applying the ferro-electric material layer [22]. The latter one is like connecting a regular FET with the NC capacitor and this also called Metal-ferroelectric-metal-insulator-semiconductor(MFMIS) approach and we adopted this approach in our work. The purpose of using the metallic layer between the two dielectrics is that it cancels out the non-uniform potential profile across channel and charge non uniformity due to domain formation in the ferroelectric [23] and controlling the matching of capacitance and overcome the inter-

ference generated due to spacer. Fig. 2(d) shows the process flow of the simulation approach.

As we go for MFMIS structure, first we simulated our baseline structure in Silvaco TCAD [24]. Before simulating the structure, TCAD tool is calibrated against the data present in reference [17]. For simulation purpose standard models like CONSRH (concentration dependent Shockley Read Hall re-combination model), AUGER (Auger recombination model), BGN (bandgap narrowing model) and CONMOB (concentration dependent mobility model) are used. For obtaining the calibrated results we tuned energy band density of states (NC300, NV300) and carrier lifetimes (electron lifetime: TAUN0, hole lifetime: TAUP0). For subsequent work, same calibrated model file and tuned parameters are used but dimensions are changed for simulation of this device. The calibrated graph for the simulator is given in the fig 1(b). After getting charge density, current characteristics and other parameters from simulation, we solve self consistently Landau-Khalatnikov (L-K) model with these simulated results and obtained the characteristics of the NCFET in the MATLAB.

According to the L-K equation [25], the Gibbs free energy density (U) of the ferroelectric layer can be expressed in the powers of the polarization (P) in the vicinity of a phase transition as:

$$U = \alpha t_f P^2 + \beta t_f P^4 + \gamma t_f P^6 - V_{fe} P \quad (1)$$

This equation can also be written in terms of charge (Q) because we consider (P=Q) in case of NCFET analysis as in reference [5]. Eq. 1 can be written as

$$U = \alpha t_f Q^2 + \beta t_f Q^4 + \gamma t_f Q^6 - V_{fe} Q \quad (2)$$

Here α , β and γ are constants (Landau parameters) which are material dependent and t_{fe} is thickness of the ferroelectric film, V_{fe} is voltage applied across the ferroelectric layer. In order to get the equilibrium state of the ferroelectric layer, minima of U is derived by differentiating the U w.r.t Q and the relation for V_{fe} is found as:

$$V_{fe} = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 \quad (3)$$

Now the voltage across the NCFET can be written as

$$V_G = V_{fe} + V_{MOS} \quad (4)$$

where V_G is the applied gate voltage across NCFET and V_{MOS} is the intermediate contact potential (gate voltage across base line device).

The 2D electrostatics for the baseline are simulated by using the same models that are used at the time of calibration as consrh, auger, conmob and bgn. The channel thickness of this device is greater than 6 nm so we have not taken Quantum simulation model here. FE-HfO₂ is used as the gate ferroelectric material which exhibit the second-order phase transition. For this FE-HfO₂, $\alpha < 0$, $\beta > 0$, and $\gamma = 0$. The nonzero parameters like α and β can be written in terms of the remnant polarization (P_r) and coercive field (E_C) [26,27] is defined as,

$$\alpha = -\frac{3\sqrt{3}}{4} * \frac{E_C}{P_r}, \beta = \frac{3\sqrt{3}}{8} * \frac{E_C}{P_r^3} \quad (5)$$

By these above formula we can alter the value of alpha and beta with E_C and P_r and obtained better capacitance matching for the NCFET operation.

3 Results and performance analysis

Assessment of capacitance matching with variation in ferroelectric parameters

Stabilizing the negative capacitance effect is a critical issue in capacitance matching among $|C_{fe}|$, C_{mos} and C_{ox} [28]. The required conditions for the same are

$$|C_{fe}| < C_{ox}$$

and

$$|C_{fe}| \approx > C_{MOS} \text{ (for non-hysteresis)}$$

It can be seen that for NCFET in order to function in negative capacitance region and to amplify V_{MOS} to achieve high performance, the C_{fe} should be approximately equal or slightly greater than C_{MOS} is a necessary condition. So during the design, appropriate capacitance matching between the capacitance of the FE layer (C_{fe}), the buffer oxide capacitance (C_{ox}) and the MOS capacitance (C_{MOS}) is very important to realize the desired operation mode. The ferro-electric capacitance is defined in terms of the E_C , P_R and t_{fe} written as

$$C_{fe} = \frac{dQ}{dV_{fe}} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)} \quad (6)$$

In above Eq. 6, we neglect higher terms of charge (Q) because its value is very less. So, it can be written as

$$C_{fe} = \frac{1}{2\alpha * t_{fe}} = \frac{2}{3\sqrt{3}} \frac{P_R}{E_C * t_{fe}} \quad (7)$$

We can obtain better capacitance matching for NCFET by varying parameters as E_C , P_R and t_{fe} [29]. SS can also be written in terms of the capacitance by which we can control the value of average SS. SS is defined at room temperature for NCFET as

$$SS = 60 * [1 + \frac{C_{MOS}}{C_{FE}}] \quad (8)$$

3.1 Optimization of Coercive Field (E_C) and Remanent Polarization (P_r)

In this section, the material parameters such as coercive field (E_C) and remnant polarization (P_r) for FE-HFO₂ are optimized according to the experimental data reported in reference [26]. To get a better understanding of hysteresis and non-hysteresis operation of the device and to acquire the optimized values of E_C and P_R , we studied the charge density (Q_g) versus FE capacitance (C_{fe}) and MOS capacitance (C_{mos}) characteristics of the reference PGP-SELBOX FET device. Thickness of ferroelectric layer is considered as $t_{fe} = 5$ nm, since it is the minimum thickness of doped HFO₂ which can be fabricated for the range of E_C and P_R values reported in reference [26]. It can be inferred from fig. 3(a) that out of all values of E_C and P_r , maximum amplification without hysteresis can be obtained for $E_C = 1.4$ MV/cm and $P_R = 6.5$ μ C/cm². For these values, FE layer capacitance is close to MOS capacitance which implies better matching to achieve maximum enhancement of the capacitance. Further it can be also seen

from Fig. 3(a) that for $E_C = 1.4$ MV/cm and P_R less than or greater than $6.5 \mu\text{C}/\text{cm}^2$, device does not perfectly match with C_{fe} . Fig 3 (b) shows change in gate capacitance with gate voltage. Gate capacitance(C_g) is given as $C_g = (C_{fe}^{-1} + C_{mos}^{-1})^{-1}$ and it is found that for $E_C = 1.4$ MV/cm and $P_R = 6.5 \mu\text{C}/\text{cm}^2$, $|C_{fe}| \approx C_{mos}$ and obtained peak in the subthreshold region. As we moves towards larger value of P_R peak is greater but slightly move towards the inversion region because at larger P_R , $|-C_{fe}| \gg C_{mos}$ and capacitance does not match properly to operate in negative capacitance region.

Fig. 3 (a) Variation of charge density with MOS capacitance (C_{mos}) and magnitude of FE capacitance (C_{fe}) for different values of P_R and fixed E_C (b) Variation of C_g with Gate voltage V_g for different P_R

From Fig. 4(a) we observed current characteristics for different values of P_R and found that as values of P_R decrease the SS decreases in the subthreshold region and smaller P_R shows a steeper sub threshold characteristic. It can also be better explained with the graphs of variation of V_{MOS} with V_g and variation of V_{fe} with V_g for different values of P_r in Fig. 4(b) and (c) respectively. It is also explained with Eq. 4, according to which when P_r is reduced, V_g decreases due to increase in $-V_{fe}$. Thus the same value of drain current at lower V_g is obtained and SS decreases. Fig. 5(a) describing the effect of variation in E_C for better capacitance matching. According to the Eq. 7 we found that C_{fe} is inversely proportional to E_C . As we increase the more value of E_C , C_{fe} decreases. For our simulation we get optimum matching at $E_C = 1.4$ because at this point $C_{fe} \approx C_{mos}$ at fixed P_R of $6.5 \mu\text{C}/\text{cm}^2$. The value of E_C is varied between 1.35 to 1.5. From analysis we found that for $E_C > 1.4$, the value of C_{fe} is decreasing and becomes less than C_{mos} and which is not desirable for NCFET. Fig. 5(b) shows the effect of gate capacitance with variation in E_C . For optimum value of E_C we found peak in subthreshold region. As value of E_C increases the peak is increasing but shifting towards inside because C_{fe} is decreasing and become less than C_{mos} and which is not desirable.

Fig. 4 (a) Current Characteristics for different values of P_R (b) Variation of V_{MOS} with V_g for different values of P_R (c) Variation of V_{fe} with V_g for different values of P_R

Fig. 5 (a) Capacitance matching for different values of E_C (b) Variation of C_g for different values of E_C

Fig. 6(a),(b),(c) are showing the current characteristics for different values of E_C , variation of V_{MOS} with V_g and variation of V_{fe} with V_g for different values of E_C . From current characteristics we found that as E_C is increasing V_{MOS} and V_{fe} is increasing more and more due to which the hysteresis is shown in the current characteristics and which is not desirable for NCFET analysis. Fig. 6(d) shows the average value of SS for different values of E_C and P_R . For optimum value of both E_C and P_R , we found average SS is 50 mV/decade which is less than the Boltzmann tyranny limit of 60mV/decade. For the baseline device the value of SS is obtained as 73 mV/decade but due to effect of negative capacitance and proper capacitance matching we obtained SS less than the baseline device. Here we also observed lower value of SS (< 50 mV/decade) but that region is not showing proper capacitance matching and having hysteresis behavior.

3.2 Variation in Ferro-electric thickness(t_{fe})

Operation of NCFET based circuits is also characterized by the ferro-electric thickness(t_{fe}). It also affects the capacitance matching condition because C_{fe} is in-

Fig. 6 (a) Current Characteristics for different values of E_c (b) Variation of V_{MOS} with V_g for different values of E_c (c) Variation of V_{fe} with V_g for different values of E_c (d) Average SS for variation in E_c and P_R

versely proportional to t_{fe} . When the value of the t_{fe} increases, $|C_{fe}|$ decreases and matching will be better. But there is a limit of increasing it because after a particular thickness we start obtaining hysteresis. In our simulation we have taken $t_{fe} = 5$ nm which is the maximum thickness for obtaining hysteresis free curve. Fig. 7(a) showing the $I_d - V_g$ curves for different values of t_{fe} and found that hysteresis starts as we move from 5 nm to 6 nm. This can also be better explained with Fig. 7(b) and 7(c) which are describing relation between V_{MOS} with V_g and V_{fe} with V_g . From there we found that as t_{fe} increases V_{MOS} becomes greater than V_g and moving towards hysteresis. Similarly V_{fe} start decreasing and becomes more negative and after a critical thickness (> 5 nm), shows hysteresis property.

3.3 R_{PE} factor

For describing the effect of P_R and E_C in a better way for capacitance matching, we define a factor R_{PE} . R_{PE} is the ratio of P_R and E_C .

For better matching between $|C_{fe}|$ and C_{mos} , the value of $|C_{fe}|$ should be close to C_{mos} and for obtaining this P_R should be less and E_C should be more. R_{PE} factor also correlated with the SS of the NCFET. Fig. 8(a) gives the $I_d - V_g$ curves for five NCFETs which having same ($R_{PE} = 5$) for different combinations of P_R and E_C and obtained almost the same current in sub-threshold region for all but slightly different current above this region. It is due to P_r as it is dominant factor as gate voltage increases. Fig. 8(b) shows that for same R_{PE} , SS and threshold voltage (V_{th}) is almost the same.

Fig. 7 (a) Current Characteristics for different values of t_{fe} (b) Variation of V_{MOS} with V_g for different values of t_{fe} (c) Variation of V_{fe} with V_g for different values of t_{fe}

Fig. 8 (a) Current Characteristics for different values of P_R and E_C for same R_{PE} as ($R_{PE} = 5$) (b) Threshold voltage and SS for Variation in P_R and E_C for same R_{PE}

3.4 Reverse DIBL and V_{th} roll off

Biasing of drain is having great impact on the electrostatic behavior of the devices particularly at the nanoscale level. As we know when the value of drain biasing increases for the simple devices (without negative capacitance effect), value of V_t decreases and we obtained drain induced barrier lowering (DIBL). It is basically due to lowering of band with the effect of high drain voltage. In our paper we selected PGP-SELBOX structure as baseline structure because in Fig. 9(a) we analyze the current characteristics of both FDSOI and PGP-SELBOX structure at drain voltage (V_d) 0.7 V and 0.07 V and found reduction in DIBL. It is because of PGP as it held high the gate induced field in comparison to without PGP structure. The DIBL is defined as

$$DIBL = \frac{V_{th}^{high} - V_{th}^{low}}{V_{DS}^{high} - V_{DS}^{low}} \quad (9)$$

where V_{th}^{high} is the threshold voltage at high V_{DS} and V_{th}^{low} at low V_{DS} . We calculated DIBL by above Eq (9)

and found 143 mV/V for simple FDSOI and 95mV/V for the PGPSELBOX.

Fig. 9 (a) Current Characteristics of FDSOI and PGP-SELBOX at $V_d = 0.7$ V and 0.07 V (b) Variation in DIBL and SS with t_{fe} for PGP-SELBOX NCFET (c) Variation in V_{th} roll off for different values of t_{fe} for FDSOI NCFET and PGP-SELBOX NCFET

In case of the negative capacitance we found the reverse effect of the DIBL or we obtained drain induced barrier rising effect (DIBR) and because of it, the V_t at high drain voltage increases and we obtained negative value of DIBL. It is observed because of increase in the potential barrier with increase in drain voltage. This drain induced barrier rising explained the negative capacitance phenomenon and is related with the recent studies. Fig. 9(b) shows the variation of Reverse DIBL and SS with t_{fe} .

For high value of drain voltage V_t decreases with increase in t_{fe} . This is due to the increase in barrier height. Because of this DIBL increases in negative direction and SS is also decreasing with t_{fe} . Fig. 9(c) shows the V_{th} roll off for both type of NCFET based on FDSOI and PGP-SELBOX. From the figure we found that V_{th} roll off improves in case of PGP-SELBOX NCFET because of its PGP type structure as it increases the gate control. Due to which V_t does not decrease as much as in case of FDSOI NCFET, hence V_{th} roll off improves in the proposed structure.

Performance comparison with counterpart technologies

Maintaining performance consistency during down-scaling of devices becomes critical. In this section we compare some recent technologies with the proposed work shown in Table 1. Tunnel FET is one of the approach to overcome the thermal limit (60mV/dec) of SS during downscaling. We found TFET with $L_g = 13$ nm, has SS of 60mV/dec and improved I_{ON}/I_{OFF} ratio but limited I_{ON} is the main drawback of it [30]. In the recent years, new class of device which having steep sub-threshold slope device has been proposed called negative capacitance FETs. Their characteristics mainly depend upon the structure on which we apply the negative capacitance concept. In FDSOI based NCFET at $L_g = 20$ nm we found SS as 56mV/dec and improved I_{ON}/I_{OFF} ratio of 10^5 [29]. We obtained good results but I_{ON}/I_{OFF} ratio is little less. In our proposed work we improve both SS and I_{ON}/I_{OFF} ratio by using PGP type structure for NCFET. We found SS as 50mV/dec and improved I_{ON}/I_{OFF} ratio of 10^8 which makes this device suitable for low power applications.

4 Conclusions

Through this work we investigate PGP-SELBOX NC FET which is advantageous in terms of design and performance (low power and better heat dissipation) and improves SCEs by inclusion of PGP. For this device, analysis for capacitance matching has been carried out by varying different ferro-electric parameters like coercivity (E_C), polarization (P_r) and FE layer thickness (t_{fe}) at $L_g = 30$ nm and $V_d = 0.7$ V. This proposed device has superior $\frac{I_{ON}}{I_{OFF}}$ ratio of 10^8 and SS of 50 mV/dec at optimized values of E_C (1.4 MV/cm), P_r (6.5 μ C/cm²) and t_{fe} (5 nm). We also analyzed the R_{PE} factor and found that for same R_{PE} , current characteristics and SS are approximately same due to similar capacitance matching. In addition we studied about short channel effects like reverse DIBL and V_{th} roll off and examine their effect with ferro-electric thickness (t_{fe}). The obtained performance analysis of the proposed device make it suitable for low power operations especially when we taken single gate architecture FETs.

5 Author Declarations

5.1 Ethics approval and consent to participate

Informed consent was obtained from all individual participants included in the study.

Table 1 Comparative analysis of technologies for various figure of merits

Device Description	Tech. (L _g)	I _{ON} ($\mu\text{A}/\mu\text{m}$)	I _{OFF} (A/ μm)	$\frac{I_{ON}}{I_{OFF}}$	SS (mV/dec)	[Ref]
NCFET with PGP-SELBOX as baseline structure	30 nm	674	1.96×10^{-11}	10^8	50	[This Work]
NCFET with FDSOI as baseline structure	20 nm	10^5	1.0×10^{-6}	10^5	56	[29]
Tunnel Field Effect Transistor	13 nm	10.0	1.0×10^{-9}	10^5	60	[30]
Planar Junctionless SOI FET	1 μm	100	50.0×10^{-6}	10^2	150	[31]

5.2 Consent for publication

Informed consent was obtained from all individual participants included in the study.

5.3 Availability of Data and Materials

There are no linked research data sets for this submission.

5.4 Competing interests

The authors declare no competing interests.

5.5 Funding

The authors have not received any funding for this work.

5.6 Author's Contributions

The main conception of this work is the brainchild of Shalini Chaudhary (Author 1). The first draft of the manuscript was written by Shalini Chaudhary. Basudha Dewan (Author 2) provided the necessary support regarding simulation and data interpretation. Chitrakant Sahu and Menka (Author 3 and 4) supervised the work and made important discussions and modifications to the final manuscript.

5.7 Acknowledgments

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6 Compliance with Ethical Standards

6.1 Disclosure of potential conflicts of interest

The authors declare that they have no conflict of interest.

6.2 Research involving Human Participants and/or Animals

Not applicable.

6.3 Informed consent

Not applicable.

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Figures

Figure 1

(a) Comparison in the current characteristics for FDSOI and the PGP-SELBOX structure (b) Calibration plot of current characteristic with data in Ref [19]

Figure 2

(a) Device parameter table of PGP-SELBOX NCFET structure (b) PGP-SELBOX NCFET device structure (c) Equivalent capacitance model of this structure (d) Process flow for simulation of the device

Figure 3

(a) Variation of charge density with MOS capacitance (C_{mos}) and magnitude of FE capacitance (C_{fe}) for different values of PR and fixed EC (b) Variation of C_g with Gate voltage V_g for different PR

Figure 4

(a) Current Characteristics for different values of P_r (b) Variation of VMOS with V_g for different values of P_r (c) Variation of V_{fe} with V_g for different values of P_r

Figure 5

(a) Capacitance matching for different values of E_c (b) Variation of C_g for different values of E_c

Figure 6

(a) Current Characteristics for different values of E_c (b) Variation of VMOS with V_g for different values of E_c (c) Variation of V_{fe} with V_g for different values of E_c (d) Average SS for variation in E_c and PR

Figure 7

(a) Current Characteristics for different values of t_{fe} (b) Variation of V_{MOS} with V_g for different values of t_{fe} (c) Variation of V_{fe} with V_g for different values of t_{fe}

Figure 8

(a) Current Characteristics for different values of PR and EC for same RPE as (RPE = 5) (b) Threshold voltage and SS for Variation in PR and EC for same RPE

Figure 9

(a) Current Characteristics of FDSOI and PGPSELBOX at Vd = 0.7 V and 0.07 V (b) Variation in DIBL and SS with tfe for PGP-SELBOX NCFET (c) Variation in Vth for different values of tfe for FDSOI NCFET and

PGPSELBOX NCFET