Au-Ag Binary Alloys on n-GaAs Substrates and Effect of Work Functions on Schottky Barrier Height

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Au-Ag Binary Alloys on n-GaAs Substrates and Effect of Work Functions on Schottky Barrier Height

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Abstract

In this study, I investigated the effect of work function (ϕ_m) of Au_xAg_{1-x} ($x=0, 0.22, 0.37, 0.71$ and 1) on the *Au-Ag/n-GaAs* Schottky diode (SD) parameters. Ag, Au and three alloys with different compositions deposited on n-GaAs substrates by thermal evaporation method. Surface morphologies of the samples were investigated by atomic force microscope (AFM). Elemental compositions of Schottky metals were conducted by the energy dispersive X-ray spectroscopy (EDX). Current-voltage (I-V) and capacitance-voltage (C-V) measurements performed at room temperature.

SD parameters such as barrier height (Φ_{b0}), ideality factor (n), series resistance (R_s), and interface state density (D_{it}) of the SD's were calculated from the obtained I-V and C-V data. Experimental results showed that all calculated SD parameters depends on alloy composition. Lowest mean barrier height value was found as 0.789 ± 0.022 eV for *Au/n-GaAs* SDs and the highest value was determined 0.847 ± 0.008 eV for *Au_{0.71}Ag_{0.29}/n-GaAs* SDs from I-V measurements. Weak dependencies of barrier height to ϕ_m was exist and gap state parameter (S) determined as 0.0526. S value was close to the Bardeen limit ($S=0$), and indicates that Fermi level was strongly pinned in *Au-Ag/n-GaAs* SDs. Also, main SD parameters like series resistance (R_s), ideality factor (n), reverse bias barrier height (Φ_b^{RB}), doping density (N_d) and density of interface states (D_{it}) were calculated via using different methods from I-V and C-V measurement results. In addition, to determine the leakage current mechanism Poole-Frenkel emission (PFE) and Schottky emission (SE) models applied on reverse bias I-V data.

Keywords

Gold-silver alloy; electrical transport; leakage current, Fermi level pinning; density of interface states.

1. Introduction

Barrier formation mechanisms of metal-semiconductor contacts have been a major research topic since the first discovery of these contacts [1-4]. In order to accurately identify the current flowing through the contact and determine the operating conditions of the devices, the basic parameter, barrier height (Φ_b), have to be defined correctly. First attempt was realized by Schottky to understand the rectifying behavior of metal-semiconductor contacts [5]. Schottky and Mott subsequently proposed a model for barrier formation and calculating the barrier height [5-7]. According to the Schottky-Mott rule [7], under the ideal condition, the factors affecting this barrier height was an electron affinity of the semiconductor (χ_s) and the work function of metal (ϕ_m), and it was simply expressed as follows;

$$\Phi_b = \phi_m - \chi_s . \quad (1)$$

Since Schottky-Mott rule is almost never verified experimentally, it can be concluded that; interface dipoles do not disappear and play a major role in determining the properties of the metal-semiconductor interface [8]. The ϕ_m value of the metal depends on two components; volume term and surface dipole term, which starts just below the surface of the metal and represents where all bulk properties are same. Both dipole terms strongly correlate with surface charge distribution and depend on the condition of the surface [9]. Moreover, it was commonly known that, when a metal and semiconductor are brought into a contact without any interface layer, the atomic sites and charge distributions change, so that the contribution of the surface dipole changes. Louie et al. to overcome this situation, used the metal's electronegativity instead of the function of the metal [10]. In addition, in the presence of states at the interface has a significant effect on the formation of barrier height and investigated in many studies [2, 7, 8, 11-15].

Although Schottky-Mott rule provides accurate estimation of band bending in a semiconductor, the validity of the proposed model, due to the presence of states at the interface between the metal and the semiconductor and the "Fermi level pinning" caused by these finite states, is a matter of discussion especially for some semiconductors [2, 16]. According to this model, if the thin insulating layer exists between a semiconductor and a metal, interface states of semiconductor are occupied by the electrons, create additional space charge region, and create potential difference. This potential difference reduces the effect of metals work function on barrier height [16]. Experimentally observed barrier height has a very limited relation to the results of this theory [8, 14, 17]. Few models proposed to reveal the formation of barrier height in a metal semiconductor contact [2, 11, 18]. Some of these models associate the independence of the barrier height from the ϕ_m with the fermi level pinning mechanism caused by high density interface states [2]. Some other models are closely interested in interfacial chemistry and address the interaction of interfacial dipole with bond polarization [11]. However, all proposed models haven't yet emerged to explain the properties of metal-semiconductor contacts precisely, are not complete and usually changes with the substrate, metal, substrate cleaning method, metal deposition method, etc. [9]. It is possible to determine the diode parameters (tuning) during the production of diodes to serve a specific purpose. It is sufficient to use metals or semiconductors with different work functions [9, 13, 19, 20].

GaAs has high thermal strength, high electron mobility and high resistance to radiation damage. It also has a direct band gap that allows efficient absorption of light emission and absorption, allowing transistors to operate at very high frequencies, reducing the noise at which higher frequencies tend to reduce electrical signal distortion in electronic circuits. Also, ternary and quaternary alloys created from GaAs utilizing elements like Al, In, P, and Sb have properties that complement those of GaAs, which allows adaptability. GaAs is an important substrate material for devices, which is used in both micro- and opto-electronic applications. Also, GaAs is a suitable substrate for basic components for high speed and low power electronics. On the condition that the properties of the semiconductor remain the same (assuming the effect of interface states to be invariant), modifications in the composition of Schottky metal should be expected to change the barrier height. Both of Au and Ag have very similar properties such as conductivity, molar heat capacity, crystal structure, atomic and covalent radius. They are miscible in all portions and known as good contact properties with GaAs.

In this study, the effect of modification in the ϕ_m of Schottky metal was investigated by depending on the composition of alloys. For this purpose, electrical measurements (current-voltage and capacitance-voltage) were performed at room temperature on produced 20 Schottky barrier diodes (SDs) which were fabricated by using two metals (Ag, Au) and three different alloys on n-GaAs. The characteristic parameters of SDs such as ideality factor (n), barrier height (Φ_b), series resistance (R_s), reverse bias barrier height (Φ_b^{RB}) etc. have been determined and compared with each other. Pinning position of the Fermi level and density of interface states (D_{it}) have been determined and the validity of the Schottky-Mott rule for the Au-Ag/GaAs was tested.

The n-type GaAs substrate used in this study was grown by the LEC method and Te-doped with a carrier concentration of $2-5 \times 10^{17} \text{ cm}^{-3}$. To remove organic contaminations on GaAs substrate, it was cleaned with some solvents (acetone, methanol, trichloroethylene, deionized water) 5 min using ultrasonic agitation in each step. Then, GaAs substrate was immersed in an HCl:H₂O (1:1) etching solution to eliminate the thin native oxide layer on the surface, rinsed with de-ionized water (18 M Ω) and high purity nitrogen gas used for drying. After the etching process, GaAs substrate inserted into the metal deposition chamber immediately.

The Ohmic contacts and transfer length method (TLM) patterns were built by thermal evaporation of Au-Ge alloy (wt.% 12), on non-polished side of substrate with a thickness of 200 nm, at 2×10^{-6} Torr base chamber pressure and thermally annealed at 350 °C for 2 min. in flowing high purity (5N) nitrogen gas in a tube furnace. TLM method [21] was used to characterize the electrical contacts, with gaps of 0.25, 0.50, 0.75 mm between 0.7x3.5 mm pads. Specific contact resistance (ρ_c), contact resistance (R_c), and the effective length (L_{eff}) derived from the measured I - V data and the calculated total resistance versus gap spacing by TLM and values were $9.899 \times 10^{-6} \text{ }\Omega\text{cm}^2$, 0.510 Ωcm and 0.770 μm , respectively.

The substrate divided into 5 parts and the area of each part was approximately 1 cm². Each part immediately inserted into the vacuum chamber of NVTs-400 to form Schottky contacts by thermal evaporation of metals and alloys. The Au_xAg_{1-x} alloys made at tungsten crucibles, using a high purity Au (4N5) and Ag (5N) parts, repeating the melt-cooling cycle at least five times

and under vacuum. Alloy composition ($x=0, 0.22, 0.37, 0.71$ and 1) was verified by *EDX* measurements and given in Table 1. Schottky contact metals/alloys thermally evaporated through a tungsten shadow mask on the front side of the wafers with diode area was 0.785 mm^2 . Electrical characteristics of *Au-Ag/n-GaAs* SDs studied from dc current-voltage (*I-V*) measurements (measured with the HP4140B picoammeter) and frequency dependent capacitance-voltage (*C-V*) measurements (measured with Agilent E4980A LCR meter) in the dark and 300 K. The forward and reverse bias *I-V* measurements evaluated using the standard thermionic emission theory, and Poole-Frenkel and Schottky emission theory. *C-V* measurement results were also evaluated using diode capacitance, and single frequency approximation for interface state density distribution model. All measurements and calculations performed with our SeCLaS-PC program [22, 23].

1. Results and Discussion

1.1. Work functions and surface morphology of binary Au-Ag alloy

The work function was one of the most basic properties of material surfaces and it is directly affects electrical properties of metal-semiconductor contacts. Although the work functions of metals are well documented for various elements, information about the work functions of alloy surfaces and its dependence on composition is limited [24]. Segregation, especially in alloys, makes it difficult to determination of work functions of the alloys [25]. Generally, Gelatt and Ehrenreich's model is used for determine the work function of the alloy [31-34] in the experimental studies. According to this method, the work function of an alloy in the form of A_xB_{1-x} was,

$$\phi_m = x\phi_{m,A} + (1-x)\phi_{m,B} + x(1-x) \left[\frac{(\phi_{m,A}-\phi_{m,B})(\rho_A/\rho_B)-1}{x(\rho_A/\rho_B)+(1-x)} \right] \quad (2)$$

where ρ_A and ρ_B are total densities of states $\phi_{m,A}$ and $\phi_{m,B}$ are the work functions, and of metal A and B, respectively. The density of states at Fermi level depends on electronic specific heat constant $C_e = (1/3)\pi^2\rho k^2T$. C_e values of Au and Ag are 0.948 and $0.645 \text{ mJmol}^{-1}\text{K}^{-2}$, respectively [26]. Contrary to the model proposed by Fain et al. [31], since this electronic specific heat constant values was not close to each other, so work functions could not show a linear variation. When the work functions considered as 5.22 eV and 4.30 eV for Au and Ag [34], respectively, obtained work functions of alloys was given in Table 1 with the corresponding atomic composition.

Grain size of Schottky metals and condition of the surface of this metal/alloy plays an important role in determining the electrical properties [27, 28]. Atomic force microscopy was used to examine the surface morphology of the Au-Ag Schottky contacts on n-GaAs. Figure 1 shows the *AFM* images of the *Au/n-GaAs* and *Ag/n-GaAs* SDs. As shown in Figure, surface morphology of the SDs was fairly smooth. Root mean square (RMS) roughness of films was found from $20 \times 20 \text{ }\mu\text{m}$ image area and values was 45.9 nm for Au, 37.8 nm for $\text{Au}_{0.71}\text{Ag}_{0.29}$, 46.2 nm for $\text{Au}_{0.37}\text{Ag}_{0.63}$, 29.5 nm for $\text{Au}_{0.22}\text{Ag}_{0.78}$ and 26.1 nm for Ag. Correlation was not observed between the RMS values of the alloys and metals. However, relatively high RMS values are the result of the island-type metallization process observed

during the metallization process [29-31]. The phenomenon of island formation of metals is typically observed between low and high surface energy materials. In order to minimize the total surface energy of the system, the metals/alloys agglomerates to minimize its surface area and exposes more surface area of the low surface energy materials (surface energies were determined as 0.86 J/m^2 , 1.51 J/m^2 and 1.97 J/m^2 for GaAs, Ag and Au, respectively) [32].

Figure 1. AFM micrographs of the Au-Ag Schottky contacts to n-type GaAs.

1.2. Forward bias *I-V* characteristics of the *Au-Ag/n-GaAs* SDs

The semi-logarithmic forward and reverse *I-V* characteristics of one *Au-Ag/n-GaAs* SDs shown in Figure 2. As can be seen in Figure 2, the rectifying properties of the SD depend on

the alloy composition and therefore they depend on the work function. These experimental plots analyzed by using thermionic emission theory, assuming the barrier was homogeneous. According to the theory, the flowing current through the diode in the forward bias region (for $V \geq 3kT/q$) is as follows [7, 33];

$$I = I_0 e^{qV/nkT} \quad (3)$$

and

$$I_0 = AA^*T^2 e^{-q\Phi_b^{IV}/kT} \quad (4)$$

where I_0 , V , n , k , T , A^* , A , q , and Φ_b^{IV} are the saturation current at zero bias, the applied bias voltage, the ideality factor, the Boltzmann constant, the temperature in Kelvin, the effective Richardson constant ($8.16 \text{ Acm}^{-2}\text{K}^{-2}$ for n-GaAs), the effective diode area, the electron charge, and the barrier height, respectively.

Figure 2. The semi-logarithmic I - V characteristics for the Au - Ag / n - $GaAs$ SDs. Only one plot shown here for each set, representing the best value for the average results obtained from the measurements.

In Equation (4), n is a dimensionless parameter and its indicator for the deviation from the theory (ideally equals unity). The experimental values of the n and the Φ_b were determined from slopes and intercepts of the linear regions of the forward bias $\ln I$ - V plots by using Equations (3 and 4). Other calculations and all least square fittings performed via our computer program SeCLaS-PC. The values of the Φ_b and n of the Au - Ag / n - $GaAs$ SD varied with alloy compositions (Table 1). As can be seen in Table 1, the ideality factors of Au - Ag / n - $GaAs$ SDs were higher than the 1. This high value of the ideality factors was generally attributed to an existence of a thin oxide layer between metal and semiconductor, surface preparation techniques, Fermi level pinning, and homogeneity of the surface of the semiconductor [28, 34].

Ideally, when the metal and semiconductor are combined to form a contact, the boundary between the metal and the semiconductor is assumed sharp, but in real situation is different. As stated in previous studies, even if the metallization process carried out at room temperature, solid-state reactions occur between the metal and the semiconductor [29, 31, 34-36]. This was more clearly seen in *Au/GaAs* SDs. Gallide phases formed at the interface was known and have a significant effect on both the n and the Φ_b^{IV} [35, 37]. In this study, similar results were obtained for n and the Φ_b^{IV} and these values vary depending on the contact metal/alloy. The ideality factor of the alloys decreases when the amount of silver increases. The possible reason for this change may be silver prevents the formation of the gallide phases.

It was a well-known method to incorporate very thin barrier metal films in order to allow metals of such diffusive nature to make better contact with semiconductors or to achieve diffusion in a controlled manner.

Table 1. Composition, work function, characteristics diode parameters and standard deviations of the *Au-Ag/n-GaAs* SDs.

Sample	Ag		Au		ϕ_m (eV)	n	$\Phi_b^{(IV)}$ (eV)
	(wt.%)	(at.%)	(wt.%)	(at.%)			
Au	0.0	0.0	100.0	100.0	5.22 [38]	1.171±0.022	0.789±0.022
Au_{0.71}Ag_{0.29}	18.28	29.00	81.72	71.00	5.07	1.158±0.019	0.847±0.008
Au_{0.37}Ag_{0.63}	51.23	63.48	48.77	36.52	4.96	1.188±0.022	0.832±0.004
Au_{0.22}Ag_{0.78}	66.32	78.24	33.68	21.76	4.65	1.238±0.022	0.825±0.010
Ag	100.0	100.0	0.0	0.0	4.30 [38]	1.255±0.027	0.802±0.006

The obtained mean value of barrier height and ideality factor for twenty *Au/n-GaAs* SDs was 0.789±0.022 eV and 1.171±0.022, respectively. These values are considerably lower than the expected barrier height value. However, many studies have obtained different values for the barrier height of these SDs [20, 39-44]. For example; Tunhuma et al. found these values 0.85 eV and 1.10 for *Au/n-GaAs* SDs at room temperature [41]. Özdemir et al. found these values 0.742 eV and 1.247 and, Korucu et al. found that 0.79 eV and 1.034 for *Au/n-GaAs* SDs around the room temperature [42, 43].

The electrical parameters of the diodes depend on the method of cleaning of the substrates [45], the metallization method [46], the etching method [47] etc. Tsukamoto et al. worked on photocatalytic properties of alloy (*Au-Ag*)/*TiO₂* junctions [19]. They founded that the work function of the Au-Ag alloy lies at the level intermediate between the monometallic Au and Ag and calculated theoretical energy-band diagram of *alloy/TiO₂* junction. According to their results, barrier heights changes 0.2 eV to 1.3 eV for *Ag/TiO₂* and *Au/TiO₂*, respectively. The *alloy/TiO₂* junction therefore creates a barrier that is larger than *Ag/TiO₂* but smaller than *Au/TiO₂*. This theoretical calculation does not take into account many parameters that have significant effects on the height of the barrier, such as presence of interface states, inhomogeneity, interface compounds, doping density etc. and defines the parameters in an ideal state. However, it is expected/founded to be compatible with the parameters obtained from the experiments. Therefore, it would be more appropriate to evaluate our diodes, which are

prepared in identical form and built on the same substrate with the approach that they are consistent among themselves.

When this information was taken into consideration, the change in barrier heights depending on the ϕ_m were given in Figure 3. Here, the data related to *Au/n-GaAs* SD not taken into consideration when evaluating the relationship between metal's ϕ_m and Φ_b values. The expected barrier height values could not be observed due to alloying behavior. This behavior causes the AuGa compounds to change the interface chemistry of the Au-GaAs interface as a result of some Ga out-diffusion and solid-state reactions with Au, and the remaining As atoms make the semiconductor highly doped [35, 37, 48]. The exact alloying mechanism that causes the degradation of the SDs was not very clear. This will result in significant field emissions along the barrier and increase the flow through it [48].

This behavior also observed in studies on AlGaIn or GaN substrates [29]. In this study, although there is no annealing process, Ga migration due to solid-state reactions also observed on the contact surface by EDX measurements.

Figure 3. Least squares fit to the *Au-Ag/n-GaAs* SDs Φ_b^{IV} and calculated ϕ_m data. * The data of *Au/n-GaAs* SDs not include fit range.

On the other hand, the presence of a small amount of Ag prevents this diffusion and prevents the gallide phases to occur at the interface [30, 31]. There are many examples in the literature (especially in SD on ternary and quaternary semiconductor substrates) where a thin layer of metal barrier is used to prevent these diffusion/out-diffusion processes [49].

As mentioned earlier, the slope of linear fit in Φ_b versus ϕ_m graph was an indicator of Fermi level pinning and called as “interface behavior parameter” or “gap states parameter” (S) of the semiconductor [2, 8]. Here, if $S=0$ state is called as a “Bardeen limit”, if $S=1$ state is called “Schottky limit”. S parameter was determined as 0.0526 and close to the Bardeen limit, in our study. Therefore, surface states or interface states stabilize the Fermi level of the metal-semiconductor system and, depending on the characteristic parameters of the metal, thus Fermi

level remains unchanged. In this case, the relationship between the density of the interface states and the S parameter given as follow,

$$S = \frac{d\Phi_b^{IV}}{d\phi_m} = \left(1 + \frac{q^2 \delta D_{it}}{\varepsilon_i}\right)^{-1} \quad (5)$$

where, ε_i and δ are permittivity of the interfacial layer and thickness of interfacial layer, respectively [2, 34]. Assuming the $\varepsilon_i = 5\varepsilon_0$ and $\delta = 5 \text{ \AA}$, we calculate $D_{it} = 1.801 \times 10^{11} \text{ eVcm}^{-2}$ from S according to the Equation (5), which has a good agreement with the later results and literature [50].

The downward curvature in I - V curves at relatively high forward bias voltage region arises from the series resistance (R_s), of the semiconductor bulk between the depletion region and Ohmic contact. The R_s values of Au - Ag/n - $GaAs$ SD were calculated using two different methods developed by Cheung's [51] and Norde [52] obtained from the forward bias current equations (Equation 3-4). According to the Cheung and Cheung theory, the barrier height as well as other diode parameters such as n and R_s was also could be determined using Cheung's functions;

$$dV/d\ln(I) = nkT/q + IR_s \quad (6a)$$

and

$$H(I) = IR_s + n\Phi_b \quad (6b)$$

the y-axis intercept and slope of a plot of $dV/d(\ln I)$ vs. I give nq/kT and R_s . Also, a plot of $H(I)$ vs. I give a straight line with the y-axis intercept equal to $n\Phi_b^{Ch}$ (not plotted in here) The slope of this plots also provides a second determination of R_s , which can be used to check the consistency of Cheung's approach. The obtained R_s , n and Φ_b^{Ch} of the SDs were given in Table 2. This serial resistance values were consistent with the literature [46, 53]

Table 2 also contains Norde method results. According to the Norde's method, Norde function ($F(V)$) were expressed as in Equation (7) and where $I(V)$ and γ was a bias dependent current value obtained from the I - V plots and dimensionless integer larger than ideality factor ($\gamma > n$), respectively,

$$F(V) = V/\gamma - kT/q \ln \left(I(V) / A A^* T^2 \right) \quad (7a)$$

and

$$R_s = \frac{kT(\gamma - n)}{qI_{min}}. \quad (7b)$$

and also barrier height (Φ_b^N) given by the

$$\Phi_b^N = F(V_{min}) + V_{min}/2 + kT/q \quad (7c)$$

where $F(V_{min})$ was a minimum point value of $F(V)$, V_{min} and I_{min} corresponding voltage and current values. The plots of $F(V)$ versus V for the Au - Ag/n - $GaAs$ SDs using. Mean values of Φ_b^N and R_s values of twenty Au - Ag/n - $GaAs$ SD were summarized in Table 2.

As can be seen from Table 2, mean Φ_b and R_s values of SD for each set was found to be consistent with the Cheung's approach and Norde's method. R_s values of an intimate metal-semiconductor contact without any desired interfacial layer must only arise from the bulk. The higher values of R_s may be arise from the contribution of the native oxide layer on the semiconductor surface to the neutral region series resistance plus imperfect Ohmic contact. However, in the process of making Ohmic contacts and SD it has contributed to contact resistance in the alloys resulting from solid-state reactions [46].

Table 2. Mean characteristics diode parameters and standard deviations of the twenty (for each set) Au-Ag/n-GaAs SDs obtained from Cheung functions and Norde plots.

Schottky metal	I_0 ($\times 10^{-11}$ A)	Cheung				Norde	
		n	R_s (Ω)	Φ_b^{Ch} (eV)	R_s (Ω)	Φ_b^N (eV)	R_s (Ω)
Au	41.27 $\pm$ 19.30	1.163 $\pm$ 0.059	31.33 $\pm$ 10.34	0.785 $\pm$ 0.033	31.24 $\pm$ 10.47	0.704 $\pm$ 0.018	29.66 $\pm$ 10.66
Au_{0.71}Ag_{0.29}	3.670 $\pm$ 1.306	1.128 $\pm$ 0.022	14.02 $\pm$ 4.35	0.856 $\pm$ 0.010	13.81 $\pm$ 4.23	0.741 $\pm$ 0.005	13.61 $\pm$ 3.46
Au_{0.37}Ag_{0.63}	6.412 $\pm$ 1.078	1.186 $\pm$ 0.044	36.28 $\pm$ 11.77	0.824 $\pm$ 0.015	36.08 $\pm$ 12.04	0.743 $\pm$ 0.007	33.31 $\pm$ 12.27
Au_{0.22}Ag_{0.78}	8.776 $\pm$ 3.947	1.236 $\pm$ 0.041	9.37 $\pm$ 4.59	0.820 $\pm$ 0.012	8.92 $\pm$ 4.69	0.742 $\pm$ 0.009	9.33 $\pm$ 3.98
Ag	20.68 $\pm$ 4.573	1.224 $\pm$ 0.041	4.37 $\pm$ 2.66	0.809 $\pm$ 0.012	3.87 $\pm$ 2.66	0.719 $\pm$ 0.008	5.98 $\pm$ 1.65

If there are interface states exist between metal and semiconductor and in equilibrium with semiconductor, the ideality factor of the SD will be greater than unity because of this conditions [16, 54]. The density of these states (D_{it}^{IV}) expressed as following equation;

$$D_{it}^{IV} = 1/q \left[\frac{\epsilon_i}{d} (n(V) - 1) - \frac{\epsilon_s}{w} \right] \quad (8)$$

Here, d and ϵ_s are the interfacial layer width and permittivity of the semiconductor, respectively. The depletion layer width was determined from the C - V measurements at a high frequency. Also, $n(V)$ is the ideality factor depending on the bias voltage and given by $n(V) = (V/kT) \ln(I/I_0)$. In an n-type semiconductor, the energy of the interface states E_{ss} with respect to the top of the conduction band (E_c) at the surface of the semiconductor is given by

$$E_c - E_{ss} = q\phi_e - qV \quad (9)$$

where, $q\phi_e = \Phi_b^{IV} + (1 - 1/n)qV$. Interface state density distribution profile of the s for Au-Ag/n-GaAs SDs were obtained from the experimental I - V plots and were shown in Figure 4. For all Au-Ag/n-GaAs SDs there was a slight exponential increment seen in D_{it}^{IV} from the nearly mid-gap towards the bottom of the conductance band. Furthermore, when the Ag content increased in the Schottky contact metal, the interface state density increases. This decreasing D_{it}^{IV} values are supports our proposed approach for interface chemistry by a Ga out-diffusion. Gallide phases causes a much lower interface state density.

Figure 4. D_{it}^{IV} vs. $E_C - E_{SS}$ plots for $Au-Ag/n-GaAs$ SDs.

1.3. Reverse bias $I-V$ characteristics of the $Au-Ag/n-GaAs$ SDs

Reverse bias $I-V$ characteristics could also be used for determine some parameters of the fabricated $Au-Ag/n-GaAs$ SDs. Figure 2 reveals that the reverse current (I_R) of the $Au-Ag/n-GaAs$ SDs increases with increasing bias, but not saturated. Different mechanisms cause a leakage current and becomes an effective. The reverse current conduction mechanism of $Au-Ag/n-GaAs$ investigated based on the Poole-Frenkel emission (PFE) and Schottky emission (SE) models [33, 55]. The reverse bias current as a function of the negative bias can be written as

$$I_R = I_{0R} \exp\left(\frac{\beta_{PF} V^{1/2}}{kT d^{1/2}}\right) \quad (10a)$$

here

$$I_{0R} = AA^* T^2 \exp\left(-\frac{\Phi_b^{RB}}{kT}\right) \quad (10b)$$

where I_{0R} , β_{PF} and Φ_b^{RB} are reverse saturation current, PFE field-lowering coefficient and reverse bias barrier height (Φ_b^{RB}), respectively. The theoretical values of field lowering coefficients given by

$$\beta_{PF}^* = 2\beta_{SE} = \left[q^3 / \pi \epsilon_s \epsilon_0\right]^{1/2} \quad (11)$$

where β_{SE} is the field-lowering coefficient of SE. According to Equation (11), the theoretical values of the field lowering coefficients (β_{PF}^*) for the $Au-Ag/n-GaAs$ SDs were determined as $4.412 \times 10^{-5} \text{ eVm}^{1/2} \text{V}^{-1/2}$. Mean values of Φ_b^{RB} and β_{PF} values of twenty $Au-Ag/n-GaAs$ SD were summarized for each set in Table 3. As can be seen from Table 3, values of experimental slope for the $Au-Ag/n-GaAs$ SDs are changes from $1.375 \pm 0.068 \text{ eVm}^{1/2} \text{V}^{-1/2}$ to $1.560 \pm 0.209 \text{ eVm}^{1/2} \text{V}^{-1/2}$, which were closely matched with the theoretical slope of SE. Thus, the dominating charge conduction mechanism for the $Au-Ag/n-GaAs$ SDs are assumed the SE.

Table 3. Mean characteristics diode parameters and standard deviations of the twenty (for each set) *Au-Ag/n-GaAs* SDs obtained from reverse bias *I-V* plots.

Schottky metal	Model	β_{PF} ($\times 10^{-5} \text{ eVm}^{1/2}\text{V}^{-1/2}$)	Φ_b^{RB} (eV)	I_0 ($\times 10^{-8} \text{ A}$)
Au	Schottky emission	1.450±0.160	0.671±0.022	5.507±9.509
Au _{0.71} Ag _{0.29}	Schottky emission	1.502±0.122	0.715±0.024	0.939±1.036
Au _{0.37} Ag _{0.63}	Schottky emission	1.540±0.198	0.704±0.026	1.305±0.888
Au _{0.22} Ag _{0.78}	Schottky emission	1.375±0.068	0.677±0.036	6.832±10.02
Ag	Schottky emission	1.560±0.209	0.711±0.040	1.848±3.170

1.4. C-V characteristics of the *Au-Ag/n-GaAs* SD

The bias dependent *C-V* characteristics of the *Au-Ag/n-GaAs* SDs measured at dark and room temperature. Figure 5 shows a plot of C^{-2} as a function of bias voltage for the Au-Ag alloy (at.% 0-100) on n-GaAs SDs at sufficiently high frequency (1 MHz or above). The main purpose of these *C-V* measurements were reveal the properties of the space charge region of SDs. The relationship between the capacitance of the space charge region and the applied dc bias in metal-semiconductor contacts given as follows [7, 12],

$$1/C^2 = \frac{2(V_{bi} - kT/q - V)}{A^2 q N_d \epsilon_s} \quad (12)$$

where, V_{bi} was the built-in potential and N_d were the doping concentration of the GaAs substrate. According to the Equation (12) ($1/C^2$) versus V plots gives straight line with the slope were equals to $2/q\epsilon_s N_d$ and intercepts the x-axis equals to V_0 (Figure 5). Here; V_0 is related with the built-in potential V_{bi} by the equation $V_{bi} = V_0 + kT/q$ and barrier height were given by equation [7],

$$\Phi_b^{CV} = V_{bi} + V_n \quad (13)$$

where, V_n is the potential difference between the bottom of the conduction band and the Fermi level in the neutral region of n-GaAs and $V_n = (kT/q) \ln(N_c/N_d)$, where N_c is the temperature dependent density of states in the conduction band and its value was calculated from the $N_c = 2(2\pi m^* kT/h^2)^{3/2}$, and $m^* = 0.063m_0$, and found $4.573 \times 10^{17} \text{ cm}^{-3}$ for GaAs at 300 K. The values of Φ_b^{CV} and N_d for the *Au-Ag/n-GaAs* SDs were given in Table 4. In Table 4, the barrier heights obtained by *C-V* method of the SDs were changes between the $1.035 \pm 0.022 \text{ eV}$ and $0.912 \pm 0.013 \text{ eV}$. These obtained barrier height values are higher than obtained from *I-V* measurements for corresponding to each alloy composition. Arulkumaran et al. prepared *Au/n-GaAs* and *Ag/n-GaAs* SDs and barrier height values varied from 0.82-0.93 eV and from 0.75-1.05 eV, respectively [44]. Also, barrier height found here were reasonable agreement with a value of 0.97 eV from *C-V* characteristics of *Au/n-GaAs* and *Ag/n-GaAs* of nearly the same doping concentration [15].

Figure 5. The C^{-2} versus reverse bias characteristics for the $Au-Ag/n-GaAs$ SDs. Only one plot shown here for each set, representing the best value for the average results obtained from the measurements.

Although the same parameter was measured, the difference between the Φ_b^{CV} 's can be attributed to existence of lateral inhomogeneity [56]. The source of this lateral inhomogeneity was potential fluctuations at the interface. These fluctuations generally attributed to the thickness of the contact metal, non-uniform distribution at the interface, dislocations, packing errors in the crystal and a thin native oxide layer at the interface, irregularities in the atomic scale on the semiconductor surface, and defects in bulk, and so on [56, 57]. These potential fluctuations affect the dc current and the capacitance measurements in different ways. Diode capacitance was caused by the displacement of the charge carriers in the space charge region due to the ac frequency signal. This displacement was observed at near the boundaries of the space charge region. Therefore, the capacitance of the diodes depends on this space charge region and causes the barrier height to be measured only as an average value. The dc current flowing through the diode preferably tends to flow only where the Φ_b^{CV} was the lowest.

Table 4. The obtained characteristics diode parameters and standard deviations of the $Au-Ag/n-GaAs$ SDs from the $C-V$ measurements.

Schottky metal	N_d ($\times 10^{17} \text{cm}^{-3}$)	V_{bi} (V)	Φ_b^{CV} (eV)
Au	9.103 ± 0.836	0.909 ± 0.012	0.912 ± 0.013
Au_{0.71}Ag_{0.29}	8.288 ± 0.789	1.032 ± 0.022	1.035 ± 0.022
Au_{0.37}Ag_{0.63}	6.939 ± 0.413	0.998 ± 0.025	1.001 ± 0.025
Au_{0.22}Ag_{0.78}	6.886 ± 0.672	0.976 ± 0.007	0.980 ± 0.007
Ag	8.097 ± 1.235	0.959 ± 0.013	0.963 ± 0.013

Besides the $I-V$ measurements, the using a single-frequency approximation method [58] on the conductance measurements results, allows the estimation of the D_{it} . This method was one of the reliable way to determine the density of interface states. According to this method, D_{it}^{CV} can be find using the following formula,

$$D_{it}^{CV} = \frac{2}{qA} \frac{(G_m)_{max}/\omega}{\left((G_m)_{max}/\omega C_{ox}\right)^2 + \left(1 - C_m/C_{ox}\right)^2} \quad (14)$$

where G_m ω are measured conductance and angular frequency of ac signal, C_m is measured capacitance. C_{ox} is the capacitance of oxide layer in accumulation region of C - V curves, $(G_m)_{max}$ conforms to maximum G - V curve and C_m is the capacitance of the diodes corresponding to $(G_m)_{max}$. Also, the series resistance of the equivalent circuit is [58, 59],

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2}. \quad (15)$$

This method was applied on C - V and G - V measurement results in the frequency range from 200 Hz to 2 MHz. Figure 6 depicts the changings in D_{it}^{CV} with the frequency, both axis is log scale. D_{it}^{CV} values of Au - Ag / n - $GaAs$ SDs strongly depend on frequencies and decrease at lower and higher frequency range. This “U” type behavior of the interface states has a minimum value that varies from diode to diode.

Figure 6. Mean D_{it}^{CV} values versus ac signal frequency plots of the Au - Ag / n - $GaAs$ SDs.

This minimum value and sufficiently constant D_{it}^{CV} values appear at relatively high frequencies attributed to the excess capacitance. This excess capacitance because of interface states which is in equilibrium with the semiconductor that can easily follow the ac signal [60]. D_{it}^{CV} values of Au - Ag / n - $GaAs$ SDs are same order as those reported by some authors. [50].

Figure 7. Mean R_s values versus frequency plots of the $Au-Ag/n-GaAs$ SDs. Inset shows bias dependent R_s values of one of the $Au/n-GaAs$ SD.

The frequency dependent series resistance values of $Au-Ag/n-GaAs$ SDs estimated according to Equation (15) using with the measured capacitance and conductance values in the frequency range from 200Hz to 2MHz at room temperature and plotted in Figure 7. This plot clearly indicates that when the frequency decreased, interface states cannot follow the ac signal and each states produces an excess capacitance and conductance, and becomes a resistive point for charge carriers and increases exponentially. Inset in Figure 7 shows that series resistance gives a peak depending on frequency in the wide negative bias range and second peak appear after 0V.

4. Conclusion

In this study, $Au-Ag/n-GaAs$ SDs fabricated by thermal evaporation method and investigated the effect of work function of metals on SD's parameters. *TLM* results indicates that Ohmic contact resistance was very low and *EDX* results indicates that the alloy's percentage (x) by weight values were 0.22, 0.37 and 0.71. Also, *AFM* images showed that the smooth contacts were made. Au_xAg_{1-x} (x=0, 0.22, 0.37, 0.71 and 1) alloys were used for fabricating SDs by following same cleaning procedure with using the n-type GaAs substrate and then, characterized by various methods and techniques. In addition, characteristic parameters of SDs have been determined and compared with each other.

The lowest mean barrier height of about 0.789 ± 0.022 eV in $Au/n-GaAs$ SDs and the highest mean barrier height 0.847 ± 0.008 eV in $Au_{0.71}Ag_{0.29}/n-GaAs$ SDs were observed (from *I-V* measurements). Φ_b values of $Au/n-GaAs$ SDs were lower than the expected value and, explained by the presence of the gallide phases at the interface. It was observed that the Ag was prevents the Au diffusion in to the GaAs substrate or out diffusion of Ga. Furthermore, it was found that an almost linear relationship between Schottky barrier height and metal work function (with $\Phi_b^{IV} = 0.0526\phi_m + 0.577$). Gap states parameter (S) found as a 0.0526 and, close to the Bardeen limit ($S=0$). In summary, Fermi level pinning model proposed by Cowley and Sze applies not only to metal-GaAs contacts but also to alloy-GaAs contacts, and indicates that

Fermi level was strongly pinned 0.577 eV below the conduction band in our SD's. Also, from this dependency, the density of states was determined as $1.801 \times 10^{11} \text{ eVcm}^{-2}$. This interface state density value was in the same order of magnitude with the D_{it}^{IV} values (calculated from I - V measurement result) and D_{it}^{CV} values (calculated from C - V measurement result).

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Figures

Figure 1

AFM micrographs of the Au-Ag Schottky contacts to n-type GaAs.

Figure 2

The semi-logarithmic I-V characteristics for the Au-Ag/n-GaAs SDs. Only one plot shown here for each set, representing the best value for the average results obtained from the measurements.

Figure 3

Least squares fit to the Au-Ag/n-GaAs SDs Φ_b IV and calculated ϕ_m data. * The data of Au/n-GaAs SDs not include fit range.

Figure 4

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Figure 5

The C^{-2} versus reverse bias characteristics for the Au-Ag/n-GaAs SDs. Only one plot shown here for each set, representing the best value for the average results obtained from the measurements.

Figure 6

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Figure 7

Mean R_s values versus frequency plots of the Au-Ag/n-GaAs SDs. Inset shows bias dependent R_s values of one of the Au/n-GaAs SD.