KLECTOR: Design of Low Power Static Random-Access Memory Architecture with reduced Leakage Current

Ananth Kumar Tamilarasan (✉ ananth.eec@gmail.com)

IFET college of Engineering <https://orcid.org/0000-0002-0494-7803>

Darwin Sundarapandi Edward

Dr Sivanthi Aditanar College of Engineering

Arun Samuel Thankamony Sarasam

National Engineering College

Research Article

Keywords: SRAM, Leakage current, LECTOR, KLECTOR, Static power

Posted Date: February 24th, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-232660/v1>

License: This work is licensed under a Creative Commons Attribution 4.0 International License.

[Read Full License](#)

KLECTOR : Design of Low Power Static Random-Access Memory Architecture with reduced Leakage Current

Ananth kumar Tamilarasan¹, Darwin Sundarapandi Edward², Arun Samuel Thankamony Sarasam³

¹Assistant Professor, Dept. of Computer Science & Engineering, IFET College of Engineering, India.

ananth.eec@gmail.com

²Assistant Professor, Dept. of Electronics and Communication Engineering, Dr.Sivanthi Aditanar College of Engineering, India.

darwin.mell@gmail.com

³Associate Professor, Dept. of Electronics and Communication Engineering, National Engineering College, Kovilpatti, Tamilnadu, India.

arunsamuelece@nec.edu.in

Abstract - A novel approach called Keeper in LEakage Control Transistor (KLECTOR) is presented in this paper to reduce leakage currents in SRAM architecture. The SRAM is significantly affected by the leakage current during the "standby mode", which is caused by the fabric which has a lower threshold voltage. KLECTOR circuit employs less power consumption by restricting the flow of current through devices of less voltage drops and relies heavily on the self-controlled transistor at the output node. It has been found from the presented results that static (leakage) power in the write operation is reduced to 63% and 69 % for the read operation. This proposed approach is designed and simulated using the Virtuoso, Cadence EDA tool.

Keywords – SRAM; Leakage current; LECTOR; KLECTOR; Static power;

I. INTRODUCTION

In VLSI circuits, the basic key elements are memories, processor and logic devices which decide the effective power utilization based on current consumed in each stage. The advancements in VLSI technology demand low power devices to enhance larger operating time which are limited by leakage currents in various operation cycle [1,2]. The low power architecture of SRAM (Static Random-Access Memory) plays a dominant role in various applications due to its speed and long-term resistance [3]. Configurable Logic Block (CLB) is a major block in VLSI design involved devices like SPARTAN and VIRTEX architecture [4-5,15]. CLB consist of 20% to 30% SRAM cell [16] because it has the advantage of reprogrammable capability and speed. There are different types of SRAM basic cells available in CLB block in which some of the basic cell is activated based on word length while remaining cells are maintained in standby mode. The Leakage current plays a dominant role in SRAM power consumption during standby mode [7] [10-13]. This technique makes the leakage power consumption more than dynamic power which directly affects the speed of the SRAM operation [14]. This results in short channel effects that exponentially increase sub-threshold leakage current. Therefore, the CMOS system will leak power due to a sub-threshold leak current of this current value. When voltage is applied to the gate, the current will flow from the source to the drain, even though there is no voltage applied to the gate. The Transistor is in the area of low inversion, i.e., Reduction of the thickness of the door oxide increases the field oxide across the door that results in electron flows from door to door or substratum to door. The resulting tunneling current fluctuates into oxide. Various methods for eliminating leakage current are used in the literature. Some common techniques include sleep transistor, stacking technique, Zigzag technology, sleepy stack technology, sleepy technique, Zigzag technique,

technical feedback on leakage, LECTOR technical, GALEOR technical and LSSR technique [6-9]. The first 7 techniques require extra monitoring input circuitry because according to SRAM work condition (active or standby mode) we need to change the input of extra adding transistor. In GALEOR technique power is reduced but voltage swing problem is occurred. In LSSR power is reduced with area penalty. So, among these techniques, LECTOR is the best technique for our application/architecture to reduce leakage current in SRAM. But the provision of sleep mode of operation for state retention is not possible. Hence, one of the devoted merits of Sleepy Keeper circuit is of state retention. The performance factors of LECTOR and Sleepy Keeper techniques were combined to focus on new emerging technique called KLECTOR to meet the trends and future projections in this area. Every technique has its limitations and can be used based on the application specific requirements [16]. To overcome the performance degradation of SRAM, KLECTOR technique is proposed and implemented in SRAM architecture to reduce the leakage current in it [17][18]. This paper is organized as follows; LECTOR approach is discussed below. Section II discusses the proposed KLECTOR technique in SRAM. The experimental results are discussed in Section III. SRAM's performance is evaluated in Section IV and Section V concludes the paper.

1.1 LECTOR APPROACH

LECTOR connects the pull-up and pull-down network transistors (pmos and nmos) in series mode. The LECTOR technology is also known as the self-control technology [9] subsequently the pmos transistor gateway is connected to the pull-down network and the nmos transistor to the network pull-up gate [3]. The transistors create a large sensitive path between VDD and GND, which reduces the SRAM leakage current during stand-by mode. Figure 1 shows the basic structure of LECTOR.

Figure 1 LECTOR approach.

The Figure of 1bit SRAM with LECTOR technique as shown in Figure 2,

Figure 2. 1bit SRAM with LECTOR approach.

The SRAM basic cell contains two access transistors (M5 and M6) and bi-stable latch (M1 to M4). LECTOR technique consists of basic SRAM cell with four leakage control transistors (M7 to M8) as shown in figure 3. For reading and writing operation, R/W is always "1," it always lets transistors reach transistors (M5 & M6) ON.

For Write "0" BL=0 and BL =1. BL=0, signal makes the transistors M3 ON and M4 OFF. M9 and M10 transistors are connected in series between M3 & M4 transistors. M3 & M4 leads to the transistors M9 & M10 are ON. BL =1 signal makes a transistors M1 OFF & M2 ON. M7 and M8 transistors are connected in series between M1 & M2 transistors. M1 & M2 leads to the transistors M7 & M8 are OFF. The output is taken from the drain of M1 transistor; M1 OFF means output is 0 and vice versa for write "1" operation.

For Read "1" BL=0 and BL =0. BL=0, signal makes the transistors M3 ON and M4 OFF. M9 and M10 transistors are connected in series between M3 & M4 transistors. M3 & M4 leads to the transistors M9 & M10 are ON. BL =0 signal makes a transistors M1 ON & M2 OFF. M7 and M8 transistors are connected in series between M1 & M2 transistors. M1 & M2 leads to the transistors M7 & M8 are ON. The output is taken from the drain of M1 transistor; M1 ON means output is 1 and vice versa for Read "0" operation use bar on BL in proper way.

II. PROPOSED: KLECTOR TECHNIQUE

The prevailing dominant technologies in leakage current detection are Keeper and LECTOR Techniques. KLECTOR Technique overcomes the disadvantages of LECTOR technique. KLECTOR is a combination of LECTOR and keeper technique.

The Figure 3 shows the basic structure of KLECTOR technique.

Figure 3 KLECTOR approach.

In this case, the transistor (pmos and nmos) of leakage control is inserted in between the network pull-up and pull-down. All pmos and nmos are linked in parallel for securing standby maintenance mode. The PMO gate is linked to the downstream and the nmos gate is linked to the upstream network so that no monitoring circuit is necessary to control the additional transistor.

The Figure 4 shows the basic 1bit SRAM cell with KLECTOR approach.

Figure 4 1bit SRAM cell with KLECTOR approach use dot or half circle in circuit to distinguish connection and cross over: like Gate of M1 and M3 is obviously not connected but this is not represented proper

The basic SRAM cell that is available contains two access transistors such as M5 and M6, one of which is on and the other is off (M1 to M4). KLECTOR technique consists of basic SRAM cell with four leakage control transistors (M7 to M10) as shown in figure 4. For Read

and write operation, R/W is always “1”, it makes transistors Access transistors (M5 and M6) always ON.

For Write “0” $BL=0$ and $\overline{BL}=1$. $BL=0$, signal makes the transistors M3 ON and M4 OFF. M9 and M10 transistors are connected in parallel between M3 & M4 transistors. M3 & M4 leads to the transistors M9 OFF & M10 ON. $\overline{BL}=1$ signal makes a transistors M1 OFF & M2 ON. M7 and M8 transistors are connected in parallel between M1 & M2transistors. M1 & M2 leads to the transistors it will cause M7 ON an M8 OFF. The output is taken from the drain of M1 transistor; M1 OFF means output is 0 and vice versa for write “1” operation.

For Read “1” $BL=0$ and $BL=0$. $BL=0$, signal makes the transistors M3 ON and M4 OFF. M9 and M10 transistors are connected in parallel between M3 & M4 transistors. M3 & M4 leads to the transistors same issue as above: M9 OFF, M10 ON. $BL=0$ signal makes a transistors M1 ON & M2 OFF. M7 and M8 transistors are connected in parallel between M1 & M2transistors. M1 & M2 leads to the transistors M8 ON and M7 OFF. The output is taken from the drain of M1 transistor; M1 ON means output is 1 and vice versa for Read “0” operation.

III. RESULTS & DISCUSSION

The implementation of LECTOR and KLECTOR technique in SRAM is done using Cadence v6.1.5 tool. The design is simulated using Spectre simulator of Cadence Design System (Spectre or HSPICE)

Figure 5 Schematic diagram of SRAM cell with LECTOR technique to write 0.

Figure 5 illustrates the SRAM cell schematic map with LECTOR technique. It contains one control signal, two inputs and one output. Control signal R/W is always high. Input BL =0 & BL=1 “0” is written in a basic cell of SRAM

Figure 6 schematic diagram of SRAM cell with LECTOR technique to write 1.

The figure 6 illustrates the schematic view of SRAM cell with LECTOR technique. It comprises one control signal, two inputs and one output. Control signal R/W is always high. Input BL =1 & BL=0 “1” is written in a basic cell of SRAM.

Figure 7 Schematic diagram of SRAM cell with LECTOR technique to read 0.

Figure 7 displays the schematic of LECTOR technology for the SRAM cell. It comprises one control signal, two inputs and one output. Control signal R/W is always high. Input BL = 1 & $\overline{BL} = 1$ "0" is read from the basic cell of SRAM.

Figure 8 schematic diagram of SRAM cell with LECTOR technique to read 1.

The above figure 8 shows SRAM cell schematic diagram with LECTOR technique. It consists of one control signal, two inputs and one output. Control signal R/W is always high. Input BL=0 & BL=0 “1” is read from the basic cell of SRAM.

Figure 9 schematic diagram of SRAM cell with KLECTOR technique to write 0.

The above figure 9 displays the SRAM cell’s schematic view with KLECTOR technique. It consists of one control signal, two inputs and one output. Control signal R/W is always high. Input BL=0 & BL=1 “0” is written in a basic cell of SRAM.

Figure 10 schematic diagram of SRAM cell with KLECTOR technique to write 1.

The figure 10 displays the SRAM cell schematic diagram with KLECTOR technique for write 1. It consists of one control signal, two inputs and one output. Control signal R/W is always high. Input BL =1 & $\overline{BL}$ =0 "1" is written in a basic cell of SRAM.

Similarly, we have developed the SRAM cell with KLECTOR technique to read 0. It consists of one control signal, two inputs and one output. Control signal R/W is always high. Input BL =1 & BL=1 "0" is read from the basic cell of SRAM. Likewise, to read 1, Control signal R/W is always high. Input BL =0 & BL=0 "1" is read from the basic cell of SRAM.

Figure 11 simulation waveform of write 0 & 1 in SRAM cell.

The above figure 11 shows the simulation waveform of SRAM cell for write operation. If $BL=0$ & $BL=1$, “0” value is display in output else if $BL=1$ & $BL=0$, “1” value is display in output.

Figure 12 Simulation waveform of read 0 & 1 in SRAM cell.

The above figure 12 shows the simulation waveform of SRAM cell for read operation. If $BL=0$ & $BL=0$, “1” value is display in output else if $BL=1$ & $BL=1$, “0” value is display in output. Figure 13 show the layout of proposed 10T KLECTOR SRAM cells using gpdk 180nm technology in Cadence EDA tool.

Figure 13 Layout of 10T KLECTOR SRAM

Power Consumption

The Static power consumption of cell with LECTOR technique to write 0 consumes power of $203.4963\mu\text{W}$ for DC power supply of 2V. The Static power consumption of cell with LECTOR technique to write 1 consumes power of $203.4963\mu\text{W}$ for DC power supply of 2V. The Static power consumption of cell with LECTOR technique to read 0 consumes power of $406.9926\mu\text{W}$ for DC power supply of 2V. The Static power consumption of cell with LECTOR technique to read 1 consumes power of 63.58605pW for DC power supply of 2V.

The Static power consumption of cell with KLECTOR technique to write 0 consumes power of 18.4859fW for DC power supply of 2V. The Static power consumption of cell with KLECTOR technique to write 1 consumes power of 18.4859fW for DC power supply of 2V.

The Static power consumption of cell with KLECTOR technique to read 0 consumes power of 13.27419fW for DC power supply of 2V. The Static power consumption of cell with KLECTOR technique to read 1 consumes power of 23.69761fW for DC power supply of 2V.

IV. PERFORMANCE EVALUATION

Table 1 Static Power Value of SRAM cell

TECHNIQUES	POWER VALUE (W)			
	TO WRITE “0”	TO WRITE “1”	TO READ “0”	TO READ “1”
LECTOR	203.4963μ	203.4963μ	406.9926μ	63.58624p
KLECTOR	18.4859f	18.4859f	13.27419f	23.69761f

Leakage current is derived from the static power value by using this formula.

Static Power = Leakage Current * Supply Voltage

$$\text{Leakage Current} = \frac{\text{Static Power}}{\text{Supply Voltage}}$$

Table 2 Leakage current value in SRAM Cell

TECHNIQUES	LEAKAGE CURRENT VALUE(A)			
	TO WRITE “0”	TO WRITE “1”	TO READ “0”	TO READ “1”
LECTOR	101.74815μ	101.74815μ	203.4963μ	32.79312p
KLECTOR	9.24295f	9.24295f	6.637095f	11.848805f
%LEAKAGE CURRENT REDUCED	63	63	68	70

In Table 1, It clearly states that the KLECTOR technique performs well in reducing the static power consumption. Table 2 shows that the leakage current in SRAM cell is reduced more than 70 times compared to previous technique.

V. CONCLUSION

In this paper, the KLECTOR technique has been designed and analyzed for low power consumptions in SRAM. The KLECTOR circuit will lead to a considerable reduction of the energy drop that occurred due to lose or leaked voltages. The SRAM power consumption is reduced as its leakage in SRAM is reduced. The static power in SRAM gets reduced by 63 percentage in write operation and 69 percentage in read operation by using KLECTOR modern technologies.

Declarations

Conflict of interest : We declare no conflict of interest.

References

1. Panigrahi, B. K., & Jena, R. K. (2021). Investigate, Analyze, and Design of Real-Time Problems in the Domain of Power Electronics and Energy Using MATLAB: Review and Application. *Advances in Energy Technology*, 235-265.
2. Arul Rathi, C., Rajakumar, G., Ananth Kumar, T., & Arun Samuel, T. S. (2020). Design and Development of an Efficient Branch Predictor for an In-order RISC-V Processor. *Journal of Nano-& Electronic Physics*, 12(5).
3. Ramaswamy, Manjith. "Proficient Static RAM design using Sleepy Keeper Leakage Control Transistor & PT-Decoder for handheld application." *Informacije MIDEM* 48, no. 4 (2019): 197-203.
4. Dilip, B., and Surya Prasad, P. (2012). LECTOR: A Technique for Leakage Reduction in CMOS Circuits. *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, 12(2), 196-205.
5. Geetha Priya, M., Baskaran, K., & Krishnaveni, D. (2011). Leakage Power Reduction Techniques in Deep Submicron Technologies for VLSI Applications. *International Conference on Communication Technology and System Design, Procedia Engineering*, 30, 1163-1170.
6. Sharroush, S. M. (2020, October). An MTCMOS Subthreshold-Leakage Reduction Algorithm. In *2020 2nd Novel Intelligent and Leading Emerging Sciences Conference (NILES)* (pp. 7-14). IEEE.
7. Cerqueira, J. P., Repetti, T. J., Pu, Y., Priyadarshi, S., Kim, M. A., & Seok, M. (2020). Catena: A Near-Threshold, Sub-0.4-mW, 16-Core Programmable Spatial Array Accelerator for the Ultralow-Power Mobile and Embedded Internet of Things. *IEEE Journal of Solid-State Circuits*, 55(8), 2270-2284.
8. Bhargav, K. N., Suresh, A & Gaurav Saini. (2014). Stacked Keeper with Body Bias: A New Approach to Reduce Leakage Power for Low Power VLSI Design, *IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT)*, 445- 450.
9. Se Hun Kim & Vincent J. Mooney III. (2006). Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design. *IFIP International Conference on Very Large Scale Integration (IEEE)*. 367-372. <https://doi.org/10.1109/VLSISOC.2006.313263>.
10. Ruchi & Dasgupta, S. (2017). 6T SRAM cell analysis for DRV and read stability. *Journal of Semiconductors*, 38(2), 025001-1 - 025001-7.

11. Achiranshu Garg & Tony Tae-Hyoung Kim. (2013). SRAM Array Structures for Energy Efficiency Enhancement. IEEE Transactions on Circuits and Systems—II: Express Briefs, 60(6), 1-5.
12. Anitha, D., Manjunathachari, K., Sathish Kumar, P & Prasad, G. (2017). Design of low leakage process tolerant SRAM cell. Analog Integrated Circuits and Signal Processing, 93(3), 531-538.
13. Rohit Lorenzo & Saurabh Chaudhury. (2017). A novel 9T SRAM architecture for low leakage and high performance, Analog Integrated Circuits and Signal Processing, 92(2), 315-325.
14. Govind Prasad & Alekhya Anand. (2015). Statistical Analysis of low-power SRAM cell structure, Analog Integrated Circuits and Signal Processing, 82(1), 349-358.
15. Pankaj Kr., Pal, Rituraj S., Rathore, Ashwani K., Rana, Gaurav Saini. (2010). New Low-Power Techniques: Leakage Feedback with Stack & Sleep Stack with Keeper. International Conference on Computer and Communication Technology (ICCCT). 296-301. <https://doi.org/10.1109/ICCCT.2010.5640514>.
16. Herrera-Alzu, I., López-Vallejo, M., (2013). Design Techniques for Xilinx Virtex FPGA Configuration Memory Scrubbers. IEEE Transactions on Nuclear Science, 60(1), 376-385.
17. Naresh Kumar Reddy, B., Ramalingaswamy Ch., Nagulapalli R & Dharavath Ramesh. (2018). A novel 8T SRAM with improved cell density. Analog Integrated Circuits and Signal Processing, <https://doi.org/10.1007/s10470-018-1309-z>.
18. Tamilarasan, A.K., Krishnadhas, S.K., Sabapathy, S. et al. A novel design of Rogers RT/duroid 5880 material based two turn antenna for intracranial pressure monitoring. Microsyst Technol (2021). <https://doi.org/10.1007/s00542-020-05122-y>

Figures

Figure 1

LECTOR approach.

Figure 2

1bit SRAM with LECTOR approach.

Figure 3

KLECTOR approach.

Figure 4

1bit SRAM cell with KLECTOR approach use dot or half circle in circuit to

Figure 5

Schematic diagram of SRAM cell with LECTOR technique to write 0.

Figure 6

schematic diagram of SRAM cell with LECTOR technique to write 1.

Figure 7

Schematic diagram of SRAM cell with LECTOR technique to read 0.

Figure 8

schematic diagram of SRAM cell with LECTOR technique to read 1.

Figure 9

schematic diagram of SRAM cell with KLECTOR technique to write 0.

schematic diagram of SRAM cell with KLECTOR technique to write 1.

Figure 11

simulation waveform of write 0 & 1 in SRAM cell.

Figure 12

Simulation waveform of read 0 & 1 in SRAM cell.

Figure 13

Layout of 10T KLECTOR SRAM