Simulation of β - Ga2O3 based MOSFETs for Depletion and Enhancement Mode Operation

Pharyanshu Kachhawa (kachhawapharyanshu@gmail.com)
CEERI Pilani: Central Electronics Engineering Research Institute CSIR https://orcid.org/0000-0002-2743-5827

Nidhi Chaturvedi
CEERI Pilani: Central Electronics Engineering Research Institute CSIR

Research Article

Keywords: β−Ga2O3 ,Recessed gate ,Depletion mode ,Enhancement-mode

Posted Date: May 20th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-232838/v1

Noname manuscript No.
(will be inserted by the editor)

Simulation of $\beta - Ga_2O_3$ based MOSFETs for Depletion and Enhancement mode operation

Pharyanshu Kachhawa · Nidhi Chaturvedi

Received: date / Accepted: date

Abstract This paper reports on TCAD-simulation of beta-gallium oxide ($\beta - Ga_2O_3$) MOSFET with the channel recessed into a 1 μm thick Si-doped ($1\times10^{18} cm^{-3}$) epitaxial layer. We optimized gate recess thickness to achieve both, depletion and enhancement mode operation. The simulated $\beta - Ga_2O_3$ MOSFET structures show optimum depletion-mode and enhancement-mode characteristics for 150 nm and 15 nm active channel thickness, respectively. A comparative study is also done to analyze the thermal and electrical effects by simulating hetero-epitaxial $\beta - Ga_2O_3$ layer on sapphire substrate and homo-epitaxial $\beta - Ga_2O_3$ layer on $\beta - Ga_2O_3$ substrate. MOSFET devices based on $\beta - Ga_2O_3$ layers on sapphire substrates show improved performance compared to devices based on $\beta - Ga_2O_3$ layers on $\beta - Ga_2O_3$ substrates in terms of drain current, trans-conductance and breakdown voltage. $\beta - Ga_2O_3$ epitaxial layers on sapphire substrates exhibit a drain current density of 77.7 mA/mm with a peak trans-conductance of 2.28 mS/mm for D-mode operation and 27.3 mA/mm drain current density with a peak trans-conductance of 3.92 mS/mm for E-mode operation. In contrast, MOSFET devices based on$\beta - Ga_2O_3$ epitaxial layers on $\beta - Ga_2O_3$ substrates show a drain current density of 64.1 mA/mm for D-mode operation and 22.2 mA/mm drain current density with 3.2 mS/mm peak trans-conductance for E-mode operation. MOSFET devices based on $\beta - Ga_2O_3$ epitaxial structures on sapphire and on $\beta - Ga_2O_3$ substrates show reliable switching properties with sub-threshold swing of 95.98 mV/dec and 87.05 mV/dec respectively as well as a high I_{on}/I_{off} ratio of 10^{11}. These simulation results show potential of laterally scaled $\beta - Ga_2O_3$ MOSFETs for power switching applications.

Keywords $\beta - Ga_2O_3$ · Recessed gate · Depletion mode · Enhancement-mode

Pharyanshu Kachhawa, Nidhi Chaturvedi
CSIR-Central Electronics Engineering Research Institute, Pilani, India

Academy of Scientific and Innovative Research (AcSIR), Ghaziabad, India
E-mail: pharyanshu@ceeri.res.in, nidhi@ceeri.res.in

1 Introduction

β-gallium oxide ($\beta - Ga_2O_3$) is emerging as new generation power semiconductor material because of its material properties such as an ultra-wide band gap of 4.8 eV and the resulting large critical breakdown field (E_c) of 8 MV/cm. These factors lead to high Figures of Merit such as Baliga's FOM (3214) and Johnson's FOM (2844), which are much larger than those of existing wide band-gap semiconductors like SiC and GaN. This enables $\beta - Ga_2O_3$ to be a potential candidate for the realization of high voltage, low-loss power switching devices for power electronics [1][2]. The proposed high electric field strength of $\beta - Ga_2O_3$ thus outperforms GaN and SiC. In addition, the possibility of bulk growth of large and uniform $\beta - Ga_2O_3$ crystals using conventional melt growth processes enables cheap production [2]. Availability of shallow donors for $\beta - Ga_2O_3$ like Si, Ge and Sn allows n-type doping with a wide range of doping concentrations from 10^{15} to $10^{20} cm^{-3}$ [3]. As p-type conductivity is absent in $\beta - Ga_2O_3$ due to the deep acceptor level of the dopants and the large hole mass all devices reported so far are unipolar devices [3][2]. After the demonstration of first MESFET/MOSFET by the Higashiwaki group from NICT, Japan $\beta - Ga_2O_3$-based devices got a significant R&D interest. Various depletion mode (D-mode) devices were explored with doping concentrations up to $10^{16} - 10^{19} cm^{-3}$ (n-type doped) which gives drain current densities up to 200 mA/mm [4]. The voltage limitations also have been explored showing high breakdown voltages up to 1-2.3 kV [5][6][7]. The devices usually have a negative threshold voltage. However, this introduces more circuit complexity if transistors are operating in a power switching system and is not generally preferable.

Enhancement mode (E-mode) devices are preferred over depletion mode devices in power electronics applications because of their fail-safe operation and the reduced system complexity. In this paper, simulations for enhancement mode $\beta - Ga_2O_3$ based MOSFETs are demonstrated and compared to D-mode device simulations. Various techniques can be applied to achieve E-mode in $\beta - Ga_2O_3$-based devices such as gate recess structure, thin channel layers so that the channel can be depleted easily by interface states and by incorporating unintentionally doped layer as channel layer in between channel layer and substrate [8][9][10][11][12]. Lateral $\beta - Ga_2O_3$ MOSFETs were also demonstrated for power electronics applications with advanced T-gate topology and nitrogen ion-implantation which shows a high-power figure of merit of 155 MW/cm^2 and breakdown voltage of 1.8 kV [**?**]. Recessed gate E-mode $\beta - Ga_2O_3$ structures demonstrated to achieve good power FOMs for DC conduction switching applications. These devices can provide advantages in various applications such as high-speed switching device, high voltage device operations and many others. In this paper, we demonstrate a laterally scaled recessed gate structure with a 1µm n-type doped (Si) epitaxial layer on 350 μm sapphire and $\beta - Ga_2O_3$ substrates, respectively. We have optimized the gate recess thickness for this epilayer structures to achieve both depletion mode and enhancement mode $\beta - Ga_2O_3$ based FETs. Device physics, struc-

tural simulation parameters and results for these structures are discussed in next section.

2 Device Structure and Simulation

All the simulations are performed using the commercially available TCAD software SILVACO ATLAS. The schematic of the device is shown below in Figure **??**.

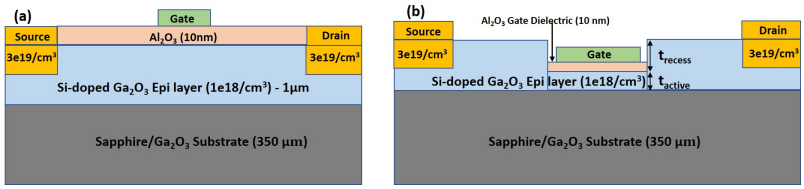


Fig. 1 Schematic of simulated device (a) without recess (b) and with recessed gate structure

A highly doped $n^{++}\beta - Ga_2O_3$ region with concentration of $3 \times 10^{19} cm^{-3}$ is created under source and drain contact regions for low contact resistance. A thin layer of Al_2O_3 with thickness of 10 nm is considered as gate dielectric. The structure is simulated with 20 μm source to drain distance (L_{sd}), gate length of 2 μm and a gate width of 100 μm. The ungated $\beta - Ga_2O_3$ channel regions are kept at a thickness of 1 μm to get best results out of it. The simulation parameters used are taken from an existing model [13][14][15] and some additional parameters are shown in Table 1. For high field saturation, field dependent mobility model FLDMOB is used for which electron saturation velocity is considered as 2.5×10^7 cm/s [2].

Table 1 $\beta - Ga_2O_3$- Parameters

Parameters	Gallium Oxide	Units
Band Gap	4.85	eV
Dielectric Constant	10	N/A
Saturation velocity	2.5×10^7	cm/sec
Electron Mass	0.28	N/A
Electron Mobility	300	cm^2/V.sec
Electron Affinity	4.0	eV

Self-heating effects are considered by incorporating lattice thermal models and solving heat flow equations. The built-in impact ionization model is also included to analyze impact ionization in the structure hence breakdown voltage is calculated. The ionization coefficient α based on Cheynoweth model is given by

$$\alpha(F) = -a.e^{\frac{-b}{F}} \quad (1)$$

Table 2 Simulated output parameters for different active channel thicknesses

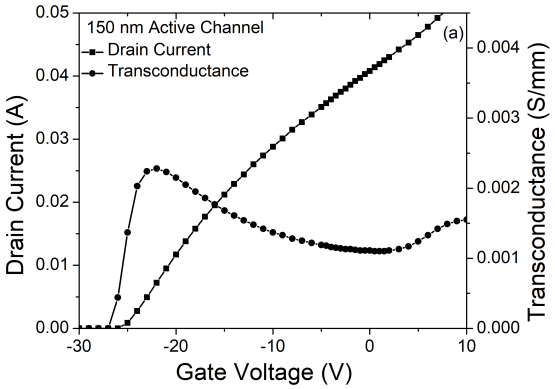
Recess Thickness	Active channel thickness	Threshold Voltage (V)	Max. Drain Current (mA/mm)	Transconductance (mS/mm)
985 nm	15 nm	1.05	27.3	3.92
950 nm	50 nm	-2.8	59.0	4.0
900 nm	100 nm	-11.2	70.4	2.74
850 nm	150 nm	-25.4	77.7	2.28

Where, a= 7.9×10^5 /cm and b= 2.92×10^7 V/cm [16]. These exact values are considered in the simulations without any modifications.

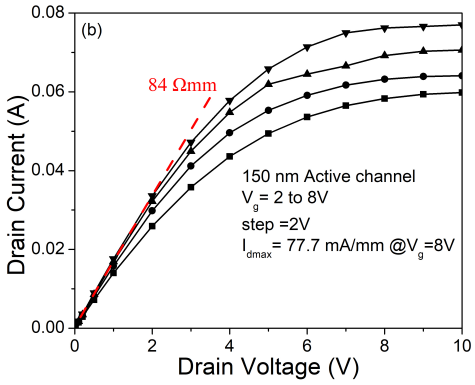
3 Results and Discussions

The above stated parameters are used for TCAD based 2-D simulations to analyze the performance of $\beta - Ga_2O_3$-based epi-layer structure. The structure is simulated to get output and transfer characteristics with high trans-conductance on this epitaxial structure (as shown in Figure 1(a)). The thick epilayer shows a large negative threshold voltage and very low trans-conductance. As we know that a decrement of channel thickness will improve trans-conductance of the device we decided to use gate recess technique to improve performance. A $\beta - Ga_2O_3$ recessed gate structure (Figure 1(b)) is simulated to check the transistor characteristics. The structure is gate recessed up to 850 nm thickness to get 150 nm active channel thickness which is used to deplete the channel. Transfer and output characteristics of $\beta - Ga_2O_3$ epilayer on sapphire substrate are simulated and shown in Figure 2.

$\beta - Ga_2O_3$ MOSFET with 150 nm active channel thickness (after gate recess) is simulated at a drain voltage V_{ds} of 25V to get depletion mode characteristic with a threshold voltage of -25.3 V and a drain current of 0.1 mA/mm. The depletion mode device shows a peak trans-conductance of 2.28 mS/mm and maximum drain current density of 77.7 mA/mm at VG=8 V. We decided to further reduce the channel thickness and we increased the recess thickness and reaches 15 nm of active channel thickness to get enhancement mode characteristics. This structure with 15 nm active channel layer shows an enhancement mode operation with a threshold voltage of +1.05 V at a drain current of 0.1 mA/mm. Simulation with E-mode operation shows a trans-conductance of 3.92 mS/mm and maximum drain current density of 27.3 mA/mm at Vg=8 V as shown in Figure 3. Further, we simulated the gallium oxide structure for a span of different recess thicknesses. Table 2 shows various calculated parameters for the span of different active channel thickness (Recess thickness from 850 nm to 985 nm). The active channel thickness for the structure is down-scaled from 150 nm to 15 nm and the respective characteristics and parameters are shown in Figure 4, Figure 5 and table 2.



(a) Transfer and trans-conductance Characteristics



(b) Drain Characteristics

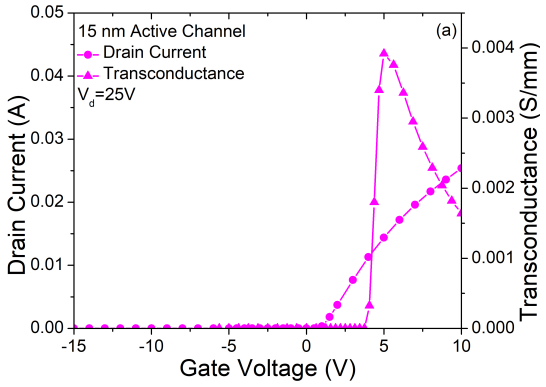
Fig. 2 Transfer, trans-conductance characteristics and output characteristics for 150 nm active channel thickness (D-mode operation)

The depletion and enhancement mode parameters are achieved with practically feasible threshold and on-resistance values [5] [12]. The structure shows a decreasing drain current trend with reducing active channel layer. This reduced drain current trend at constant gate voltage can be co-related with the R_{SD} drop voltage across the channel. As the relation is given by [17]

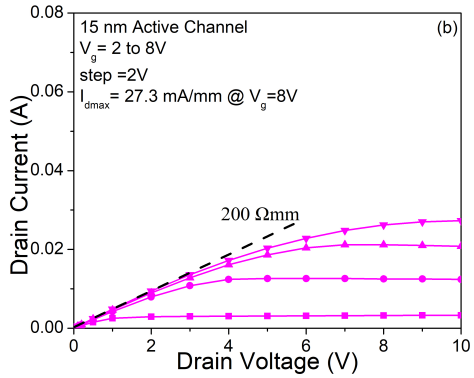
$$\Delta V_{D,Sat} = \tilde{}\Delta(R_{SD} I_{DS,Sat}) \tag{2}$$

The R_{SD} is inversely proportional to the thickness of the channel hence the drain current can be co-related as a function of the channel thickness as follows:

$$I_{DS,Sat}(V_{GS} = 8V) = \tilde{}I_0(V_{GS} = 8V).e^t \tag{3}$$



(a) Transfer and trans-conductance Characteristics



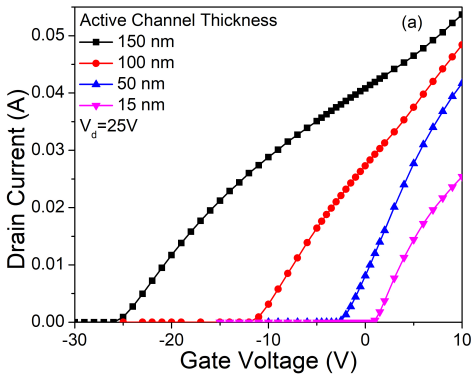
(b) Drain Characteristics

Fig. 3 Transfer, trans-conductance characteristics and output characteristics for 15 nm active channel thickness (E-mode operation)

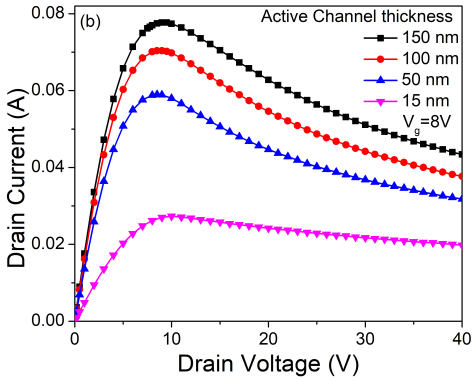
Where, t is the thickness of the channel. This relation interprets the output drain current variation with active channel thickness.

3.1 Comparison of gallium oxide epitaxy on different substrates

In previous section, we have optimized the gate recess thickness to achieve both depletion and enhancement mode operation. In this section we have performed a simulation comparison of $\beta - Ga_2O_3$ epilayer on sapphire substrate and $\beta - Ga_2O_3$ epilayer on $\beta - Ga_2O_3$ substrate. The simulations are carried out to see the performance of both type of structures based on their characteristics. Although, the $\beta - Ga_2O_3$ epilayer on sapphire substrate will



(a) Transfer Characteristics



(b) Drain Characteristics

Fig. 4 Transfer and output characteristics for different active channel thickness

always provide inferior crystal quality (in terms of defect density) compared to $\beta - Ga_2O_3$ on $\beta - Ga_2O_3$ substrate structure we have performed simulations to see the thermal influence of the different substrates in perspective of the low thermal conductivity issue of $\beta - Ga_2O_3$ (10-25 W/m.K) compared to sapphire (40 W/m.K). The simulation bases on a substrate thickness of 350 μm for a realistic observation of self-heating. The active channel thickness is fixed to 15 nm (985 nm gate recess) for both structures. For simulation it is assumed that carrier transport is confined to channel and heat elements are places at contact pads and substrate which acts as heat sinks to define the thermal effects within the structure. In the simulator heat source is defined at gate edge near the drain and to detect thermal effects. The simulated structure comprises of 1 μm gallium oxide epilayer with an n-type Si doping of 1×10^{18}

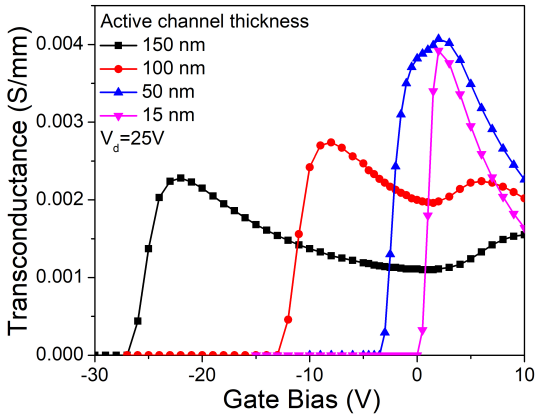


Fig. 5 Trans-conductance characteristics for different active channel thicknesses

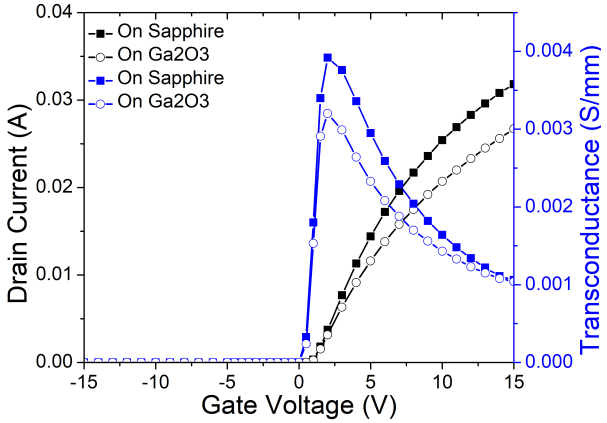


Fig. 6 Comparison of different $\beta - Ga_2O_3$ epitaxial structures (E-mode)

doping concentration on sapphire and gallium oxide substrates. Device parameters dimensions of L_{sd}=20 μm, L_g=2 μm are taken by keeping in mind the limitation of the contact lithography. A coupled electro-thermal simulation models are used to get transfer and trans-conductance characteristics for both structures (shown in Figure 6).

A threshold voltage of +1.02 V with a peak trans-conductance of 3.2 mS/mm is observed for $\beta - Ga_2O_3$ epilayer on $\beta - Ga_2O_3$ substrate structure. Whereas the $\beta - Ga_2O_3$ epilayer on sapphire substrate shows a threshold voltage of +1.05 V with a peak trans-conductance 3.92 mS/mm. Output characteristics for both structures for depletion and enhancement mode are also

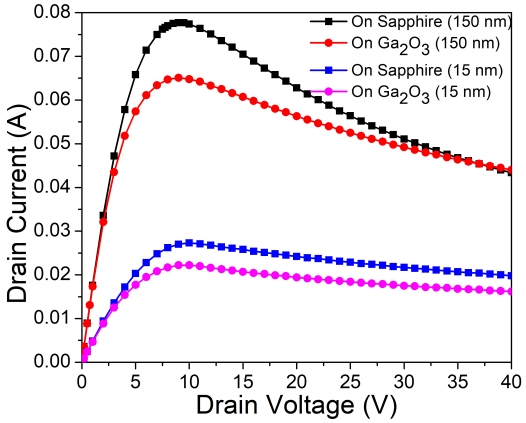


Fig. 7 Drain characteristics with self-heating effects for different epitaxial structures

plotted and shown in Figure 7. Maximum drain current of 27.3 mA/mm and 22.2 mA/mm at Vg=8 V is extracted for $\beta - Ga_2O_3$ on sapphire substrate and gallium oxide on gallium oxide substrate structures respectively for enhancement mode operation. Similarly, for depletion mode operation a maximum drain current of 77.7 mA/mm and 64.1 mA/mm at Vg=8 V is extracted for $\beta - Ga_2O_3$ on sapphire substrate and $\beta - Ga_2O_3$ on $\beta - Ga_2O_3$ substrate structures respectively. The $\beta - Ga_2O_3$ on $\beta - Ga_2O_3$ structure shows reduced current comparative to $\beta - Ga_2O_3$ on sapphire substrate due to the reduced thermal conductivity of the $\beta - Ga_2O_3$ substrate. Therefore, assuming the same power dissipation in the channel, the $\beta - Ga_2O_3$ on $\beta - Ga_2O_3$ substrate devices get hotter.

The reduction in the drain current at high drain voltages can be interpreted by the following self-heating model [18]. The epilayer thickness at gate area is too thin to be neglected. Hence, the thermal impedance for the structure can be given by

$$R_{Th} = \frac{1}{\pi k} \ln \frac{8 t_{sub}}{\pi L_g} \tag{4}$$

Where, k is the thermal conductivity of the substrate, tsub is the thicskness of the substrate and Lg is the gate length. As per the drift-diffusion and heat flow equation taking experimental temperature dependent thermal conductivity for both gallium oxide [19] and sapphire [20] is given by:

$$k_{GalliumOxide}(T) = 0.234 \frac{T}{300}^{-1.27} [W/cm.K] \tag{5}$$

$$k_{Sapphire}(T) = 0.49 \frac{T}{300}^{-1} [W/cm.K] \tag{6}$$

Where, T is the position-dependent absolute temperature in $\beta - Ga_2O_3$ and the approximate T^{-1} relationship is characteristic of phonon-dominated thermal transport. From the above equations thermal resistance and the thermal conductivity can be correlated. The thermal resistance is inversely proportional to the thermal conductivity of the material. As, $\beta - Ga_2O_3$ has lower thermal conductivity compared to sapphire a higher thermal resistance has to be expected. which is responsible for the reduced output drain current. Output characteristics for these structure shows a Ron of 206 ω.mm and 215 ω.mm at lower drain voltage (Vd) for $\beta - Ga_2O_3$ on sapphire substrate and $\beta - Ga_2O_3$ on $\beta - Ga_2O_3$ substrate structure respectively. $\beta - Ga_2O_3$ on sapphire structure shows less Ron as compared to fabricated structure [12] which has a Ron of 215 ω.mm. The simulated structure shows a good sub-threshold swing of 95.95 mV/dec and 87.05 mV/dec for $\beta - Ga_2O_3$ epilayer on sapphire substrate and $\beta - Ga_2O_3$ epilayer on $\beta - Ga_2O_3$ substrate respectively.We defined substrate properties ($\beta - Ga_2O_3$ and sapphire) in the simulator to simulate two different structures. For both the structure all these scaled $\beta - Ga_2O_3$ MOSFETs simulations shows a very high I_{on}/I_{off} ratio of 10^{11} leads to high performance, fast switching, low leakage and increased gate control over device.

In order to check the high voltage performance of these recessed-gate structures, we set gate voltage near pinch off (V_g=0V in this case) value and keep on increasing the drain voltage. $\beta - Ga_2O_3$ on $\beta - Ga_2O_3$ structure and $\beta - Ga_2O_3$ on sapphire structure shows a minor difference in the breakdown voltage. In case of $\beta - Ga_2O_3$ on $\beta - Ga_2O_3$ structure it is 462 V and for $\beta - Ga_2O_3$ on sapphire structure it is 473 V. The minor change/increment in breakdown voltage may be due to the high thermal conductivity of the sapphire substrate. The simulated device structure characteristics shows comparable results with compared to the fabricated data reported by Chabak et al. [12].

4 Conclusion

In this paper, TCAD simulation using Silvaco ATLAS 2D is performed for recessed gate $\beta - Ga_2O_3$ MOSFET structure. In the simulated structure, recessed gate thickness has been varied to get for depletion and enhancement mode operation of the $\beta - Ga_2O_3$ MOSFET. The depletion mode characteristics has been optimized with 150 nm active channel thickness (gate recess thickness of 850 nm). We further recessed it for 15 nm active channel thickness to get enhancement mode characteristics for the $\beta - Ga_2O_3$ MOSFETs. For better understanding of gate recess thickness variations, simulations have been carried out for a span of recess thickness varying from 850 nm to 985 nm. For comparison the thermal and electrical effects caused by $\beta - Ga_2O_3$ epilayers on $\beta - Ga_2O_3$ substrate and sapphire substrate have been compared to each other. For the same parameters the $\beta - Ga_2O_3$ on sapphire substrate structure shows an increment of 21.2% in drain current for the depletion type operation. $\beta - Ga_2O_3$ epilayer on sapphire substrate shows a drain current density of 77.7 mA/mm with peak trans-conductance of 2.28 mS/mm for D-mode operation

and 27.3 mA/mm drain current density with a peak trans-conductance of 3.92 mS/mm for E-mode operation. In contrast, $\beta - Ga_2O_3$ epilayer on $\beta - Ga_2O_3$ substrate shows a drain current density of 64.1 mA/mm for D-mode operation and 22.2 mA/mm drain current density with 3.2 mS/mm peak trans-conductance for E-mode operation with an I_{on}/I_{off} ratio of 10^{11}. Further improvement in breakdown voltage and performance can be achieved with incorporation of field plate structure and gate dielectric engineering. These simulations illustrate the advantages of scaled $\beta - Ga_2O_3$ MOSFETs towards low loss high voltage switching power electronics applications.

Acknowledgements The authors gratefully acknowledge the financial support of CSIR mission mode project budget head: HCP-0012. Authors acknowledge Dr.-Ing. Joachim Wuerfl, Mr. Shivanshu Mishra and Mr. Amber Kumar Jain for their valuable suggestions and discussion.

References

1. Higashiwaki, Masataka, et al. "Gallium oxide (Ga2O3) metal-semiconductor field-effect transistors on single-crystal β-Ga2O3 (010) substrates." Applied Physics Letters 100.1 (2012): 013504.
2. Pearton, S. J., et al. "A review of Ga2O3 materials, processing, and devices." Applied Physics Reviews 5.1 (2018): 011301.
3. Higashiwaki, Masataka, and Gregg H. Jessen. "Guest Editorial: The dawn of gallium oxide microelectronics." (2018): 060401.
4. Joishi, Chandan, et al. "Deep-Recessed β-Ga2O3 Delta-Doped Field-Effect Transistors With In Situ Epitaxial Passivation." IEEE Transactions on Electron Devices 67.11 (2020): 4813-4819.
5. K. Tetzner et al., "Lateral 1.8 kV β -Ga2O3 MOSFET with 155 MW/cm2 Power Figure of Merit," in IEEE Electron Device Letters, vol. 40, no. 9, pp. 1503-1506, Sept. 2019, doi: 10.1109/LED.2019.2930189.
6. Mun, Jae Kyoung, et al. "2.32 kV breakdown voltage lateral β-Ga2O3 MOSFETs with source-connected field plate." ECS Journal of Solid-State Science and Technology 8.7 (2019): Q3079.
7. Chabak, Kelson D., et al. "Lateral β-Ga2O3 field effect transistors." Semiconductor Science and Technology 35.1 (2019): 013002.
8. Chabak, K.D., McCandless, J.P., Moser, N.A., Green, A.J., Mahalingam, K., Crespo, A., et al.: 'Recessed-gate enhancement-mode β-ga2o3 mosfets', IEEE Electron device letters, 2017, 39, (1), pp.67–70.
9. Bhuiyan, M.A., Zhou, H., Jiang, R., Zhang, E.X., Fleetwood, D.M., Peide, D.Y., et al.: 'Charge trapping in Al2O3/ β-ga2o3-based mos capacitors', IEEE Electron Device Letters, 2018, 39, (7), pp. 1022–1025.
10. Zhou, H., Si, M., Alghamdi, S., Qiu, G., Yang, L., Peide, D.Y.: 'High performance depletion/enhancement-ode β-ga2o3 on insulator (gooi) field-effect transistors with record drain currents of 600/450 mA/mm, IEEE Electron Device Letters, 2016, 38, (1), pp. 103–106.
11. Wong, M.H., Nakata, Y., Kuramata, A., Yamakoshi, S., Higashiwaki, M.: 'Enhancement-mode ga2o3 mosfets with si-ion-implanted source and drain', Applied Physics Express, 2017, 10, (4), pp. 041101.
12. Chabak, Kelson D., et al. "Recessed-Gate Enhancement-Mode β-Ga2O3 MOSFETs." IEEE Electron device letters 39.1 (2017): 67-70.
13. Chabak, K.D., Moser, N., Green, A.J., Walker.Jr, D.E., Tetlak, S.E., Heller, E., et al.: 'Enhancement-mode ga2o3 wrap-gate fin field-effect transistors on native (100) β-ga2o3 substrate with high breakdown voltage', Applied Physics Letters, 2016, 109, (21), pp. 213501.

14. Higashiwaki, Masataka, et al. "Vertical Gallium Oxide Transistors with Current Aperture Formed Using Nitrogen-Ion Implantation Process." 2020 4th IEEE Electron Devices Technology and Manufacturing Conference (EDTM). IEEE, 2020.
15. SILVACO, A.: 'Atlas simulation of a wide bandgap ga2o3 mosfet', The Simulation Standard, 2013, 23, (4), pp. 7–9.
16. Ghosh, K., Singisetti, U.: 'Impact ionization in β-ga2o3', Journal of Applied Physics, 2018, 124, (8), pp. 085707.
17. Karsenty, A., and A. Chelly. "Modeling of the channel thickness influence on electrical characteristics and series resistance in gate-recessed nanoscale SOI MOSFETs." Active and Passive Electronic Components 2013 (2013).
18. Gaska R, Chen Q, Yang J, Osinsky A, Khan MA, Shur MS. High-temperature performance of AlGaN/GaN HFET's on SiC substrates. IEEE Electron Dev Lett 1997;18:492–4.
19. Z. Guo, A. Verma, X. Wu, F. Sun, A. Hickman, T. Masui, A. Kuramata, M. Higashiwaki, D. Jena, and T. Luo, Appl. Phys. Lett. 106, 111909 (2015).
20. Freeman JC. Channel temperature model for microwave AlGaN/GaN power HEMTs on SiC and Sapphire. IEEE MTT-S Dig 2004:2031–4.

Figures

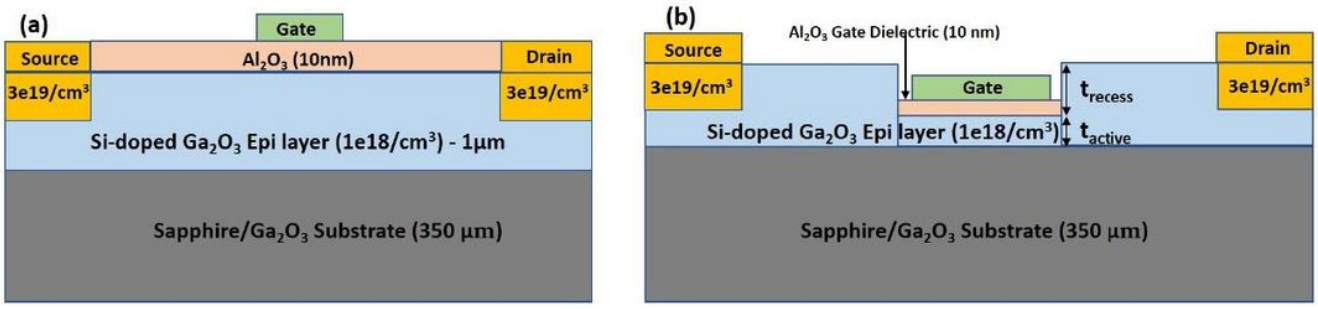
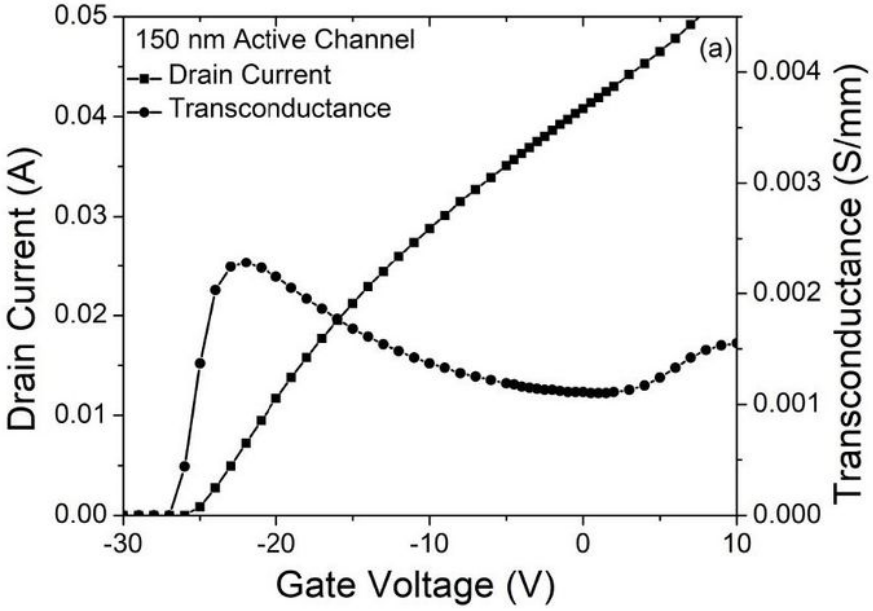
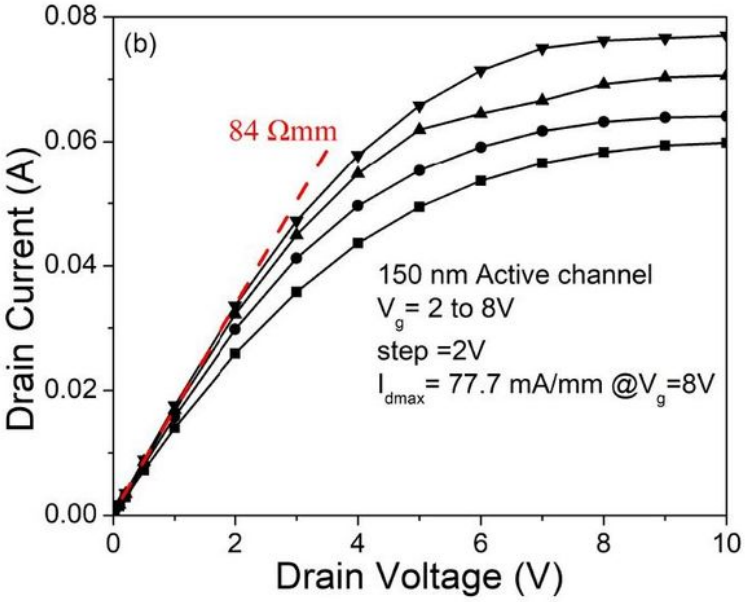


Figure 1

Schematic of simulated device (a) without recess (b) and with recessed gate structure



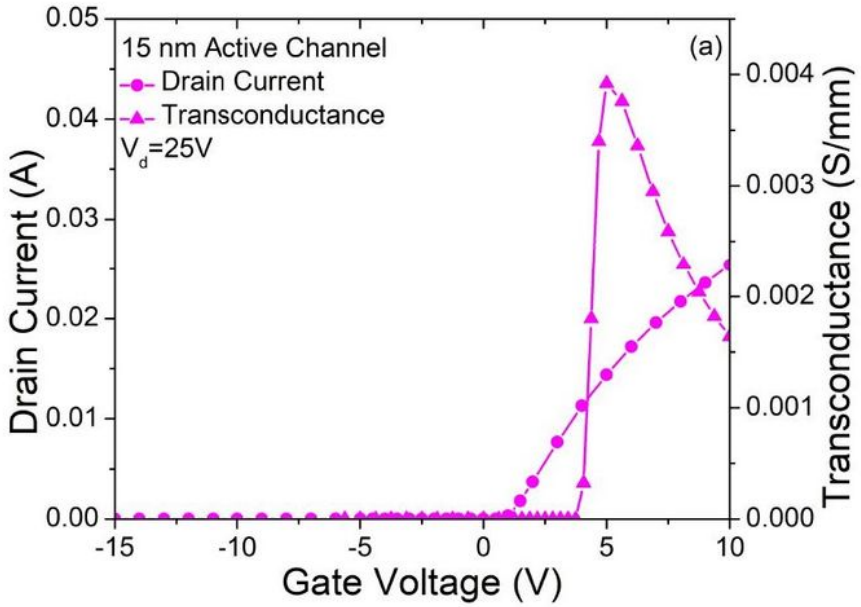
(a) Transfer and trans-conductance Characteristics



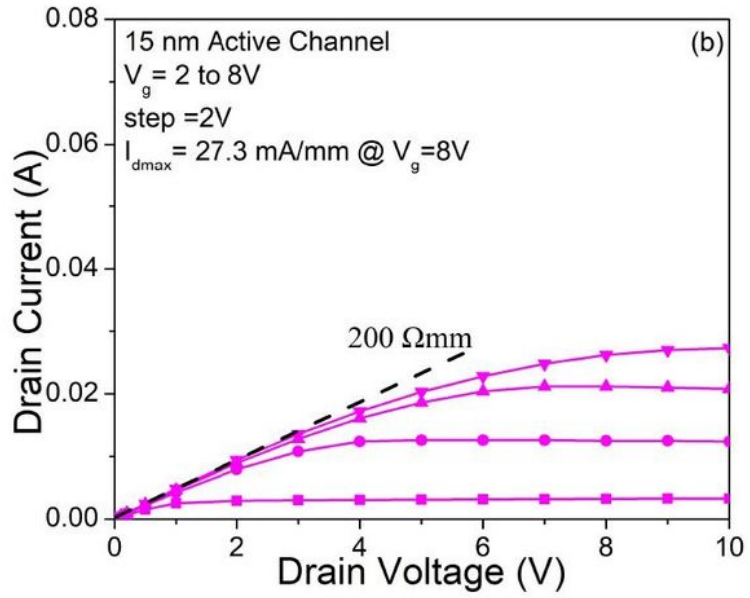
(b) Drain Characteristics

Figure 2

Transfer, trans-conductance characteristics and output characteristics for 150 nm active channel thickness (D-mode operation)



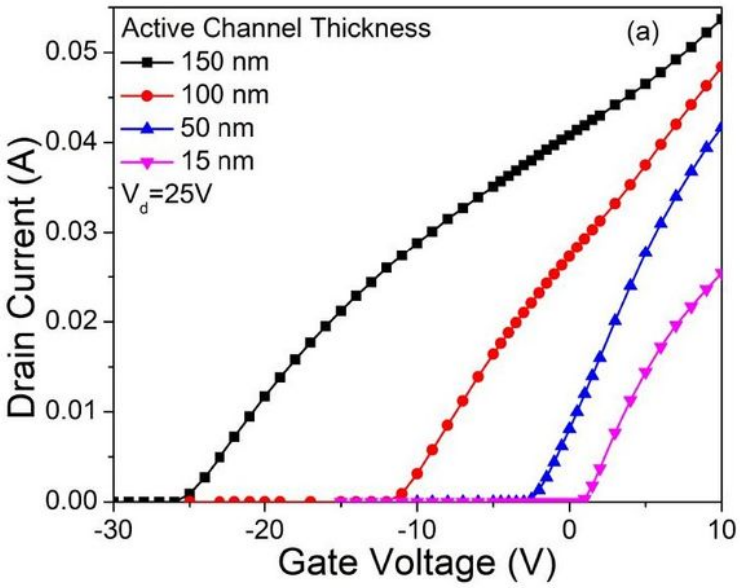
(a) Transfer and trans-conductance Characteristics



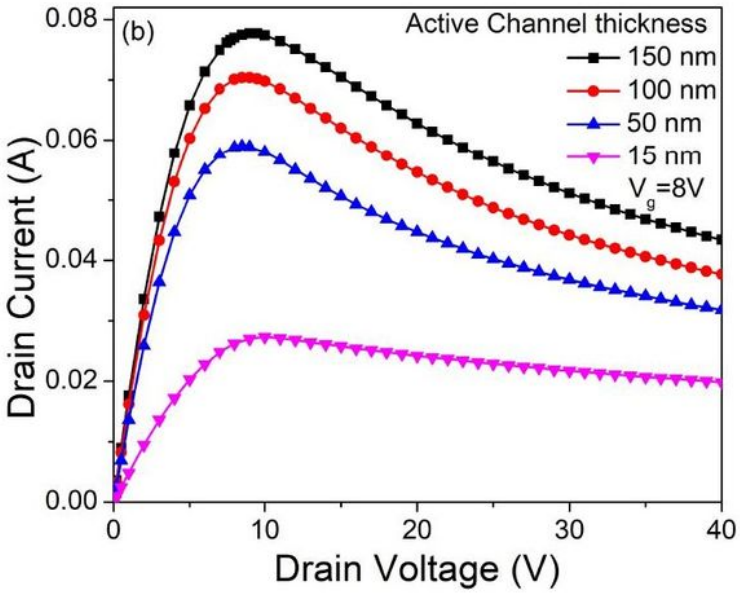
(b) Drain Characteristics

Figure 3

Transfer, trans-conductance characteristics and output characteristics for 15 nm active channel thickness (E-mode operation)



(a) Transfer Characteristics



(b) Drain Characteristics

Figure 4

Transfer and output characteristics for different active channel thickness

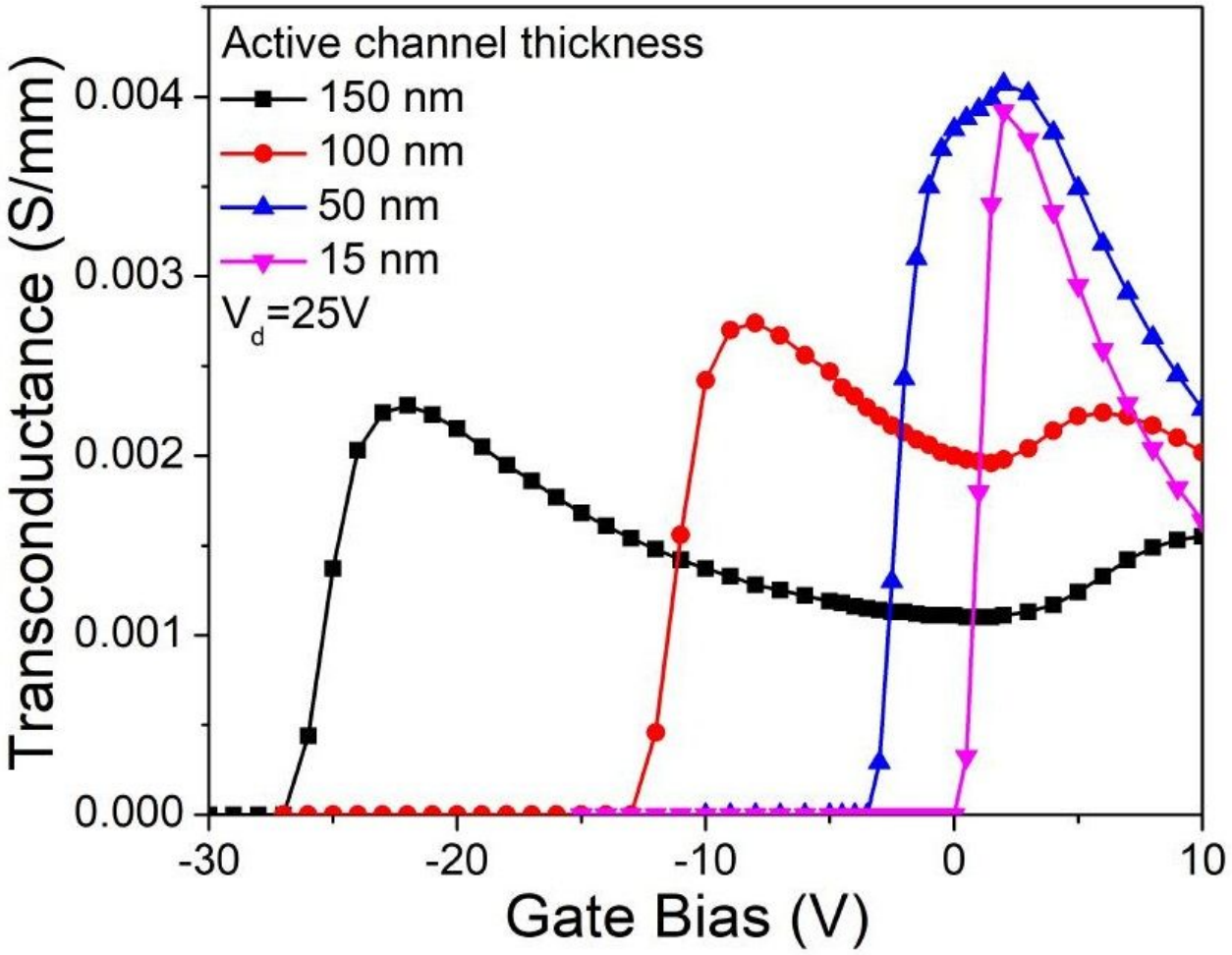


Figure 5

Trans-conductance characteristics for different active channel thicknesse

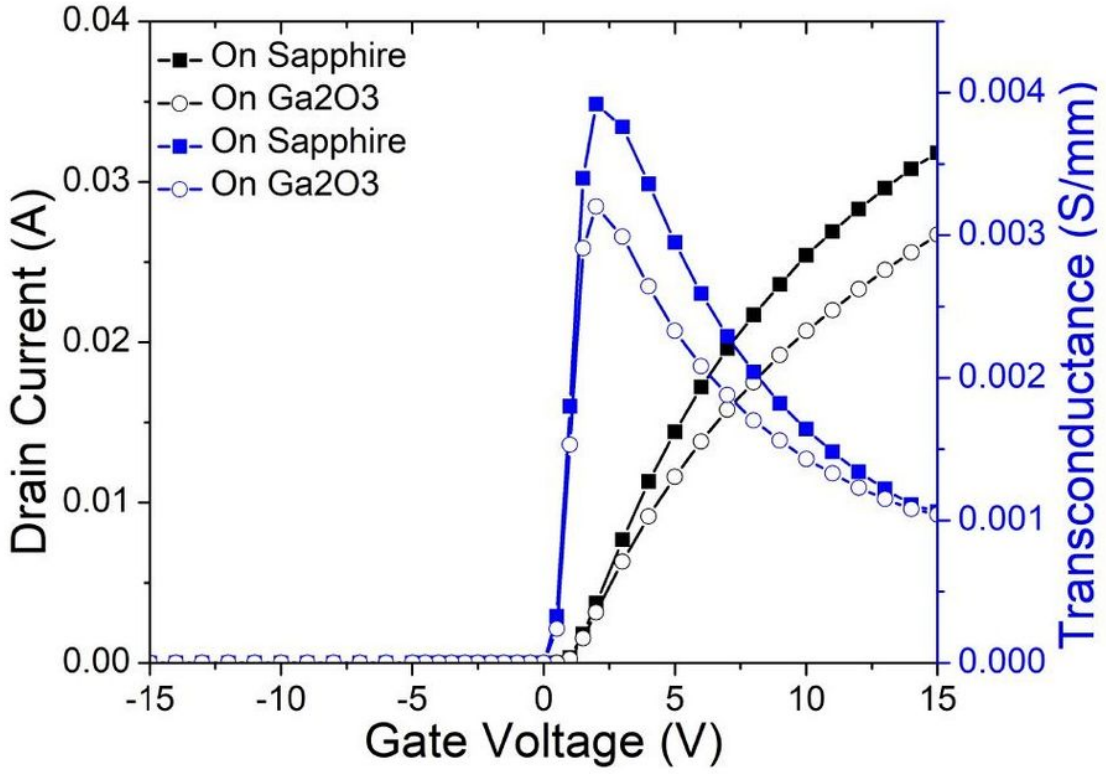


Figure 6

Comparison of different β − Ga2O3 epitaxial structures (E-mode)

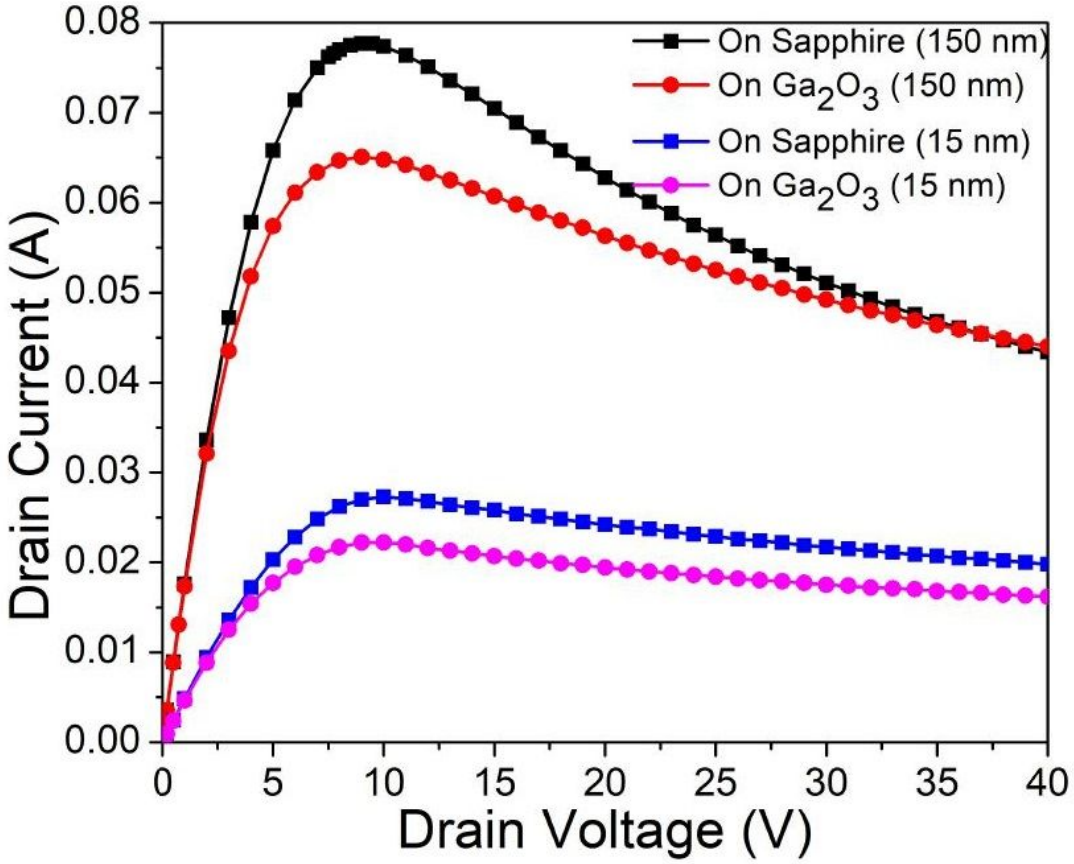


Figure 7

Drain characteristics with self-heating effects for different epitaxial structures