

Splay Tree Hybridized Multicriteria ant Colony and Bregman Divergencive Firefly Optimized Vlsi Floorplanning

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SPLAY TREE HYBRIDIZED MULTICRITERIA ANT COLONY AND BREGMAN DIVERGENCIVE FIREFLY OPTIMIZED VLSI FLOORPLANNING

Abstract

Floorplanning is a basic designing step in VLSI circuit to estimate chip area before the optimized placement of digital blocks and their connections. The process of Floorplanning involves identifying the locations, shape, and size of components in a chip. The floorplanning is a hard problem since the consumption of energy and heat generation was high for the placement of modules. In order to improve the optimized floor planning, a novel Splay tree Hybridized Multicriteria Ant Colony and Bregman Divergencive Firefly Optimized Floor Planning (STHMAC-BDFOFP) technique is proposed. Main objective of STHMAC-BDFOFP technique is to efficient floor planning with minimum time. Initially, a number of modules are given with their connections obtained from benchmark dataset. In STHMAC-BDFOFP, a Splay tree-based non-slicing floor planning model constructing trees via modeling geometric relationship among modules. A splay tree is build after performing different operations namely splaying, join, split, insertion, and deletion on modules for floor planning. The constructed floorplan design is optimized by Hybridized Multicriteria Ant Colony and Bregman Divergencive Firefly algorithm. At first, the ant colony optimization is applied for finding the local optimum solution from the population of modules in the Splay tree with Multicriteria functions namely energy consumption, heat generation, space occupied, and wire length. Depends on fitness measure, the local optimum solution is determined. Then the global solution is attained by applying the Bregman Divergencive Firefly ranked algorithm. In this way, optimum modules in the splay tree are identified and obtain efficient floorplanning in VLSI design. Discussed results indicate that STHMAC-BDFOFP technique improves the performance of energy and heat aware floor planning as compared to conventional works.

Keywords: VLSI floorplanning, Splay tree-based non-slicing floor planning model, Hybridized Multicriteria Ant Colony, and Bregman Divergencive Firefly ranked optimization

1. Introduction

VLSI is the procedure for manufacturing numbers of transistors into single chip or Integrated Circuit. Physical VLSI design process discovers the physical position of active devices and interconnections among them within boundary of integrated circuit in which floorplanning is essential one. The floor planning is organizing a group of modules in rectangular chip region thus, the performance of wirelength, heat generation, space consumption are optimized. Resulting layout is called as a floorplan. The floorplanning problem has been proved by applying different evolutionary and optimization algorithms to lessen area and wirelength.

A 'Lion Optimization Algorithm (LOA) floorplanner was introduced in [1] for minimization of wirelength and area. However, the designed floorplanner failed to consider the heat and energy-aware floorplanning. In [2], a novel Interactive Self-Improvement based Adaptive Particle Swarm Optimization (ISI-APSO) was presented to offer better efficiency of floorplanning by considering wirelength and area. However, the temperature generation and space consumption were not reduced considerably.

A generic solution was presented in [3] to solve the problem of the rectangular floorplane. But it failed to cover other aspects such as the style, functionality, contextual constraints during the floorplanning process. A multi-objective design space exploration framework was developed in [4] for large-scale on-chip power grid VLSI designs. However, the designed framework was not efficient to provide the optimized VLSI design with lesser time consumption.

A Diffusion Oriented Time-improved Floorplanner was developed in [5] to optimize the temperature, chip area as well as wire length. However, the energy-aware floor planning remained unsolved. A hybrid genetic paired mutation algorithm was designed in [6] for Very-large-scale integration (VLSI) placement optimization. The designed algorithm reduces the time complexity but it failed to solve the multiobjective constraints for efficient placement optimization.

Lion's pride inspired algorithm was designed in [7] to solve multi-objective VLSI floor planning to optimize the area minimization. However, the energy and heat aware optimization was not solved. Multi-Objective Bat Algorithm (MOBA) was designed in [8]. Designed algorithm reduces the wirelength and dead space but the other objectives such as heat generation, energy-based floorplanning were not considered.

In [9], A Self-Adaptive Particle Swarm Optimization (SA-PSO) was designed for VLSI design. But the VLSI design failed to extend other objectives namely chip area, size, critical path delay, and wirelength. A modified adaptive symbiosis based algorithm was presented in [10] to resolve multiobjective optimization issue of VLSI floorplanning. But it has more time complexity.

For efficient floorplans with lesser peak temperature, a genetic search algorithm and modified simulated annealing search algorithm were designed in [11]. A Genetic algorithmic program (GA) with harmony search algorithm was presented in [12] to lessen space and wire length. But time complexity of floorplanning was not minimized.

Different heuristic and meta-heuristic algorithms were developed in [13] for a multi-objective VLSI Floorplan. But the tree-based floor planning was not performed to reduce the complexity involved in the floor planning. A conjugate gradient scheme was developed in [14] to efficiently use the thermal resistance model for floorplanning. But the variety of objective functions is not optimized to improve the floorplan efficiency.

A temperature-aware floorplanning algorithm was designed in [15] depends on simulated annealing for efficiently minimize the chip peak temperature and reasonable area, wirelength, and time overhead. But the efficient heat generation minimization was not achieved. For fixed-outline 3D floorplanning, a fast thermal analysis technique was designed in [16]. However, the optimization technique was not applied for efficient floorplanning. A flow-based partitioning method was developed in [17] to reduce the wirelength penalty and area cost. However, the designed method failed to consider the heat, and energy-aware floor planning was not performed.

A communication-centric floorplanning algorithm was developed in [18] using Simulated Annealing for floor plan for minimizing the area of the entire floorplan. However, time consumption was not reduced. A flow-based partitioning algorithm was designed in [19] to reduce the wirelength. An improved multi-objective optimization technique using learning automata was developed in [20] based on the design of a variety of functional circuits.

1.1. Our contribution

Motivated by the above argument, in this paper a novel STHMAC-BDFOFP technique is introduced for fixed-outline floorplanning. Some key technical contributions of this STHMAC-BDFOFP are listed as follows,

- To obtain efficient heat and energy-aware floorplanning in VLSI design, the STHMAC-BDFOFP technique is introduced. This contribution is achieved through the splay tree and Hybridized Multicriteria Ant Colony and Bregman Divergencive Firefly algorithm.
- To minimize the computation time of floorplanning, a splay tree-based non-slicing model is introduced. The splay tree is constructed through modeling the geometric relationship between the modules taken from the benchmark dataset. As a result, the modules are arranged in the tree.
- To obtain the optimal floorplanning in VLSI, Hybridized Multicriteria Ant Colony and Bregman Divergencive Firefly algorithm is introduced. Initially, modules in splay tree are initialized as population to find local best optimum through the fitness measure with multicriteria function namely energy consumption, heat generation, space occupied, and wire length. Then the global solution is obtained by applying the Bregman Divergencive ranked Firefly algorithm. This helps to obtain the energy and heat optimized floor planning in VLSI design. Besides, the wire length and space occupied results also gets reduced.

- Finally, extensive simulations are conducted using a benchmark dataset to evaluate the performance of our STHMAC-BDFOFP technique and other related works. The obtained result demonstrates that our STHMAC-BDFOFP technique is highly efficient than the other methods.

1.2 Paper outline

The rest of article is ordered as follows. Section 2 describes STHMAC-BDFOFP technique for solving the multicriteria floorplanning problem. Experimental evaluation of STHMAC-BDFOFP is presented in sections 3 with benchmark dataset. The simulation results are offered in Section 4. Section 5 concludes the article.

2. Proposal methodology

Floorplanning is the basic process of physical design in the VLSI domain. The floor planning is employed to estimate the relative position of blocks inside the fixed outline. The planning is to optimize the Wirelength and area occupied by the circuit. This directs the quite high attention to tend for VLSI floor planning. So our objective is to attenuate the chip area and fix the modules or blocks within the fixed outline. During this paper, a novel hybrid technique called STHMAC-BDFOFP is applied to enhance efficiency and accuracy than the conventional single optimization techniques. It is an essential design step to estimate the chip area by considering the optimal placement of modules and their interconnections. Each block consists of several hundred or thousands of cells that perform a specific operation. The block diagram of the proposed STHMAC-BDFOFP technique is designed as given below,

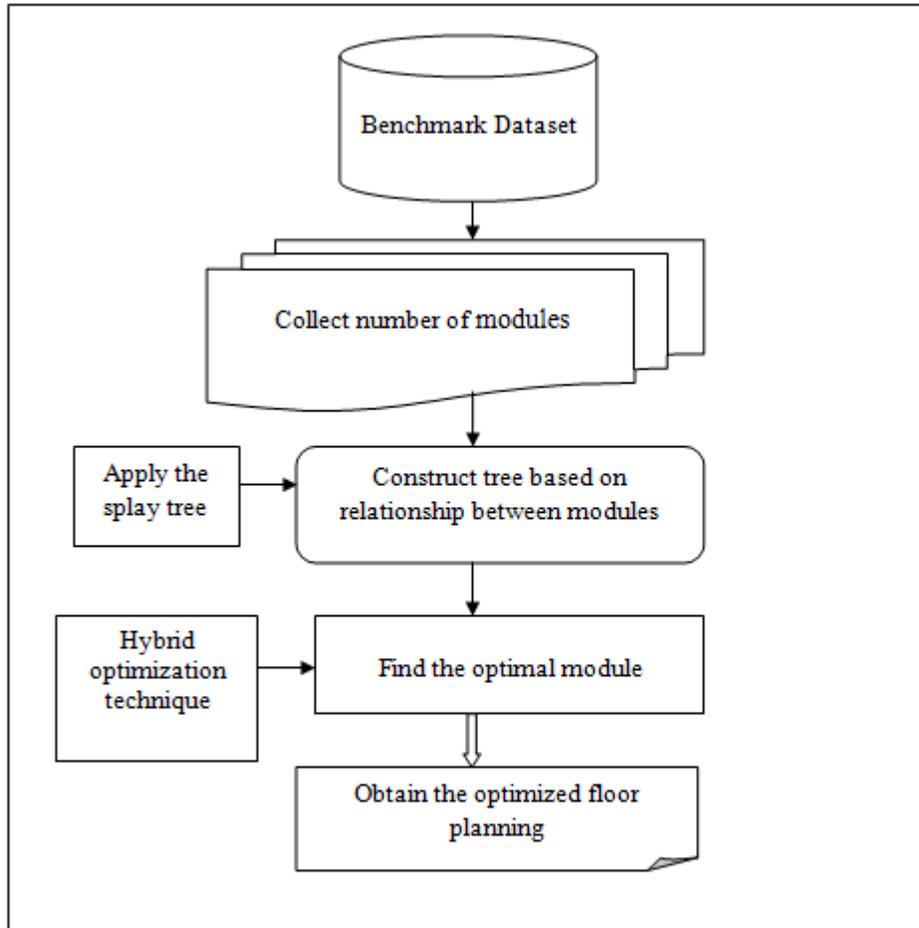


Figure 1 Flow process of the proposed STHMAC-BDFOFP technique

Figure 1 given above illustrates the architecture of the proposed STHMAC-BDFOFP technique which comprises the two stages such as tree construction and optimization. At first, numbers of modules are gathered from dataset. Splay tree is constructed based on the relationship between the modules. Followed by, the hybrid optimization technique discovers optimal solution for achieving energy and heat aware floor planning. These two processes of the proposed STHMAC-BDFOFP technique are explained in the succeeding sections.

3.1 Splay tree-based non-slicing floor planning

The proposed STHMAC-BDFOFP technique starts to perform the floorplanning based on tree construction. In general, the floorplanning is performed based on two processes namely slicing and non-slicing operation. The slicing operation is the process of repetitively partitioning

the floorplan either horizontally or vertically. Whereas, the non-slicing operation not bisecting the floorplan repetitively. In our work, the non-slicing operation is taken to create trees with number of modules from dataset.

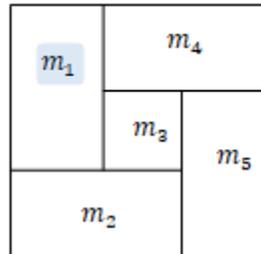


Figure 2 non-slicing based floor planning

Let us consider dataset ‘ D ’, and modules $M = m_1, m_2 \dots m_n$ that represents the floor plan membership. Each specific module has its height (H), width (W). Every module is free to rotate. The objective of floor planning is to present certain space for each module without any overlies between them. A splay tree is a binary search tree employed for quick access again. Splay tree partition a binary search tree into set of preferred paths. The basic operations of the splay tree are Splaying, Join, Split, Insertion, and Deletion. The splay tree is constructed based on the directed graphical model $G = (v, e)$ where v denotes a vertex (i.e. modules) and ‘ e ’ indicates an edge (i.e. connection between the modules).

Let us consider the modules $M = m_1, m_2, m_3, m_4, m_5$. In the splay operation, a node m_1 is accessed and the splay operation is performed on it to move it to the root. The splay operation is performed as follows,

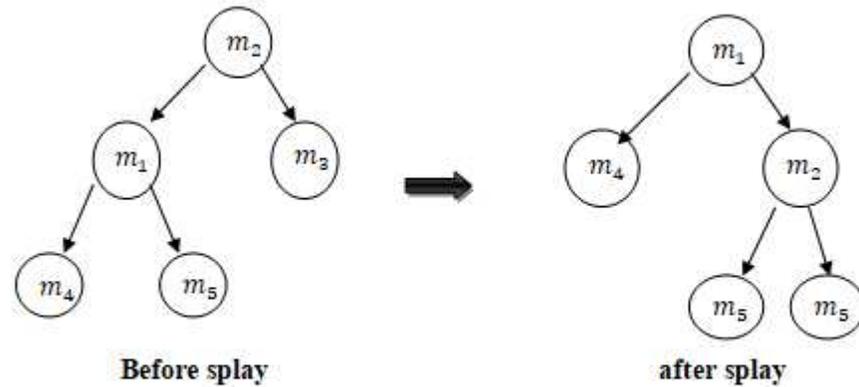


Figure 3 Splay tree constructions

Figure 3 illustrates the tree construction based on the relationship between the modules. To perform a splay operation on the node ' m_1 ' and it moves to the root and each of other node moves ' m_1 closer to the root. By applying the splay operations on the node after every access, the newly accessed nodes are kept near the root and the tree other nodes are balanced. Then the join operation is performed by concatenating the two auxiliary trees that the top node of one tree is a child of the bottom node of the other. Then the split operation is carried out by partitioning the chosen path into two parts at a particular node such as a top part and a bottom part. Finally, the Insertion process is carried out using the splay process. The newly inserted node becomes the root of the tree. In the deletion operation, the particular node is removed. Then the splay is performed to parent of the removed node to top of tree. Splay tree is constructed based on the non-slicing method.

3.2 Energy and Heat Aware hybridized Optimization

After the tree construction, based on input modules taken from dataset, hybridized Optimization is performed for optimized floor planning with lesser heat generation. The proposed technique uses multicriteria hybridized Optimization for finding the global optimum.

The single ant colony and firefly algorithm are hard to optimize the more than one objective functions at the same time to obtain the global optimum solution.

The ant colony optimization technique combined with the firefly algorithm effectively finds the global best solution through the ranking approach concerned with more than one objective function. The proposed technique uses multi-criteria optimization to find the best optimal paths in weighted graphs. The proposed optimization is a population-based metaheuristic to resolve complex multicriteria optimization issues depends on real ants behavior. The behavior of the ants is to search their food source. While searching the food source, the ants moved from one place to another by depositing an organic compound called pheromone on the ground. The communications between the ants are performed through the pheromone trails. The pheromone deposition is based on the amount of food the ant carries. Afterward, other ants also smell the deposited pheromone trails and follow that path. The shorter path from nest to food source having a higher probability of choosing that path since it has a more pheromone value.

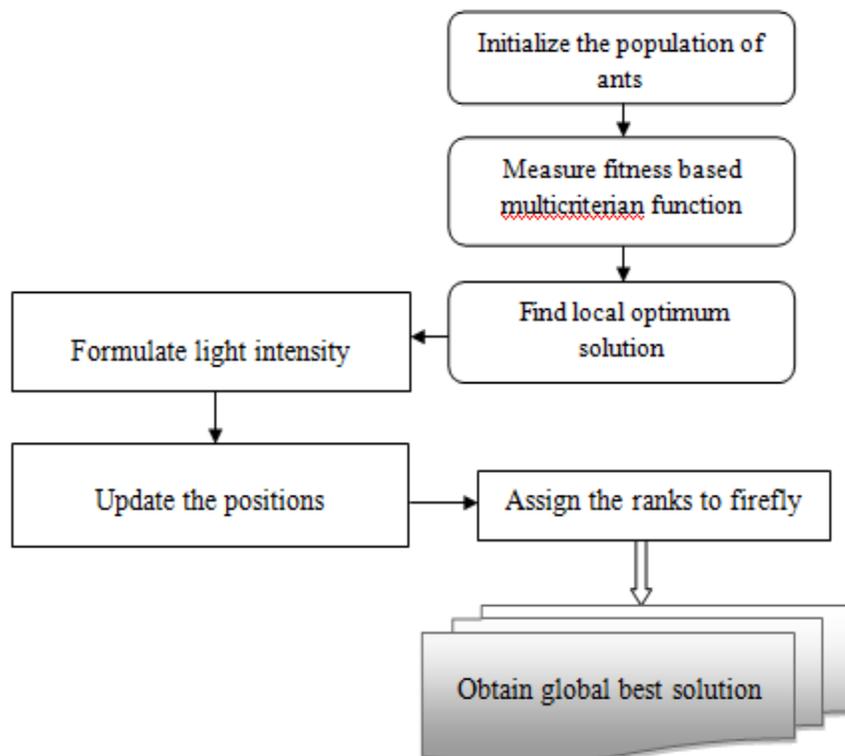


Figure 4 flow process of Hybridized Multicriteria Ant Colony and Bregman Divergencive Firefly Optimization

Figure 4 illustrates the flow process of the hybrid optimization to obtain the global optimal solution. Here, the ants are related to the modules in splay tree and the food source is represented as the multicriteria functions such as energy consumption, heat generation, space occupied, and wire length. Initialize the population of the ants in the search space,

$$M = m_1, m_2 \dots m_n \quad (1)$$

For each ant in the population, the fitness is measured based on the multicriteria function. The fitness is measured as follows,

$$F = a_r + \omega_1 \frac{a_1}{a_{1t}^*} + \omega_2 \frac{a_2}{a_{2t}^*} + \omega_3 \frac{a_3}{a_{3t}^*} + \omega_4 \frac{a_4}{a_{4t}^*} \quad (2)$$

Where, F denotes a fitness, ' a_r ' symbolizes the aspect ratio to control the floor plan operations, ' ω_1 ', ' ω_2 ', ' ω_3 ', ' ω_4 ' indicates a constant value ranging from 0 to 1. From the above (), the a_1 , a_2 , a_3 , a_4 indicates a multi-criterion function such as ' a_1 is the energy consumption', ' a_2 ' is the heat generation', ' a_3 denotes a space occupied' and ' a_4 indicates a wire length'. Let ' a_{1t}^* , a_{2t}^* , a_{3t}^* and a_{4t}^* ' are the average value of the energy consumption, heat generation, space occupied, and wire length based on randomly generated 1000 kinds of floor plan calculation. Therefore, the objective functions are measured as follows. Initially, the energy consumption is calculated as given below,

$$a_{1i} = \frac{\Delta T_{ij}}{R_j} \quad (3)$$

Where, ' a_{1i} ' indicates energy taken by module ' i ', ' ΔT_{ij} ' indicates temperature rise at module ' i ' with respect to transfer resistance at module ' R_j '. Heat generation of Module is given below,

$$a_{2i} = R_j * P_i \quad (4)$$

Where, R_j denotes a transfer resistance at module 'j', ' P_i ' are power consumed by the i^{th} module, ' T_A ' stand for ambient temperature. Then the space occupied by the module is evaluated as given below,

$$a_{3i} = h_i * w_i \quad (5)$$

Where, a_{3i} denotes a space occupied by the module ' h_i ' indicates a height and ' w_i ' denotes a width of the i^{th} module. Then, the wire length of ' i ' module is measured using Half-Perimeter Wire length (HPWL). The wire length of the module is formulated as given below,

$$a_{4i} = (x_{ih} - x_{il}) + (y_{ih} - y_{il}) \quad (6)$$

Where, a_{4i} indicates a wire length of the module, ' x_{ih} ' and ' x_{il} ' indicates greater and lower values of x - coordinates of HPWL bounding box of i^{th} module. ' y_{ih} ' and ' y_{il} ' denotes a higher and lower value of y -coordinates of HPWL bounding box i^{th} module.

Based on the fitness value, the local optimum solution is determined from population. Local optimum solution is finding out by sorting modules according to fitness function.

$$M = \{m_1 > m_2 > \dots > m_b\} \quad (7)$$

Once the modules are sorted according to the fitness, then the local optimum is determined to find the global optimum with minimum time. The modules with better fitness are chosen for finding the global optimum.

Then the global best solution is attained by applying the Bregman divergencive ranked firefly optimization is applied. This approach is designed based on the behavior of flashing light behavior of fireflies. Here the local best modules in the splay tree are initialized.

The entire fireflies are unisexual and any of the fireflies get attracted by the other fireflies based on their light intensity (i.e. fitness value). The attractiveness of the firefly depends on the light absorption coefficient. Firefly attractiveness ' A ' is represented as,

$$A = A_0 \exp(-\gamma r^m), m \geq 1 \quad (8)$$

Where, A_0 indicates attractiveness at $r = 0$, ' r ' denotes the distance, γ denotes a light absorption coefficient, ' m ' symbolizes a number of fireflies.

The firefly with less intensity is attracted towards the brighter one and the intensity of the firefly gets increased. Whereas the intensity of the firefly is reduced having the lesser fitness of the current best solutions. From the results, the brighter one is selected as the global best solution.

Let us consider the number of fireflies (local best) $m_1, m_2 \dots m_n$. For each firefly, the light intensity is formulated with the fitness function F .

$$I = F \quad (9)$$

Where I indicates a light intensity of the firefly. The firefly with high light intensity attracts to another one i.e. $I(f_j) > I(f_i)$ where $j = 1, 2, 3, \dots, n$ but $i \neq j$. Based on the intensity measure, the position of the global best is updated based on the Bregman distance as given below,

$$t_{i+1} = t_i + A \exp(-\gamma r_{ij}^2) |t_{best} - t_i| + \alpha_t \epsilon_t \quad (10)$$

Where, t_{i+1} denotes an updated position of the firefly, t_i indicates a current position of the firefly, A denotes attractiveness, γ denotes a light absorption coefficient, r_{ij}^2 denotes a distance, $|t_{best} - t_i|$ indicates a Bregman divergence or distance, ' α_t ' indicates parameter managing step size, ' ϵ_t ' indicates vector drawn from Gaussian or other distribution. Bregman distance measure discovers global optimum solution. With updated light intensity outcomes, fireflies are ranked in descending order. The first ranked firefly gets chosen as a global optimum than the others. In this way, the optimum modules in the tango tree are selected for achieving efficient floor planning in VLSI design.

Algorithm 1: Splay tree Hybridized Multicriteria Ant Colony and Bregman Divergencive Firefly Optimized Floor Planning

Input: dataset ‘ D ’, and modules $M = m_1, m_2 \dots m_n$

Output: Accurate Floor Planning in VLSI Design

Begin

Step 1: Collect a set of modules $M = m_1, m_2 \dots m_n$ from dataset ‘ D ’

Step 2: Construct a splay tree based on the relationship between modules

Step 3: Initialize the population of modules in the search space

Step 4: For each module ‘ m ’

Step 5: Measure multiple objective functions a_1, a_2, a_3, a_4

Step 6: Measure the fitness ‘ F ’

Step 7: While ($T < \text{Max_iteration}$) **do**

Step 8: **Sorting the m** based on F

Step 9: Select local optimum ‘ m ’ in a splay tree

Step 10: Initialize the population of fireflies

Step 11: Formulate light intensity based on fitness

Step 12: **if** ($I_j > I_i$) **then**

Step 13: Move firefly i towards firefly j

Step 14: **end if**

Step 15: Update the light intensity t_{i+1}

Step 16: Rank fireflies according to the light intensity

Step 17: $T=T+1$

Step 18: end while

Step 19: Best_solution ← global best ‘ m ’

end

Algorithm 1 illustrates process of Floor Planning in VLSI Design. Initially, the set of modules are collected from the dataset. Based on the relationship between the modules, the splay tree is constructed with different operations such as splaying, join, split, insertion, and deletion. After that, modules in the tango trees are initialized and measure the multicriteria functions such as energy consumption, heat generation, space occupied, wire length. Based on the above-said

function, the fitness is measured. After finding the fitness, the local best solution is identified by sorting the modules. Then the local best solutions are given to the firefly algorithm for identifying the global best. Initialize the population of local best solutions in search space. Then, the light intensity is formulated to fitness function based on multiple objective functions. If light intensity of one firefly is higher, then movement takes place. After movement, the position of firefly is updated based on Bregman divergence. The process gets repeated until it reaches the termination. Finally, the fireflies are ranked and find the best solution. As a result, efficient floor planning is obtained in VLSI design with minimum time.

3. Experimental setup

Experimental evaluation of STHMAC-BDFOFP technique and LOA floorplanner [1], ISI-APSO [2] are implemented in MATLAB 2015b with 3.4 GHz Intel Core i3 processor, 4GB RAM, and Windows 10 platform. Dataset is taken from the (https://s2.smu.edu/~manikas/Benchmarks/MCNC_Benchmark_Netlists.html). MCNC benchmark netlists are employed in numerous floor planning concepts. The benchmark circuits are in Yet Another Language (YAL) format. For experimental consideration, the modules are taken from the benchmark dataset. The modules are defined as a circuit used for floor planning. Table 1 offers circuit description of MCNC Benchmark dataset.

Table 1 Standard MCNC Benchmark Circuits

Circuit	Modules	Nets	I/O pad	Pins	Area (mm ²)
apte	9	97	73	287	46.5616
ami33	33	123	42	522	1.1564
ami49	49	408	22	953	35.4454
xerox	10	203	2	698	19.3503
hp	11	83	45	309	8.83

Table 1 describes five circuit standards such as apte, ami33, ami49, xerox, and hp from MCNC Benchmark. Every circuit standard is described with five columns.

3.1 Implementation scenario

In this section, the implementation of the proposed STHMAC-BDFOPF technique is discussed with the Benchmark Circuits Data Set. Initially, the apte Circuits is taken from the MCNC Benchmark dataset. In apte circuit, 9 modules are considered for experimentation. Initially, the splay tree is constructed with the 9 modules taken from the apte circuit.

Here, the ants are related to the modules in splay tree and the food source is represented as the multicriteria functions such as energy consumption, heat generation', space occupied, and wire length'. Initialize the population of the ants in the search space,

$$M = m_1, m_2 \dots m_n$$

Let us consider the population size of modules $M = 9$. For each ant in the population, the fitness is measured based on the multicriteria function. Initially, the energy consumption is calculated as given below, Let us consider $\Delta T_{ij} = 6 \text{ }^\circ\text{C}$, $R_j = 1.1 \text{ } \Omega$

$$a_{1i} = \frac{\Delta T_{ij}}{R_j} = \frac{6}{1.1} = 5.4545$$

Let us consider $R_j = 1.1 \Omega$, $P_i = 10$ watts. Then the heat generation of the module 1 is given by,

$$a_{2i} = R_j * P_i = 1.1 * 10 = 11$$

Let us consider, the height of the module 1 is $h_i = 1$, width of module 1 ' $w_i = 1$. The space occupied by the module is expressed as follows,

$$a_{3i} = h_i * w_i$$

$$a_{3i} = 1 * 1 = 1$$

Let us consider $x_{il} = 0mm$, $x_{ih} = 22 mm$, $y_{il} = 0mm$, $y_{ih} = 22 mm$. The wirelength of the module 1 as given below,

$$a_{4i} = (x_{ih} - x_{il}) + (y_{ih} - y_{il})$$

$$a_{4i} = (22 - 0) + (22 - 0) = 44mm$$

The fitness of the module 1 is expressed as follows,

$$F = a_r + \omega_1 \frac{a_1}{a_{1t}^*} + \omega_2 \frac{a_2}{a_{2t}^*} + \omega_3 \frac{a_3}{a_{3t}^*} + \omega_4 \frac{a_4}{a_{4t}^*}$$

Let us consider $a_r = 0.3$, $\omega_1 = 0.1$, $\omega_2 = 0.2$, $\omega_3 = 0.3$, $\omega_4 = 0.4$. $a_1 = 5.4545$, $a_2 = 11$, $a_3 = 1$, $a_4 = 44$, the fitness of the module 1,

$$F = 0.3 + 0.1 * \frac{1}{2} + 0.2 * \frac{11}{15} + 0.3 * \frac{1}{3} + 0.4 * \frac{44}{48}$$

$$F (\text{module 1}) = 0.2 + 0.1 * 0.5 + 0.2 * 0.73 + 0.3 * 0.33 + 0.4 * 0.91 = 0.859$$

Similarly, the fitness is measured for remaining modules in the apte circuit. Based on the fitness value, the local optimum solution is determined

$$M = \{m_1 > m_2 > \dots > m_9\}$$

Once the modules are sorted according to the fitness, then the local optimum is determined. The module which has fitness above 0.5 has a local optimum. Then the global best solution is attained by applying the Bregman divergencive ranked firefly optimization is applied.

Let us consider the 5 modules as local optimum. The population of firefly is = 5 . The attractiveness of the firefly is given below. Let us consider the $A_o = 1$, $\gamma = 1.0$, $r = 1.414$
 $m = 2$

$$A = A_o \exp(-\gamma r^m), m \geq 1$$

$$A = 1 \exp(-1 * 1^2) = 1 * \exp(-1) = 1 * 0.36 = 0.36$$

The light intensity is formulated with the fitness function F .

$$I = F$$

If $(f_j) > I(f_i)$, the position of the global best is updated based on the Bregman distance as given below. Let us consider the $t_i = 0.859$

$$t_{i+1} = t_i + A \exp(-\gamma r_{ij}^2) |t_{best} - t_i| + \alpha_t \epsilon_t$$

$$t_{i+1} = 0.859 + 0.36 \exp(-1 * 1^2) |1 - 0.859| + 0.2 * 0.1$$

$$t_{i+1} = 0.859 + 0.36 * 0.36 * 0.141 + 0.2 * 0.1$$

$$t_{i+1} = 0.859 + 0.0182 + 0.02 = 0.8972$$

Where, t_{i+1} denotes an updated position of the firefly. Similarly all the firefly positions get updated and ranked into the descending order. Finally, high ranked fireflies (i.e. module in tree) are selected.

4. Performance results discussions

The performance evaluation of STHMAC-BDFOFP technique and existing LOA floorplanner [1], ISI-APSO [2] are performed with metrics namely space occupied by circuits, heat generation, wire length, and processing time. The results of the various parameters are discussed using a table and graphical representation. The description of the various parameters are discussed as given below,

Space Occupied by the circuit: It is calculated as product of width of every module and height of module. It is mathematically formulated as given below,

$$SO = \sum_{i=1}^n h_i * w_i \quad (12)$$

Where, SO indicates a Space Occupied by circuit, ' h_i ' denotes height of module, ' w_i ' indicates width of module. It is measured in square of millimeter (mm^2).

Heat Generation: It is measured as the product of thermal resistance and power consumed by module. The heat generation is mathematically formulated as given below,

$$HG_i = R_i * P_i \quad (13)$$

Where, HG_i indicates a heat generation of i^{th} module, ' R_i ' is thermal resistance of i^{th} module. ' P_i ' indicates power consumed by i^{th} module. It is measured in degree Celsius ($^{\circ}\text{C}$).

Wirelength: Wire length of circuit is calculated as maximum and minimum values of both ' x ' and ' y ' coordinates of each module. The length of the wire is calculated as given below,

$$\text{Wirelength} = \sum_{i=1}^n (x_{ima} - x_{imi}) + (y_{ima} - y_{imi}) \quad (14)$$

Where, ' x_{ima} ' and ' x_{imi} ' indicates maximum and minimum value of ' x ' coordinates. ' y_{ima} ' and ' y_{imi} ' indicates maximum and minimum value of ' y ' coordinates. It is calculated in millimeter (mm).

Processing time: PT is calculated as amount of time taken by the algorithm to find optimized modules for efficient floor planning. Therefore, the overall time is calculated as given below,

$$PT = \text{end time} - \text{start time} \quad (19)$$

Where ‘*PT*’ denotes a processing time. *PT* is measured in milliseconds (ms).

Table 2 Tabulation for Space occupied by Circuits

Circuits	Space occupied by Circuits (mm ²)		
	STHMAC-BDFOFP	LOA floorplanner	ISI-APSO
apte	44.50	47.8	49.3
ami33	1.05	2.7	3.91
ami49	33.55	37.8	39.6
xerox	17.85	20.9	24.7
hp	7.74	9.6	11.4
Mean	20.93	23.76	25.78
Deviation	17.98	18.88	18.91

Table 2 describes the performance analysis of the Space occupied by circuits versus the different circuits taken from the MCNC benchmark netlists. The reported results of the Space occupied using three methods namely the STHMAC-BDFOFP technique and existing LOA floorplanner [1], ISI-APSO [2] are shown in table 2. From the obtained results, it indicates that the STHMAC-BDFOFP achieves lesser space consumption than the existing two methods. For example, apte circuit is considered for experimentation. By applying the STHMAC-BDFOFP technique, 44.50 mm² of space is occupied whereas the 47.8 mm² and 49.3 mm² are obtained using LOA floorplanner [1], ISI-APSO [2] respectively. Similarly, various space occupied results are obtained for different circuits. From the observed results, the proposed technique outperforms well the other two related approaches. The overall comparison results indicate that the average of five results using the STHMAC-BDFOFP technique is reduced by 23% and 32% than state-of-the-art methods.

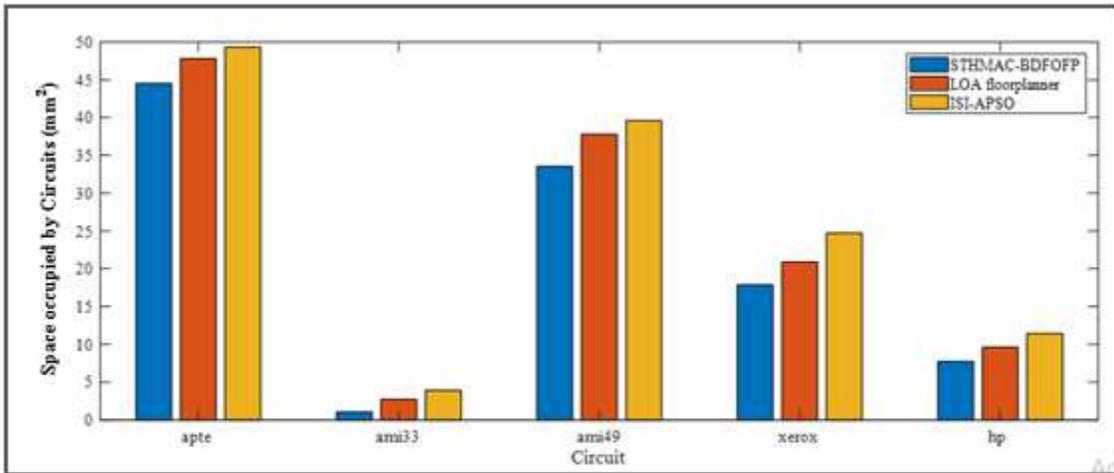


Figure 5 performance results of space occupied by circuits

Figure 5 exhibits the simulation result of Space occupied by circuits using three methods namely the STHMAC-BDFOFP technique and existing LOA floorplanner [1], ISI-APSO [2]. The various circuits are taken in the horizontal direction and the results are obtained in a vertical axis. As shown in the graphical chart, the blue color column indicates the Space occupied by circuits using the STHMAC-BDFOFP technique whereas the red and yellow color column indicates Space occupied results of existing [1] [2] respectively. The plot indicates that the proposed STHMAC-BDFOFP technique achieves better performance. The reason for this significant improvement is to apply the Hybridized Multicriteria Ant Colony and Bregman Divergencive Firefly Optimized Floor Planning. The Hybridized technique accurately finds the modules with lesser space consumption. This helps to reduce the overall circuit space occupied.

Table 3 Tabulation for Heat Generation

Circuits	Heat Generation (°C)		
	STHMAC-BDFOFP	LOA floorplanner	ISI-APSO
apte	64.54	68.75	70.10
ami33	90.21	93.62	96.51
ami49	58.76	63.22	66.40
xerox	75.65	78.10	80.21
hp	69.12	72.11	75.34
Mean	71.65	75.16	77.71
Deviation	12.07	11.64	11.73

Table 3 displays the heat generation of the three different methods of STHMAC-BDFOFP technique and existing LOA floorplanner [1], ISI-APSO [2]. In order to statistically estimate the heat generation, the different circuits are taken from the benchmark datasets. For each run, different counts of modules are taken as input. From the observed result, the heat generation of the proposed STHMAC-BDFOFP technique is smaller than the other two conventional methods. This is proved through statistical analysis. Let us consider the ami49 circuit and it comprises the 49 modules. The heat generation of the circuit using the STHMAC-BDFOFP technique is 58.76 °C. Whereas, the heat generation of the circuit using the existing LOA floorplanner [1], ISI-APSO [2] are observed as 63.22 °C and 66.40 °C respectively. Similarly, the various heat generation results are observed for each method with respect to different types of modules. 5 different circuits are taken from the benchmark dataset. The average of comparison results indicates that the heat generation is considerably minimized by using the STHMAC-BDFOFP technique by 5% when compared to [1] and 8% when compared to existing [2].

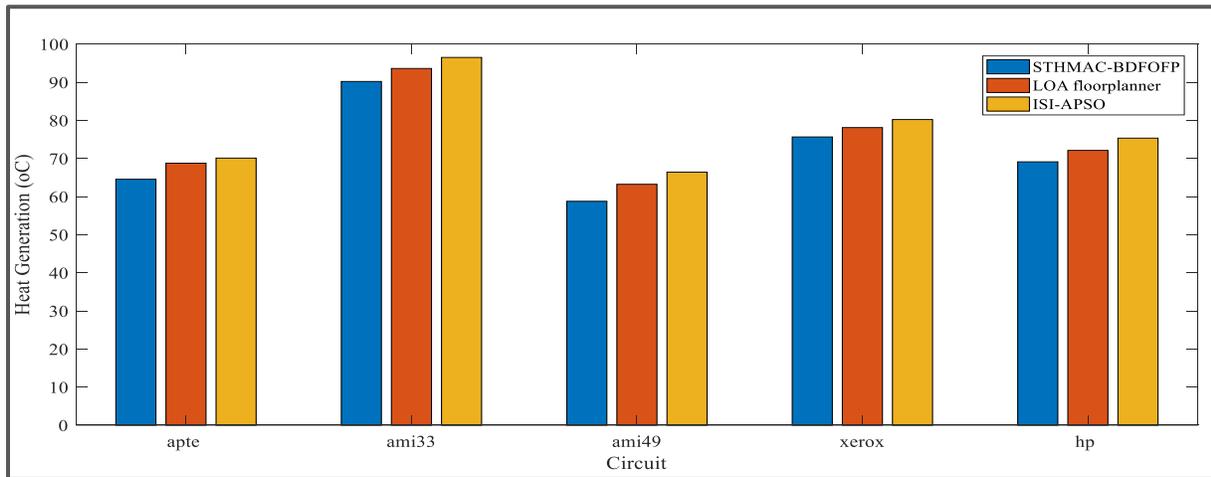


Figure 6 performance results of heat generation

The graphical representation of the performance results of heat generation using three methods is illustrated in figure 6. As shown in figure 6, where the horizontal axis illustrates the five different circuits taken from the benchmark datasets and the vertical axis demonstrates the heat generation (in degree celicius). The above simulation results illustrate the heat generation of the STHMAC-BDFOFP technique is minimal when compared to the existing LOA floor planner [1], ISI-APSO [2] respectively. This major enhancement is achieved by applying the hybridized optimization technique. The STHMAC-BDFOFP technique uses the ant colony and Bregman Divergencive Firefly algorithm. Initially, the modules in the tree are given to the input of the ant colony optimization based on the multicriteria fitness function. Then the local best is applied to the Bregman Divergencive Firefly algorithm to update the given solution and obtain the global optimum solution. The modules in the tree with lesser heat generation are chosen for floor planning in VLSI design.

Table 4 Tabulation for Wirelength

Circuits	Wirelength (mm)		
	STHMAC-BDFOFP	LOA floorplanner	ISI-APSO
apte	397.45	410.22	422.30

ami33	43.44	46.52	49.54
ami49	695.72	710.46	724.33
xerox	375.02	393.10	410.22
hp	139.06	147.04	160.33
Mean	330.13	341.46	353.34
Deviation	254.41	259.0	262.28

Table 4 demonstrates the comparison results of Wirelength with respect to the number of Circuits. The wirelength is measured in terms of a millimeter (mm). The experimental evaluation is accomplished with the ami33 circuit, the wirelength of the STHMAC-BDFOFP technique is 43.44mm and the results of wirelength using LOA floorplanner [1], ISI-APSO [2] are observed as 46.52mm and 49.5mm respectively. Similarly, the other runs are performed with different counts of input circuits. The overall performance results of Wirelength of the proposed STHMAC-BDFOFP technique are compared with existing methods. The average of five results noticeably proved that the Wirelength is minimized by 4% and 9% as compared to other related methods LOA floorplanner [1], ISI-APSO [2] respectively.

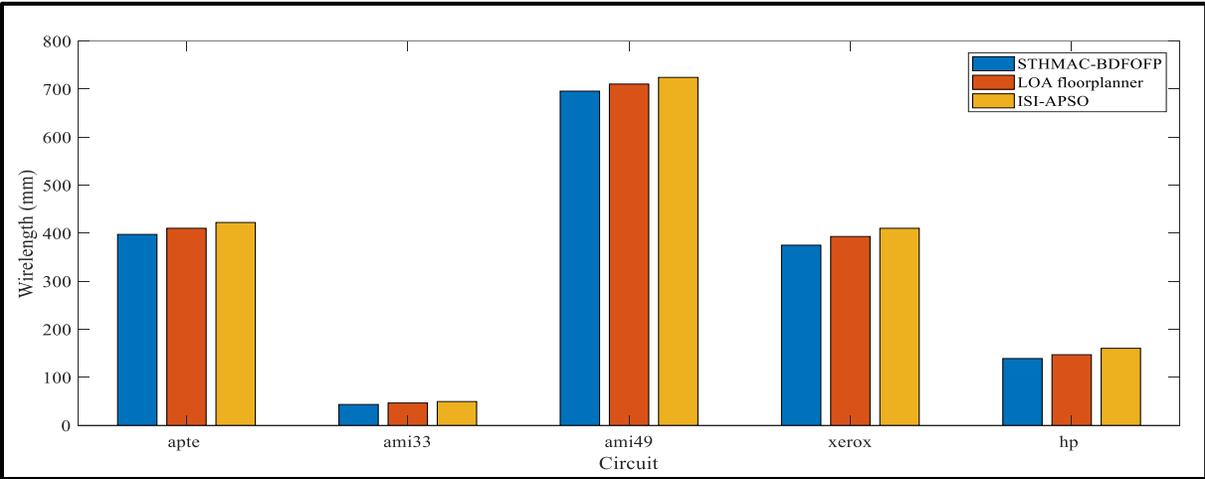


Figure 7 performance results of wirelength

Figure 7 perceives the performance results of wirelength for different circuits. The graphical plot indicates that the STHMAC-BDFOFP technique outperforms well in terms of

achieving lesser wirelength than the existing methods. The appropriate reason to select wirelength of circuit is minimized by lessen the space occupied. If modules are exactly located with lesser space consumption, then wirelength of circuit is reduced. Minimal space occupied modules are chosen by hybrid optimization technique.

Table 5 Tabulation for Computation time

Circuit	Number of modules	Computation time (ms)		
		STHMAC-BDFOFP	LOA floorplanner	ISI-APSO
apte	9	12	15	18
ami33	33	23	28	30
ami49	49	30	34	36
xerox	10	13	16	19
hp	11	14	17	20

Table 5 demonstrates the performance analysis of the computation time of floor planning with respect to the number of circuits. Computation time is calculated as an amount of time taken to perform the efficient floor planning. The tabularized computation time indicates that the STHMAC-BDFOFP technique provides superior performance than the other two existing methods. The experiment is conducted with 49 modules, STHMAC-BDFOFP technique consumes the time of 30ms and the computation time of LOA floorplanner [1], ISI-APSO [2] are observed 34ms and 36ms respectively. Similarly, the other counts of modules are taken for conducting the simulation. Totally five runs are observed for each method with different counts of input modules. The overall processing time of the STHMAC-BDFOFP technique is evaluated with the other two conventional methods. The average of five results noticeably proved that the computation time is minimized by 17% and 27% as compared to other related methods [1] [2].

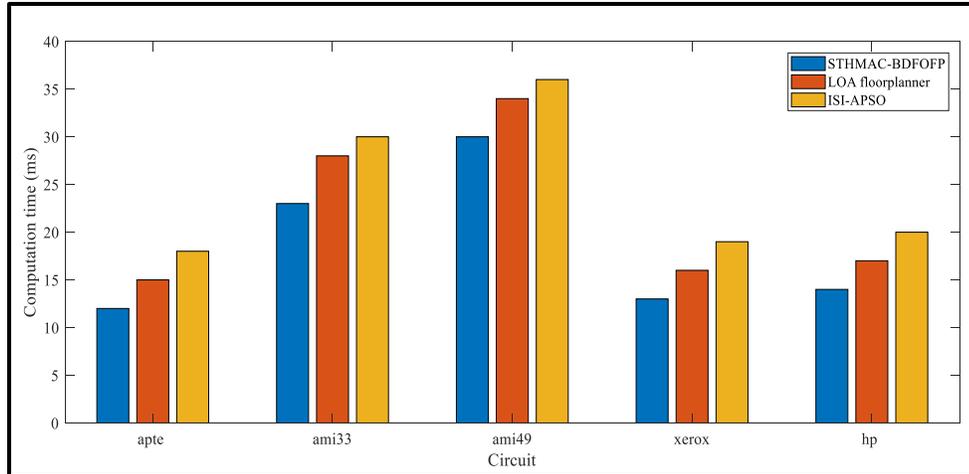


Figure 8 performance results of computation time

Figure 8 illustrates results of computation time for efficient floor planning performance in VLSI design. The graphical plot indicates that the processing time gets increased while increasing the number of input counts. Among the different methods, the proposed STHMAC-BDFOFP technique outperforms well in terms of achieving lesser computation time. The suitable reason that the splay tree is constructed based on the relationship between the modules. After that, the integration of two optimization techniques is applied for finding the local best and global modules hence it minimizes the computation time of floor planning.

5. Conclusion

A new optimization algorithm called STHMAC-BDFOFP has been presented in the physical design of VLSI Chip with minimum time. STHMAC-BDFOFP is presented by combination of splay tree as well as hybrid optimization techniques. Here multicriteria floorplanning problem is solved by arranging and placing the modules in a chip in such a way that aim like minimum space occupied, lesser heat energy, wirelength area achieved. The splay tree is constructed based on the relationship between the modules. Then the integrated optimization technique is applied to the modules in the splay-tree. The hybrid optimization discovers the better modules which have lesser energy and heat generation for designing the VLSI Chip. This provides efficient floor planning with lesser computation time. Simulation is performed to estimate the performance of the STHMAC-BDFOFP technique over the two

conventional methods and different performance metrics such as space occupied by circuits, heat generation, wirelength, and computation time. Statistical results illustrate that STHMAC-BDFOFP produces improved performance in minimization of wirelength, space occupied and heat generation than the conventional methods.

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Figures

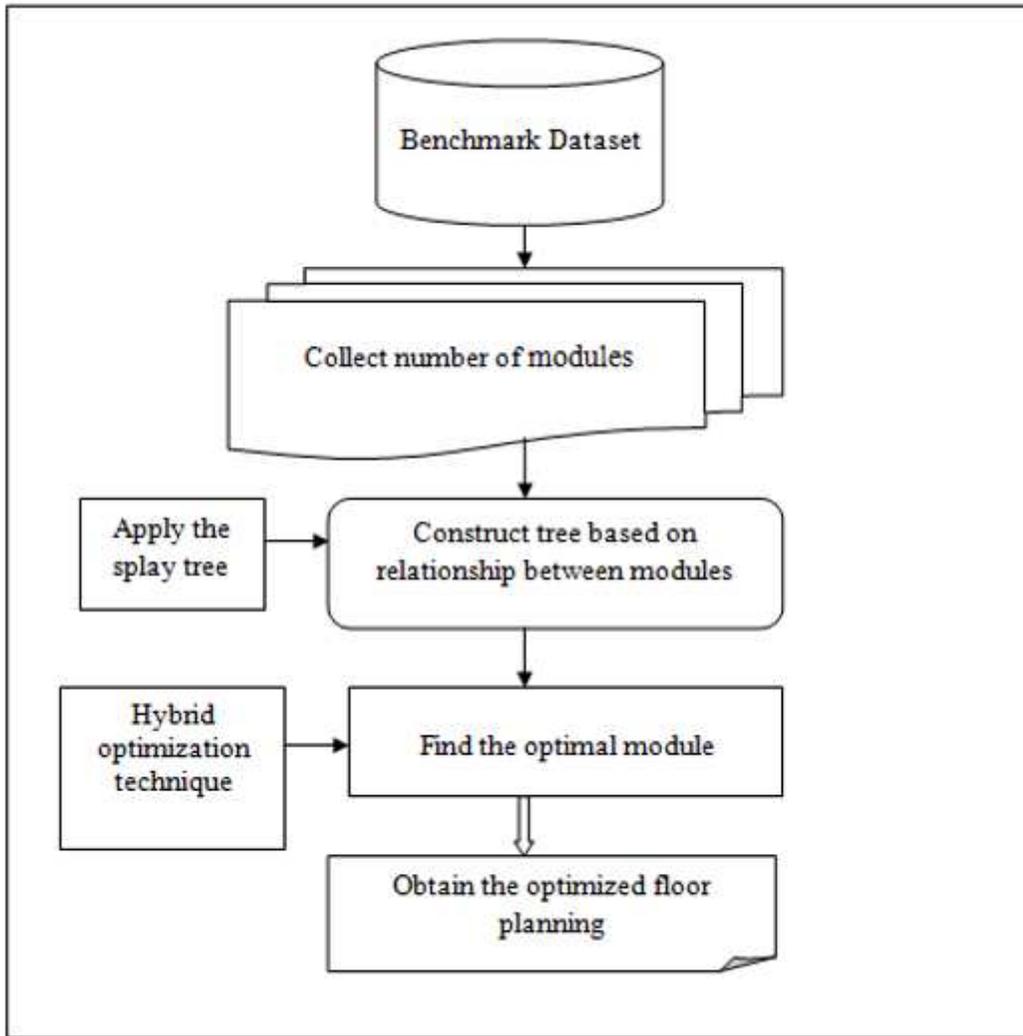


Figure 1

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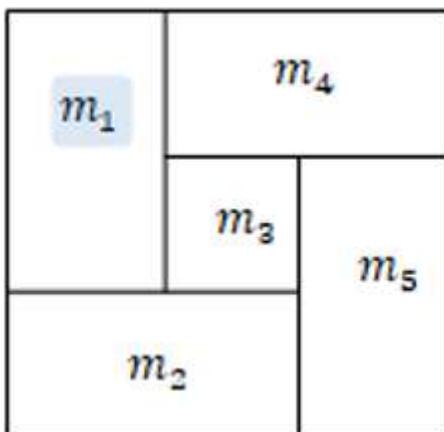


Figure 2

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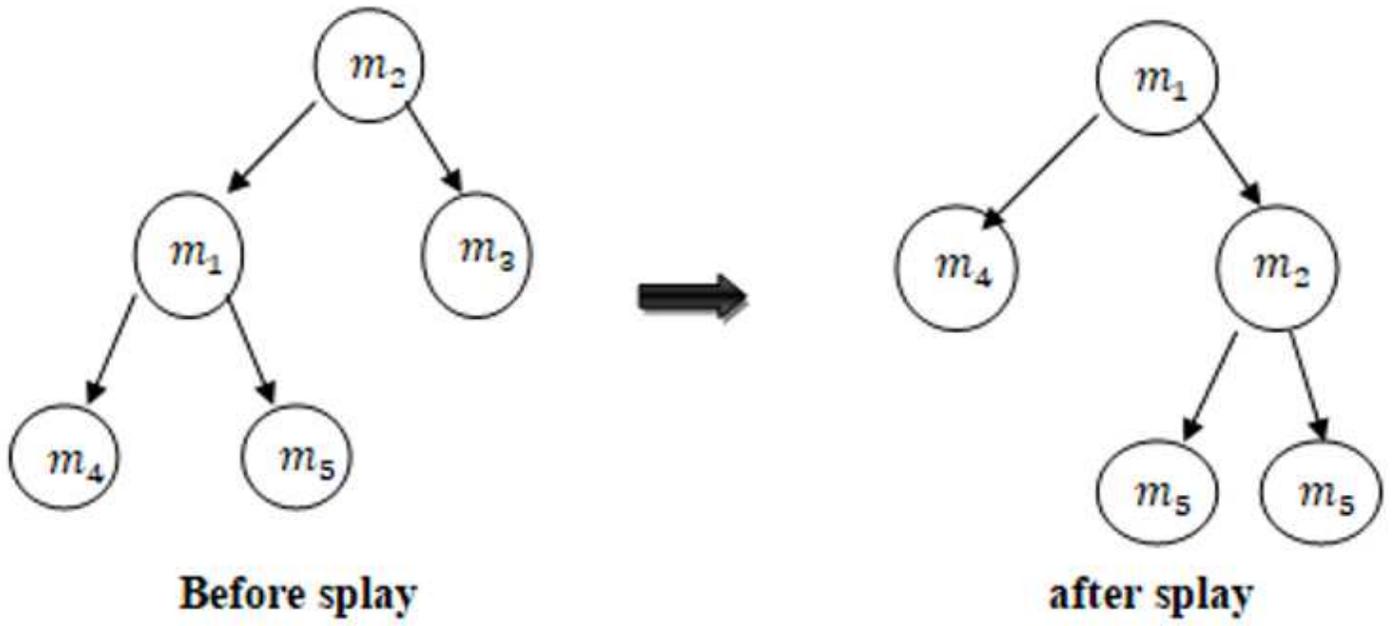


Figure 3

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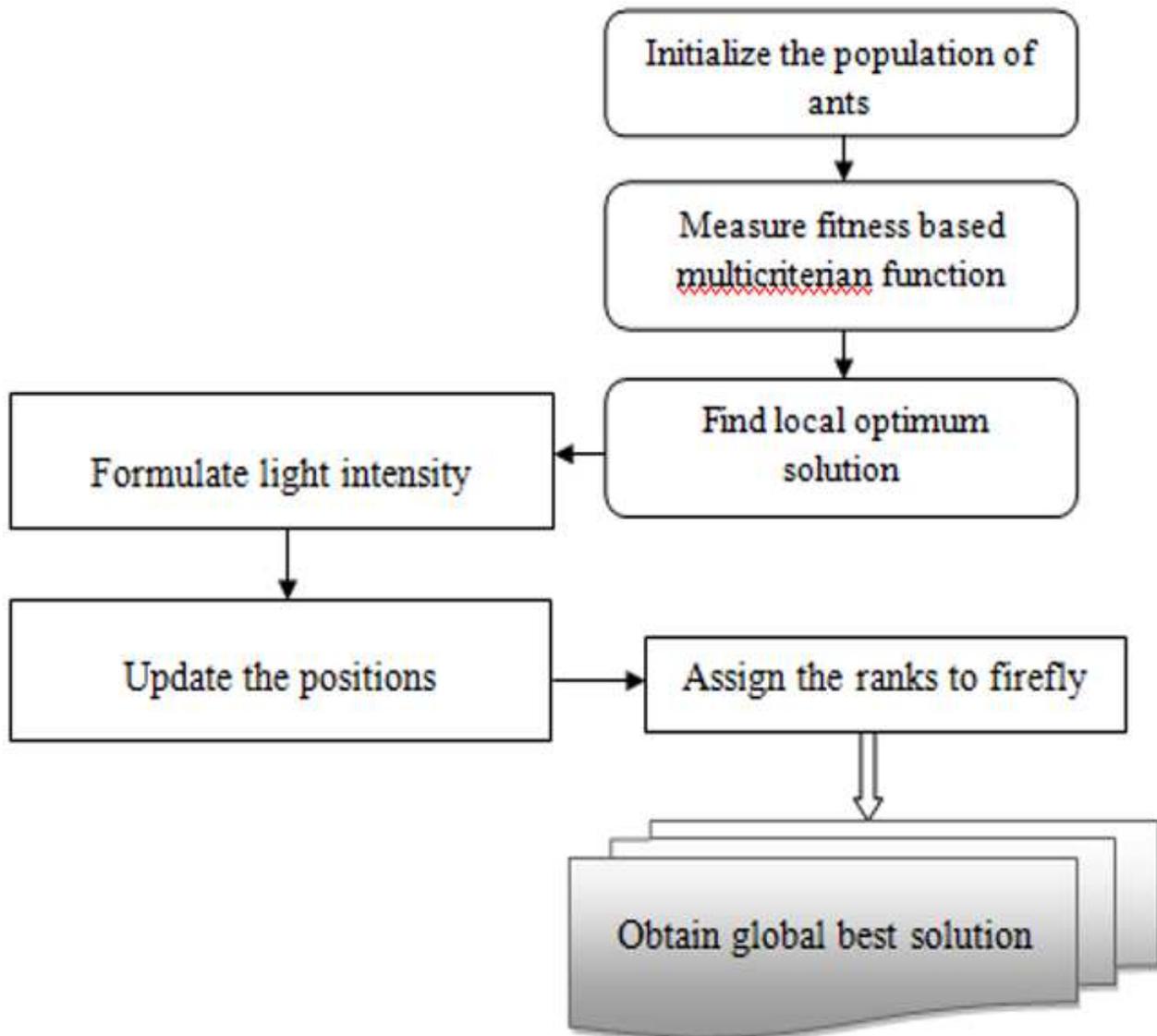


Figure 4

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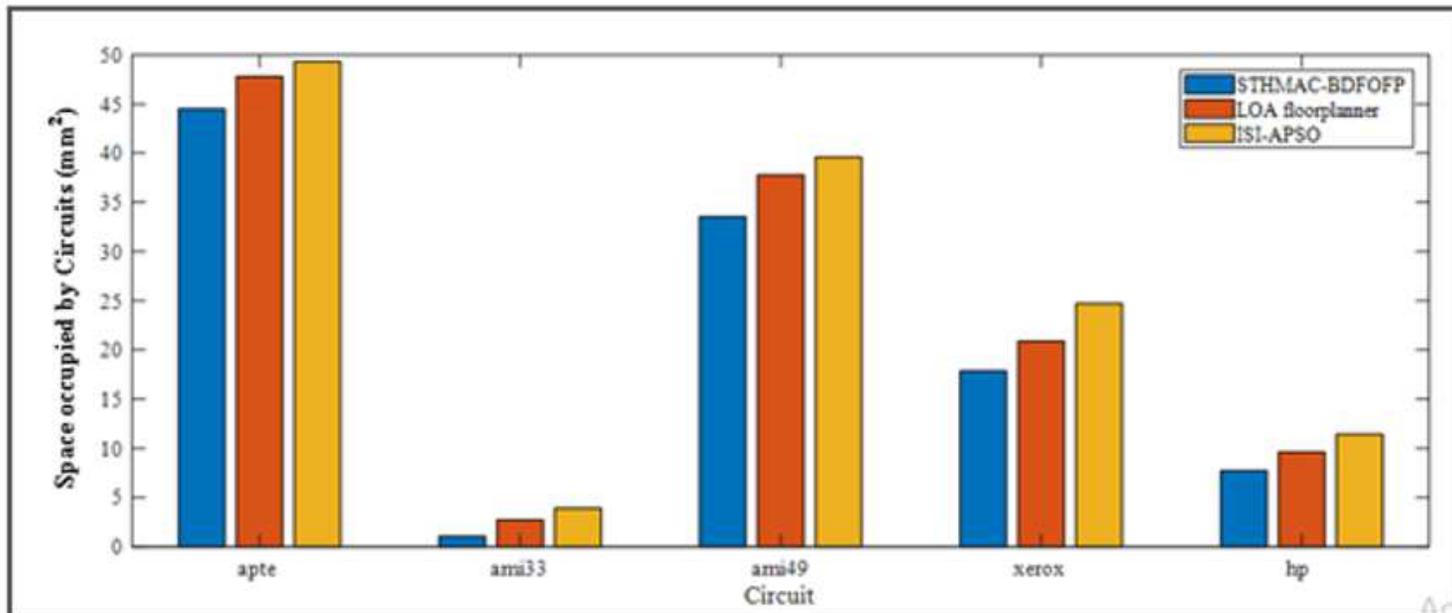


Figure 5

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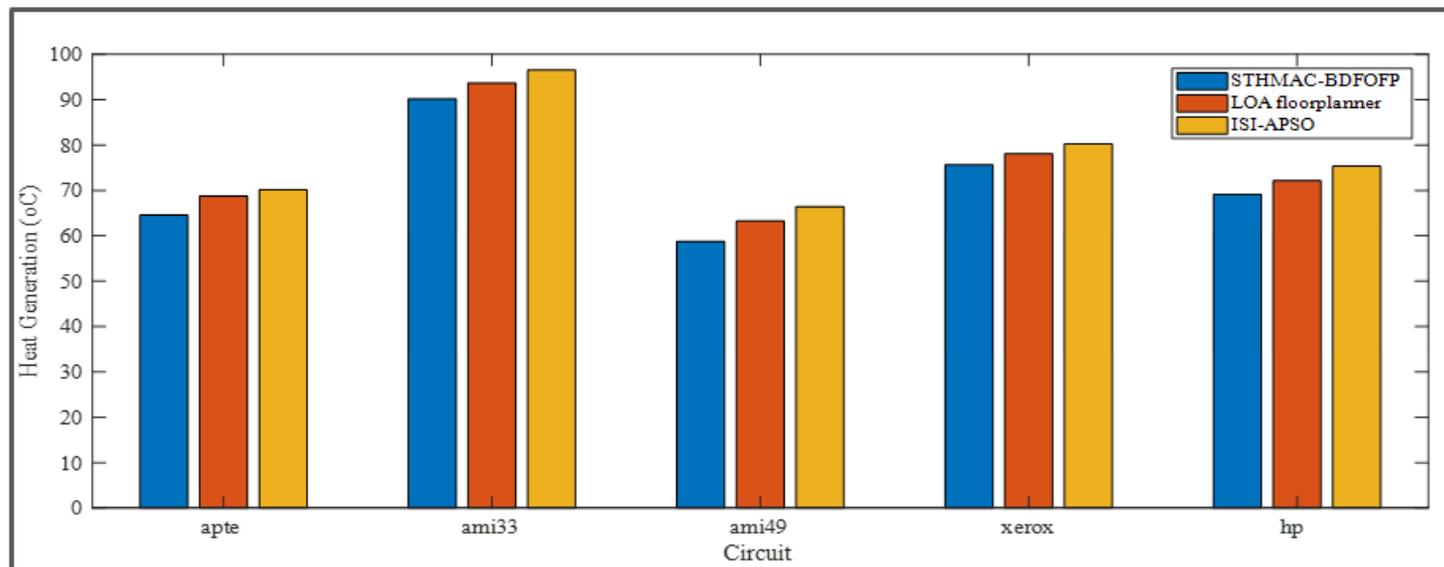


Figure 6

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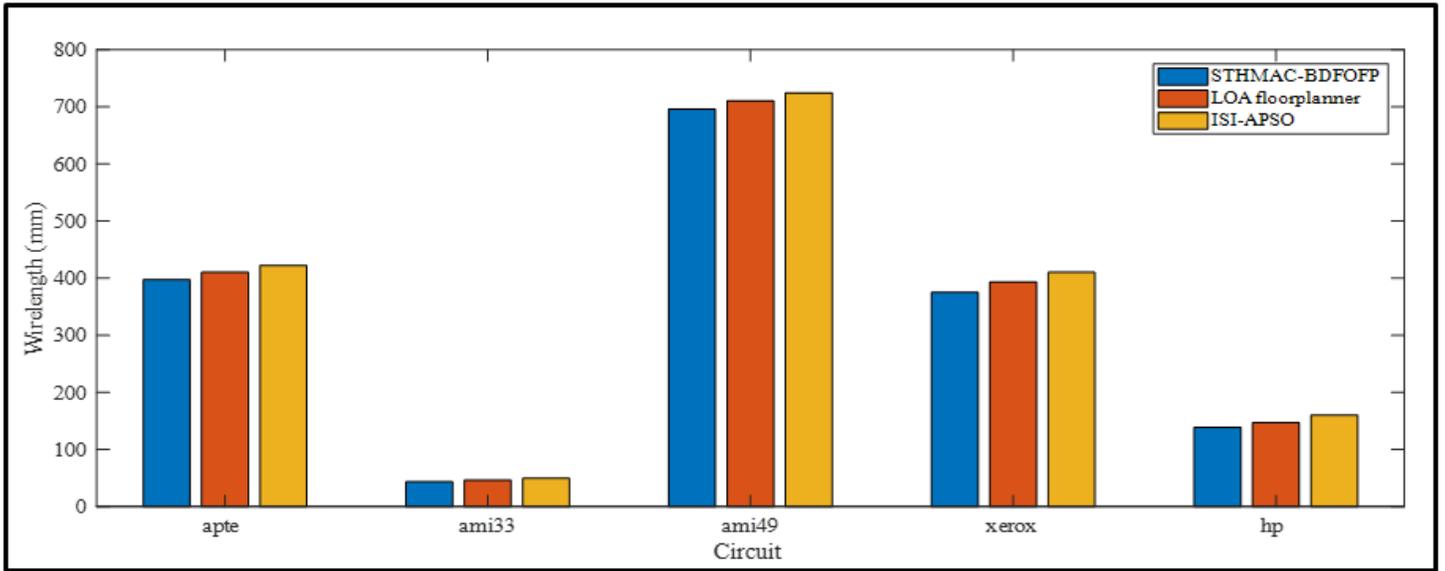


Figure 7

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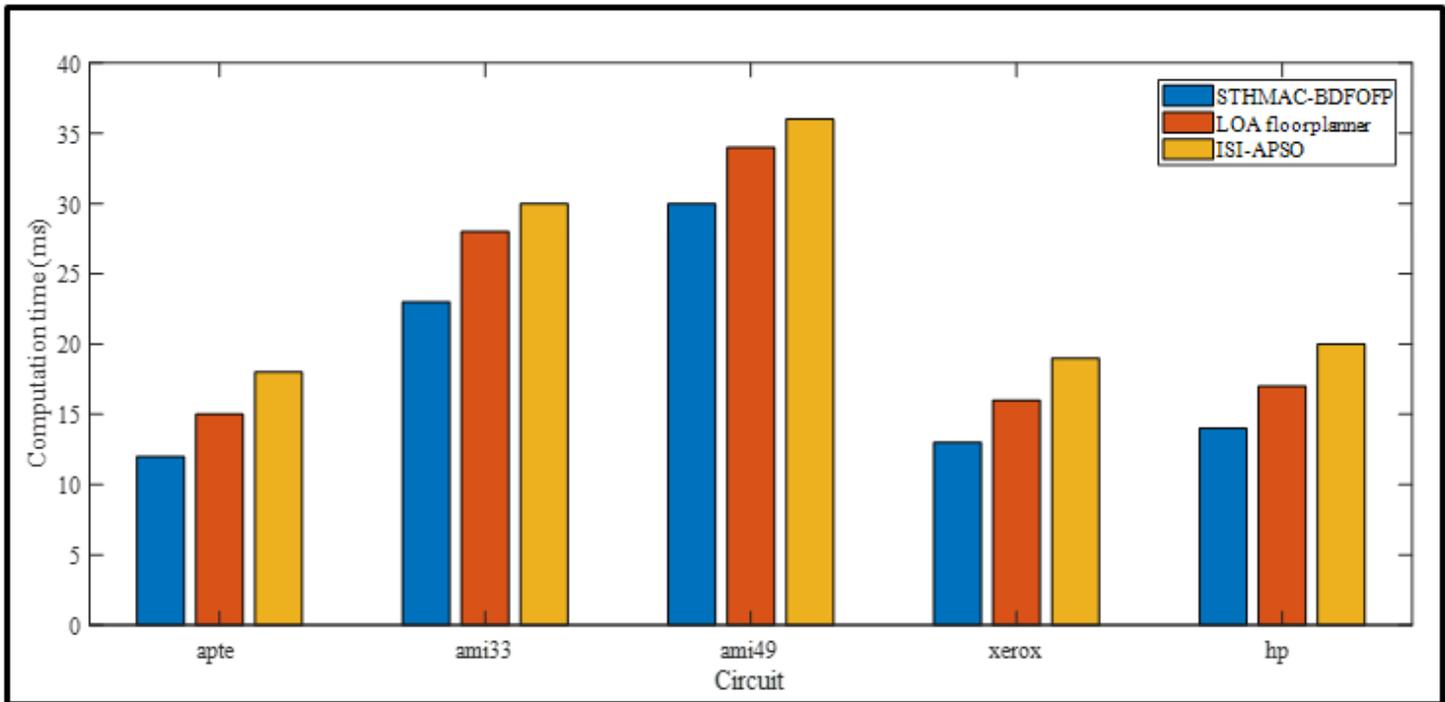


Figure 8

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