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# Comparative Analysis of Open and Short Defects in embedded SRAM using Parasitic Extraction Method for Deep Submicron Technology.

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**Research Article**

**Keywords:** Fault Models, Open Faults, Short Faults, Parasitic Extraction Method

**Posted Date:** March 20th, 2023

**DOI:** https://doi.org/10.21203/rs.3.rs-2384499/v1

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**Version of Record:** A version of this preprint was published at Wireless Personal Communications on August 28th, 2023. See the published version at https://doi.org/10.1007/s11277-023-10704-w.

# Abstract

The technology advances from the micron level to the Nanometer level. This striking change in the technology with so many factors might influence the embedded device design and its performance. In the fast-growing technology, it is very difficult to find suitable algorithms to test embedded SRAM. It is noticed that while going to deep sub-nano technologies, the existing test methods may not fully satisfy the test results due to the increased number of faults and defects. Scale-down technologies have an impact on the parasitic effects, creating an additional source of faulty behavior, and making the existing test techniques less effective in detecting them. In this paper we propose a new method, taking the parasitic effect into the consideration, which gives the fault information along with its location. In the proposed method we have considered node-to-node open and short defects for different technologies (45nm, 32nm, and 7nm). It is observed that the proposed test method gives 100% fault coverage which is independent of technology variation.


# 1. Introduction

After the invention of integrated circuits in 1949, technology advanced rapidly, integration changed from small-scale integration to very large-scale integration, and the transistor count increased from tens to ten billion. As technology advances, the feature size decreases, hence the number of stack layers increases. This makes the physical verification and electrical verification more complex and also more critical throughout the design process.

Earlier memory test challenges were few because the size and usage of memory was less. The algorithms written for testing were developed with a mathematical base, but given less importance for their practical usage. The impact of the circuit's physical malformation on the circuit characteristics can be called a fault. Later on, the fault models and test algorithms were developed based on physical defects [1].

Memory tests are performed to confirm the correct functioning of a memory device. Various test methodologies have been implemented to identify memory defects. Traditional test methods are zero/one, checkerboard, GALPAT, walking 1/0, and sliding diagonal to name a few. Initially, investigations were carried out based on fault and fault modeling. The majority of the test methodologies are based on the type of fault that occurs in the memory. The eSRAM fault is defined as the representation of a physical defect at the proper level of abstraction [2]. For ensuring the SRAM operating correctly different testing methods are used. March tests are efficient for ensuring the correct functionality of SRAMs [3, 4]. March tests as an example of algorithmic implementation, often target a definite fault model [17]. Faults may be single or multiple. In multiple faults again we have two types of faults linked faults and unlinked faults. In linked faults, a fault in one cell will change the behavior of the other cell [5, 18] whereas in unlinked cells change in the behavior of one cell, does not affect the behavior of the other cell. [18] Proposed a new type of March tests to detect multiple faults. Address decoder faults which are non-classical faults are the other type of faults [7] and also static faults and dynamic faults are other type of faults. If the faults are sensitized by performing a single operation are called static faults [20], Dynamic Faults are those faults that require more than one operation (Read/Write) to be sensitized [9]. Scale-down technologies influence parasitic parameters like capacitance and resistance. This parasitic effect causes additional faults, which are not detected by the existing test methods. [8,16,19,21] Proposed a new parasitic extraction method that gives fault coverage with fault location. Resistive-opens/shorts falls [10–15] are timing-dependent fault models. Furthermore, it is important to consider resistive open faults become important because of the increased number of interconnection layers in contemporary technologies

# 2. Existing Method

Now a day's technology advances towards miniaturization, high error-prone designs may result in dense eSRAMs. This causes a reduction in memory and SoC yield. Thus, some sort of solution is required, that should be free from technology variations as well as independent of the fault chosen[6]. The latest testing technique does not consider the impact of the parasitic memory effect, this is another drawback, which results in an incomplete test. Aiming this we proposed a testing method for eSRAM using parasitic R, C extraction from a fault-induced layout, which gives an extreme fault detection

As shown in Fig. 1, in 6T SRAM layout contains seven nodes (Q, QB, WL, BL, BLB, VDD, and VSS). In the proposed method, parasitic R, and C values are observed at each individual node (Q, QB, BL, BLB, and WL). On selecting a particular node, it gives the total parasitic R, and C values at that node. Parasitic capacitance is a combination of metal capacitance, cross-talk capacitance, diffusion

capacitance, and gate capacitance. Similarly, parasitic resistance comprises metal resistance, poly resistance, via resistance, and diffusion resistance.

## 2.1 Faults in proposed SRAM Cell

In general, fault modeling is the translation of a physical defect into a mathematical construct or electrical construct that can be implemented algorithmically, and understood by a software simulator for providing metrics for quality measurement. Memory testing requires a detailed modeling activity, which precisely describes the effect that the physical defect may produce on the memory. To detect all modeled faulty behaviors, one needs to use efficient test algorithms and test architectures. The main objective of fault modeling is to identify the source of the defect that is causing the fault.

In the proposed Parasitic Extraction Method, initially, we extract the R and C values at each node. Later we impose the short/open between each node and then extract the R, C values at each node, these extracted values are compared with the R, C values of fault-free SRAM cell. The deviation between the extracted R and C values of the faulty and fault-free cell indicates the fault at the node. Hence the following steps are involved in the parasitic extraction method. i) model the circuits with fault imposed ii) categorize the fault types iii) Get the fault model circuit's defect-induced layout out and check for wire shorts, open circuits, or missing wires. iv) collect parasitic R and C samples from every faulty layout, and compare them with a prototyped fault-free layout

## 2.2 Types of Faults in single 6T SRAM

The faults in single-cell SRAM are classified based on the way the fault behaves within itself. Faults are classified as simple and linked faults based on the behavior.

The difference between simple faults and linked faults depends upon the number of cells that have actively participated in creating a fault in a particular cell

The behavior of a simple fault in one cell cannot be influenced by the fault behavior in another cell; that means masking cannot occur. Whereas in linked faults the behavior of a certain fault can change the behavior of another, such that masking can occur.

Based on the fault type, cell data may retain its correct data but return wrong data during the read operation. Similarly, the read data might be accurate, by keeping incorrect or random data within the cell. Based on these possibilities, a set of faults are defined in terms of fault models.

## 3. Proposed Fault Model With Short/open Defects In Single Cell Sram

Several open and short faults are analyzed in the proposed method. Figure 3 and Fig. 4 depict the scheme of 6T-SRAM cell with all possible open and Short Defects

Figure 1 shows 6T SRAM cell with seven main nodes Q, QB, BL, BLB, WL, VDD, and VSS. Out of which Q and QB are internal nodes through them the cell state can be monitored and WL, BL and BLB are external nodes through these writing and reading operations can be performed. The VDD and VSS are supply and ground nodes respectively.

Table 1
Shows the node equivalence corresponding to main nodes.

| S.No | Node | Node Equivalence |
|---|---|---|
| 1 | Q | $M_2D$, $M_1D$, $M_5D$, $M_3G$, $M_4G$ |
| 2 | QB | $M_3D$, $M_4D$, $M_6S$, $M_2G$, |
| 3 | WL | $M_5G$, $M_6G$ |
| 4 | BL | $M_5S$ |
| 5 | BLB | $M_6D$ |
| 6 | VDD | $M_2S$, $M_3S$ |
| 7 | VSS | $M_1S$, $M_4S$ |

Internal node Q is a common point to drain $M_1$ ($M_1D$), $M_2$ ($M_2D$), and $M_5$ ($M_5D$) transistors. It is also the common point for the gate of $M_3$ ($M_3G$) and $M_4$ ($M_4G$) transistors. Hence short between $M_1D$ to QB is equivalent to a short between Q and QB. It is true with other equivalent nodes. Including equivalent nodes, all possible short defects between the internal and external nodes are 259. However, excluding equivalent nodes, the actual short defects found are only 21. For simplicity, the short defects are represented with SD (abbreviation for Short Defects) listed in Table 2.

Table 2
6T SRAM Cell short defect list for different technologies

| S.No | Fault Representation | Short between Nodes | Technology | | |
|---|---|---|---|---|---|
| | | | 45nm | 32nm | 7nm |
| 1 | $SD_1$ | Q-QB | UWF, URF | USWF, URF | USWF, URF |
| 2 | $SD_2$ | WL-BL | SA1 | TF | WBAF, TF |
| 3 | $SD_3$ | WL-BLB | USF | USRF-1 | WBAF, USRF-1 |
| 4 | $SD_4$ | WL-VDD | Error(NAF) | Error | Error |
| 5 | $SD_5$ | WL-VSS | Error(NAF) | Error | Error |
| 6 | $SD_6$ | WL-Q | SA0, URF | SA0, URF | SA0, URF |
| 7 | $SD_7$ | WL-QB | SA1,URF | SA1, URF | SA1, URF |
| 8 | $SD_8$ | VDD-VSS | UWF, URF0 | UWF, URF0 | UWF, URF0 |
| 9 | $SD_9$ | Q-VDD | URF, UWF | URF0, UWF0 | URF0, UWF0 |
| 10 | $SD_{10}$ | Q-VSS | URF, UWF | URF1, UWF1 | URF1, UWF1 |
| 11 | $SD_{11}$ | QB-VDD | IOF | IOF | IOF |
| 12 | $SD_{12}$ | QB-VSS | UWF, URF0 | TF, URF0 | TF, URF0 |
| 13 | $SD_{13}$ | Q-BLB | URF | URF | URF |
| 14 | $SD_{14}$ | QB-BLB | WBAF | WBAF, USWF0, USRF0 | USWF0, USRF0 |
| 15 | $SD_{15}$ | Q-BL | SA0(WBAF) | WBAF, SA0 | SA0 |
| 16 | $SD_{16}$ | QB-BL | USWF, USRF | WBAF, USWF, USRF | USWF, USRF |
| 17 | $SD_{17}$ | BL-BLB | USWF, USRF | USWF, USRF | USWF, USRF |
| 18 | $SD_{18}$ | BL-VDD | Error(NAF) | Error(NAF) | Error(NAF) |
| 19 | $SD_{19}$ | BL-VSS | Error(NAF) | Error(NAF) | Error(NAF) |
| 20 | $SD_{20}$ | BLB-VDD | Error(NAF) | Error(NAF) | Error(NAF) |
| 21 | $SD_{21}$ | BLB-VSS | Error(NAF) | Error(NAF) | Error(NAF) |

Similarly, as shown in Fig. 3. We analyzed the SRAM cell for open faults also. We found totally 25 open faults defects by excluding equivalent faults. The analysis of open faults and different types of faults observed at each node is shown in Table3. Open Faults are represented with OF (abbreviation for Open Fault)

Table 3
6T SRAM Cell open defect list for different technologies

| Defect Representation | Open Defect at nodes | Technology | |
|---|---|---|---|
| | | 7nm | 32nm |
| $OF_1$ | $BL\text{-}T_5S$ | NAF | NAF |
| $OF_2$ | $WL\text{-}T_5G$ | NAF | NAF |
| $OF_3$ | $WL\text{-}T_6G$ | URF | URF |
| $OF_4$ | $Q\text{-}T_1D$ | UWF1 | UWF1 |
| $OF_5$ | $Q\text{-}T_2D$ | UWF0 | UWF0 |
| $OF_6$ | $Q\text{-}T_1DT_2D$ | NAF | NAF |
| $OF_7$ | $Q\text{-}T_3G$ | UWF0, URF0 | TF |
| $OF_8$ | $Q\text{-}T_4G$ | UWF1, URF1 | TF |
| $OF_9$ | $Q\text{-}T_3GT_4G$ | NAF | NAF |
| $OF_{10}$ | $VDD\text{-}T_1S$ | UWF1 | UWF1 |
| $OF_{11}$ | $VDD\text{-}T_3S$ | UWF0, URF0 | TF |
| $OF_{12}$ | $VDD\text{-}T_1ST_3S$ | UWF,URF0 | UWF,URF0 |
| $OF_{13}$ | $VSS\text{-}T_2S$ | UWF0 | UWF0 |
| $OF_{14}$ | $VSS\text{-}T_4S$ | UWF1, URF1 | TF |
| $OF_{15}$ | $VSS\text{-}T_2ST_4S$ | UWF, URF1 | UWF, URF1 |
| $OF_{16}$ | $QB\text{-}T_3D$ | UWF0, URF0 | TF |
| $OF_{17}$ | $QB\text{-}T_4D$ | UWF1,URF1 | UWF1,URF1 |
| $OF_{18}$ | $QB\text{-}T_3DT_4D$ | URF, UWF0 | URF0, UWF |
| $OF_{19}$ | $QB\text{-}T_1G$ | UWF1 | UWF1 |
| $OF_{20}$ | $QB\text{-}T_2G$ | UWF0 | UWF0 |
| $OF_{21}$ | $QB\text{-}T_1GT_2G$ | UWF | UWF |
| $OF_{22}$ | $T_1G\text{-}T_2G$ | UWF | UWF |
| $OF_{23}$ | $T_3G\text{-}T_4G$ | NAF | NAF |
| $OF_{24}$ | $BLB\text{-}T_6S$ | URF | URF |
| $OF_{25}$ | $WL\text{-}T_5GT_6G$ | NAF | NAF |

The functional Fault model is the difference between the observed and expected fault model. To detect the fault, we use fault primitives (FPs). The faults detected by using FPs are called detectable faults. There are some faults, which cannot detect by using fault primitives. These faults are called undetectable faults. By using the proposed method, we can detect both faults.

Using the proposed Parasitic R, C method, existing faults identified are Undefined Read and Write faults( URF, UWF), Transition Faults(TFs), Stuck at Faults(SAFs), Write Before Access Faults (WBAF), Un stabilized Read and Write Faults (USRF, USWF), No Access

Faults(NAFs), in addition to these faults we identified a new fault, named as Undefined Short Fault (USF). We also observed that the fault behavior of the cell changed, when technology changed.

**Stuck at Faults**:

If the cell sticks at a given value for all performed operations. These faults are known as stuck-at faults. There are two types of stuck-at faults Stuck at Zero (SA-0) and Stuck at One (SA-1). SA-0 fault occurs when the output is always connected to the ground. We can observe this fault at SD-6(short between the nodes WL-Q), $SD_{10}$ (short between the nodes Q-VSS), and $SD_{15}$ (short between the nodes Q -BL). SA-1 occurs when output is always connected to VDD). We can observe this fault at $SD_2$ (When WL-BL shorted), $SD_7$ (WL-QB shorted), and $SD_{12}$ (QB-VSS shorted)

**Transition Faults**

A '0' should be allowed to be entered in a cell that has a '1' stored in it, and vice versa. However, TF appears if the cell doesn't make a transition from its first stored value. In the proposed method TF happens for open defect faults at nodes $OF_7$, $OF_8$, $OF_{11}$, $OF_{14}$, and $OF_{16}$ as shown in Table 3.

**Undefined Read Fault**:

For the read operation if the cell goes to the undefined state, the cell is said to have an undefined read fault, Undefined means, the cell state goes to neither '1' nor '0' with the read operation. This fault observed for

the short defect at $SD_1$, $SD_6$, $SD_7$, $SD_8$, $SD_9$, $SD_{10}$, $SD_{12}$, and $SD_{13}$ and for open defects fault induced at $OF_3$, $OF_{15}$, $OF_{17}$, $OF_{18}$ and $OF_{24}$.

For proper Read-1 operation, when we will make Bit Lines BL = 1, BLB = 1, and when we will enable the write line, we need to get BL0 = 1 and BLB0 = 0, but as shown in Fig. 8, for Read-1 operation we are getting BL0 = 1 and BLB0 = 1. This indicates the undefined state. The same operation we can observe for the Read-0 operation

**Undefined Write Fault**:

An undefined Write Fault is defined as the cell going to the undefined state, when we will perform the write operation of the cell. UWF fault identified for the short faults induced at $SD_1$, $SD_8$, $SD_9$, $SD_{11}$, and for the open faults this fault identified at $OF_4$, $OF_5$, $OF_{10}$, $OF_{12}$, $OF_{13}$, $OF_{15}$, $OF_{17}$, $OF_{19}$, $OF_{20}$, $OF_{21}$ and $OF_{22}$. Where SD represents Short Faults and OF represents Open Faults.

**Undefined Short Fault**:

An undefined short fault occurs when we introduce a short between the nodes WL-BLB. As shown in Fig. 9 for the fault defect at WL-BLB, the cell goes to the undefined state for the write 1 operation, it stores logic 1 automatically for the read operation after that the cell value is flipped from logic 1 to logic 0 when we will set the bit line values to zero. This type of fault is not defined by any fault primitive, hence it is observed as a new fault and named an Undefined Short fault.

## 4. Results And Comparison

For the design of embedded SRAM, three technologies have been selected 45nm, 32nm, and 7nm technologies. Table 4. gives the comparison and the overview of the key parameters like supply voltage, delays, current, and length and width of the transistors for the different technology nodes. In the analysis of the parameters, we have considered three modes of operation, Standard, High Voltage, and High Speed. For example in the calculation of delays Tdelay represents standard time delay, the delay represents the delay in high voltage mode and THs represent high-speed mode.

Table 4
Comparison of Transistor Parameter for different technologies

| Parameter | 180nm | 120nm | 90nm | 65nm | 45nm | 32nm | 14nm | 7nm |
|---|---|---|---|---|---|---|---|---|
| VDD(V) | 2 | 1.2 | 1 | 1 | 1 | 1 | 0.8 | 0.8 |
| Tdelay(ns) | 0.03 | 0.03 | 0.005 | 0.005 | 0.003 | 0.0025 | 0.0016 | 0.0012 |
| THvDelay(ns) | 0.1 | 0.06 | 0.02 | 0.01 | 0.008 | 0.007 | 0.007 | 0.004 |
| THsDelay(ns) | 0.6 | 0.02 | 0.004 | 0.003 | 0.002 | 0.002 | 0.005 | 0.002 |
| TWireDelay(ns) | 0.1 | 0.07 | 0.005 | 0.002 | 0.0015 | 0.0014 | 0.001 | 0.001 |
| Tcurrent(mA) | 0.6 | 0.5 | 0.1 | 0.1 | 0.08 | 0.07 | 0.03 | 0.04 |
| ML(um) | 0.18 | 0.12 | 0.1 | 0.07 | 0.05 | 0.03 | 0.016 | 0.007 |
| $MH_VL$(um) | 1.5 | 0.36 | 0.3 | 0.2 | 0.18 | 0.036 | 0.01 | 0.01 |
| MNW(um) | 1.5 | 1 | 0.5 | 0.3 | 0.3 | 0.08 | 0.048 | 0.024 |
| MPW(um) | 1.5 | 2 | 1 | 0.5 | 0.5 | 0.108 | 0.048 | 0.024 |

The numbers 180nm, 120nm, 90nm, 65nm, 45nm, 32nm, 14nm, and 7nm are representing the minimal channel length that can be fabricated.

The comprehensive fault model dictionary with all three technologies with a list of short defects and corresponding fault models for a single-cell SRAM is shown in Table 2.

It is found that few short defects are exhibiting the same faulty behavior in all three technologies chosen. For example, defect models VDD-VSS represent UWF and URF faults. The UWF Fault occurs with a write operation and the same fault model exhibits URF faults with a read operation. This is due to the fault model VDD being shorted to VSS, then which makes the VDD to the ground potential, hence inverter transistors $M_1$ and $M_3$ always stay ON position, leading Q and QB always remain at “0”. Hence while writing “1” or writing “0”, the node Q and QB will be inactive for accepting new values. For read '0', both BL and BLB results with '0' cause an Undefined Read Fault (URF). The same is true for read operation QB.

Apart from the existing faults, few undetectable faults are identified. For example, defect model WL-BLB for 45nm technology results in **Undefined Short Faults**, however, the same defect model is observed as an Unstabilized Read Fault in 32nm technology, and Write before Access Faults and Unstabilized Read fault for 7nm technology.

Similarly, WL-BL behaves as Stuck at Faults in 45nm, but in the other two technologies, it behaves as Transition faults (TF) and Write Before Access Faults (WBAF). Fault models QB-VSS, WL-BLB follow the same.

Table 5. displays the retrieved parasitic R and C values for three different technologies of fault-free SRAM. Additionally, these values are used in comparison with problematic SRAM cell parasitic for fault detection.

Table 5
Parasitic R, C values of Fault Free SRAM Cell for different technologies

| **Input-output nodes** | **Fault free SRAM Cell Parasitic R, C values** | | | | | |
|---|---|---|---|---|---|---|
| | **45nm** | | **32nm** | | **7nm** | |
| | **R(Ω)** | **C(aF)** | **R(Ω)** | **C(aF)** | **R(Ω)** | **C(aF)** |
| Q | 6881 | 1900 | 677 | 1800 | 433 | 2900 |
| QB | 7585 | 1800 | 497 | 1500 | 1170 | 3100 |
| WL | 4712 | 663 | 421 | 791 | 180 | 1800 |
| BL | 1216 | 664 | 75 | 701 | 158 | 1100 |
| BLB | 240 | 354 | 79 | 637 | 54 | 783 |
| VDD | 6600 | 1900 | 31 | 313 | 2071 | 2700 |
| VSS | 2823 | 1300 | 13 | 313 | 402 | 1700 |

## 4.1 Fault Detection Using Parasitic R, C Method for short faults

Table 6. Variation of parasitic R, C values for SRAM short defect model

| nodes | Short defect fault model | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | WL-BL (WBAF, TF) | | VDD-VSS (UWF, URF0) | | QB-VDD (IoF) | | Q-BL (SA0) | | QB-BL (USWF, USRF) | |
| | Fault Free | | Effected Node | | Effected Node | | Effected Node | | Effected Node | | Effected Node | |
| | C(fF) | R(Ω) | C(fF) | R(Ω) | C(fF) | R(Ω) | C(fF) | R(Ω) | C(fF) | R(Ω) | C(fF) | R(Ω) |
| Q | 2.9 | 433 | 2.90 | 433 | 2.90 | 433 | 2.90 | 407 | NA | NA | 2.90 | 407 |
| QB | 3.1 | 1170 | 3.10 | 1170 | 3.10 | 1170 | NA | NA | 3.10 | 1170 | NA | NA |
| WL | 1.8 | 180 | NA | NA | 1.80 | 180 | 1.80 | 178 | 1.80 | 180 | 1.80 | 180 |
| BL | 1.8 | 158 | 1.60 | 236 | 1.10 | 158 | 1.00 | 157 | 2.90 | 529 | 3.50 | 941 |
| BLB | 0.783 | 54 | 0.783 | 54 | 0.783 | 54 | 0.753 | 54 | 0.783 | 54 | 0.783 | 54 |
| VDD | 2.7 | 2071 | 2.70 | 2071 | 2.40 | 1670 | 4.00 | 2787 | 2.70 | 2071 | 2.70 | 2071 |
| VSS | 1.7 | 402 | 1.70 | 402 | 2.00 | 805 | 1.70 | 402 | 1.70 | 402 | 1.70 | 402 |

Figure10 illustrates the fault detection method based on parasitic capacitance change for 7nm technology. Fault model WBAF, TF is created by a short between WL and BL. As expected, parasitic capacitances at other nodes Q, QB, BLB, VDD, and VSS are the same as fault free except at nodes WL and BL, for this fault model node WL is absorbed represented with NA (Node Absorbed).

Similar to the fault model UWF, the parasitic capacitance change is more pronounced at impacting nodes VDD and VSS while remaining the same at other nodes that are fault free. URF0 corresponds to a short defect simulated by the short between VDD and VSS. When QB is shorted to VDD to simulate a short defect, parasitic variation is seen at VDD, while node QB is absorbed. For the short defect characterized by Q-BL for fault model SA0, The parasitic variation seen at BL and node Q is absorbed.

Figure11. depicts the resistance variation at each node for fault detection. On the graph, X-axis represents the all possible faults, whereas Y-axis represents the resistance in ohms. The same justification applies to fault detection using parasitic resistance

Table 7
Complete Fault Model Dictionary using 32nm Technology for SRAM short defect model

| S.No | Open Defect | Node Q | | Node QB | | Node WL | | Node BL | | Node BLB | | Node VDD | | Node VSS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Ideal C = 2900aF, R = 433Ω | | Ideal C = 3100aF, R = 1170 Ω | | Ideal C = 1800aF, R = 180Ω | | Ideal C = 1100 aF, R = 158Ω | | Ideal C = 783aF, R = 54Ω | | Ideal C = 2700 aF, R = 2071Ω | | Ideal C = 1700 aF, R = 402Ω | |
| | | C in aF | R in Ω | C in aF | R in Ω | C in aF | R in Ω | C in aF | R in Ω | C in aF | R in Ω | C in aF | R in Ω | C in aF | R in Ω |
| 1 | Q-QB | 5500 | 1583 | - | - | 1800 | 178 | 1000 | 157 | 0750 | 53 | 2700 | 2071 | 1700 | 402 |
| 2 | WL-BL | 2900 | 433 | 3100 | 1170 | - | - | 1600 | 236 | 0780 | 54 | 2700 | 2071 | 1700 | 402 |
| 3 | WL-BLB | 2900 | 433 | 3100 | 1170 | 2100 | 219 | 1000 | 159 | - | - | 2700 | 2071 | 1700 | 402 |
| 4 | WL-VDD | - | - | - | - | - | - | - | - | - | - | 2800 | 2164 | 1700 | 402 |
| 5 | WL-VSS | - | - | - | - | - | - | - | - | - | - | 2700 | 2071 | 2700 | 553 |
| 6 | Q-WL | 4000 | 565 | 3100 | 803 | - | - | 1000 | 157 | 0750 | 54 | 2700 | 2071 | 1700 | 402 |
| 7 | QB-WL | 2900 | 433 | - | - | 4300 | 1331 | 1000 | 157 | 0750 | 54 | 2700 | 2071 | 1700 | 402 |
| 8 | VDD-VSS | 2900 | 433 | 3100 | 1170 | 1800 | 180 | 1100 | 158 | 0780 | 54 | 2400 | 1670 | 2000 | 805 |
| 9 | Q-VDD | - | - | 3000 | 971 | 1800 | 178 | 1000 | 158 | 0780 | 54 | 3600 | 2409 | 1700 | 402 |
| 10 | Q-VSS | - | - | 3000 | 971 | 1800 | 178 | 1000 | 158 | 0750 | 53 | 2700 | 2071 | 3100 | 743 |
| 11 | QB-VDD | 2900 | 407 | - | - | 1800 | 178 | 1000 | 157 | 0750 | 54 | 4000 | 2787 | 1700 | 402 |
| 12 | QB-VSS | 2900 | 407 | - | - | 1800 | 178 | 1000 | 157 | 0750 | 53 | 2700 | 2071 | 3500 | 1146 |
| 13 | Q-BLB | 3100 | 445 | 3100 | 803 | 1800 | 180 | 1000 | 157 | - | - | 2700 | 2071 | 1700 | 402 |
| 14 | QB-BLB | 2900 | 407 | 3400 | 842 | 1800 | 180 | 1000 | 157 | - | - | 2700 | 2071 | 1700 | 402 |
| 15 | Q-BL | NA | NA | 3100 | 1170 | 1800 | 180 | 2900 | 529 | 0780 | 54 | 2700 | 2071 | 1700 | 402 |
| 16 | QB-BL | 2900 | 407 | - | - | 1800 | 180 | 3500 | 941 | 0780 | 54 | 2700 | 2071 | 1700 | 402 |
| 17 | BL-BLB | 2900 | 407 | 3100 | 803 | 1800 | 180 | 1300 | 196 | - | - | 2700 | 2071 | 1700 | 402 |
| 18 | BL-VDD | - | - | - | - | - | - | - | - | - | - | 2800 | 2198 | 1700 | 402 |
| 19 | BL-VSS | - | - | - | - | - | - | - | - | - | - | 2700 | 2071 | 1800 | 528 |
| 20 | BLB-VDD | - | - | - | - | - | - | - | - | - | - | 2800 | 2101 | 1700 | 402 |
| 21 | BLB-VSS | - | - | - | - | - | - | - | - | - | - | 2700 | 2071 | 1700 | 430 |

The complete fault model dictionary for proposed fault models with parasitic R and C values using 32nm technology for 6T SRAM cell is shown in Table 7. The complete fault model dictionary gives all fault model parasitic values taken from nodes Q, QB, BL, BLB, WL,

VDD, and VSS. These variations are further compared with fault free. At which node the fault is imposed that corresponding node parasitics are affected in particular with high parasitic R, C variation?

## 4.2 Fault Detection Using Parasitic R, C Method for Open Faults

Table.8 shows the R, C values of the different fault models, modeled by open faults at each node.

Table 8
Variation of parasitic R, C values for SRAM open defect model

| Node | Fault Free | | NAF (BL-M5S) | | URF (WL- M6G) | | TF (Q-M3G) | | UWF (M1G_M2G) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | C(fF) | R(Ω) | C(fF) | R(Ω) | C(fF) | R(Ω) | C(fF) | R(Ω) | C(fF) | R(Ω) |
| Q | 1.7 | 800 | 1.80 | 805 | 1.80 | 813 | 1.60 | 527 | 1.70 | 803 |
| QB | 1.5 | 498 | 1.50 | 498 | 1.50 | 498 | 1.50 | 498 | 1.30 | 239 |
| WL | 0.77 | 296 | 0.78 | 296 | 0.52 | 155 | 0.78 | 296 | 0.78 | 296 |
| BL | 0.626 | 71 | NA | NA | 0.63 | 71 | 0.63 | 71 | 0.63 | 71 |
| BLB | 0.815 | 91 | 0.82 | 91 | 0.82 | 91 | 0.82 | 91 | 0.82 | 91 |
| VDD | 0.31 | 13 | 0.31 | 13 | 0.31 | 13 | 0.31 | 13 | 0.31 | 13 |
| VSS | 0.31 | 13 | 0.31 | 13 | 0.31 | 13 | 0.31 | 13 | 0.31 | 13 |

The graphical representation of fault detection using the parasitic R, C extraction method for open faults is shown in Fig. 12 and Fig. 13. No Access Faults (NAF), arise when we open between the nodes BL and Source of the transistor $T_5$, whereas node BL absorbed. For open between node WL and gate of transistor $T_6$, causes the fault model Undefined Read Fault (URF), for this fault at node WL the parasitic R, and C values changed to 0.52fF, 155ohms respectively whereas the actual values are 0.77fF, 256 ohms respectively. The explanation is valid and holds for all other faults also.

Table 9
Complete Fault Model Dictionary using 7nm Technology for SRAM open defects

| S.No | Open Defect | Node Q | | Node QB | | Node WL | | Node BL | | Node BLB | | Node VDD | | Node VSS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Ideal C = 1.700aF, R = 800Ω | | Ideal C = 1500aF, R = 498 Ω | | Ideal C = 776aF, R = 296Ω | | Ideal C = 626aF, R = 71Ω | | Ideal C = 815aF, R = 91Ω | | Ideal C = 313aF, R = 13Ω | | Ideal C = 313aF, R = 13Ω | |
| | | C in fF | R in Ω | C in fF | R in Ω | C in fF | R in Ω | C in fF | R in Ω | C in fF | R in Ω | C in fF | R in Ω | C in fF | R in Ω |
| 1 | BL-M5S | 1.80 | 805 | 1.50 | 498 | 0.78 | 296 | NA | NA | 0.77 | 87 | 0.31 | 13 | 0.31 | 13 |
| 2 | WL- M5G | 1.80 | 813 | 1.50 | 498 | 0.60 | 159 | 0.60 | 70 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 3 | WL- M6G | 1.80 | 813 | 1.50 | 498 | 0.52 | 155 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 4 | Q-M1D | 1.40 | 682 | 1.50 | 498 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 5 | Q-M2D | 1.50 | 755 | 1.50 | 498 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 6 | Q-M1DM2D | 0.68 | 80 | 1.50 | 498 | 0.73 | 293 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 7 | Q-M3G | 1.60 | 527 | 1.50 | 498 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 8 | Q- M4G | 1.60 | 551 | 1.50 | 498 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 9 | Q-M3GM4G | 1.30 | 257 | 1.50 | 498 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 10 | VDD-M1S | 1.70 | 711 | 1.60 | 511 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 11 | VDD-M3S | 1.80 | 813 | 1.60 | 511 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 12 | VDD-M1SM3S | 1.70 | 711 | 1.60 | 511 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 13 | VSS-M2S | 1.70 | 800 | 1.60 | 511 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 14 | VSS-M4S | 1.70 | 800 | 1.60 | 511 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 15 | VSS-M2SM4S | 1.80 | 813 | 1.60 | 511 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 16 | QB - M3D | 1.80 | 813 | 1.20 | 392 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 17 | QB - M4D | 1.80 | 813 | 1.30 | 444 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 18 | QB_M3DM4D | 1.70 | 803 | 0.70 | 75 | 0.78 | 296 | 0.60 | 70 | 0.77 | 87 | 0.31 | 13 | 0.31 | 13 |
| 19 | QB_M1G | 1.60 | 793 | 1.50 | 375 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 20 | QB_M2G | 1.80 | 813 | 1.40 | 362 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 21 | QB_M1GM2G | 1.70 | 803 | 1.30 | 239 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 22 | M1G_M2G | 1.60 | 793 | 1.30 | 239 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 23 | M3G_M4G | 1.30 | 257 | 1.50 | 498 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 24 | BLB - M6S | 1.80 | 805 | 1.50 | 498 | 0.78 | 296 | 0.63 | 71 | 0.82 | 91 | 0.31 | 13 | 0.31 | 13 |
| 25 | WL-M5GM6G | 1.80 | 813 | 1.50 | 498 | NA | NA | 0.60 | 70 | 0.77 | 87 | 0.31 | 13 | 0.31 | 13 |

## 5. Conclusion

Fault, fault model, and fault coverage with minimal test latency against the technology variation are the three major concerns of the testing embedded SRAM. In this paper, we implemented a new test technique for embedded SRAMs using a parasitic extraction

method for obtaining maximum defect coverage for short and open defects. Using three levels of technologies 45nm, 32nm, and 7 nm, the fault models are developed the overall fault models developed using all the technologies are 72 for short defects and 75 for open defects as shown in Table 2 and Table 3 respectively. Using the proposed method we found existing fault models such as SAF, UWF, URF, TF, NAF, etc., along with an undetectable fault named an Undefined Short Fault. To implement this we used Microwind 3.9 simulation tool. The proposed parasitic test technique provides 100% fault coverage for static and dynamic faults including a few undetectable faults for single-cell SRAM. At the same time, the test method provides a fault dictionary at each technology level under consideration. Based on this fault dictionary, identifies equivalent faults and unique faults at each technology with 100% fault coverage, which cannot be seen with other existing techniques.

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## Figures

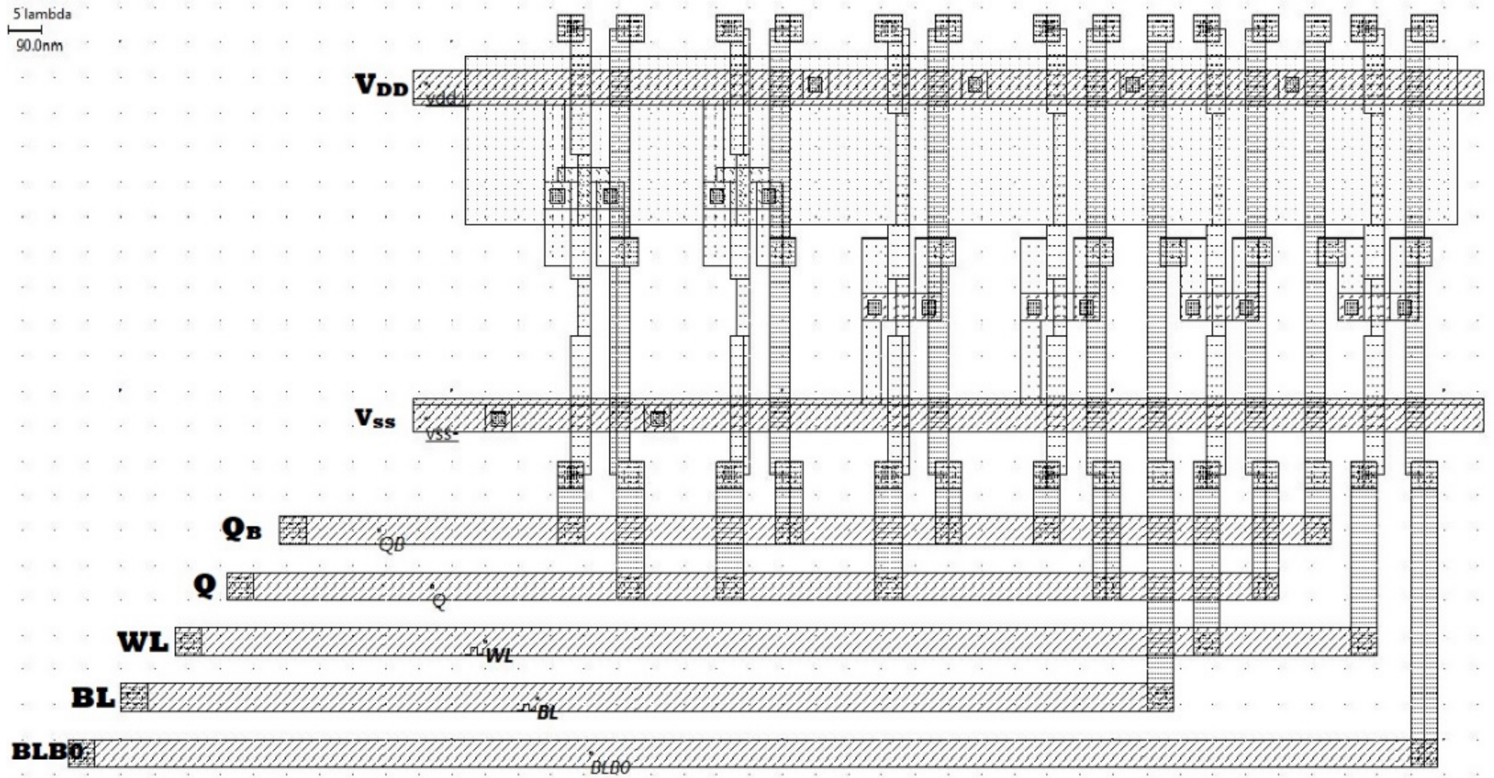


**Figure 1**

Layout Diagram of 6T SRAM

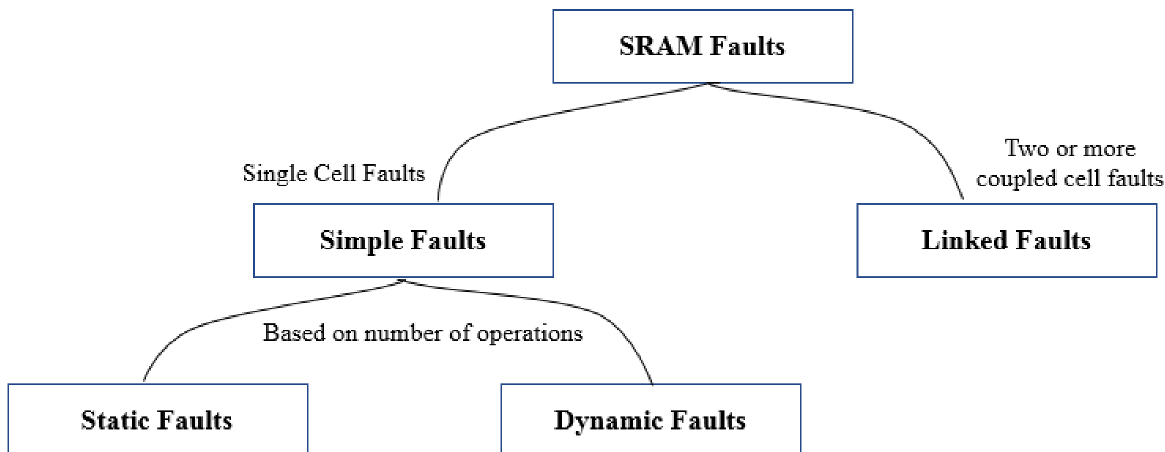


**Figure 2**

Fault hierarchy in SRAM cell

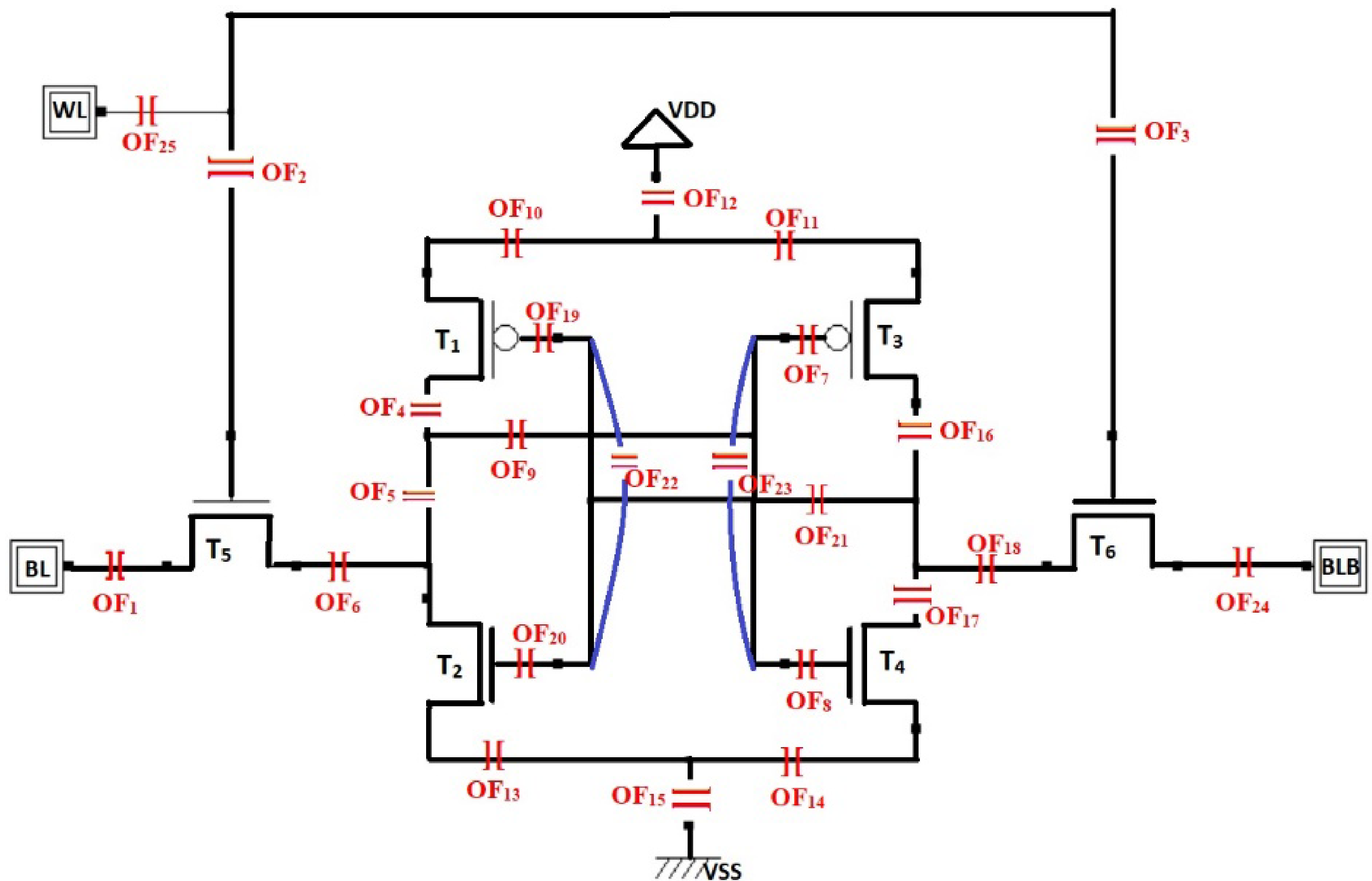


**Figure 3**

6T-SRAM Cell fault model for Open Faults

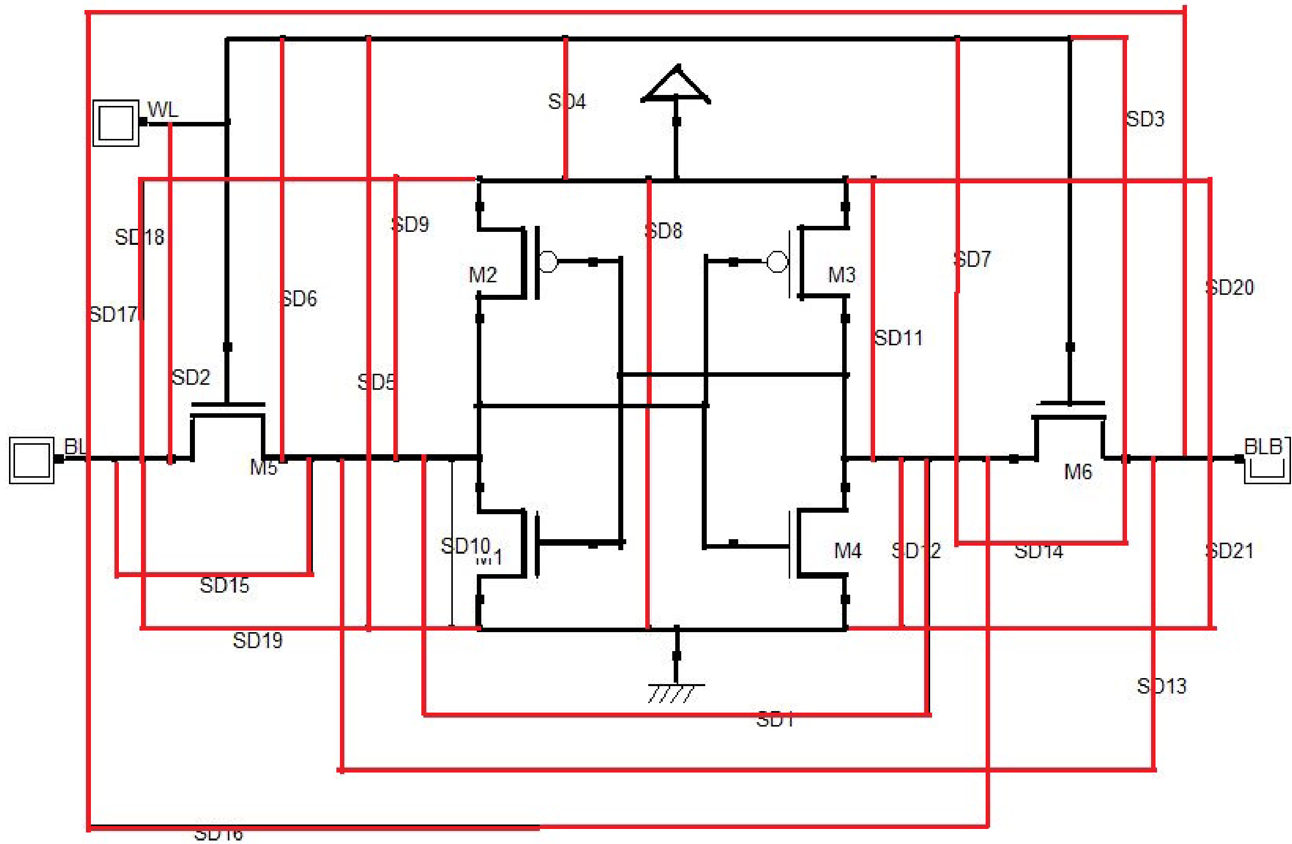


**Figure 4**

6T-SRAM Cell fault model for Short Faults

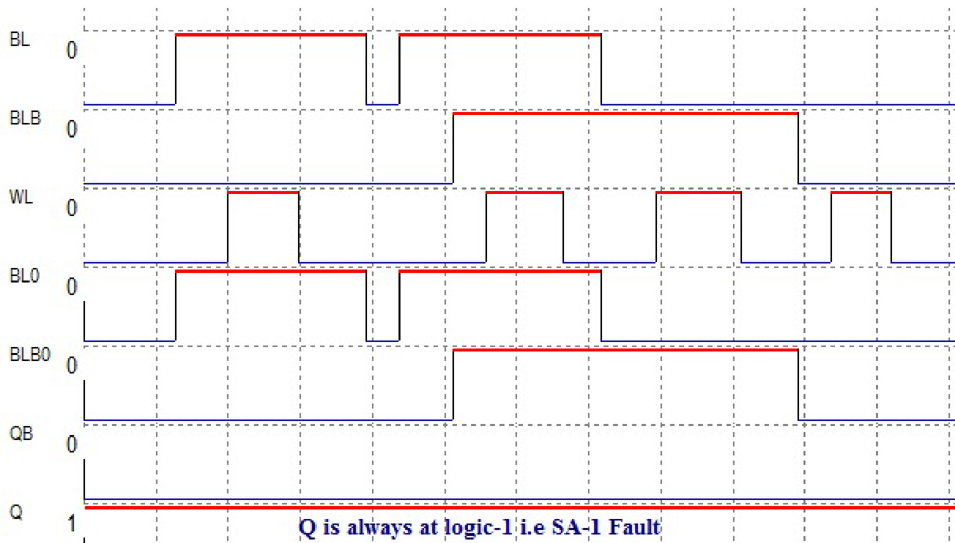


**Figure 5**

simulation results for SA-0 Faults

**Figure 6**

simulation results for SA-1 Faults

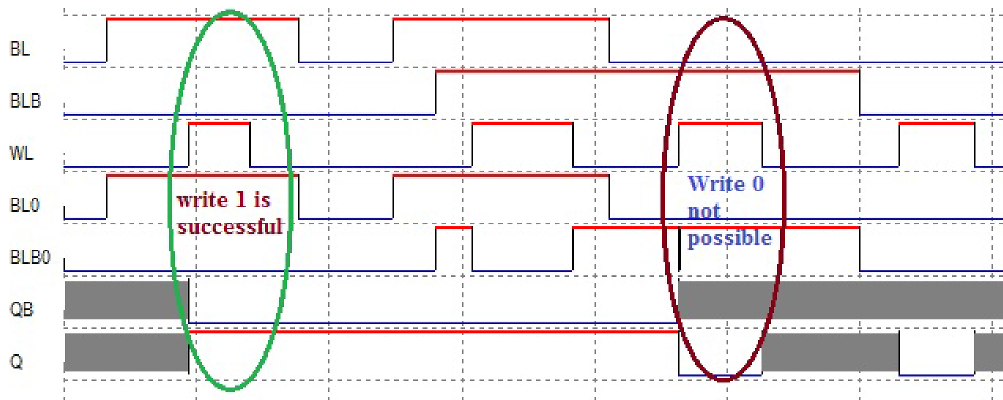


**Figure 7**

Simulation results for TF

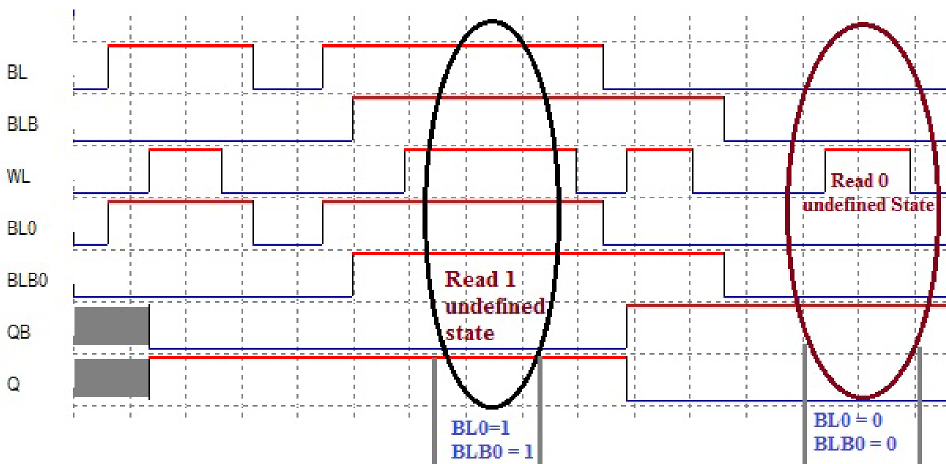


**Figure 8**

Simulation results for URF

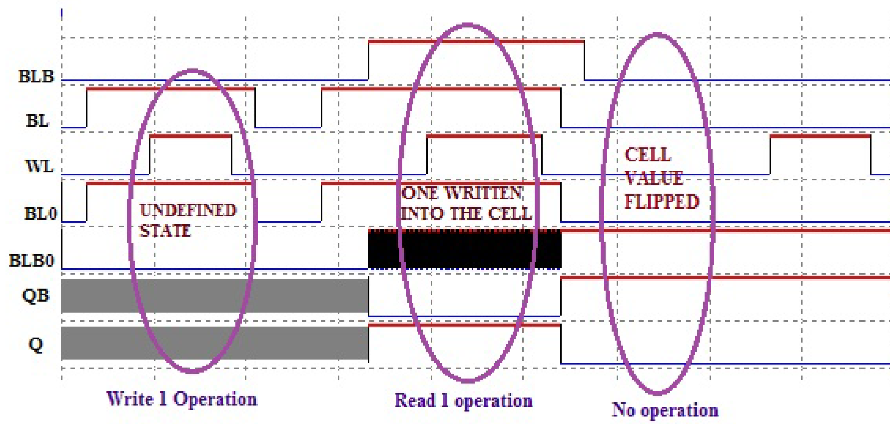


**Figure 9**

Undefined Short Fault at nodes WL-BLB

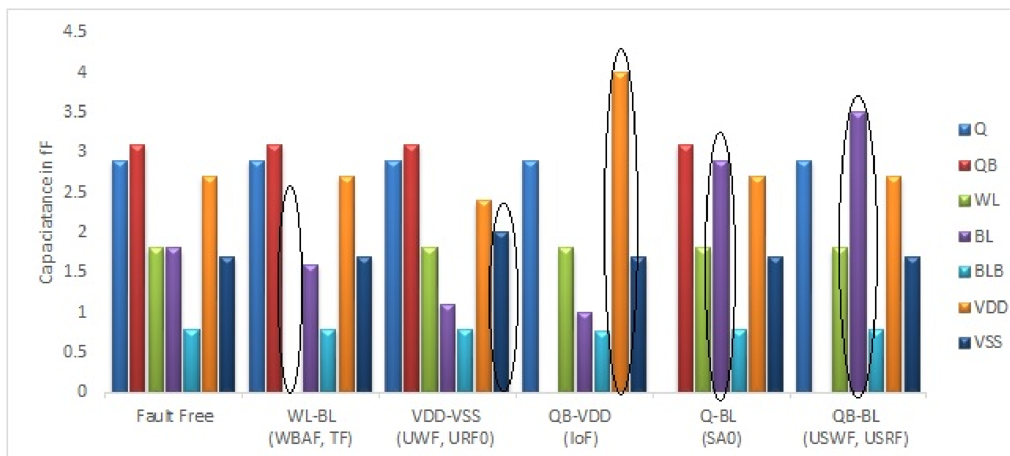


**Figure 10**

Fault detection based on parasitic capacitance variation for short defects

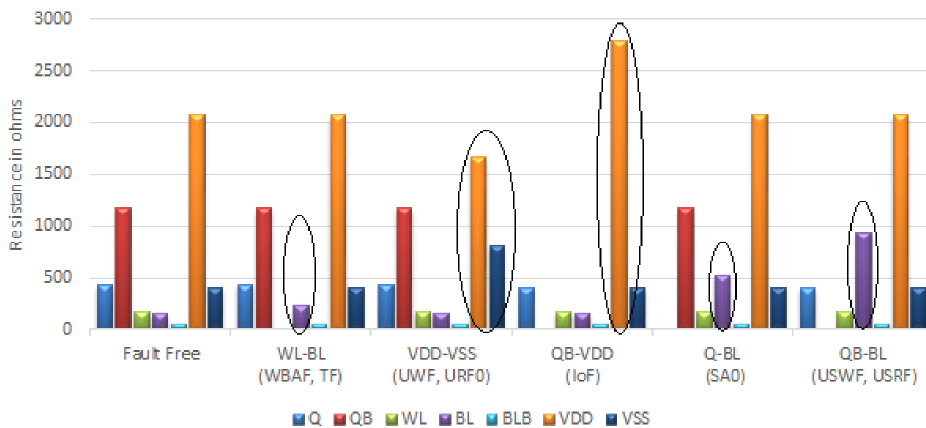


**Figure 11**

Fault detection based on parasitic resistance variation for short faults

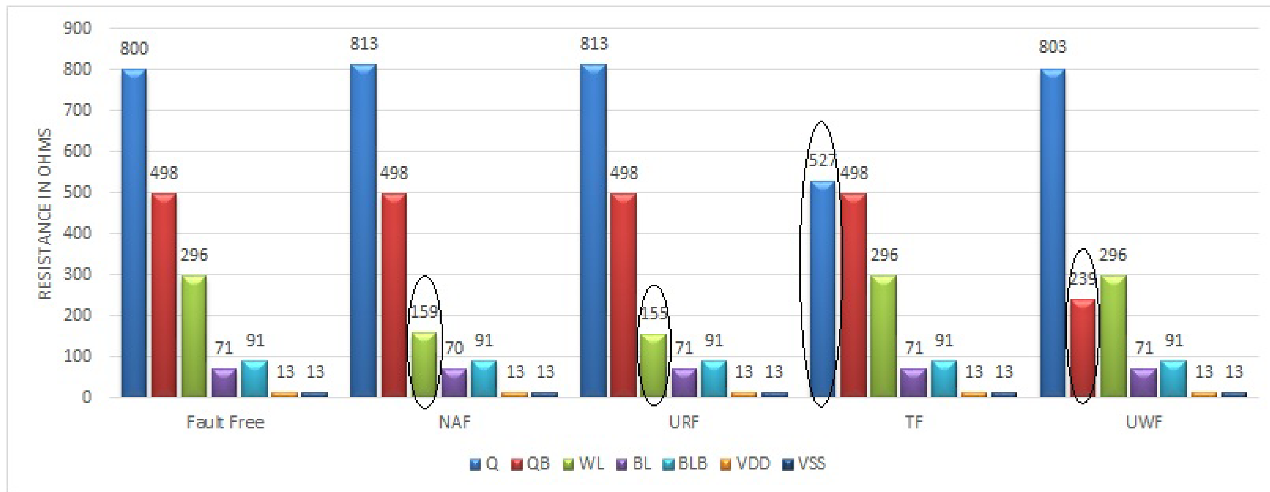


**Figure 12**

Fault detection based on parasitic resistance variation for open defects

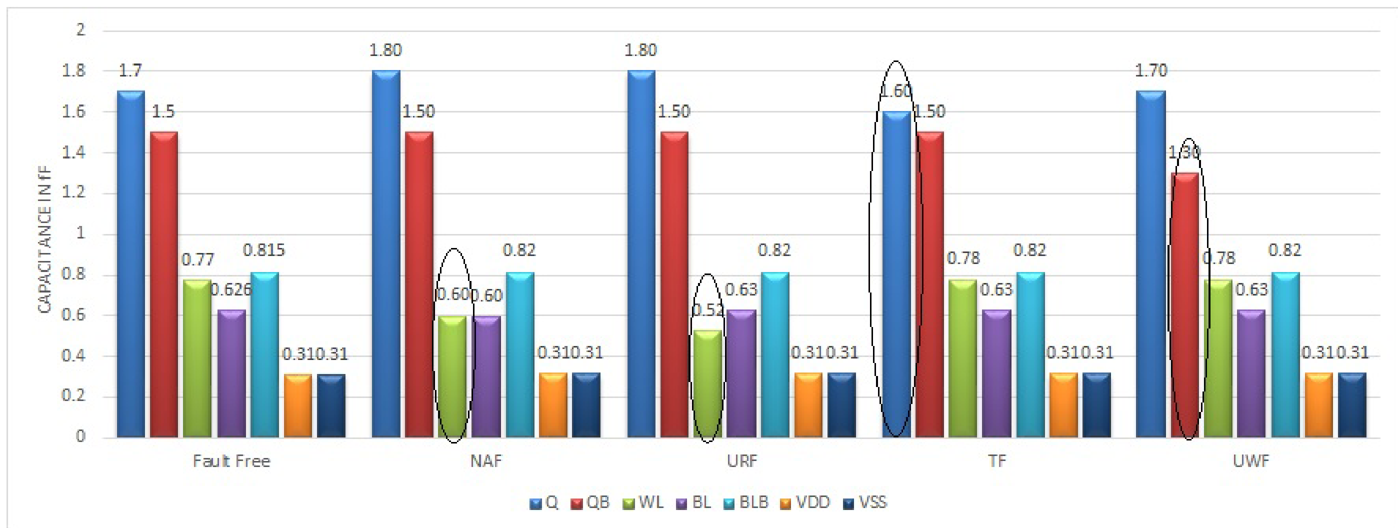


**Figure 13**

Fault detection based on parasitic capacitance variation for open defects

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