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Influence of Back Contact Annealing temperature in the mc-Si solar cell Fabrication Process

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Abstract:

The boron doped multi-crystalline silicon (mc-Si) ingot was grown using the directional solidification process. Grown ingots were converted into bricks and then to wafers. We have fabricated silicon solar cells from the multi-crystalline silicon wafers. The minority carrier lifetime of the wafers is around 15-25 μ s. Annealing was made after back and front contact during the fabrication process. The effect of back contact annealing temperature has been investigated. Annealing the device at 583⁰C for 5 sec gives better results. Typical open circuit voltage (V_{oc}) of the devices is around ~540-550mV. The best cell had a power conversion efficiency of ~9 % with a typical acceptor doping density ~ 2.35 E+15 per cm³ (The devices reported here do not have AR coating layer, no passivation was done and the surfaces are also not textured).

Keywords: Directional Solidification Process, Multi crystalline Silicon solar cell.

1. INTRODUCTION

For normal growth of this technological word, energy conversion is very crucial. Among the renewable energy sources, eco-friendly solar cells technology is most important one. In this photovoltaic (PV) market 95 % is occupied by the crystalline silicon (c-Si) solar cells. In the c-Si market mc-Si solar cells occupies 62 % due to low cost and high efficiency. 70 % of global module production is by China and Taiwan. Development of mc-Si solar cells is very important due to the lower material cost (20 to 30 %) than mono-crystalline silicon [1]. Normally mc-Si ingot is grown by the directional solidification (DS) process because of low cost, mass production and simple operating process compared to other mass production method like Czochralski (Cz) growth process. We have grown mc-Si ingot by using the DS process. The grown ingots (Fig.1b) are converted to brick (Fig.1c) then to wafers (Fig.1d). Prepared wafers are subjected to cell making. During the cell making the metallization is crucial one, because it affects the solar cell's efficiency. Currently many researchers are attempting optimization of

metallisation. Low-cost and low-temperature chemical oxide passivation process was investigated by Yadav et al, thus improving the conversion efficiency by 0.3 % [2]. Meili Cui et al reduced Fe concentration and improved lifetime by the low temperature annealing process after the diffusion [3]. C Chan analysed the post-firing thermal process on PERC solar cells [4]. Ana Peral et al studied the Impact of Extended Contact Cofiring on multicrystalline Silicon Solar Cell [5]. Catherine E. Chan et al investigated the suppression of Carrier induced degradation of PERC mc-Si solar cells [6]. Shiliang Wu et al investigated the electrical properties of mc-Si solar cell by the different front contact firing [7]. Extended co-firing was done by Ana Peral et al [8]. For all type of solar cell making optimization of the Series and Shunt resistance is needed. In this work we investigate on the influence of back contact annealing temperature and time. During the device fabrication process we vary the back contact annealing temperature and find out the suitable annealing temperature. Fabricated solar cells are characterized by IV, QE and Capacitance measurements.

Directional Solidification Process:

We have grown mc-Si ingot by using the DS process. The DS furnace is shown in Fig.1a. In this (DS) process there are five steps: First step is heating the furnace, before heating the furnace the feed stock materials are loaded in the quartz crucible. Second step is melting; furnace is heated above the silicon melting point. After melting silicon feed stock materials, furnace is maintained for a few hours for homogenisation of molten silicon. Third step is crystallization, after the melting, furnace temperature is reduced for crystallization of molten silicon. Fourth step is annealing process; mc-Si ingot is annealed at suitable temperature for a particular time. Then finally (Fifth step) the furnace is cooled. Harvested ingots are converted to brick and bricks are converted to wafer. The wafer size is 34 mm* 34 mm, thickness of the wafer is 300 micron. Initially our wafers are subjected to lifetime measurement, after the cleaning process, the life time of the wafers is 15 and 25 micro sec.

FIGURE 1a. Directional Solidification Furnace

FIGURE 1b. As-grown Multi-crystalline Silicon

FIGURE 1c. As-Cut Brick from the

FIGURE 1d. Multi-Crystalline silicon wafer

2. FABRICATION PROCESS STEPS

We have done metallization by using the thermal evaporator system. After the metallization we have annealed following two step annealing process, first annealing is after the back contact and second annealing is after the front contact. Both annealing process is done in nitrogen atmosphere by the RTP system.

2.1 Saw Damage Removal (SDR) Etching

The as cut wafers are very rough. Using a solution of NaOCl, KOH and H₂O the samples were etched for 15 min at 80 degree Celsius in an effort to reduce the roughness caused by the slicing of the wafers. Etching rate of this SDR etching is 1.4 micro metre per min. After the SDR etching process the thickness of that sample was calculated by using the mass difference method. The amount of material removed is roughly 20 micrometre. After the SDR etching the samples are cleaned by the RCA1 and RCA2 cleaning process. Before starting the fabrication of solar cells using the silicon wafers, all the organic and ionic impurity present on the surface of the wafers was removed.

2.2 First Oxidation

The oxidation was done by using the oxidation furnace. This oxidation protects the back surface during the n⁺ diffusion. This process was done for 4 hr at 1050° C with 1slpm O₂ gas flow. The oxide thickness is around 200nm. After the oxidation process SiO₂ is removed from one side by using the HF etching. The oxide is removed from the side where we will do the diffusion. During the etching process we used Dilute HF solution [1(HF): 10(DI water)].

2.3 Diffusion Process

Diffusion process is done to make a P-N junction. The N layer formed on the top of the P wafer for P-N junction formation is done by using phosphorus solid source. This process was done for 15 min at 875°C. Before the diffusion, phosphorus sources are activated at 925°C for 8 hours. During the diffusion and activation 1 slpm nitrogen gas flow is maintained. The thickness of the N-layer formed is 600 nm. After the diffusion, wafers are immersed in a 2% HF solution to remove the oxides formed on the wafer during diffusion. The side which is diffused (we call it front side) will form a P₂O₅ and back is having the oxide grown in first oxidation process.

2.4 Second Oxidation

This oxidation is done for masking lithography process. Oxidation was done by using the oxidation furnace. Process is done for 2 hr at 700 °C. During the oxidation oxygen was admitted at 1 slpm. Approximate thickness of the oxide layer formed is 20 nm.

2.5 Lithography

The lithography is done to make small mesas of area $1.1 \times 1.1 \text{ cm}^2$ and $0.49 \times 0.49 \text{ cm}^2$ on the single wafer. The lithography setup and patterned mc-Si wafer are shown in Fig.2.

(a)

(b)

FIGURE 2 Lithography (a) Lithography setup (b) Patterned mc-Si wafer

2.6 Metallization

Metallization is the end process of solar cell fabrication process. We have made back and front side contacts in the vacuum evaporation deposition system. The annealing of the contacts is done in the Rapid thermal Process system.

2.7 Back side contact

By using the vacuum system we deposited Al on the back of the wafer. During the back contact edges are prevented from getting deposited by covering them with the mica sheet. Fig.3a. shows the mc-Si wafer after the back side contact. After the back contact wafers are

annealed by using the RTP system. Our samples are subjected to different back contact annealing, the details are listed in the Table.1.

Table.1 Back contact annealing details.

	Sample Name	Annealing Temperature and Time (Nitrogen atmosphere)
Set 1	A	590 C 5 min
	B	600 C 5 min
Set 2	C	590 C 5 min twice
	D	600 C 5 min twice
Set 3	E	610 C 5 min then 575 C 5 min
Set 4	F	583 C 5 sec
	G	594 C 5 sec

2.8 Front side contact

The vacuum system is used to make as stack of Ti and Ag on the Top of the wafer inside the MESA's. The front contact deposition is done through a mask (Compatible to the Lithography mask) which will allow deposition through it such that bus bar and Fingers are deposited on it (Fig. 3b). Fig.3c shows the mc-Si wafer after the front side contact. After the front contacts are made the sample is annealed by using the RTP system. Our sample is annealed at 285° C for 20 sec.

(a)

(b)

(c)

FIGURE 3 Front contact (a) mc-Si wafer after the Front side contact (b) Metal mask (c) mc-Si wafer after the Back side contact

3 RESULT AND DISCUSSION

During the device fabrication, after the back contact and after the front contact, annealing process is very crucial. Annealing temperature, time period and ramp up time influence the metallization part diffusing from one side to another side through the grain boundary of the mc-Si wafer. The details of the back contact annealing temperature are listed in table.1. After the metallization our devices are subjected to dark and light IV measurement.

FIGURE 4 Dark IV curve of various annealing experiments. A, B, C, D, E, F and G are corresponding to 590⁰ C 5 min, 600⁰ C 5 min, 590⁰ C 5 min two times, 600⁰ C 5 min two times, 610⁰ C then 575⁰ C 5 min, 583⁰ C 5 sec and 594⁰ C 5 sec.

Fig 4. shows the semi log graph of dark IV curve of various annealing experiments, in each experiment five devices were tested. The area of 1 and 2 is 1.21 cm² and 3, 4 and 5 is 0.49 cm². The mc-Si wafers were subjected to four set of back contact annealing experiments, the details are listed in the table 1. In first set of experiment the leakage current of Case A is in the range of 10⁻⁶ to 10⁻⁴ A and for Case B it is from 10⁻⁵ to 10⁻³ A. In second set of experiment the leakage current of Case C is in the range of 10⁻⁵ to 10⁻³ A and for Case D it is from 10⁻⁴ to 10⁻³ A. In third set of experiment the leakage current of Case E is in the range of 10⁻⁴ to 10⁻² A. And in the fourth set of experiment the leakage current of Case F is in the range of 10⁻⁸ to 10⁻⁴ A and for Case G it is from 10⁻⁵ to 10⁻² A. In all the sets of experiments the leakage current is higher for higher annealing temperature. This is because of metal part diffused to the opposite side, that it acts as pipe line from one side to another side. The better leakage current was obtained in case F. In case F the leakage current is in the range of 10⁻⁸ to 10⁻⁴ A. If we increase the

temperature or time, the metal parts would be diffused through the grain boundary of the mc-Si. The shunt resistance of fabricated devices is listed in the table 2. In all the sets of experiments the shunt resistance is higher in the lower annealing temperature cases. In those experiments Al spike opposite side through the grain boundary. The maximum shunt resistance is case F in the order of 10^7 ohm range. We calculated the shunt resistance from the normal dark IV curve, it is listed in table 2.

Table 2. Shunt Resistance [in ohm]

Device Number	A	B	C	D	E	F	G
1	3.20E+06	6.63E+03	3.33E+03	3.33E+02	5.00E+02	4.00E+04	1.04E+04
2	4.00E+04	4.76E+00	1.25E+03	3.57E+03	2.00E+02	1.25E+03	7.00E+02
3	2.00E+03	2.63E+03	1.59E+03	1.25E+04	7.41E+01	1.03E+07	1.79E+02
4	2.38E+04	8.25E+04	7.14E+03	7.25E+02	1.85E+03	3.77E+05	3.57E+02
5	7.05E+05	3.33E+03	9.52E+03	5.85E+02	3.12E+02	3.00E+04	7.14E+03

FIGURE 5 Light IV curve of various annealing experiments. A, B, C, D, E, F and G are corresponding to 590⁰ C 5 min, 600⁰ C 5 min, 590⁰ C 5 min two times, 600⁰ C 5 min two times, 610⁰ C then 575⁰ C 5 min, 583⁰ C 5 sec and 594⁰ C 5 sec.

Light IV of the different annealing experiments was shown in fig.5. In each annealing experiments, we compared five devices. From the dark IV analysis we observed that shunt resistance is higher in the case F than other cases. The IV parameter of those curves is listed in table 3. Table 3A and 3B is comparing the Jsc and Voc of fabricated devices. From all the experiments the lower annealing experiments give better Jsc and Voc than other cases. Table

3C and 3D compares FF and conversion efficiency. In set 2 and Set 4 the lower annealing temperature gives better FF and conversion efficiency. Form these sets of analysis, the case F has given better Voc than other. The fill factor of case F is around 0.65 to 0.72 which is high compared to other cases and hence it leads to the higher efficiency. At higher temperature Al spiked to other side due to the over firing of wafer, it reduces the shunt resistance. Sticking of Al on wafer is very poor at lower temperature, it increases the series resistance. If we further do the series of systematic experiments we can get precise back contact annealing condition.

Table 3. IV Parameter

Table 3A. Jsc (A/cm²)

	A	B	C	D	E	F	G
1	13.39	13.39	13.22	9.75	17.19	15.21	15.04
2	11.65	15.21	16.94	11.90	13.64	16.03	14.21
3	12.69	12.90	17.55	12.37	14.57	17.82	13.88
4	10.78	20.18	17.94	16.90	21.43	25.51	18.43
5	21.02	14.10	14.43	18.06	16.63	23.67	18.22

Table 3B. Voc (mV)

	A	B	C	D	E	F	G
1	530	327	518	236	540	550	550
2	526	467	518	347	530	550	550
3	516	467	508	317	440	560	490
4	516	367	508	427	540	560	520
5	544	391	508	508	520	560	560

Table 3C. FF

	A	B	C	D	E	F	G
1	0.31	0.43	0.60	0.34	0.55	0.65	0.65
2	0.34	0.51	0.61	0.40	0.59	0.66	0.44
3	0.34	0.52	0.57	0.43	0.26	0.72	0.40
4	0.34	0.45	0.49	0.46	0.57	0.63	0.44
5	0.32	0.52	0.54	0.36	0.51	0.69	0.68

Table 3D. Efficiency

	A	B	C	D	E	F	G
1	2.20	1.90	4.10	0.77	5.17	5.46	5.46
2	2.10	3.62	5.36	1.65	4.29	5.89	3.52
3	2.19	3.15	5.03	1.66	1.69	7.24	2.75
4	1.89	3.35	4.41	3.33	6.62	9.07	4.27
5	3.66	2.93	3.93	3.30	4.42	9.23	6.97

3.1 Capacitance Measurement

After the device fabrication better efficiency devices are subjected to the capacitance measurement by using the LCR meter to find V_{bi} and N_A values of our wafers. The capacitance versus voltage graph is shown in Fig 6 and data listed on Table 4. In order to achieve $9.4E15$ atoms/cm³ acceptor concentration, 2.3 grams of heavily boron doped silicon wafer was added for 10 kg feed stock. The equation of the acceptor calculation (N_A) is follows:

$$\frac{A^2}{C^2} = \left(\frac{2}{q\epsilon\epsilon_0 N_A}\right) \left(\psi_{bi} - \frac{2kT}{q} - V\right)$$

$$\frac{1}{C^2} = \frac{-kV + k\left(\psi_{bi} - \frac{2kT}{q}\right)}{A^2}$$

Where

$$k = \left(\frac{2}{q\epsilon\epsilon_0 N_A}\right)$$

In the plot $1/C^2$ Versus V the slope value is K

$$N_A = \frac{2}{q\epsilon\epsilon_0 k}$$

Where

$$q = 1.6 \text{ E-19 C/F}$$

$$\epsilon\epsilon_0 = 1.062 \text{ E-10 F/m}$$

A is Area.

FIGURE 6 Capacitance Measurement

Table.4. Capacitance Measurement Details

Area	Sample Name	K	N _A (1/cm ³)	Mobility (cm ² /V S)
0.49	1	5.00E+15	2.35E+15	374.58
0.49	2	5.00E+15	2.35E+15	374.58

3.2 EQE Measurement

FIGURE 7 EQE Measurement

Fig 7 is EQE measurement of our device, We get 60 % efficiency. Because our devices are not subjected to the ARC during the device making.

4 CONCLUSION

The boron doped multi-crystalline silicon (mc-Si) ingot was grown using the directional solidification process. Grown ingots were converted into bricks and then to wafers. The investigation on the annealing temperature has been carried out. The mc-Si wafers were subjected to four set of back contact annealing experiments. Annealing the device at 583⁰C for 5 sec gives better results. Typical V_{oc} of the devices ~540-550mV. The best cell had a power conversion efficiency of ~9 % with a typical acceptor doping density ~ 2.35 E+15 per cm³. Our devices are not subjected to the texturization, ARC and passivation. If we include all process we get 17.6 % conversion efficiency [9].

Table.5. Expected Efficiency

Efficiency of our wafer (for FF=0.69)	9.23%
Expected Efficiency (If FF=0.80)	10.6%
Expected Efficiency with Passivation (4%)	11.01%
Expected Efficiency with ARC (24 %)	13.2%
Expected Efficiency with ARC and Passivation (55 %)	16.4%
Expected Efficiency with ARC, Passivation and Texturization (61 %)	17.1%

Declarations

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Conflicts of interest/Competing interests

The authors have no conflicts of interest to declare that are relevant to the content of this article.

Compliance with Ethical Standards

Not Applicable

Consent to participate

Not Applicable

Consent for Publication

Not Applicable

Availability of data and material

Not applicable.

Code availability

Not applicable.

Authors' contributions

Authors	Contribution
G. Aravindan	<i>Conceptualization, Methodology, Formal analysis, Investigation, Data Curation, Resources, Writing - Original Draft, Writing - Review & Editing</i>
S. Sanmugavel	<i>Methodology, Formal analysis, Investigation</i>
S. G. Nagarajan	<i>Investigation, Validation</i>
V. Kesavan	<i>Formal analysis</i>
M. Srinivasan	<i>Visualization</i>
P. Ramasamy	<i>Supervision</i>

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Figures

A

B

C

D

Figure 1

1a. Directional Solidification Furnace 1b. As-grown Multi-crystalline Silicon 1c. As-Cut Brick from the grown ingot 1d. Multi-Crystalline silicon wafer

(a)

(b)

Figure 2

Lithography (a) Lithography setup (b) Patterned mc-Si wafer

(a)

(b)

(c)

Figure 3

Front contact (a) mc-Si wafer after the Front side contact (b) Metal mask (c) mc-Si wafer after the Back side contact

Figure 4

Dark IV curve of various annealing experiments. A, B, C, D, E, F and G are corresponding to 590-0 C 5 min, 6000 C 5 min, 5900 C 5 min two times, 6000 C 5 min two times, 6100 C then 5750 C 5 min, 5830 C 5 sec and 5940 C 5 sec.

Figure 5

Light IV curve of various annealing experiments. A, B, C, D, E, F and G are corresponding to 590-0 C 5 min, 6000 C 5 min, 5900 C 5 min two times, 6000 C 5 min two times, 6100 C then 5750 C 5 min, 5830 C 5 sec and 5940 C 5 sec.

Figure 6

Capacitance Measurement

Figure 7

EQE Measurement