Highly Accurate Memristor Modelling Using Mos Transistor for Analog Applications

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Research Article

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HIGHLY ACCURATE MEMRISTOR MODELLING USING MOS TRANSISTOR FOR ANALOG APPLICATIONS

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Abstract: Memristor technology has grown at a breakneck pace over the last decade, with the promise to transform data processing and storage. A memristor is a non-linear electrical component with two terminals that connects electric charge and magnetic flux. The ability to store and process data in the same physical location is a fundamental benefit of memristors over traditional electrical components. It has a unique feature in that its resistance may be preset (resistor function) and then saved (memory function). Memristors, unlike other types of memory used in modern electronics, are stable and retain their state even if the device is turned off. In this work, a new highly accurate asymmetrical memristor is proposed for highly efficient analog applications. The proposed work used 5 Complementary metal-oxide-semiconductor (CMOS) devices in a parallel and series-connected manner. A bypass transistor is used to control the current flow between two terminals to perform a stable operation. A differential amplifier circuit is used to validate the proposed memristor performance. The proposed work is implemented using TSMC 45nm CMOS technology. This application consumes less power and has good performance when compared with conventional techniques. In this work, a 1V power supply occupies a 67.5 µm2 layout area. The experimental results are improved when compared with the existing circuit.

Keywords: - Memristor, Analog devices, magnetic flux, MOS Transistor, Complementary metal-oxide-semiconductor (CMOS), magnetic flux

I. INTRODUCTION

Memristors are an intriguing possibility for the construction of low-power circuits. Memory and resistor are the two terms that were combined to create the word memristor. It's a

passive component, similar to the resistor, inductor, and capacitor, which are key devices for describing voltage and current, flux and current, and voltage and charge, respectively. In 1971, Leon Chua first demonstrated a memristor to the general audience. It was initially introduced as a component and is considered the fourth fundamental passive device that represents the link between charge and flux [1].

The innovative new gadget consists of two terminal resistive components and a non-volatile memory that can store data despite its minimal space utilisation. The memory can do this by adjusting its resistance depending on the circumstances. Because of this device's one-of-a-kind behaviour, it is attractive not only for the design of memories but also for a wide variety of other applications, including analogue circuit design, signal processing, neural network design, and logic design, in addition to all other applications that use memristors. A bold move toward the development of future VLSI technology is represented by the logic architecture based on memristors. A memory resistor is all that a memristor is and nothing more. It is a passive device with two terminals that is non-ohmic and non-linear in nature. Even though it does not reproduce the functions of a resistor, an inductor, or a capacitor due to the inherent properties that it has, the memristor can keep its internal state of resistance (also known as memristance) even after the power is turned off. When a voltage is placed across a memristor, the total memristance will change according to the polarity of the voltage [2]. This will cause the total memristance to either raise or decrease. Titanium dioxide (TiO2) thin film was used to create the first-ever physical model of a memristor in 2008 by Hewlett-Packard laboratories, which did this by placing the film between two electrodes made of platinum (Pt). Conventional CMOS-based technologies are now confronted with several design issues, the most significant of which are the constant scaling down of the minimum feature size following Moore's law, latency, and power consumption. The fact that technologies based on memristors can address these issues is one of the primary reasons why researchers have shown such an interest in them. Memristors are widely used in a variety of applications, such as the neuromorphic system. After all, it functions in a manner analogous to a synapse and non-volatile memory because it maintains their data integrity even after the power is turned off. The use of the memristor in logical calculations is one of the possible applications that may be found for it [3].

Memory and neuromorphic application are both present in memristors' characteristic behaviour. Memory apps make excellent use of it since it does not lose data when the power is turned off and it takes up a very tiny amount of space. In addition to this, it has a resistance that can be adjusted, as well as features of pulse-based operation for neuromorphic applications. These characteristics make it perfect for modifying the synaptic weights of neuromorphic cells. Lastly, it has a pulse-based operation. With the technology that we have today, it is challenging to fabricate memristors, even though they are excellent for memory applications. As a result, the emulators of memristor would be a suitable replacement for the design of application circuits. Integration of numerous memristor crossbar arrays is often required to realise a memristor-based neuromorphic computing system that is both feasible and useful. In general, separating the weights into many arrays is advantageous for parallel computing, which is becoming an increasingly necessary technique as the sizes of networks continue to grow. However, past demonstrations of memristors depended on a single array since it was difficult to produce highly reproducible arrays. This was

the primary reason for this limitation. It is generally agreed that the unpredictability and other less-than-ideal properties of memristive devices provide significant challenges to the implementation of neuromorphic computing [4-5].

In order to construct integrated memristor-based chaotic circuits that are both more practical and sophisticated, a completely integrated memristor emulator as well as a scroll-controllable hyperchaotic system have been described and proven [6-8]. These advancements have allowed for the construction of integrated memristor-based chaotic circuits that are both more practical and sophisticated. The results of the post-layout simulations performed by the Cadence The completely integrated memristor and memristor-based scroll-controllable hyperchaotic system reported all possible and reachable, according to IC Design Tools, and the fully integrated technique will further advance the practical uses of chaotic circuits and systems [9-12]. The findings of these simulations show that the fully integrated strategy will help chaotic circuits and systems find more practical applications. Memristor-CMOS methods combine nanoscale memristor devices with CMOS at the back end of the line (BEOL), allowing them to avoid some of the issues that have previously been noted. To begin, there is an increase in the amount of space that is utilised since the memristor fabric is embedded vertically rather than outwardly. This is because vertical embedding uses more room. Other types of non-volatile memory, like Flash, make use of floating gates, which take up space on the silicon. Now that the combination of memristors and CMOS is accessible in commercial processes (for example, the TSMC 40 nm RRAM-process), [13-14].

In this work, a new circuit is proposed to perform memristor operation using digital CMOS devices. The proposed memristor circuit used 5CMOS devices in which one CMOS acts as a bypass current control device for both legs of the memristor. This circuit is flexible and stable for memristor operation for digital and analog-related signal processing-related applications. TSMC45nm technology library is used to model the memristor circuit. This paper is organized as follows: Section II presents a survey the literature survey, in section III, found the detailed explanation of the proposed method. Section IV presents results and discussion. Finally, section V concludes this work.

II. LITERATURE SURVEY

Previously various circuits were proposed to perform memristor operations. The authors used FET, MOS and transistors to implement the memristor circuits. Some of the previous techniques proposed to perform memristor implementation are discussed below:

Fatih Gul proposed a model for a MOS-based circuit that simulates the behaviour of a TiO2 memristor to begin, a TiO2-based memristor device with a thickness of 10 nm for the active layer was built. The verification of the structural properties of the equipment was made possible by the use of energy dispersive X-ray spectroscopy. By delivering a time-dependent voltage, the memristive properties of the device were brought to light and resolved. To produce the conventional memristive loops of pinched hysteresis by analysing the current-voltage relationships. After the device had been physically built and characterised, a circuit model was created utilising just four MOS transistors to imitate the produced TiO2 memristor. This was done

after the physical construction of the device. The suggested circuit model is not only capable of simulating the produced memristor, but it is also applicable to generic applications that are based on memristors. To attain memristive features, the circuit did not use any active elements or circuit blocks in any way. Both the simulation and the experiment provide outcomes that are consistent with one another. When compared to the circuits that were shown in earlier research that was published in the literature, this one is straightforward, and it was successful in imitating the created memristor. TSMC CMOS process parameters at 180 nm were used throughout every simulation that was run [15].

Liao proposed the affective associative memory neural network's memristor-based circuit is meant to accomplish progressive changes in emotional intensity, and the gradual learning, forgetting, and transferring of emotions is proposed. The frequency of neuronal activity in the circuit that was built is highly associated with the degree of emotional arousal that a person is experiencing. When there is a higher frequency of firing in the output neurons, there is a greater degree of emotional intensity. According to the associative memory rule, the dynamical change in synaptic weights causes a progressive fluctuation in the frequency of output neurons. This variation is caused by the associative memory rule. As a result, the function of changing emotional intensity may be brought to fruition, and slow processes can be brought about. The results of the PSPICE simulation are shown to demonstrate that the suggested circuit is capable of gradually achieving the functions of emotional learning, forgetting, and transferring [16].

Peng proposed Photoelectric memristor device. This study constructed a simulation model of a photoelectric-motivated memristor and activated its memristive properties. The simulation shows that the gadget goes from not triggered to activated to not triggered. The current and voltage curves then fit within this instrument's hysteresis loop. This test on a genuine photoelectrically-motivated memristor helps confirm this test's findings. Because of the memristive features of this device, it may be employed to examine the memristor circuit merged with an avalanche photodiode and a signal processing circuit. Additionally, it may be employed in neural networks and as a novel form of photoelectric memory [17]. Pershin et al. proposed the built logic circuit uses two volatile memristors to accomplish four logic operations. We also record the current-voltage characteristics of each emulator and find self-sustaining oscillations in a resistor-volatile memristor circuit. Because of its ease of use, its striking resemblance in response to volatile memristors, and its relatively cheap cost, the recently created emulator presents an excellent opportunity for research into memristive circuits [18].

Valeri and Stoyan proposed to achieve this purpose, a combination of Biolek and sinusoidal window functions are utilised to create a unique memristor model with highly nonlinear ionic drift suitable for computer simulations of titanium dioxide memristors across a broad voltage range. The new memristor model is based on the GBCM Model and the Biolek Model, but it has a greater degree of nonlinearity of the ionic drift due to the addition of a weighted sinusoidal window function. Biolek made both models. The Pickett memristor model is compared to the modified model in this article. The modified Biolek model's fundamental links are then made compatible with the Pickett model. After performing several simulations, observed that new model's behaviour

is equal to that of the realistic Pickett model. However, unlike the Pickett model, the model does not have convergence difficulties, therefore it is suitable for computer simulations [19].

Mohammed et al. proposed two versatile discrete and continuous memristor models with their FPGA implementations. These models can produce a variety of pinched hysteric behaviours, including multi-state switching behaviour, symmetric pinched hysteresis, and asymmetric pinched hysteresis. In order to demonstrate the memristive behaviour, the closed form expression for the enclosed region is also derived. This implementation was successfully generated and tested on a Xilinx Nexys4 FPGA running at up to 231 MHz with less than 1% usage. An empirically validated digital implementation of the memrisitive-Chua chaotic circuit is used to evaluate the proposed cores' functionality [20].

S. C. Yener et al. proposed construction of a completely CMOS chaotic circuit using just a DDCC-based memristor and inductance simulator as its components. These active blocks make up our design, which is built using CMOS technology with a 0.18-micron production node and symmetric supply voltages of 1.25 volts. As the inductance simulator, a brand novel topology based on a single DDCC+ circuit is used. The results of the simulation demonstrate that the suggested design is capable of satisfying both the memristor features and the chaotic behaviour of the circuit. The results of the simulations that were carried out demonstrate the viability of the suggested design for the implementation of CMOS-based chaotic applications [21].

Ayten et al. proposed for brand new analogue memristor emulator circuits that are based on current backward transconductance amplifier (CBTA) and passive parts. Simply switching around the CBTA output terminals allows them to simulate both incremental and decremental memristors. It merely makes use of a single CBTA, two resistors, a single capacitor, and a single multiplier in order to emulate a grounded memristor. In comparison to previously constructed emulator circuits, they have a lower number of CMOS transistors and provide a larger range of output values. Also presented is a CMOS version of the CBTA with specifications for 0.18 lm level-7 TSMC CMOS technology. It operates with a 0.9 V DC supply voltage and employs 23 CMOS transistors for processing data. By running SPICE simulations, theoretical derivations and associated findings are checked for accuracy [22].

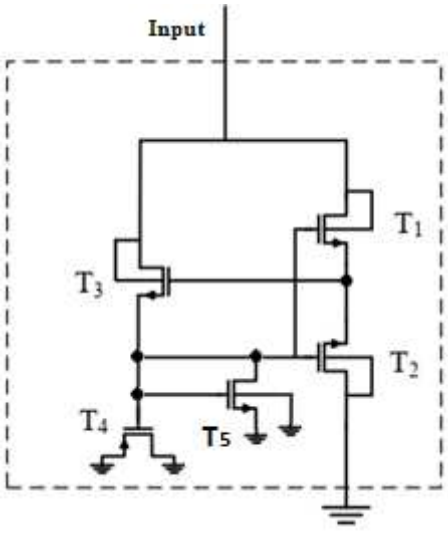
C.Sánchez-López and Aguila proposed grounded memristor emulator circuit operating from 16 Hz to 860 kHz. The emulator circuit is comprised of a resistor, a capacitor, a four-quadrant analogue multiplier, and a plus-type second generation current conveyor. Controlling the zero crossing of the frequency-dependent pinched hysteresis loop over a broad range of amplitude of the input signal, and especially when the memristor emulator circuit is operating at high frequency, requires the use of two different DC voltage sources. These sources are used when the memristor emulator circuit is operating at high frequency. In it, the process of deriving the behavioural model of the proposed emulator circuit is described in great depth. This process includes the consideration of parasitic components and demonstrates that the charge-controlled memductance is a first-order function. In addition to this, a design guide that explains how to choose the numerical value of each discrete element based on the operating frequency and amplitude of the input signal is provided [23].

Yunus et al. proposed This article presents an operational transconductance amplifier (OTA)-based TiO2 memristor emulator that is simple and practical. An OTA with several outputs, an analogue multiplier, a resistor, and a capacitor are the building blocks of the memristor emulator that was suggested. By adjusting the biassing current of the OTA, it is possible to electrically control the settings of the memristor emulator that has been presented. An advantage is provided by the ability to change the transconductance gain of the OTA. This benefit is referred to as a "externally controlled memristor." In this article, the non-volatile resistive switching properties of this suggested memristor as well as an application of it are discussed. In addition, the OPA860, a component that is readily accessible, is used to create the memristor emulator [24].

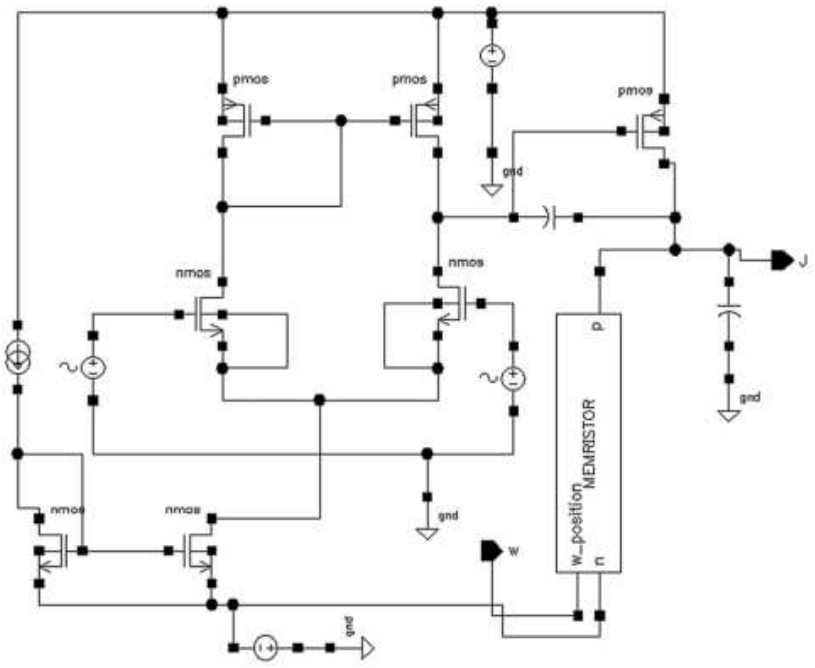
Babacan and Firat proposed It is possible to create a compact memristor that has a high memristance value. The simulations are carried out using the LTspice software, and the results that were anticipated using sinusoidal are acquired. Link two memristor emulators in serial and parallel and give the findings, which seem good. The results of running a simulation with a positive pulse train applied to both of the memristor's terminals [25]

III. PROPOSED MEMRISTOR WITH APPLICATION CIRCUIT

As illustrated in Fig. 1, the suggested memristor emulator circuit is built with only four MOS transistors. In this circuit, the T1 and T2 transistors' source terminals are linked to the DC power supply, while their drain terminals are connected to the gates of the T3 and T4 MOS transistors. The memristor's main current equals the T3 transistor's drain-source current. The capacitor is a critical component in providing the memristor's memory effect. To execute the flexible operation, transistor T5 is employed as a bypass transistor to regulate the bypass current.



(a)



(b)

Fig.1. (a) Memristor using 4CMOS, (b) Application circuit

The memristor was originally defined in terms of a non-linear functional relationship between magnetic flux linkage $\Phi_m(t)$ and the amount of electric charge that has flowed, $q(t)$:

$$\int \left(\Phi \mathrm{m}(t), q(t)\right) = 0$$

The magnetic flux linkage, Φ_m, is generalized from the circuit characteristic of an inductor. The symbol Φ_m regarded as the integral of voltage over time. As a result, each memristor is distinguished by its memristance function, which describes the charge-dependent rate of change of flow with charge [26].

$$M(q) = \frac{d\Phi \mathrm{m}}{dq}$$

When the flux is considered to be the time integral of the voltage, and the charge is considered to be the time integral of the current, the more practical representations are as follows;

$$M(q(t)) = \frac{d\Phi/\mathrm{dt}}{dq/dt} = \frac{V(t)}{I(t)}$$

To comprehend the connection between the memristor and the resistor, capacitor, and inductor, isolate the term M(q), which characterizes the device [27-31], and construct it as a differential equation.

A. Memristor circuits

Because researching the perfect memristor is quite challenging in the real world, we will instead talk about several different electrical devices that may be modelled using memristors. If you are looking for a mathematical explanation of a memristive device, you may look it up in [32]. It is possible to represent a discharge tube as a memristive device, in which case the resistance would be a function of the number of conduction electrons n_e

$$V_m = R(n_e)i_m$$

$$\frac{dn_e}{dt} = \beta n + \alpha R(n_e)i_m^2$$

V_m is the voltage across the discharge tube, i_m is the current flowing through it and n_e is the number of conduction electrons [33]. The memristance function is $R(n_e) = \frac{F}{n_e}$. $\alpha, \beta,$ and F are parameters depending on the dimensions of the tube. Regarding an experiment that demonstrates such a property for a regular discharge tube [34-35]. A significant shift in resistance may be brought about by applying either current or voltage to some memristors. The amount of time and energy that must be expended to effect the desired change in resistance can be utilised as a determining factor in determining whether or not such devices can be regarded as switches [36].

B. Memristive systems

In the more overall perception of an n^{th} order memristive scheme the crucial equations are

$$y(t) = g(A, i, t)u(t)$$

$$x = f(A, i, t)$$

where i(t) represents an input signal, o(t) represents an output signal, x represents a collection of n state variables that characterise the device, and g and f are incessant functions. In a current-controlled memristive system, the signal i(t) denotes the current signal i(t), and the signal o(t) denotes the voltage signal v.

where x is solely determined by charge (A = q) and the charge is proportional to the present. via the time derivative dq/dt = i(t).

IV. RESULTS AND DISCUSSIONS

The proposed memristor which consists of five transistors is simulated using TSMC 45nm technology using cadence virtuoso software in Linux environment. Proposed memristor circuit is tested using a differential amplifier circuit. Sweep waveform is used to analyses the memristor and differential amplifier performances. Cadence spectre tool is used to perform the spice simulation generated code for the proposed circuit.

A. Memristor and application circuit

Fig.2. shows the Memristor Model using CMOS.Fig.3. shows the transient response. Fig.4. shows DC Sweep. Fig.5. shows the transient response. Fig.6. Memristor with differential amplifier circuit.

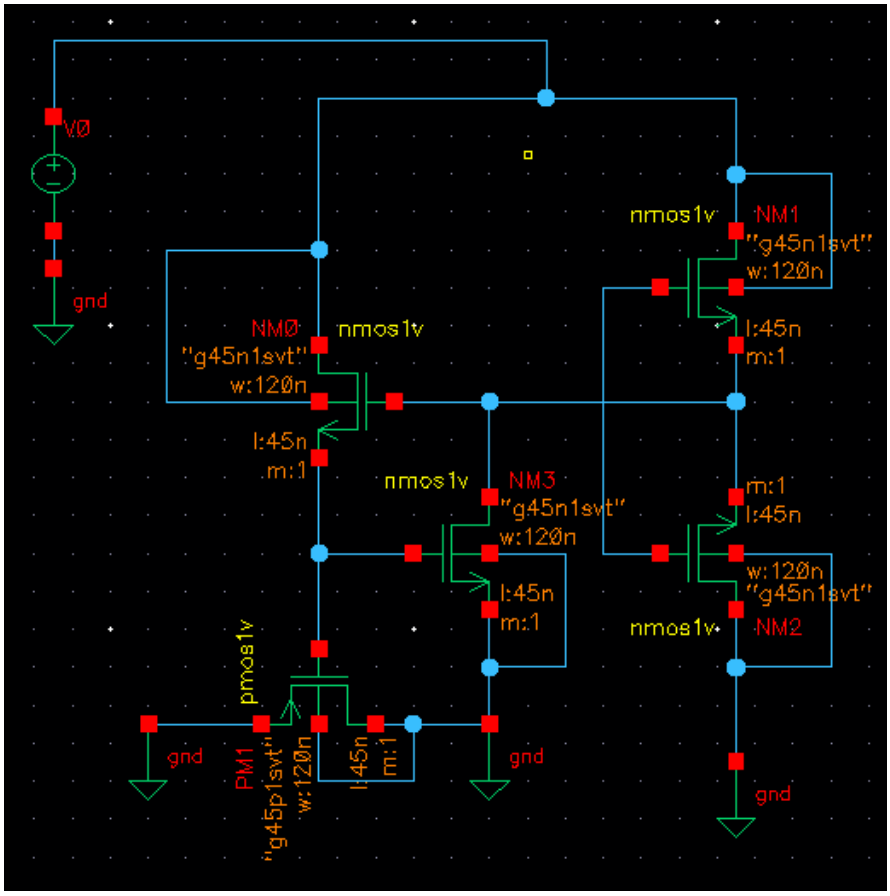


Fig.2. Memristor Model using CMOS

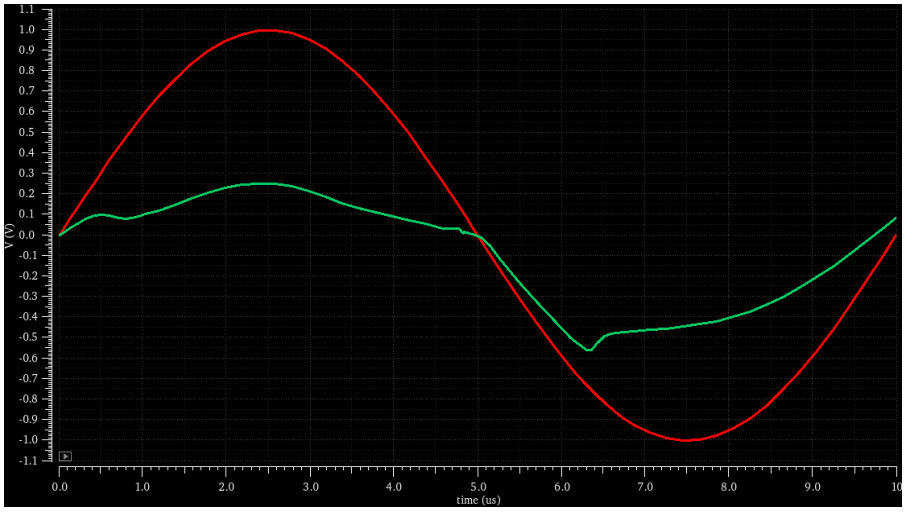


Fig.3. Transient response for input AC voltage with time period of 1µ sec(1 MHz)

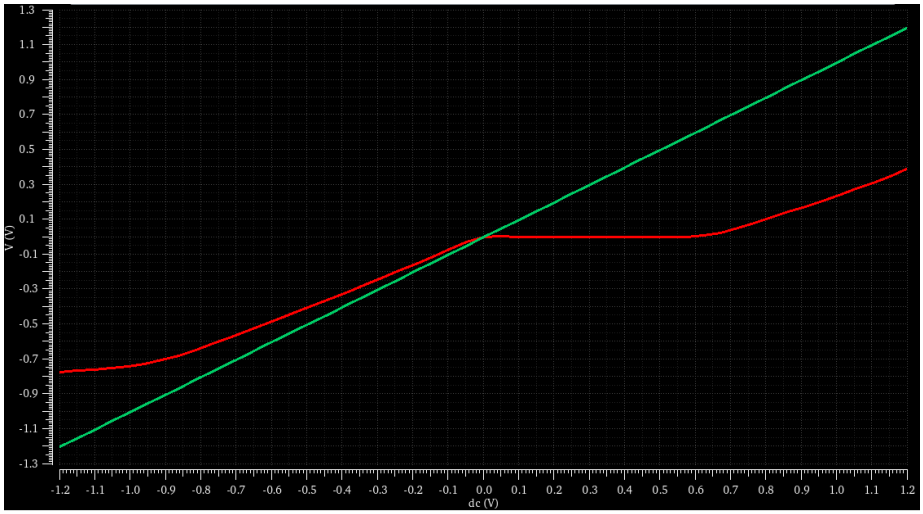


Fig.4. DC Sweep for linear DC volts with the variation from -1.5V to 1.5V with an increment of 0.1V

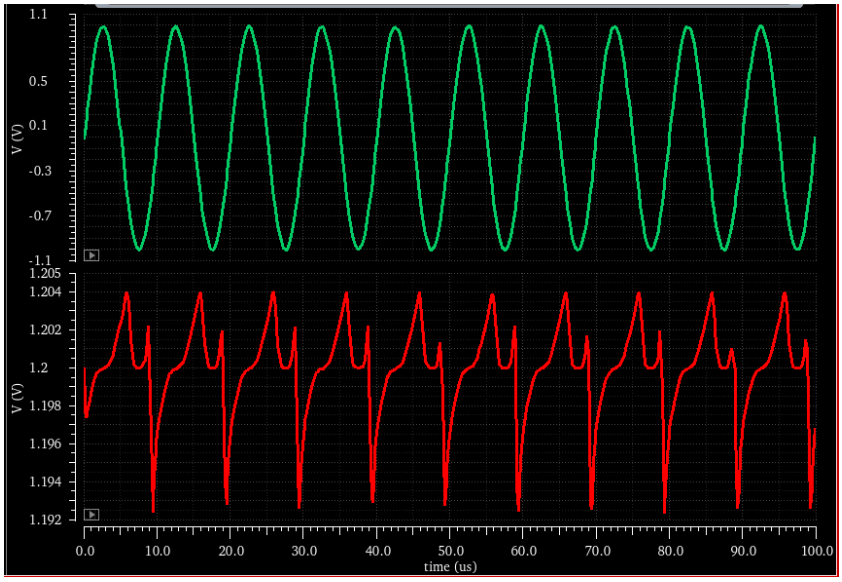


Fig.5. Transient response for multiple AC input

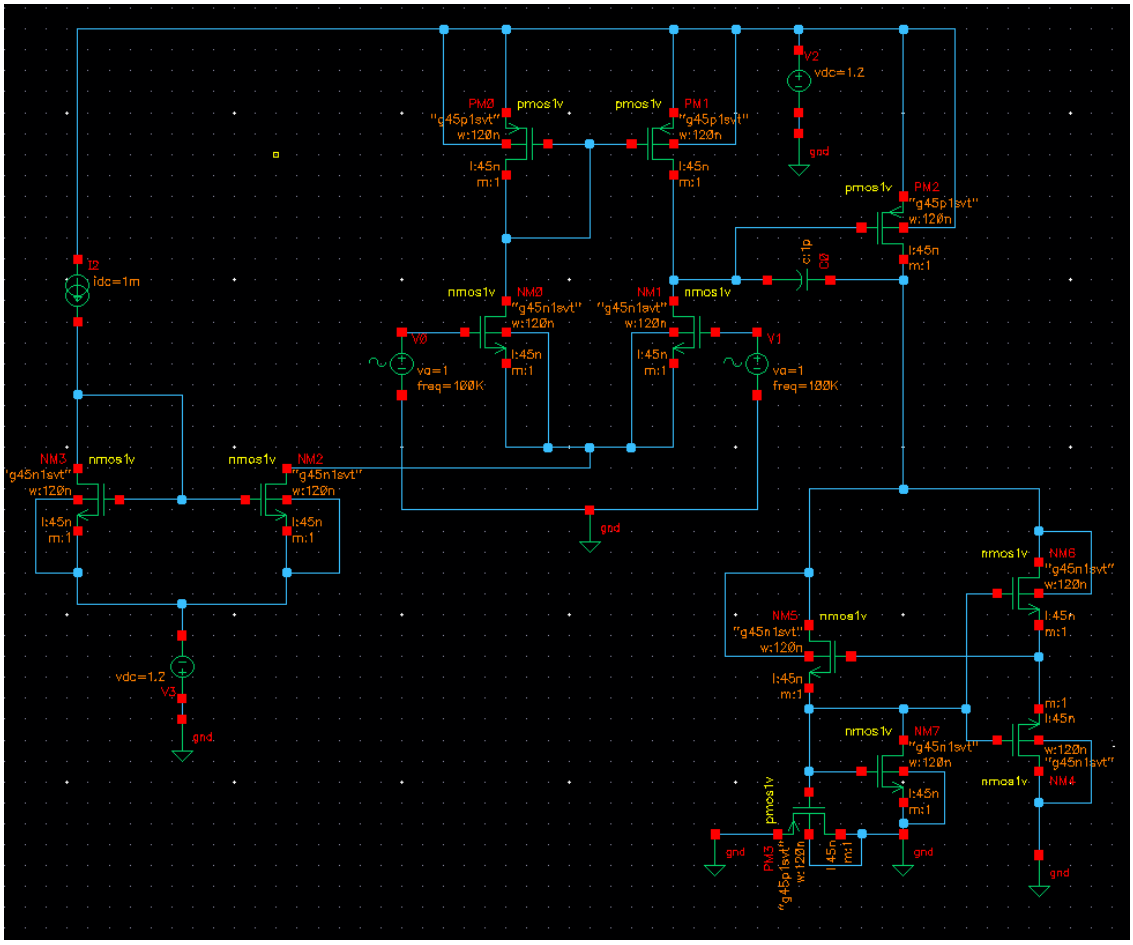


Fig.6. Proposed memristor with differential amplifier circuit

B. Performance Analysis

Table. I. shows the Voltage Vs Current. Table. II. Shows the Time vs Memristance & Voltage. Table. III. Shows the performance Comparison

Table. I. Voltage Vs Current

Voltage	-1.2	-0.8	-0.4	0	0.4	0.8	1.2
Current(uA)	-60	-40	-10	0	5	20	40

Table. II. Time vs Memristance & Voltage

Time	0	4	8	12	16	20	24
Voltage	0	1	1	0	0	-1	-1
Memristance	0	18	0	0	0	20	0

Table. III. Performance Comparison				
	# of Active components	# of passive	Power Supply	Approximate Layout

		element		Area*
Sánche et al.	1 DDCC, 1 Multiplier	1R,1C	10V	N/A
Yesil et.al	7 Transistors	1C	10V	257 μm^2+1C
Elwakil et.al	17 Transistors	1C	5V	136 μm^2+1C
Abuelma et.al	1 VDTA (16 Transistors), 1 MOS-cap	1C	10V	348 μm^2
This work	5CMOS	-	1V	67.5 μm^2

Table. IV.CMOS Specifications

Device Type	CMOS
Channel Length	45nm
Channel Width	120nm
S/D Metal Width	60n
Drain Diffusion	1.1667
Source Diffusion	1.1667
SCA	226.00151
SCB	0.11734
SCC	0.02767
Gate Spacing	160n
Technology	TSMC 45nm

Fig.7. shows the performance of channel width and current. It takes the three-voltage channel. Such as V=1.2, V=1.0, V=0.8. From the 30 channel width all the three channel accept 200 ua current. 40 channel width gets V=1.2 has 207ua,V=1.0 has 205ua, V=0.8 has 203ua. On this way it can be slightly increased. Finally 120 channel width gets V=1.2 has 232ua,V=1.0 has 228ua, V=0.8 has 225ua.

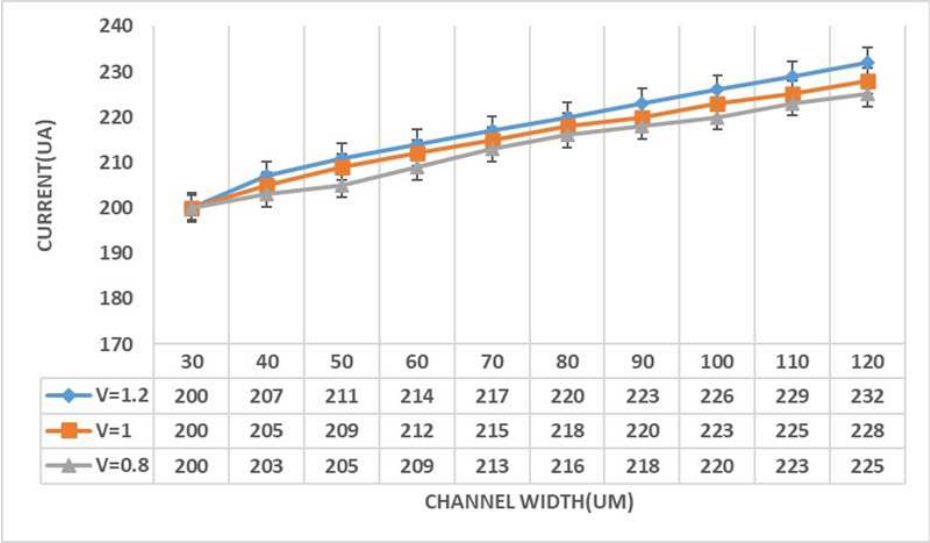


Fig.7. Performance of channel width and current

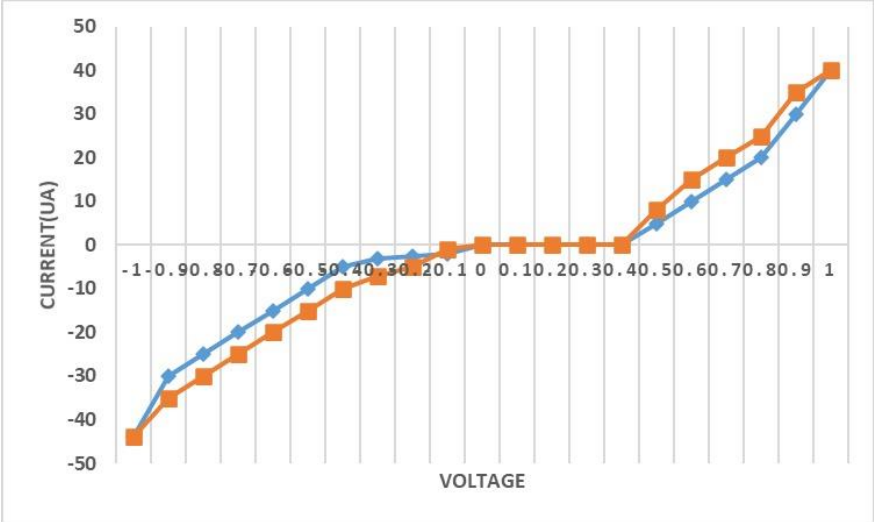


Fig.8. Performance of voltage and current

Fig.8. shows the performance of voltage and current. -1.0 voltage has -50ua current. -0.9 gets -35ua current in that manner the current was increased to 0 voltage at that stage the current is also 0 and 0.1 to 0.4 voltage does not improve the current. But also, after the 5.0 voltage, the current gain. Finally, 1.0 voltage gets 4.ua current.

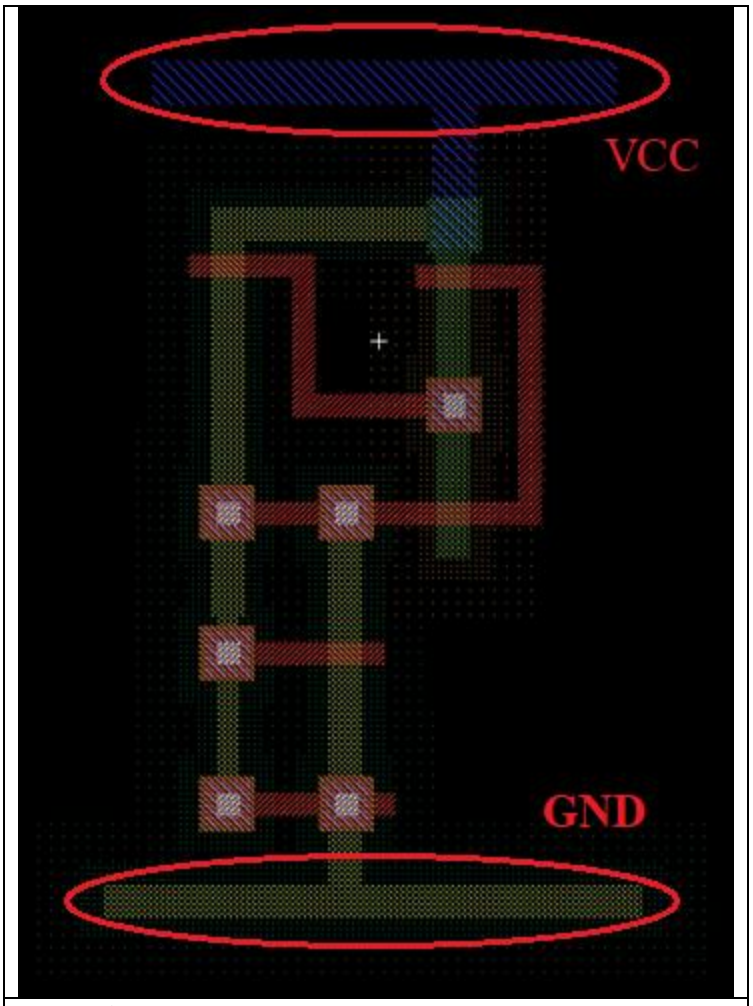


Fig.9. Layout for proposed memristor circuit

Figure.9 shows the layout generated for the proposed memristor circuit. Here 5 CMOS transistors are used. The VCC and ground are connected top and bottom respectively. The layout occupies a sum of 67.5 µm2 in the TSMC 45nm technology library.

V. CONCLUSION

In this paper, a simple and efficient asymmetrical memristor circuit is proposed to perform the operations in digital circuits. This circuit has been built using five CMOS transistors among that one CMOS is used as a bypass transistor to perform the current control operation in the memristor circuit. The proposed circuit is implemented using cadence virtuoso to model the memristor circuit. The functionality of the proposed memristor is tested using a differential amplifier circuit. Transient voltage and current profiles are evaluated to validate the real-time performance of the modeled circuit. High efficiency and stability are the advantages of the proposed memristor circuit. Proposed memristor circuits that consume TSMC 45nm CMOS process model parameters have

been carried out for all simulations. This design consumed 67.5 μm^2 of the area in CMOS 45nm technology.

Declarations

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Conflict of Interest:

On behalf of all authors, the corresponding author states that there is no conflict of interest.

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