

A Low Leakage 9T SRAM Cell With Improve Stability in Sub-Threshold Region for IoT Applications

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Research Article

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Posted Date: March 16th, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-271775/v1>

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A low leakage 9T SRAM cell with improve stability in sub-threshold region for IoT applications

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Abstract This paper presents a single-ended read and differential write half select free 9T static random access memory (SRAM) cell operates in the sub-threshold region. Proposed 9T SRAM cell shows a reasonable reduction in read and write power dissipation by a factor of $1.41\times$ and $2.1\times$ respectively as of conventional 6T (Conv.6T) SRAM cell. The stacking of transistors at core latch network minimizes the leakage power of the cell. The read static noise margin (RSNM) and write margin (WM) are upgraded by $2.16\times$ and $2.06\times$ respectively as of Conv.6T cell. A forward body bias technique is utilized in read path which results to decreases in read access time by a factor of $2.72\times$ as of standard 6T SRAM cell. The mean value of I_{on}/I_{off} ratio of the proposed cell is improved by $2.92\times$ as compared to the Conv.6T SRAM cell. It is attributed to a reduction in bit-line leakage current. To achieve more soundness in characteristics of the proposed 9T SRAM cell, process variation effect on RSNM, power dissipation, and read current is calculated through Monte Carlo (MC) simulation at 5000 points. The obtained results are compared with reference SRAM cells at 0.3V supply voltage.

Keywords Sub-threshold · Stability · Low power · I_{on}/I_{off} ratio

1 Introduction

Nowadays, a major electronics boom has been seen in internet of things (IoT) based wearable electronics such as wireless sensor node, smart-watches and fitness bands. In these devices IoT sensor contains microcontroller (MCU), a

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wireless device (Bluetooth, Wi-Fi), and SRAM as shown in Fig.1. Sensor nodes work on low data rates and low power. The devices communicate among themselves over a serial bus such as the Serial Peripheral Interface (SPI) or Inter IC Communication (I2C) protocol. The MCU serves as the master controller for the IoT node to negotiate all transactions between the devices. The wireless device is responsible for sending the sensor's data to the nearest gateway and receiving control instructions from the gateway as well. The sensor measures environmental parameters (temperature/humidity/etc.) and the data is digitized and transmitted over the SPI/I2C serial communication bus. The SRAM is used to store local data when a gateway is not available for communication. This cell is widely distributed in the modern application and occupies a large portion of System-on-chip [1].

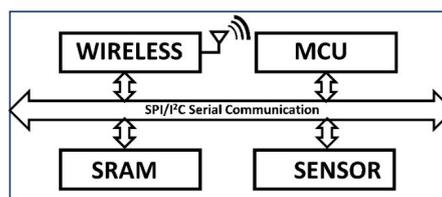


Fig. 1: Typical IoT sensor node

In SRAM cell, power dissipation becomes the prominent factor in the rising demand for Internet of Things (IoT) based portable devices. A straight and effective method to decrease the power dissipation is to decline the supply voltage insistently to the sub-threshold region. It results to decrease in both dynamic and leakage power due to their quadratic and exponential relationship with supply voltage [2]. Sub-threshold SRAM cell design has appeared as a better solution for power constraint devices. In 6T SRAM cell, re-

duction in voltage (V_{dd}) degrades the static noise margin (SNM) which increases the memory failure probability [3]. Besides, a decrease in read static noise margin in the sub-threshold region also leads to read failure in Conv.6T SRAM cell [4]. It occurs due to the formation of a voltage divider in between access transistors and pull-down network of Conv.6T SRAM as depicted in Fig.2(a). This creates a disturbance at the storage node which influenced Conv.6T SRAM cell [5]. The half-select problem is a major challenge in 6T SRAM cell design. A small change in voltage from 0V to δV at the storage node of the unselected cell may change the data in the sub-threshold region [6]. In Conv.6T SRAM during read activity, the size of access transistors is kept minimum to reduce the bit-line capacitance that increases the read noise margin of the cell. Although, during write activity, access transistor width also kept enough to support higher current capability for better write ability in the cell. This shows a conflicting relationship between read and write stability of Conv.6T SRAM cell [6]. Moreover, the width of access transistors is not only degraded read stability but may also increase the bit-line leakage current which ultimately lowers the I_{on}/I_{off} ratio of the cell. This I_{on}/I_{off} ratio represents the density of SRAM cell at the bit-line [7].

To minimize the issues related to Conv.6T SRAM cell various SRAM topologies are reported. The supply voltage reduction technique [8–11] is utilized to enhance the write noise margin of SRAM cells. In this technique, reduction in power supply incapacitates the pull-up network of SRAM cell that helps to easily write the data at the storage node. Besides, an increase in voltage at the virtual ground signal in pull-down network also improves the write ability [12–14]. V.Bhatnagar et al. [15] reported an 11T SRAM cell with remarkable improvement in write noise margin. It happens because of the ground signal is replaced with boosted negative bit line voltage. However, write power dissipation is increased as compared to Conv.6T SRAM cell. S.Naghizadeh et al. [16] proposed a read decoupled structure with multi-threshold voltage transistors to increase read margin and decreases read delay of the cell. Although, this topology suffers from the half-select issue and does not show significant improvement in the write margin (WM). C.Kushwah et al. [17] reported an 8T sub-threshold SRAM cell with increase in stability along with decreases in power dissipation. It is attributed to the use of a feedback control mechanism in the cell. An isolated read structure along with feedback cut-off 12T SRAM cell is introduced to increase read and write noise margin of the cell [3]. Further, the stacking of access transistors in the cell increases the resistance at the storage node which decreases the bit-line leakage current. This improves the I_{on}/I_{off} ratio of the cell. The isolated read structure are also reported in PCF10T [18] and LP12T [19] as depicted in Fig.2(b) and Fig.2(c). During read activity, isolation structure between storage nodes and bit-

lines prevent to flow read current through the storage nodes that eliminate the capacitive noise generated through bit-lines which enhance read noise margin of cell. This structure does not show any upsurge in write margin. Furthermore, isolated read structure suffer with bit-line leakage current in the read path that increases the read failure probability. Read and write-assist techniques are used in SPG11T SRAM cell as shown in Fig.2(d) [20] for simultaneous improvement in read and write stability. S.Pal et al. [21] reported a differential 8T (DF8T) SRAM cell in which read buffer transistors are utilized at pull-down network as shown in Fig.2(e) to expand read noise margin and read current of the cell. It also reduces the leakage power due to the stacking effect at the pull-down network. However, implementation of read/write assist techniques require additional silicon space which is one of the substantial trade-offs. R.Saeidi et al. [6] reported an 8T SRAM cell with a feedback cutting approach that enhance read noise margin of the cell. In this cell, the wider access transistor improves the write noise margin of the cell with a penalty of an area in the devices.

In IoT based devices, there is a crucial demand for low power devices which can support long-term operation with extend battery life. In 6T SRAM cell, differential bit-line structure increases read and write power dissipation as of single-ended 6T SRAM cell [1]. Single ended SRAM topologies [1, 16, 22–24] are reported to reduce the power dissipation during read/write operation. P.Singh et al. [18] proposed a positive feedback-controlled (PCF10T) SRAM cell with a single ended read operation. In this cell, read power and read stability are improved. Further, the feedback control signal minimizes the leakage power along with enhance the write margin of the cell. However, read/write access time of the cell is increases. A voltage controlled method [25] is used to minimize the leakage and dynamic power with plenty of increased area of the SRAM cell. A data-dependent supply voltage technique in 11T SRAM cell is utilized to decrease power consumption of the cell [19]. Besides, transmission gate is used at storage node of TG8T SRAM cell as presented in Fig.2(f) to decrease write power consumption in the cell [26]. In this cell, a stacked transistor is used at a pull-down network to decrease standby power in the cell. Hence, a lot of efforts are going on in the area of SRAM cell design to decrease leakage power, increase read/write stability at ultra-low supply voltage. In this article, a low-power, highly stable novel 9T SRAM cell [here after called low-power 9T (LP9T)] is proposed. For a fair comparison, the proposed LP9T cell as well as reference cells are simulated at 45nm technology node at cadence virtuoso tool. Monte Carlo simulation is performed with three sigma variation in device parameters for 5000 random samples at 0.3V supply voltage to achieve more soundness in results. The simulated results are compared with Conv.6T[30],DF8T[21],TG8T[29], PCF10T

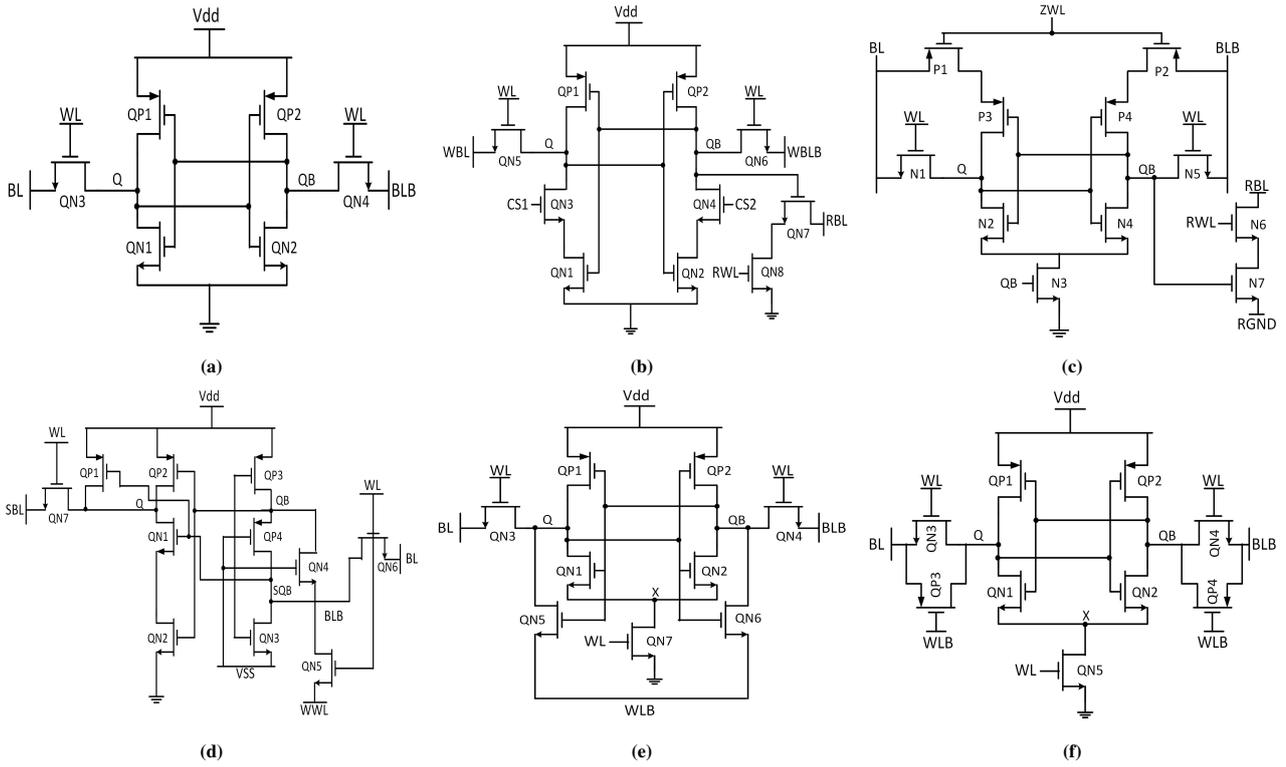


Fig. 2: Schematic of considered (a) Conv.6T,(b) PCF10T,(c) LP12T,(d) SPG11T,(e) DF8T ,(f) TG8T SRAM cells

[26],SPG11T [20] and LP12T [28] SRAM cells. The contribution of proposed work is summed up as follows::

- (i) Improvement in read/write noise margin along with a commendable reduction in power dissipation is the significant achievement of the proposed LP9T SRAM cell.
- (ii) The LP9T SRAM cell also exhibits reduction in read access time as of considered cells.
- (iii) The higher value of I_{on}/I_{off} ratio in the proposed cell signifies the larger bit-cell density.
- (iv) The LP9T SRAM cell has better electrical quality metric (EQM) as of reference SRAM cells.

The organization of the paper is as follows: Section II includes the working mechanism of the proposed LP9T circuit. In Section III, the detailed analysis of proposed cell characteristics along with comparison among considered SRAM cell topologies has been discussed. Section IV, concludes the paper.

2 Proposed 9T SRAM cell

To resolve, the issues allied with 6T SRAM cell in the sub-threshold region, a 9T SRAM cell is reported as presented in Fig.3. Transistors P3, P4, and N3 are used to form a core latch circuitry. This latch circuitry differs from Conv.6T latch due to the absence of NMOS transistor in a pull-down network of storage node (Q). A strengthened NMOS transistor

N2 is incorporated in between node Q and bit-line BL. This transistor is utilized to perform the role of an absent transistor. During read and hold operation, BL is kept at logic '0'. Transistors N1 and N2 are used during write mode of the proposed cell. Whereas, read activity is performed through N4 and N5 transistors. To minimize the standby power, stack transistors (P1 and P2) are employed at the top of the core-latch.

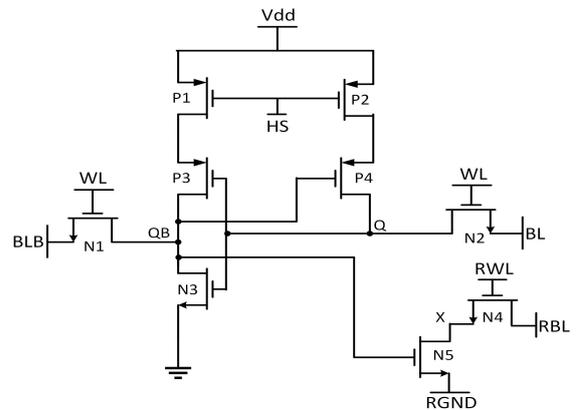


Fig. 3: Proposed LP9T SRAM cell

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Table 1: Control signals of LP9T SRAM cell

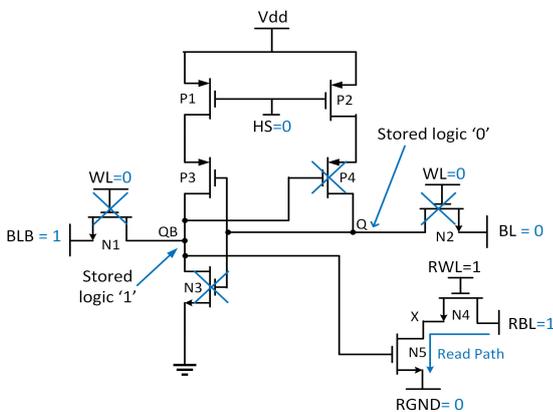
Control signals	Hold mode	Read mode	Write mode
HS	0	0	0
BL	0	0	0/1
BLB	1	1	1/0
RBL	1	1	1
RWL	0	1	0
WL	0	0	1
RGND	1	0	1

2.1 Hold mode

In proposed cell, during hold mode, the read wordline (RWL) and write wordline (WWL) signals are kept at logic '0' which disconnect the storage nodes from the bit lines. Initially, logic low level voltage is assumed at storing node Q which turns on P3 transistor and logic high is apparent at storage node QB. Now, logic '1' is assumed at storing node QB, it disable transistor P4 that disconnects the power supply from the storage node Q. The bit-line BL is connected to the ground. The effective off-state resistance from storage node Q to the ground must be minimum which can be achieved by strengthening the N2 transistor. This transistor discharges the residual voltage in the form of leakage current in the sub-threshold region.

2.2 Read mode

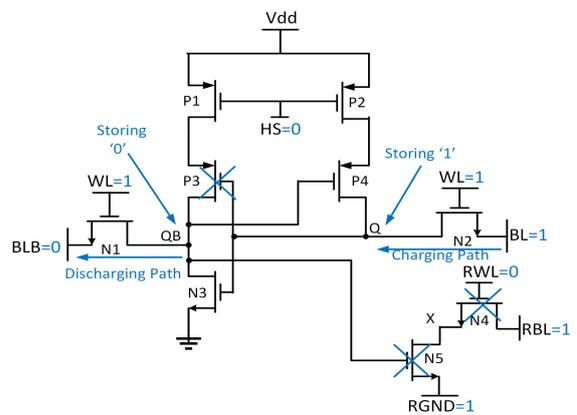
In Conv.6T SRAM cell, read activity is accomplished by enabling the access transistors to pass the storage node data at output terminals (BL and BLB). In the proposed cell, a single-ended read operation is performed through read bit-line (RBL).

**Fig. 4:** LP9T SRAM during read operation

During read operation, RBL is pre-charged to Vdd, and read word-line (RWL) signal is kept at Vdd as shown in Table 1. RWL signal turns-on N4 transistor to discharge the RBL node voltage. The node voltage QB, turns on/off transistor N5. Suppose, logic low is present at storing node Q. It turns-on the P3 transistor which charged the storage node QB to Vdd. This turns-on the N5 transistor which provides discharging path to RBL signal through N4 and N5 transistors which is displayed in Fig.4. It ensures that the logic low is available at the storing node Q. Now, logic high is presumed at the storing node Q that turns on the N3 transistor to retain logic low at the storing node QB which disable N5 transistor to sustain the read bitline signal at Vdd. This indicates the logic high is visible at node Q.

2.3 Write mode

A differential write operation is carried out in the proposed LP9T SRAM cell as related to the Conv.6T SRAM cell. Amid write operation, RBL, WL, and RGND signals are connected to logic '1,' while RWL signals have been connected to logic '0,' which is shown in Fig.5. Logic '0' and logic '1' are initially assumed to be stored at Q and QB nodes. Now, to write logic '1' at node Q and logic '0' at node QB, each bit-lines, BL and BLB are wired to Vdd and ground. The WL signal enables the N1 and N2 transistors which pass input signal to node QB and Q respectively. Due to the node Q voltage, transistor N3 conducts which maintains the provided input data at node QB. Similarly, due to node QB voltage, P4 transistor turns-on which maintains the data at node Q.

**Fig. 5:** LP9T SRAM during Write operation

2.4 Half Select Issues

The half-Select problem occurs during read or write activity at the storage node of an unselected cell in a selected row or column. To remove, row half select problem during read operation, the RWL signal is in logic '1' developed by a row decoder to provide read path while read ground signal (RGND) is developed by a column decoder. These developed signals create a cross-point (separate row and separate column signal) which eliminated the row half select problem for unselected cell during the read activity.

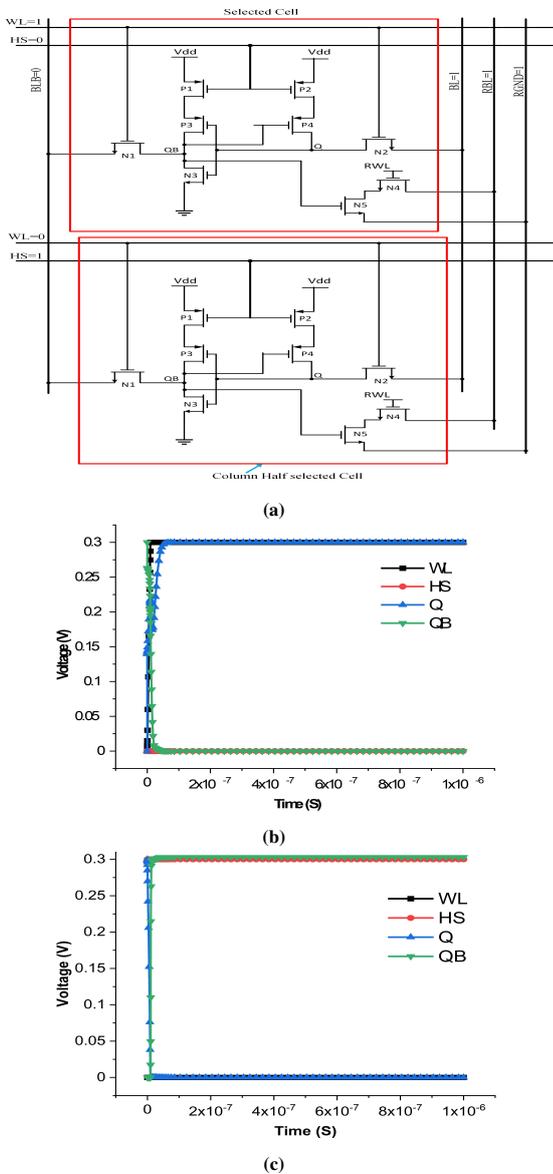


Fig. 6: (a) Elimination of Column Half selected issue in LP9T SRAM cell, (b) Transient wave form of selected cell, (c) Transient wave form of unselected cell during write operation.

To remove the half-select column problem during the write operation, the HS control signal is held at logic '0' and the WL signal is held at logic '1' for the selected cell. However, HS signal is provisionally changed to logic '1' and WL signal is at logic '0' for unselected rows as shown in Fig.6(a). This affects the stored logic '1' node with slightly high voltage and complementary storage node is still maintain at logic '0'. Negative-coupling noise generated by bit-lines (BL and BLB) affects the hold stored logic '1' node. This results in an improvement in hold stability during the floating period for unselected cells [27]. Thus, HS and WL signals facilitate cross-point write access mechanism for the unselected column which eliminates column half-select problem in LP9T SRAM cell. The transient waveform of the selected cell and unselected cell during write operation is shown in Fig.6(b) and Fig.6(c) respectively.

3 Simulation results

The properties of the SRAM cells are achieved by adjusting the supply voltage around 0.3V to 0.5V via the virtuoso cadence tool at the 45nm CMOS technology node. Process variation effects on different SRAM characteristics are studied by Monte Carlo simulation with $\pm 10\%$ difference in system parameters under 5000 random samples. Simulated results are compared with Conv.6T [28], DF8T [21], TG8T [26], PCF 10T [18], SPG11T [20] and LP12T [19] SRAM cells. Necessary device size is one of the main criteria for a proper functioning of the SRAM cell. In the proposed LP9T SRAM cell, the transistors P1, P2, P3, P4 and N3 are held at a minimal channel width, i.e. 120nm. The width of the N1 and N2 transistors is increased by $1.2\times$ and $1.3\times$ of the minimum width to enhance cell efficiency. The width of the N4 and N5 transistors is $1.1\times$ and $1.2\times$ of the minimum width. Every simulation outcome is addressed after post-layout simulations using a spectre simulator in a cadence.

3.1 Read/Write Power dissipation

The read/write power dissipation of SRAM cells is measured at the time of the active state of the cell. The read power consumption is determined whenever logic '1' is presented at storage node of SRAM cell. Effect of Variation in supply voltage at read power dissipation is illustrated in Fig.7(a). It is noticed that read power dissipation upsurges with increase in the supply voltage from 0.3V to 0.5V. It happens due to the quadratic relationship between the supply voltage and power dissipation. Further, the read power consumption of LP9T SRAM cell is decreased by $1.41\times$, $1.40\times$, $1.39\times$, $1.33\times$, $1.38\times$, $1.40\times$ as compared to Conv.6T [28], DF8T [21], TG8T [26], PCF10T [18], SPG11T [20], LP12T [19] SRAM cells respectively.

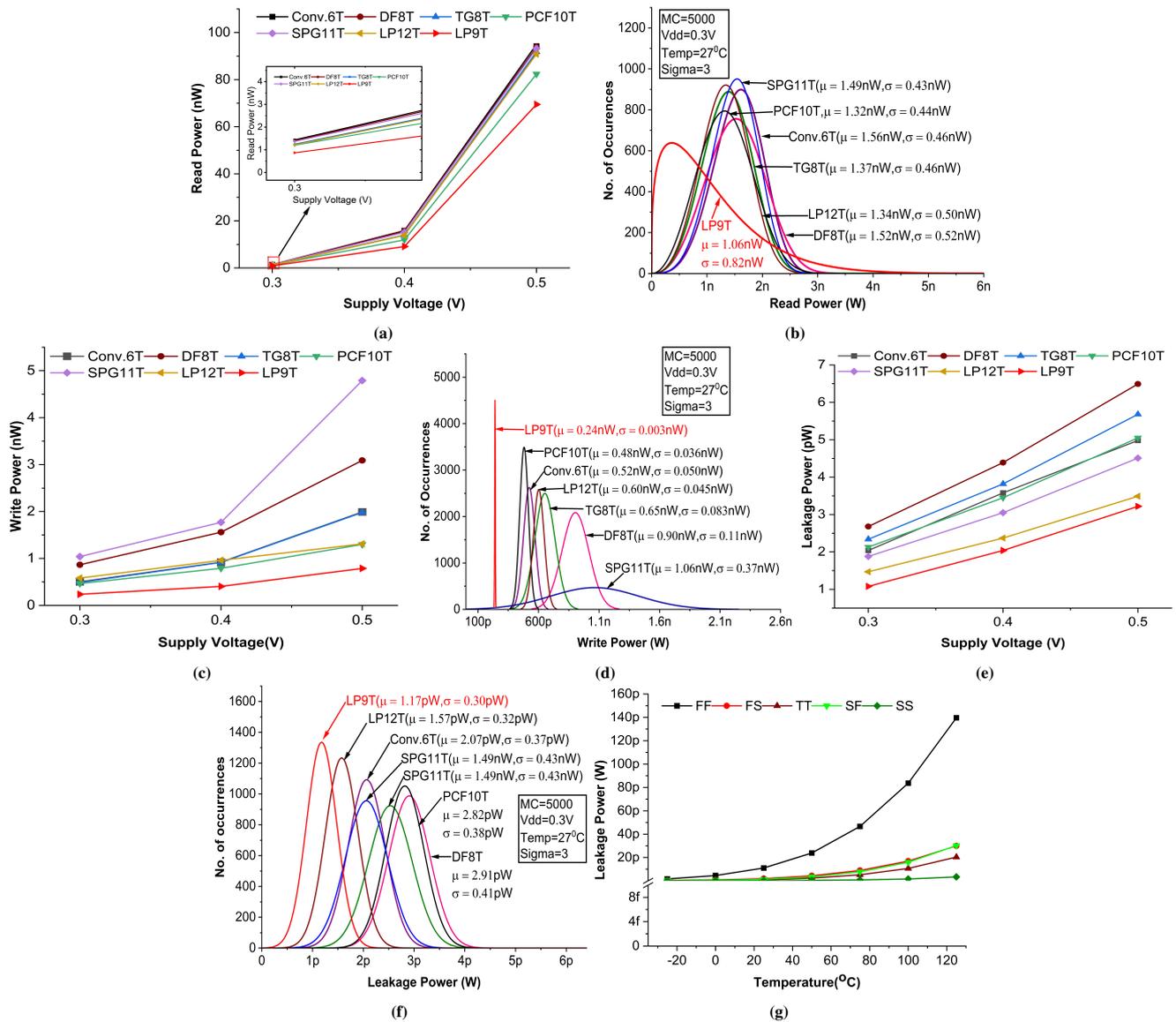


Fig. 7: (a)Read Power at different supply voltage,(b) MC of read power at 0.3V, (c) Write power at different supply voltage,(d) MC of write power at 0.3V, (e) Leakage power at different supply voltage, (f) MC of leakage power at 0.3V, (g) Leakage power with temperature at 0.3V supply voltage.

It is because of single sided read structure that minimizes the read bit-line capacitance. However, Conv.6T SRAM cell displays the highest read power consumption as of considered cells. It is due to differential read operation which increases the bit-line capacitance of the cell. Additionally, process variation effect at read power of SRAM cells is analyzed at 0.3V supply voltage as depicted in Fig.7(b). The LP9T SRAM cell has the lowest mean value of read power ($\mu=1.06\text{nW}$) at 5000 random samples. Though, Conv.6T SRAM cell is the highest mean values of read power i.e. ($\mu=1.56\text{nW}$) among all considered cells.

The average write power consumption is evaluated during write logic low and logic high at node Q and QB corre-

spondingly. The write power consumption at different supply voltages has seen in Fig.7 (c). It has indicated that the write power of the LP9T SRAM cell is decreased $2.1 \times, 3.64 \times, 2.06 \times, 1.96 \times, 4.23 \times, 2.45 \times$ as compared to Conv.6T [28], DF8T [21], TG8T [26], PCF10T [18], SPG11T [20], LP12T [19] SRAM cells respectively. This happens due to the weaken of pull-up path through PMOS (P1 and P2) transistors. In addition, the write power of the SPG11T SRAM cell is highest among the cells mentioned. It occurs due to the write assist transistor. The process variation effect on write power dissipation of SRAM topologies is illustrated in Fig.7(d). The mean value of write power dissipation in LP9T SRAM cell is 0.24nW

which is the lowest among considered SRAM cells. It denotes the least deviation in write power of LP9T SRAM cell.

3.2 Leakage Power dissipation

In the nanometer regime, stand by leakage current becomes a challenging issue in SRAM cell. This current is one of the main contributors to maximize the power dissipation of the cell. The total leakage current includes sub-threshold leakage (I_{sub}), gate leakage (I_g), and junction leakage (I_{jn}) are given by the following equation:

$$I_{sub,Conv.6T} = I_{subQP1} + I_{subQN2} + I_{subQN3} \quad (1)$$

$$I_{jn,Conv.6T} = I_{jnDQP1} + I_{jnDQN2} + I_{jnDQN3} + I_{jnSQN4} + I_{jnDQN4} \quad (2)$$

$$I_{gate,Conv.6T} = I_{gDQP1} + I_{gDQP2} + I_{gSQP2} + I_{gDQN1} + I_{gSQN1} + I_{gDQN2} + I_{gDQN3} + I_{gDQN4} + I_{gSQN4} \quad (3)$$

$$I_{Leakage,Conv.6T} = I_{sub,Conv.6T} + I_{jn,Conv.6T} + I_{gate,Conv.6T} \quad (4)$$

The above Eq.[1]-[4]is obtained from the leakage current expressions of Conv.6T SRAM cell given by S.Pal et al. [21]. The main leakage current sources of the proposed LP9T SRAM cell are described by Eq.(5)-(8):

$$I_{sub,LP9T} = I_{subP3} + I_{subP4} + I_{subP2} + I_{subN1} + I_{subN4} + I_{subN5} \quad (5)$$

$$I_{jn,LP9T} = I_{jnDN2} + I_{jnSN2} + I_{jnDN3} + I_{jnSN3} + I_{jnDP2} + I_{jnSP2} + I_{jnDN1} + I_{jnDN5} + I_{jnDN4} \quad (6)$$

$$I_{gate,LP9T} = I_{gDP3} + I_{gSP3} + I_{gDP4} + I_{gSP4} + I_{gDP2} + I_{gDN2} + I_{gSN2} + I_{gDN3} + I_{gSN3} + I_{gDP1} + I_{gSP2} + I_{gDN1} + I_{gDN5} + I_{gDN4} \quad (7)$$

$$I_{Leakage,LP9T} = I_{sub,LP9T} + I_{jn,LP9T} + I_{gate,LP9T} \quad (8)$$

The leakage power at different value of supply voltages is shown in Fig.7(e). It can be seen that leakage power of LP9T SRAM cell is reduced by $1.88\times, 2.49\times, 2.17\times, 1.97\times, 1.74\times, 1.36\times$ as compared to Conv.6T [28],DF8T [21], TG8T [26],PCF10T [18], SPG11T [20],LP12T [19] SRAM cells respectively. This is attributed to the stack effect of PMOS transistors at the pull-up network. Transistors P1 and P2 increases resistive path between Vdd to ground. This resists the flow of leakage current in the cell during standby mode. The process variation effect on the leakage power of SRAM cells is presented in Fig.7(f). It is recognized that the LP9T SRAM cell has the least mean value leakage power along with lowest standard deviation. This signifies that the deviation in leakage power of LP9T SRAM cell is least among considered SRAM cells. Fig.7(g) shows the effect of temperature on LP9T SRAM cell at different process corners. The leakage power is observed to be increase with rising in temperature. This is due to the exponential relationship among leakage power and temperature.

3.3 Read/Write access time

In differential mode, read delay or read access time (T_{RA}) is specified as the time difference between activation of word line (WL) and discharging of bitline at least 50mV from Vdd [21]. In the single-ended read operation, T_{RA} is defined as the time duration between the activation of read word line (RWL) Signal and drain the RBL node voltage from its peak voltage to at least 50mV voltage difference. The write delay is the absolute delay to develop the charge up to 90% of Vdd for write '1' and discharged to 10% of Vdd for write '0' at the storage nodes Q and QB respectively. The read and write delay plays an important role in those topologies that display a reduction in overall power dissipation. Fig.8(a) shows the time of read access which considered SRAM topologies at various supply voltages value. It is noticed that the LP9T SRAM cell, read access time has been improved by $2.72\times, 2.5\times, 3.55\times, 8.15\times, 3.49\times, 5.56\times$ as compared to Conv.6T [28],DF8T [21],TG8T [26],PCF10T [18], SPG11T [20],LP12T [19] SRAM cells respectively. It is attributed to the forward body bias technique in read path which reduces the threshold voltage of N5 transistor which takes minimum time to discharge the read bit-line. The read access of PCF 10T cell is maximum as of reference cells. It happens due to single-ended read structure which takes more time to discharge the read bit-line signal. The write access time or write delay T_{WA} of SRAM topologies with different value of supply voltages is illustrated in Fig.8(b). It has been observed that the write access time of SRAM cell is decreased with increase in supply voltage. This is attributed to an increase in mobility of charge carriers which further increase the write current and improve the write delay. In

addition to this, the write access time of LP9T SRAM cell is improved by $1.09\times, 2.09\times, 1.63\times, 2.85\times, 2.04\times$ as compared to DF8T [21], TG8T [26], PCF10T [18], SPG11T [20] and LP12T [19] SRAM cells respectively. It occurs because of increased write word line voltage which strengthens N2 and N3 transistors. This increases the flow of current from bit-line to storage nodes.

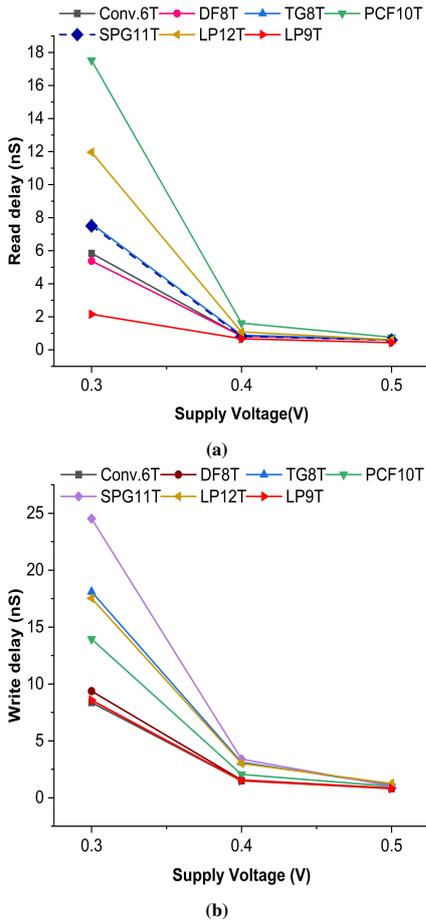


Fig. 8: (a) Read delay at different supply voltages, (b) Write delay at different supply voltages

3.4 Static Noise Margin

Static Noise Margin (SNM) is the minimal dc noise voltage that can alter the data placed at the storage node in the SRAM cells. It defines the stability of the cell. The higher value of SNM shows more stable of SRAM cell. SNM is categorized as Hold SNM (HSNM), RSNM, and write margin. The hold stability of the SRAM cell is determined with the help of butterfly curve [29]. The hold stability at varying supply voltages is seen in Fig.9. It is observed that the HSNM values of the LP9T cells and considered cells are

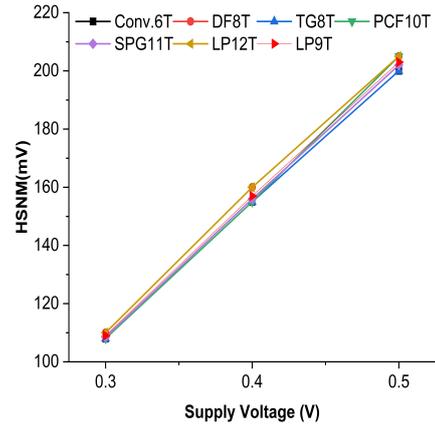


Fig. 9: HSNM at different supply voltage

nearly equivalent to 110 mV. This occurs due to the similar core latch configuration of the SRAM cells.

3.5 Read Static Noise Margin

Conv.6T SRAM cell is more susceptible to noise during the read operation. This is due to the creation of a voltage divider between the access transistors and the pull-down transistors. It develops small positive voltage at stored logic '0' node. This small voltage may be sufficient to flip the content of the storage node which degrades the read stability of the cell. An improvement in the read stability can be achieved with a higher cell ratio (CR) which helps to minimize unwanted positive voltage at stored logic '0' node [21]. The read stability of the SRAM cell is characterized by a butterfly curve as can be seen in Fig.10 (a). It is measured as the length of the edge of the highest square that can be marked within the butterfly bend [29]. The RSNM of SRAM cells at different supply voltages has seen in Fig.10 (b). It is noted that RSNM of SRAM cells is increased with an increase in supply voltages from 0.3V to 0.5V. The RSNM value of proposed LP9T, PCF10T [18], and LP12T [3] SRAM cells are approximate equal due to similar read structure. Further, LP9T SRAM cell shows improvement in RSNM by $2.16\times, 1.96\times, 2.16\times$ and $1.03\times$ as compared to Conv.6T [28], DF8T [21], TG8T [26], and SPG11T [20] SRAM cells respectively. It is caused by separate read and write operations in LP9T SRAM cell. In addition to this, the gate terminal of the N5 transistor is coupled to the node QB which eliminates the occurrence of leakage path between the storage node and read bit-line (RBL). It also results in an improvement in RSNM of the cell. It is important to note that RSNM is almost equivalent to HSNM in the proposed LP9T SRAM cell due to isolated read structure. The MC simulation results of read stability at 0.3V supply voltage as shown in Fig.10(c). The mean and standard deviation values of RSNM in LP9T

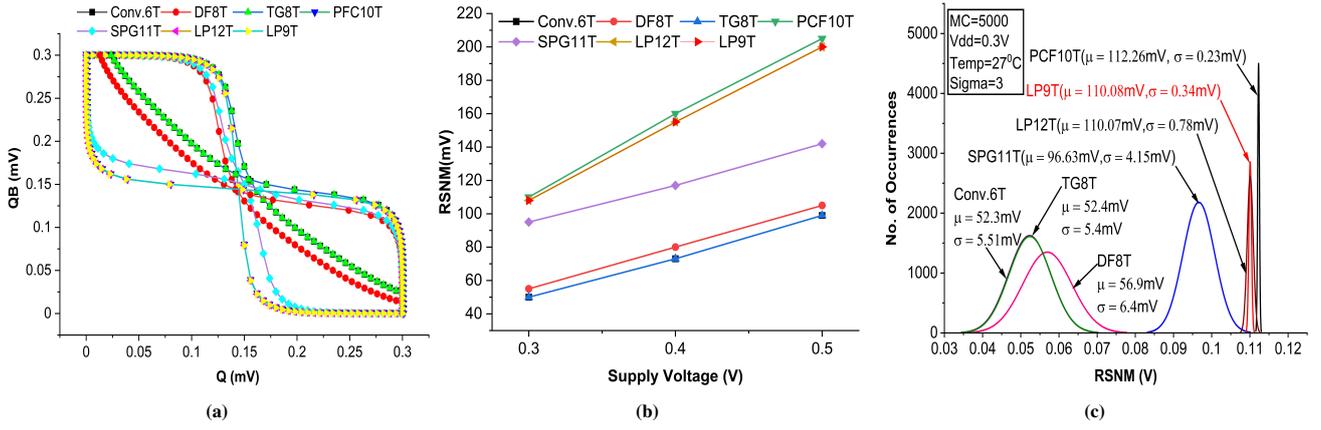


Fig. 10: (a) Butterfly curves of SRAM cell, (b) RSNM at different supply voltages, (c) MC simulation of RSNM at 0.3V supply voltage.

SRAM cell are 110.08mV and 0.34mV respectively. These values signify a very small deviation in read stability.

3.6 Write ability

Write margin (WM) is used to calculate the write ability of the cell. A higher value of WM signifies the better write ability. The bit-line swept method [30] used to calculate the write margin of the SRAM cells. The word-line signal turns-on the write access transistors and input is applied on the bit-lines. Read/write stability are interrelated concepts due to common access transistors during read/write mode. In LP9T SRAM cell, access transistors conflict is eliminated because of separate read and write operations. The write margin at different supply voltage is seen in Fig.11. It is noted that write margin of SRAM cells increases with an increase in voltage from 0.3V to 0.5V. The write margin of the LP9T SRAM cell has been boosted by $2.06\times$, $2.69\times$, $1.84\times$, $1.98\times$, $1.5\times$, $1.07\times$, better write margin as compared to Conv.6T [28], DF8T [21], TG8T [26], PCF10T [18], SPG11T [20], LP12T [19] SRAM cells respectively. It happens because of the in-

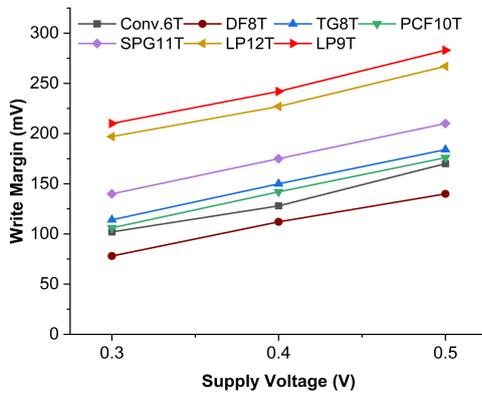


Fig. 11: Write margin of SRAM cells

capacitating of pull-up path through the stack of PMOS (P1 and P2) transistors. Further, the word-line boosting technique is applied to improve the current capability of write access transistors (N1 and N2). It improves the write margin of LP9T SRAM cell. The write margin of DF8T SRAM cell is lowest among considered cells due to access transistors conflict and extra transistors are used in pull-down network.

3.7 I_{on}/I_{off} ratio

The SRAM bit-cell density in an array is determined by the I_{on}/I_{off} ratio. In Conv.6T SRAM cell, bit-cell density is limited by a large value of bit-line leakage current which degrades the I_{on}/I_{off} ratio. To sustain the stability of Conv.6T SRAM cell in the subthreshold region, cell ratio and pull-up ratio should be greater than 1.66 and less than 1 respectively. This may lead to an increase in access transistor width which increases the bit-line leakage current. It degrades the I_{on}/I_{off} ratio of the cell. The I_{on} and I_{off} current of proposed LP9T SRAM cell is represented by Eq.9 and 10. These current are calculated when at the storage nodes Q and QB logic '0' and logic '1' is presented respectively.

$$I_{on,LP9T} = I_{N4}(V_{GS} = V_{dd} - V_X, V_{DS} = V_{dd} - V_X) \quad (9)$$

$$= I_{N5}(V_{GS} = V_{dd} - V_{RGND}, V_{DS} = V_X)$$

$$I_{off,LP9T} = I_{subN5} + I_{subN4} + I_{jndN5} + I_{jndN4} + I_{gdN5} + I_{gdN4} \quad (10)$$

I_{on}/I_{off} ratio has been measured through average current during read and hold activity of the cell. Higher value of I_{on}/I_{off} dictates the higher number of cells per bit-line. The MC simulation results of I_{on}/I_{off} ratio of SRAM cells are illustrated in Fig.12. It has been noted that the LP9T SRAM

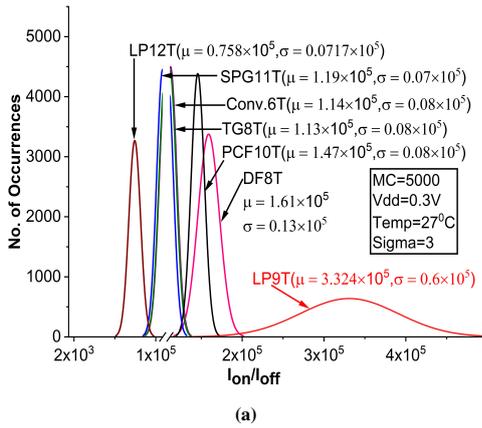


Fig. 12: MC of I_{on}/I_{off} ratio at 0.3V supply voltage

cell mean value increased by $2.92 \times, 2.06 \times, 2.94 \times, 2.26 \times, 2.79 \times, 4.38 \times$ higher as compare to Conv.6T [28], DF8T [21], TG8T [26], PCF10T [18], SPG11T [20], LP12T [19] SRAM cells respectively. It is attributed to improvement in read access time which implies the higher value of read current. In addition to this, during hold mode, read access transistor N5 is in off-state and its body and gate terminal are shorted together which increases the threshold voltage. It gives a higher resistive path, which minimize the leakage current of bit-line. Thus, the highest read current value and the lowest read bit-line leakage current indicate an increase in the I_{on}/I_{off} ratio of the cell. It is important to note that the lowest value of I_{on}/I_{off} ratio is observed in LP12T SRAM cell. It occurs due to a single ended read arrangement that decreases the read current of the cell.

3.8 Process variation

As the technology node of the MOS devices shifted into the nanometer region, it generates statistical quality deviations in transistor metrics including threshold voltage, channel length, and mobility [31]. Deviation in channel length leads to a change in threshold voltage which is a big challenge in nanoscale technology. This affects the characteristics of SRAM cell. Hence, process variation effects become very significant issues in the nanometer regime. In this work, process corners (Fast NMOS and Slow PMOS (FS), Slow NMOS and Slow PMOS (SS), Slow NMOS and Fast PMOS (SF), Fast NMOS and Fast PMOS (FF)) analysis is performed through MC simulation with 5000 random sample.

Fig.13(a) to (d), shows the MC simulation of read current, read power, write power, leakage power at different Corners. It is found that the LP9T SRAM cell has a minimal read current value. (0.64nA), read power (72pW), write power(140pW), and leakage power (291fW) at SS corner (slow NMOS slow PMOS). It occurs due to less mobility of

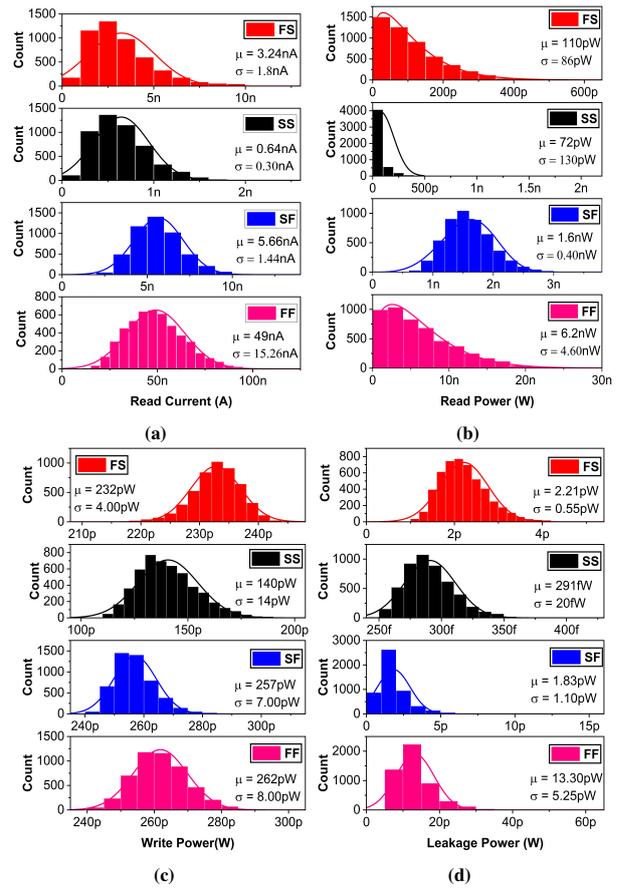


Fig. 13: LP9T SRAM cell (a) Read Current at Corners,(b) Read Power at Corners,(c) Write Power at Corners,(d) Leakage Power at Corners

charge carriers of NMOS and PMOS transistors at SS corner as compared to the nominal corner (TT). This resists the flow of current and implies the worst performance as compared to other corners. Further, it is worthy to notice that the variability (σ/μ) of read current and read power is minimum at SF corner as compared to other corners. It is attributed to the mobility of charge carriers in slow NMOS is nearly equal to the mobility of charge carriers in fast PMOS. Moreover, the variability of write power is least at FS corner as compared to other corners. It's due to slow PMOS transistor which provides higher resistance at pull up network.

3.9 Layout of SRAM Cells

In portable devices, area of SRAM cell is the main concern to form a large array. The layout represents the geometric shape of an integrated circuit which corresponds to the pattern of metal, oxide, and semiconductor layers. It depends on the number of transistors, the length of the channel, the width and the topological complexity. Presented layout of SRAM cell has been satisfied with design principles such as design rule check (DRC), layout vs. schematic (LVS), and

RC extraction through spectre simulator. Fig.14 shows the

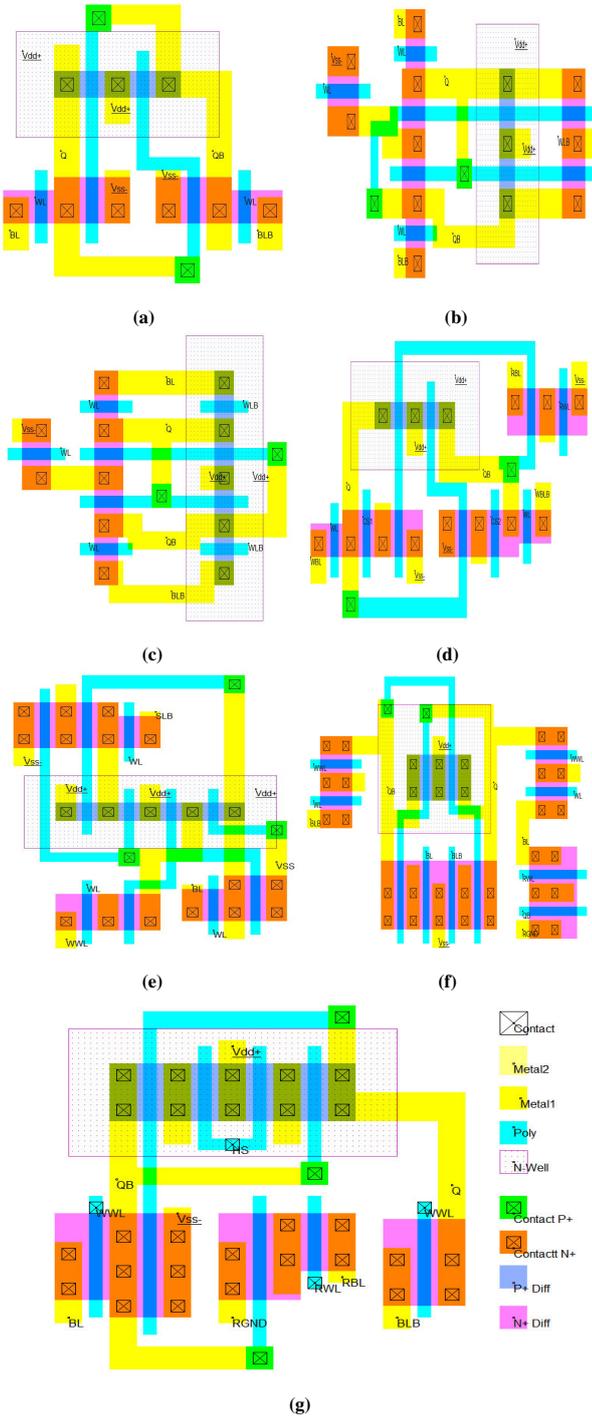


Fig. 14: Layout of (a) Conv.6T, (b) DF8T, (c) TG8T, (d) PCF10T, (e) SPG11T, (f) LP12T, (g) Proposed LP9T SRAM cell

layout view of Conv.6T [28],DF8T [21],TG8T [26],PCF10T [18],SPG11T [20] and LP12T [19] SRAM cells. The relative area overhead with regard to Conv.6T SRAM cell is represented in Table 2. The area overhead of LP9T SRAM cell

is $1.52\times$ as of Conv.6T SRAM cell. The DF8T [21],TG8T [26],PCF10T [18],SPG11T [20] and LP12T [19] SRAM cells has also larger area as of Conv.6T cell.

3.10 Electrical Quality Metric

The quality of SRAM cells is investigated through obtained simulation results. The improved simulation results in all aspects are rarely possible. Various design parameters are reported to analyze the overall efficiency of the SARM cell [26,32,33]. S.Salahuddin et al. [32] reported a SRAM electric quality metrics (SEQM). In this metric, stability and leakage power are the main part of this equation whereas access time and area are not taken into consideration. H.Jiao et al. [33] has also reported an EQM metric which includes stability, power dissipation, read access time, and SRAM cell area. In this metric, write access time is not considered to check the overall efficiency of the cell. Here, a modified EQM is proposed which includes stability, power, access time, and area under consideration and represented by Eq.11.

$$EQM = \frac{RSNM \times WSNM \times HSNM}{T_{RA} \times T_{WA} \times P_R \times P_W \times P_L \times A} \quad (11)$$

Here RSNM, WM, and HSNM is considered as read, write and hold stability of the cell. T_{RA} and T_{WA} is the term which indicate the Read and write access times, respectively. P_R are read and write power P_W dissipation of cell. P_L denotes the leakage power of the cell during standby mode. Area of the cell is indicated by A. Fig.15 shows the overall quality of all simulated SRAM topologies with reference to (w.r.t) Conv. 6T SRAM cell. It is evident from Fig.15 that the LP9T SRAM cell seems to have the utmost EQM value of all the cells considered.

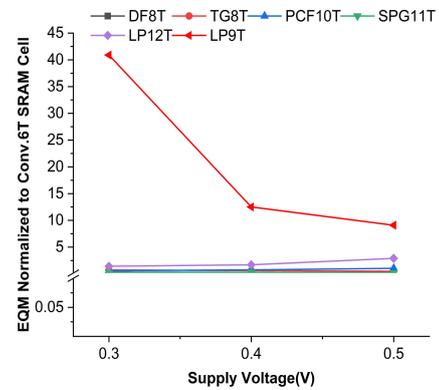


Fig. 15: Overall performance of SRAM cells

Table 2: SRAM characteristics at 0.3V Supply voltage

SRAM Parameters	Conv.6T [28]	DF8T [21]	TG8T [26]	PCF10T [18]	SPG11T [20]	LP12T [19]	LP9T
Vdd	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Read Power(nW)	1.44	1.40	1.25	1.20	1.37	1.22	0.87
Write Power(nW)	0.51	0.87	0.49	0.47	1.1	0.58	0.24
Leakage Power(pW)	2.04	2.69	2.34	2.13	1.88	1.47	1.08
Read Current(nA)	5.17	5.51	5.17	5.0	5.01	5.48	7.07
Read delay(nS)	5.84	5.38	7.63	17.52	7.5	11.96	2.15
Write delay(nS)	8.37	9.37	18.01	13.94	24.53	17.53	8.58
HSNM(mV)	110	110	110	110	109	110	110
RSNM(mV)	40	52	48	110	109	110	110
WM(mV)	102	78	114	106	140	197	210
I_{on}/I_{off} (MC)	1.14	1.61	1.13	1.47	1.19	0.76	3.32
Normalized area w.r.t 6T SRAM	1×	1.59×	1.56×	1.66×	2.81×	2.08×	1.52×

4 Conclusion

In this paper, after surveying the lot of latest research papers, a new LP9T SRAM cell has been developed. The achieved characteristics of SRAM cells are concise in the form of table 2. This LP9T cell demonstrates a substantial decrease in read and write power dissipation and a boost in read-access time relative to the considered SRAM cells. Proposed LP9T SRAM cell is free from half select issue and also shows an enhancement in read and write margin. An analytical model has been presented to evaluate the read current and bit-line leakage current. The I_{on}/I_{off} ratio of the proposed cell is significantly improved which represents higher bit cell density. The trade-off related to such improvements is increased in cell area. Furthermore, this cell demonstrates its robustness against process variation effects in the sub-threshold region using the Monte-Carlo simulations. Hence, the proposed 9T SRAM cell is a viable choice in scaled technology for low-power, high-noise tolerant SRAM cells.

5 Declarations

In this research, there is no fund has provided by any organization. The authors do not have any conflicts.

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Figures

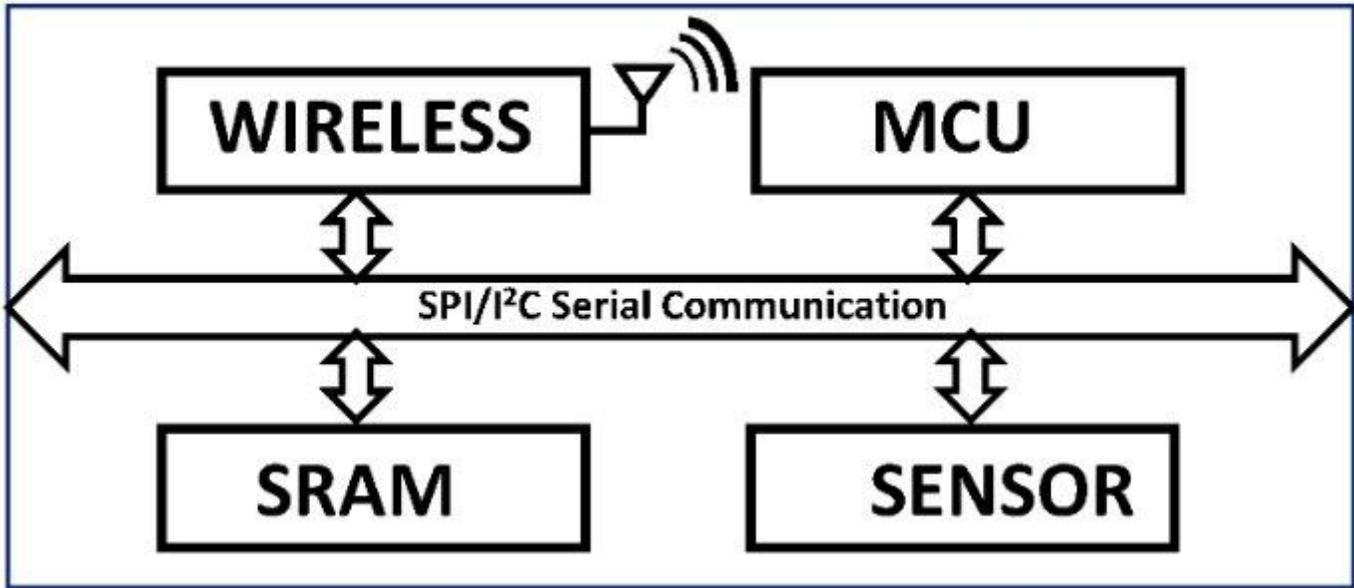


Figure 1

Typical IoT sensor node

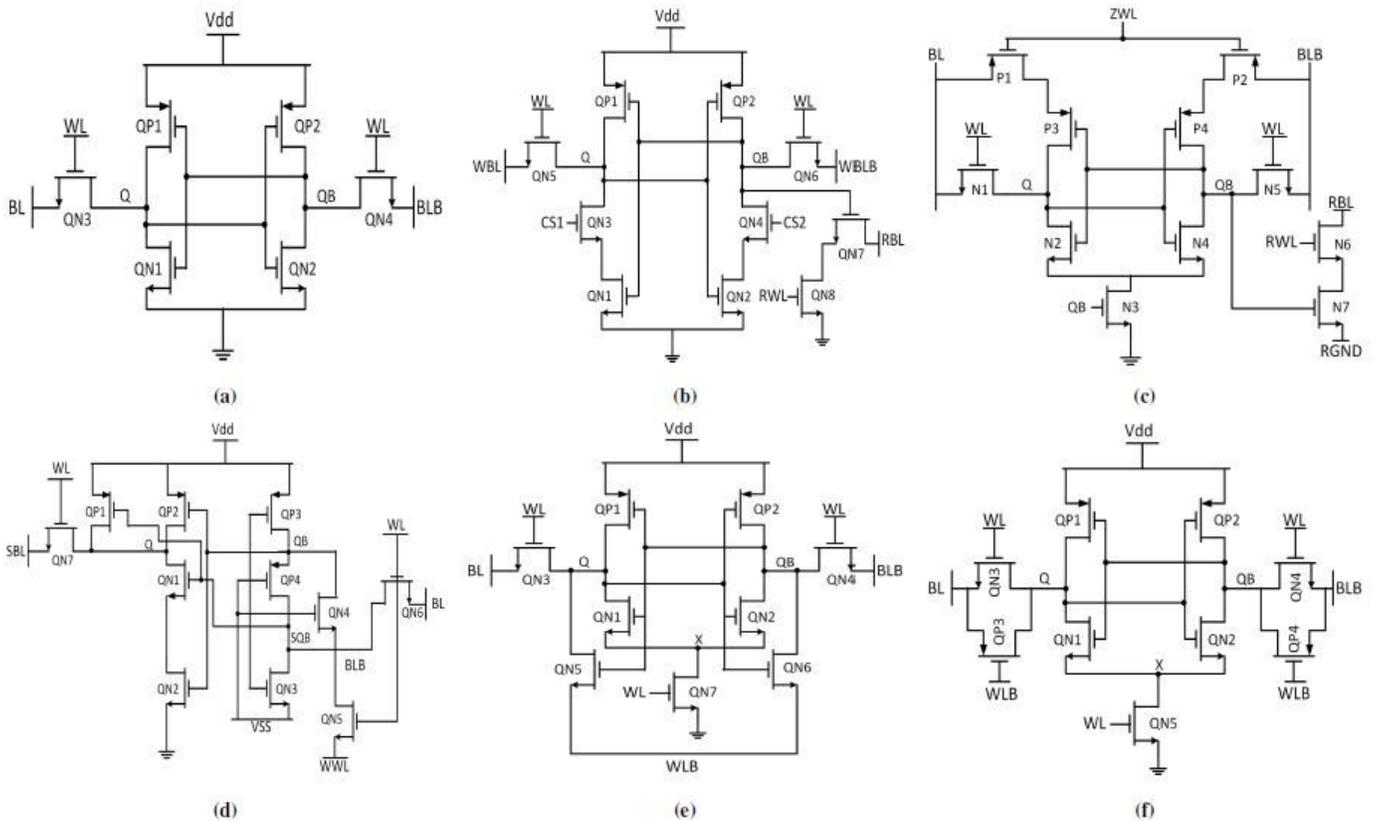


Figure 2

Schematic of considered (a) Conv.6T,(b) PCF10T,(c) LP12T,(d) SPG11T,(e) DF8T ,(f) TG8T SRAM cells

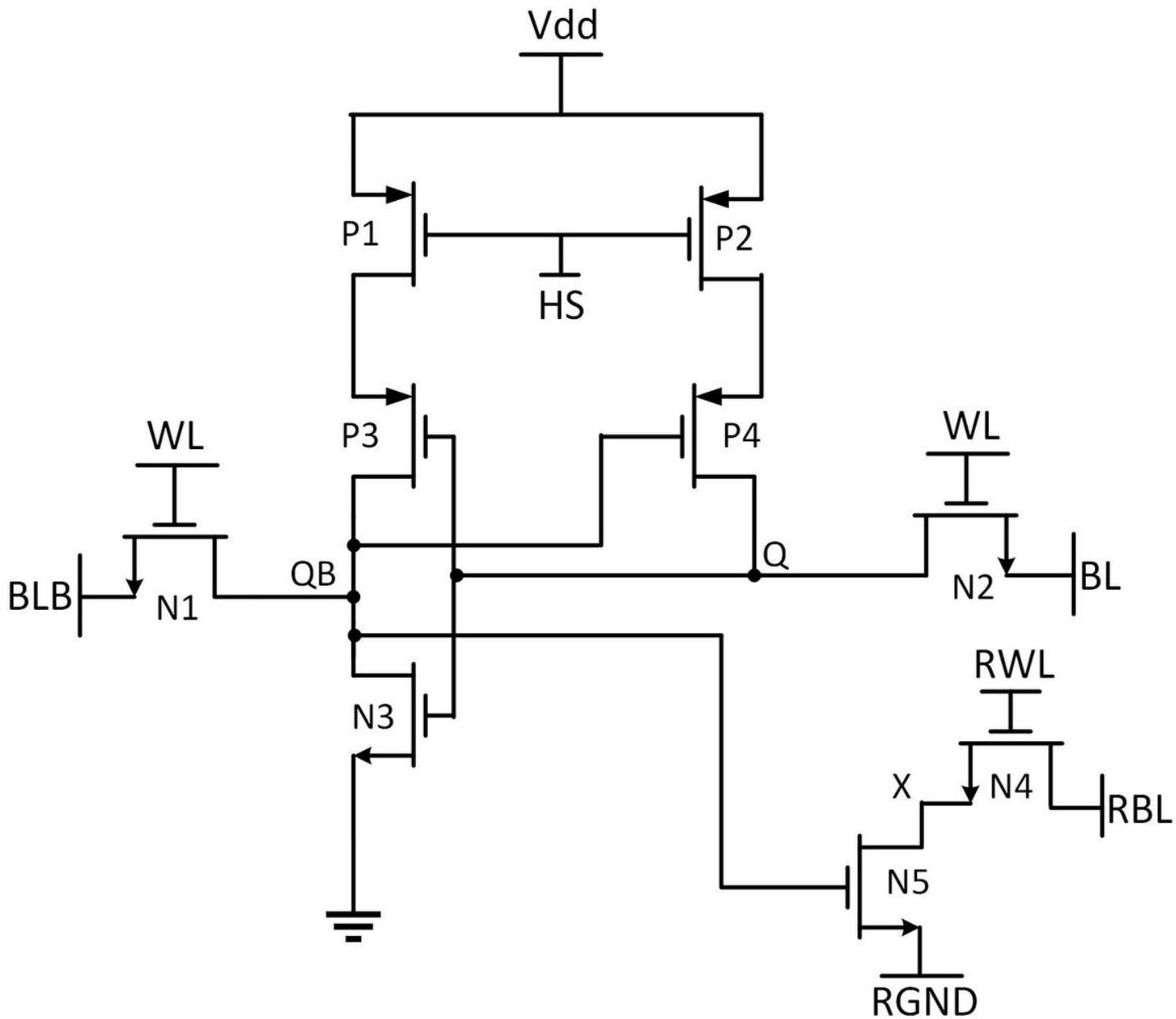


Figure 3

Proposed LP9T SRAM cell

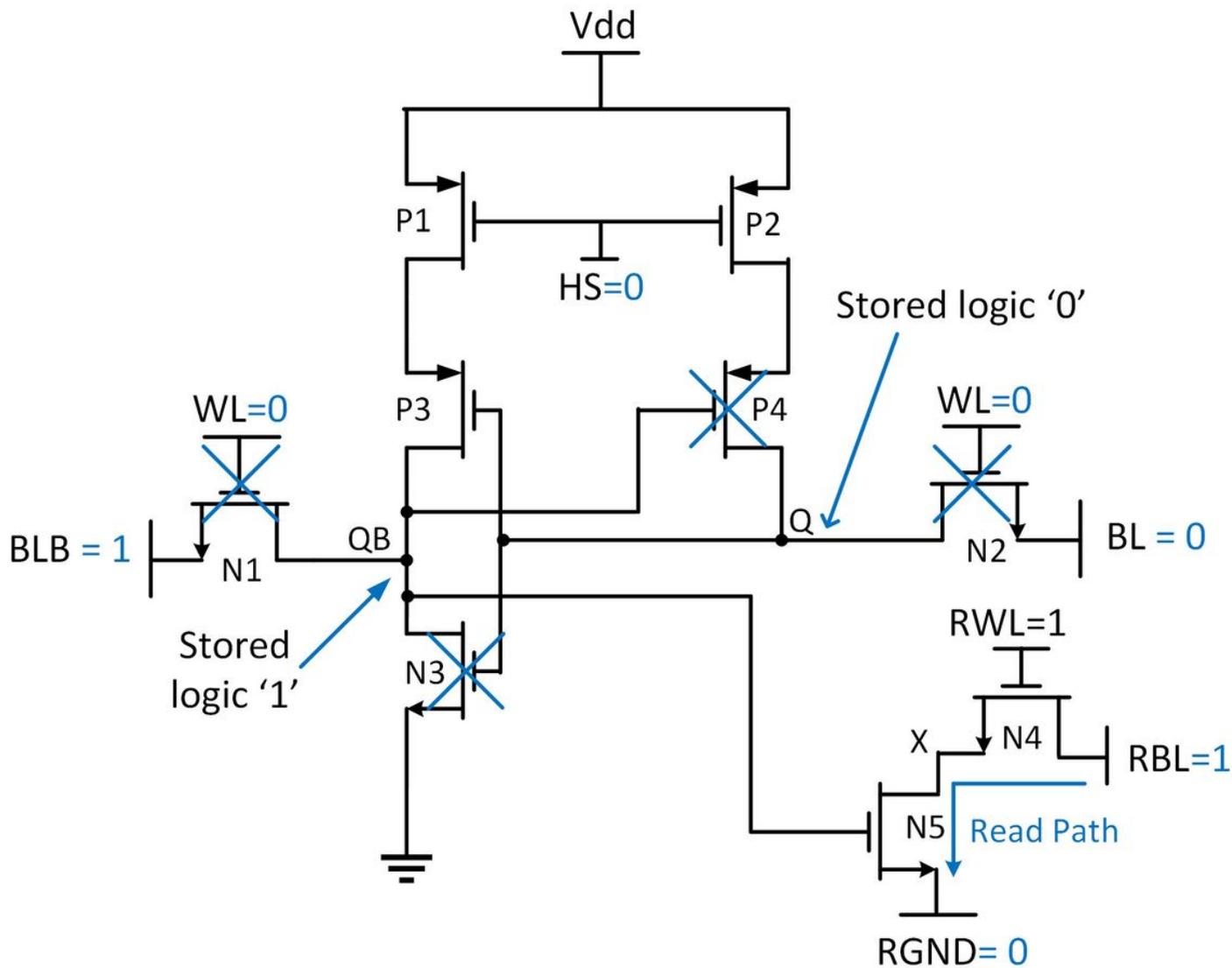


Figure 4

LP9T SRAM during read operation

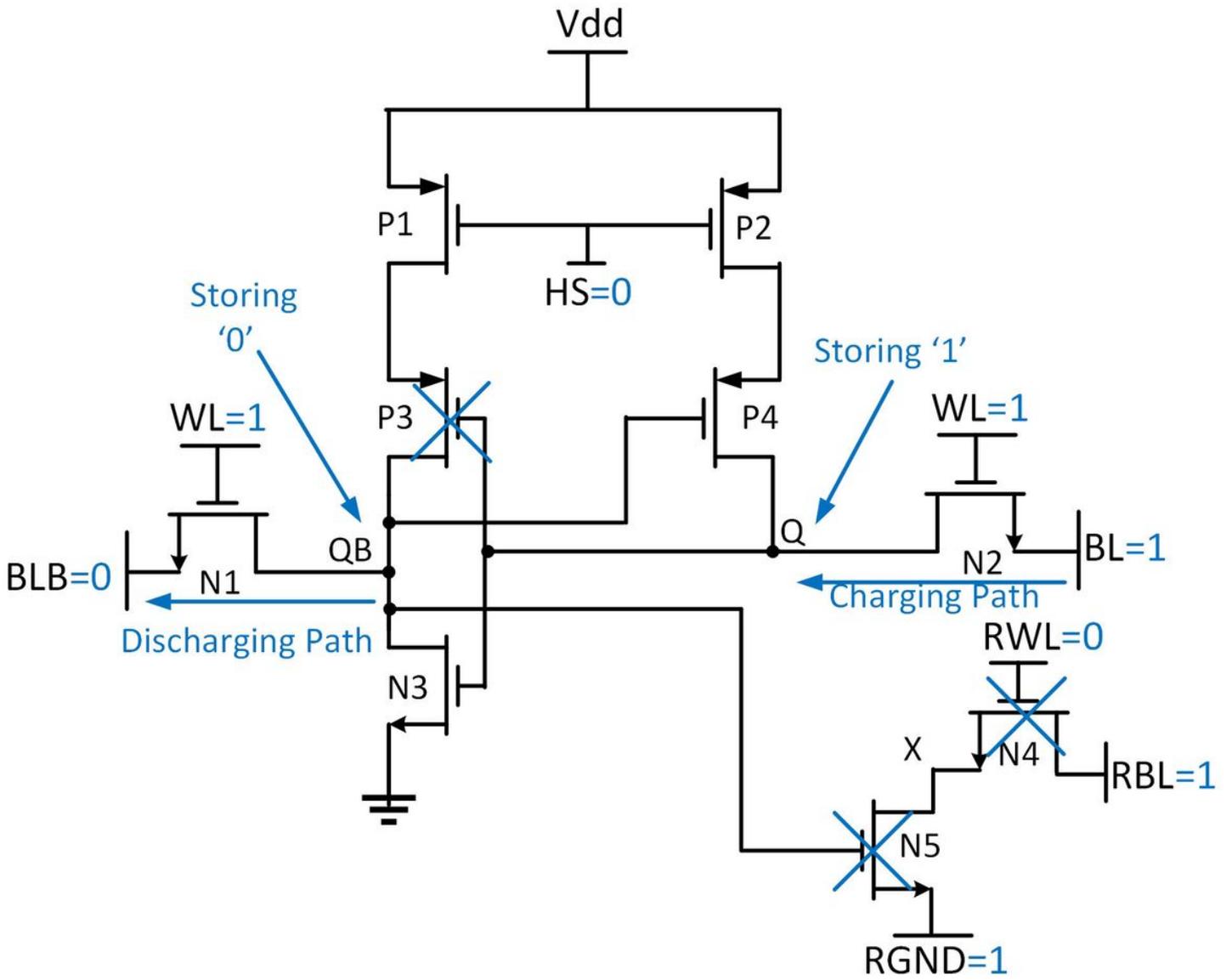
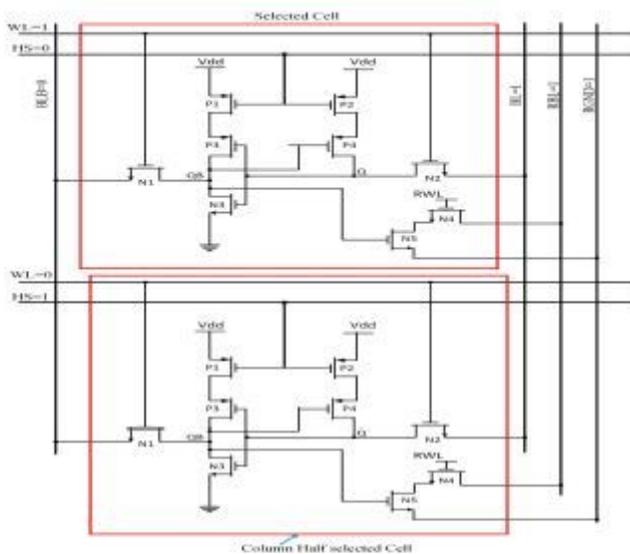
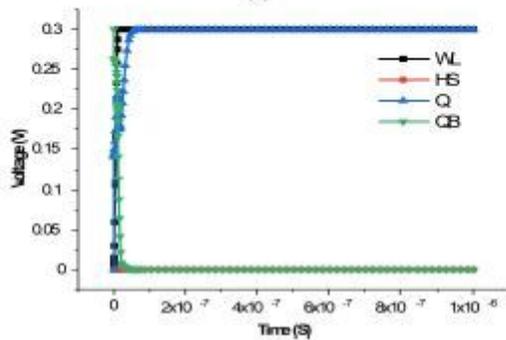


Figure 5

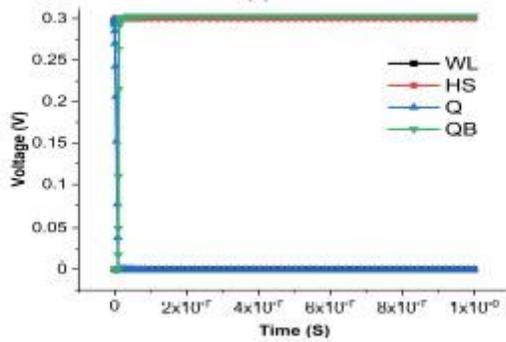
LP9T SRAM during Write operation



(a)



(b)



(c)

Figure 6

(a) Elimination of Column Half selected issue in LP9T SRAM cell, (b) Transient wave form of selected cell, (c) Transient wave form of unselected cell during write operation.

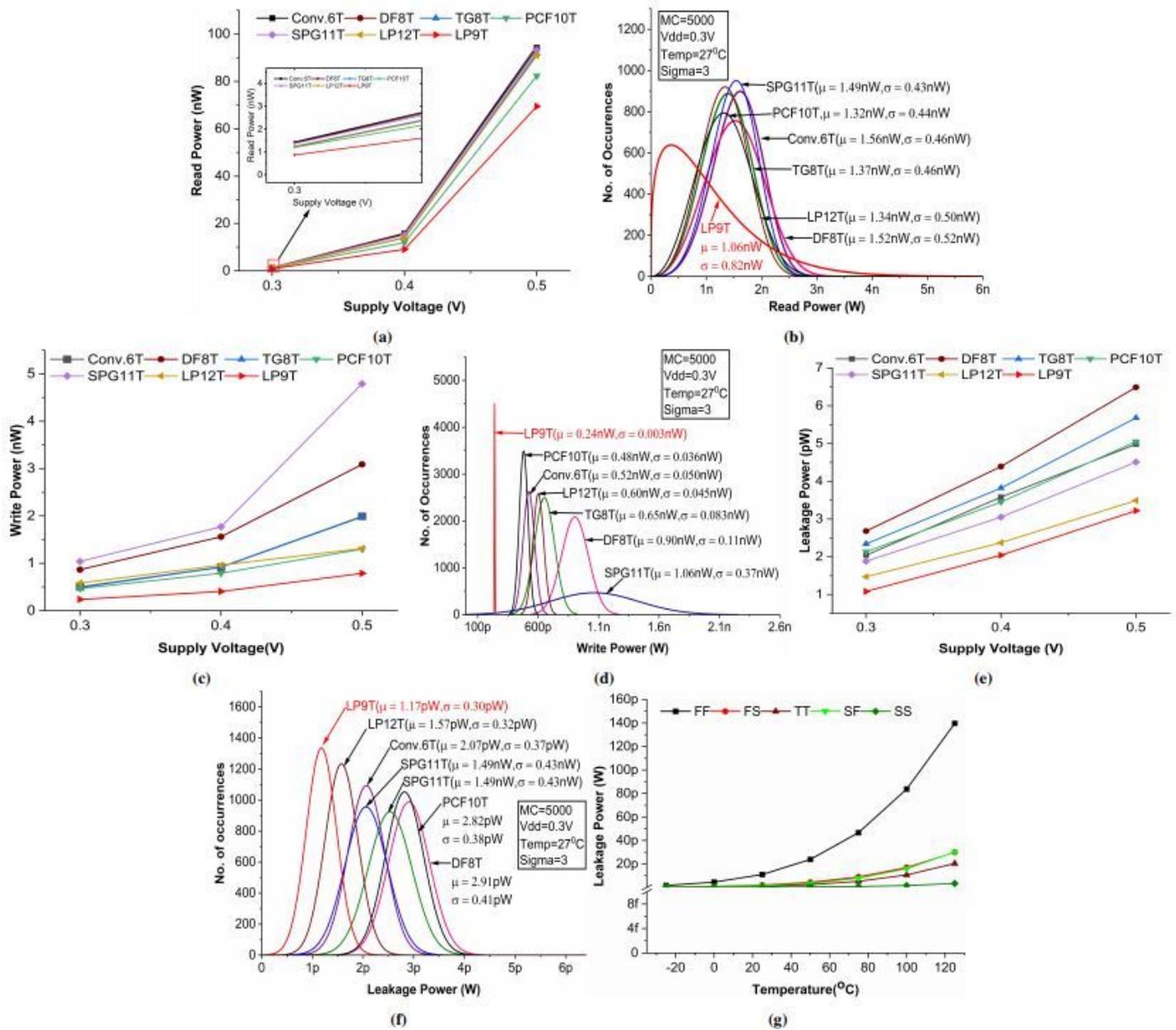
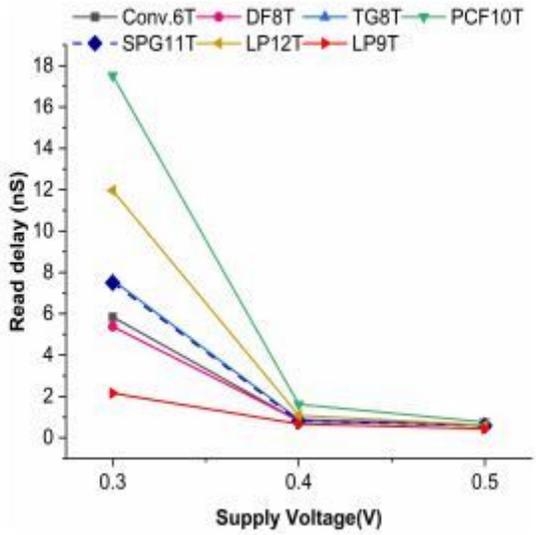
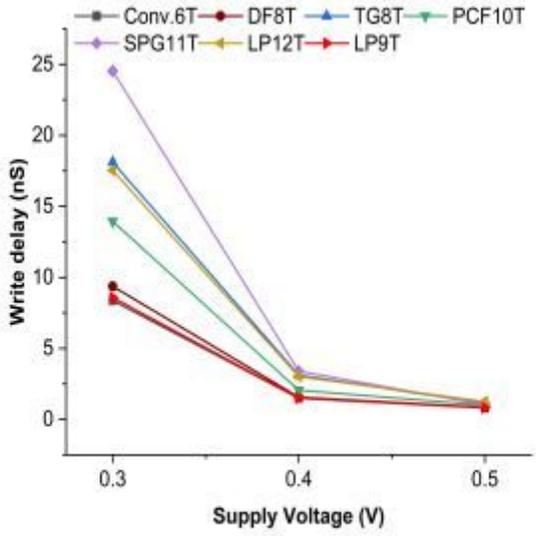


Figure 7

(a) Read Power at different supply voltage, (b) MC of read power at 0.3V, (c) Write power at different supply voltage, (d) MC of write power at 0.3V, (e) Leakage power at different supply voltage, (f) MC of leakage power at 0.3V, (g) Leakage power with temperature at 0.3V supply voltage.



(a)



(b)

Figure 8

(a) Read delay at different supply voltages, (b) Write delay at different supply voltages

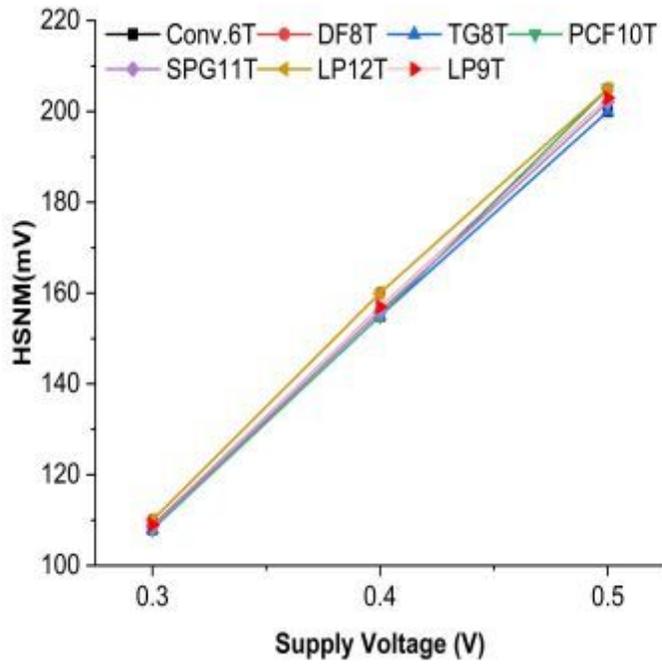


Figure 9

HSNM at different supply voltage

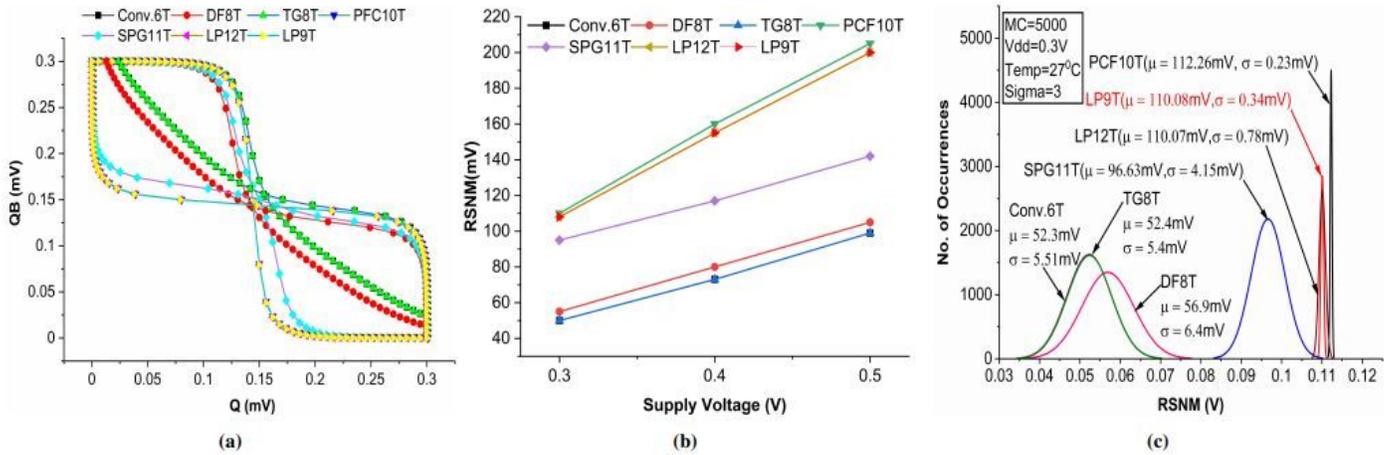


Figure 10

(a) Butterfly curves of SRAM cell, (b) RSNM at different supply voltages, (c) MC simulation of RSNM at 0.3V supply voltage.

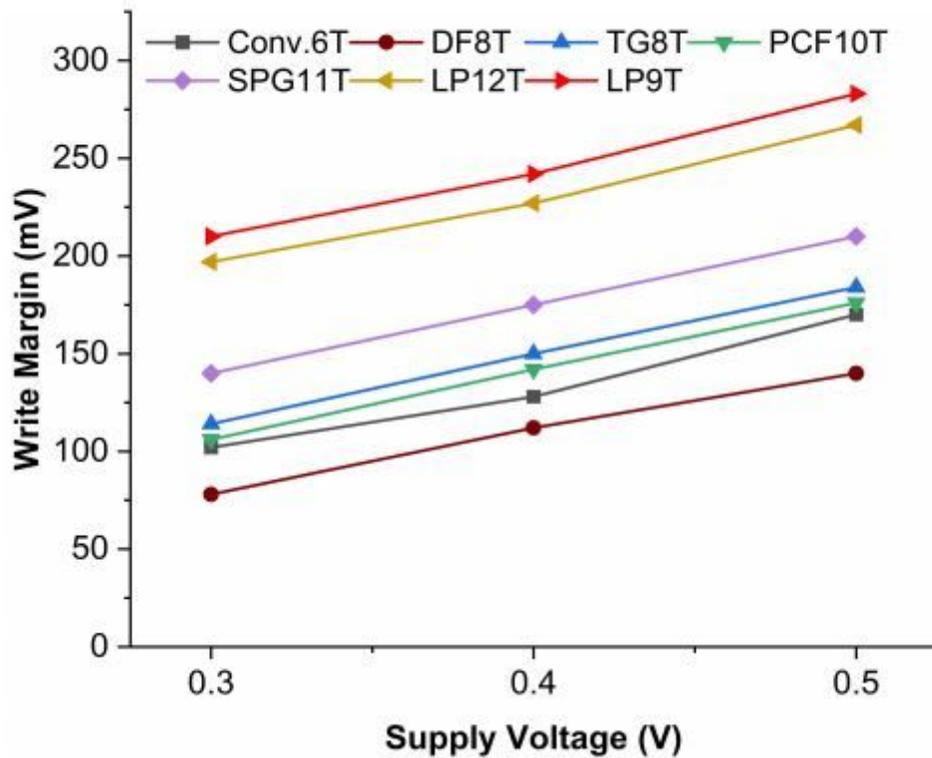


Figure 11

Write margin of SRAM cells

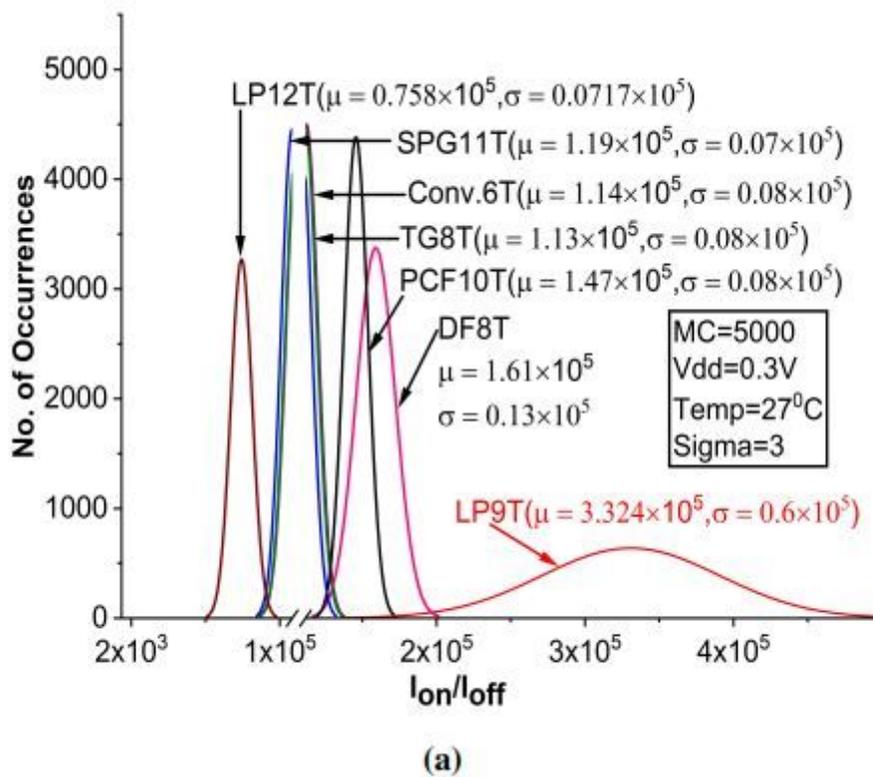


Figure 12

MC of Ion/Ioff ratio at 0.3V supply voltage

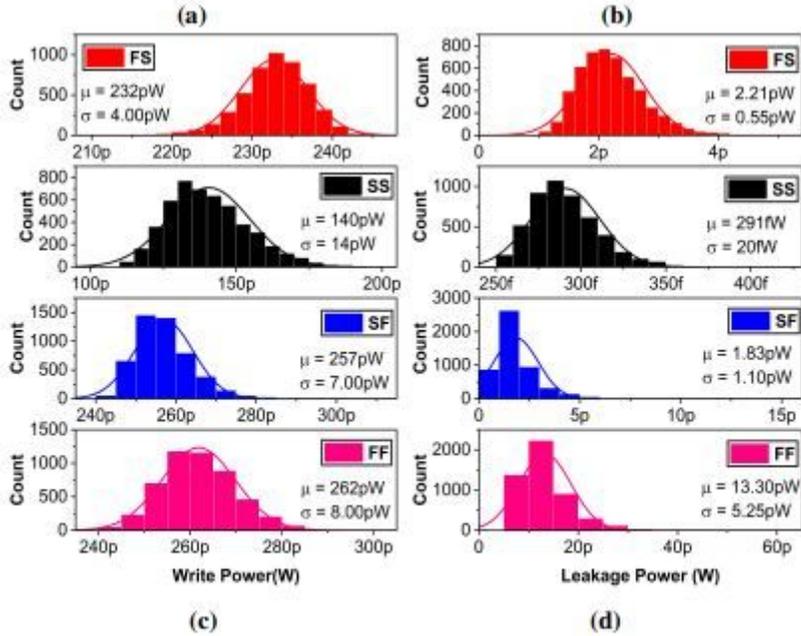
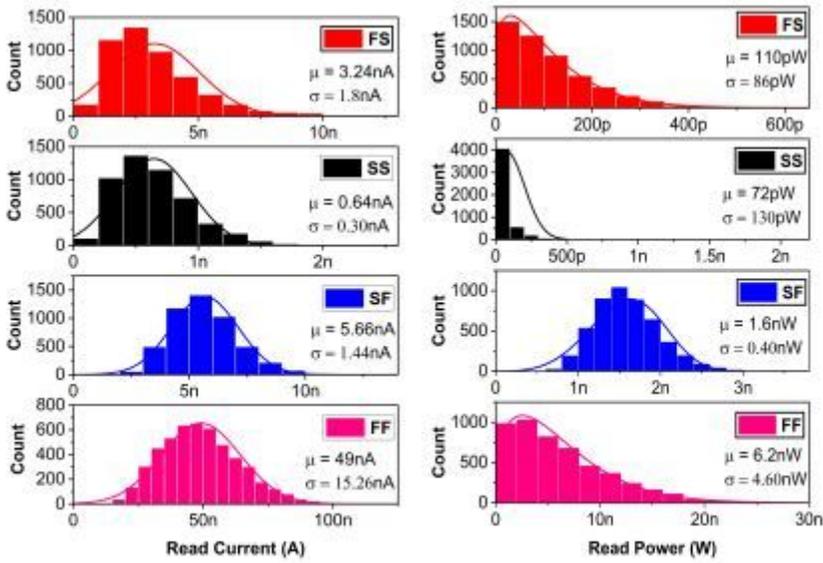


Figure 13

LP9T SRAM cell (a) Read Current at Corners,(b) Read Power at Corners,(c) Write Power at Corners,(d) Leakage Power at Corners

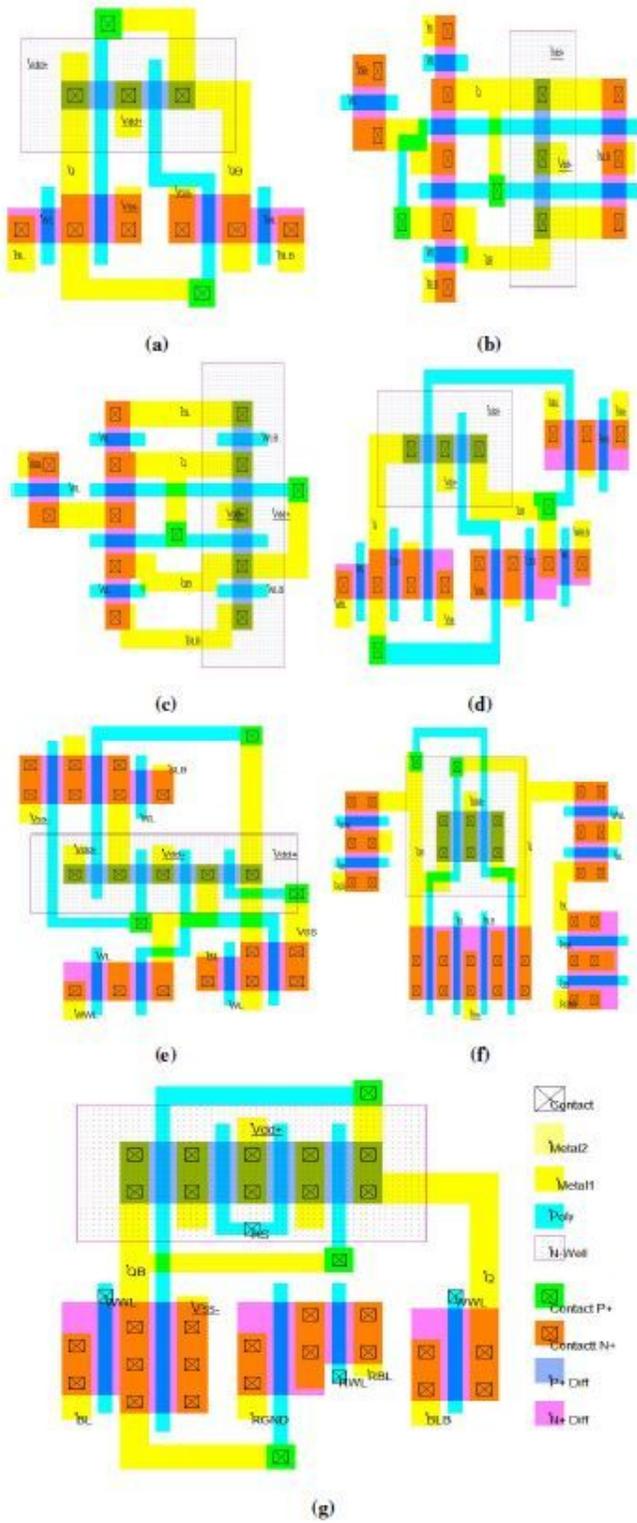


Figure 14

Layout of (a) Conv.6T, (b) DF8T, (c) TG8T, (d) PCF10T, (e) SPG11T, (f) LP12T, (g) Proposed LP9T SRAM cell

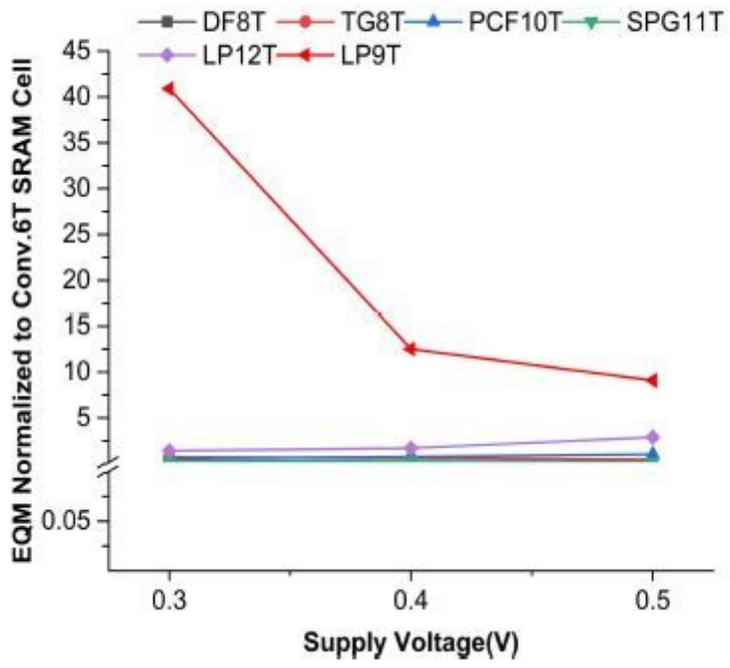


Figure 15

Overall performance of SRAM cells