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# Scalable High-Speed Hybrid Complementary Integrated Circuits based on Solution-Processed Organic and Inorganic Transistors

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## Abstract

Printed electronics offer a cost-efficient way to realise flexible electronic devices. The combined use of p-type and n-type semiconductors would yield silicon-like integrated circuits with low power consumption and stability. However, printing complementary circuits is challenging due to a lack of suitable material systems. To counter this, we employed a hybrid system to integrate p-type organic semiconductors (OSCs) and n-type amorphous metal oxide semiconductors (MOSs). These damage-free patterned OSC- and MOS-based thin-film transistors with improved process durability allowed the fabrication of hybrid complementary circuits on flexible substrates. These inverters functioned well even after exposure to air for 5 months. A large noise margin and power gain of 38 were realised with a supply voltage as low as 7 V. Furthermore, a five-stage ring oscillator with a stage propagation delay of 1.3 μs was achieved, which is the fastest operation ever reported for printed, flexible complementary inverters.

## Introduction

The rapid implementation of Internet of Things (IoT) in everyday applications and devices has increased the demand for trillions of electronic devices. Though the conventional Si-based technology can meet the electrical performance requirements of these devices, the complex, vacuum-based, and high-temperature processes required to fabricate them are driving up costs. In addition, in terms of flexible applications, the mechanical properties of conventional devices are far from satisfactory. Printed electronics, which allow the ideal production of low-cost and flexible electronic elements, are of vital interest to both industry and academia. Printing complementary integrated circuits (ICs) with high-mobility and performance-balanced p- and n-channel thin-film transistors (TFTs) is crucial in advanced applications such as radio-frequency identification (RFID) tags and sensors as they can enable high operation speeds, low power dissipation, high noise margin, and an easy and compact circuit design.

Among the available printable semiconductor materials, organic semiconductors (OSCs) are the most promising owing to their low fabrication temperature and high compatibility with flexible substrates[1]. Thus far, several materials and device-fabrication methods have been developed to facilitate the implementation of OSCs in ICs, especially for single or well-aligned crystals[2–9]. Meanwhile, solution-processable amorphous metal oxide semiconductors (MOSs) have been developed as potential candidates for printed n-channel TFTs[10–15] because of their high electron mobility, excellent uniformity, and good ambient stability. Despite the advancement of p-type OSCs and n-type MOSs, both systems are encumbered by a unipolar nature[16–18]. The development of n-type OSCs is still lagging behind that of their p-type counterparts owing to their less effective packing structure and energetics of electron injection[19]. Similarly, p-type MOSs rarely exhibit high performance owing to difficulties in hole formation and the unfavourable hole-transport path due to the presence of highly

occupied localised oxygen 2*p* orbitals[20]. Such a lack of suitable material systems restricts the implementation of solution-processed semiconductors in advanced complementary ICs composed of p- and n-channel TFTs on the same substrate. Therefore, most of the reported solution-processed ICs are used for ambipolar operation with single p-type OSCs or n-type MOSs[21–25] or complementary circuits with an unsatisfactory performance[26–31].

Hybridisation is one way to overcome the limitations faced by a single material and this approach has been used to build complementary circuits[16–18]. However, hybrid complementary ICs based on solution-processed p-type OSCs and n-type MOSs have rarely been demonstrated despite their promise (although single complementary inverters have often been reported)[17,18,32,33]. This is probably due to the different and complex chemical characteristics of the materials being integrated into the same circuit. For instance, OSCs are self-assembled in solid states *via* weak van der Waals forces, whereas MOSs are covalently linked, which leads to inconsistencies between their processing parameters, such as temperature, heat and chemical resistance, and adaptability to lithographic processes. In addition, fine patterning is mandatory in both semiconductors and electrodes to avoid crosstalk and realise high-speed operations. Therefore, the scalable fabrication of high-performance OSC-MOS hybrid complementary ICs with a high degree of integration of their finely patterned TFTs on the same substrate is challenging. Although a few solution-processed hybrid complementary ICs have been demonstrated with photolithographic processes, their performances, such as mobility and the on-off switching rate of TFTs, were compromised because of the low mobilities of the macromolecular OSCs used and the chemical degradation of MOSs[34,35]. The fabrication of advanced flexible devices introduces additional difficulties due to the instability of conventional flexible substrates, such as their poor heat and chemical resistance[36–38].

In this study, we demonstrate complementary ICs composed of solution-processed TFTs based on single crystals of a small-molecule OSC, 3,11-dinonylldinaphto[2,3-*d*:2',3'-*d'*]benzo[1,2-*b*:4,5-*b'*]dithiophene ($C_9$-DNBDT-NW), and amorphous indium zinc oxide (IZO) as the p- and n-channel materials, respectively. These materials were selected because of their high carrier mobility, uniformity, and scalability[39,40]. A technology was developed for scaling up these systems for high-speed operations with a special focus on damage-free patterning for both OSC- and MOS-based TFTs and the process durability of MOS-based TFTs for further integration. In the following sections, we shall describe these flexible hybrid complementary inverters, which exhibit desirable switching properties, excellent long-term stability, and good flexibility. Five-stage complementary ring oscillators were used to discuss the stage propagation delay of the fabricated hybrid inverters. We achieved a propagation delay of 1.3 μs with an operation voltage of 10 V, which indicates that this facile method combining the advantages of p-type OSC and n-type MOS can potentially meet future IoT demands.

## Results

### Integrated process

The hybrid complementary inverter on a polyimide (PI) substrate with $C_9$-DNBDT-NW single crystals as the p-channel material and amorphous IZO as the n-channel material is schematically illustrated in **Figure 1**. Both the p- and n-channel TFTs have bottom-gate top-contact structures. As illustrated in **Figure S1**, for the IZO-based n-channel TFT, gate electrodes were fabricated by photolithography and a lift-off process. Meanwhile, the $AlO_x$ gate dielectric layer was formed by atomic layer deposition (ALD). The IZO layer was deposited by spin coating and patterned via photolithography and wet-etching. To reduce the number of photolithography steps, source/drain (S/D) electrodes of n-channel TFTs and gate

electrodes of p-channel TFTs were fabricated simultaneously. Polymethylmethacrylate (PMMA)/parylene acts as a gate dielectric for p-channel TFTs and doubles as a passivation layer for n-channel TFTs to protect the back-channel of IZO-based TFTs against potential damage during subsequent integration processes. $C_9$-DNBDT-NW was formed using a continuous edge casting method[8,41] and then transferred to the top of the PMMA/parylene dielectric layer[42].

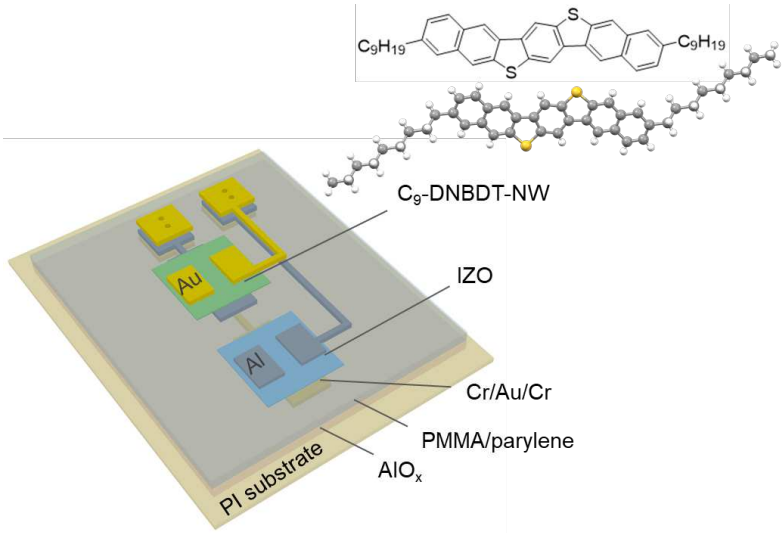


**Figure 1** Schematic structure of a hybrid complementary inverter with IZO as the n-channel material and $C_9$-DNBDT-NW single crystal as the p-channel material

A cross-polarised optical micrograph of $C_9$-DNBDT-NW single crystals on the as-fabricated IZO-based TFTs before patterning (**Figure S2**) revealed a clear crystal domain. Scanning electron microscopy (SEM) images of the cross-section of the $C_9$-DNBDT-NW channel produced by focused ion beam (FIB) machining indicated that almost no gate barrier was formed on the edges of the gate electrode of the p-channel TFT (**Figure S3**), which was key to the successful fabrication of the $C_9$-DNBDT-NW single crystal layer. OSC patterns and Au S/D electrodes were formed via a two-step patterning process, in which photosensitive dielectric materials (PDMs, a dry-film photoresist)/PMMA double sacrificial layers were employed for a damage-free patterning of OSC-based TFTs. As shown in **Figure S4**, PDM

(the top layer) enables the formation of the OSC and S/D patterns while PMMA facilitated the stripping of the resist with acetonitrile, thus causing little damage to the OSC. The dry-film photoresist PDM was laminated on the substrate and patterned by photolithography[43,44], while the PMMA layer was deposited via spin coating and etched with $O_2$ plasma. Furthermore, the PDM dry film contributed to the damage-free fabrication of OSC-based TFTs as the solvent content in the PDM dry film was less than 2 wt.% and the PDM patterning process is based on the polymerization of double bonds rather than the generation of photoacids. Therefore, the potential damage induced by solvents or acids in conventional photolithography could be eliminated effectively. The contact resistance ($R_c$) of $C_9$-DNBDT-NW-based TFTs fabricated by this technology was studied using the transfer-line method, as described in the Supporting Information (**Section S1**). The intrinsic mobility ($\mu_{int}$) of $C_9$-DNBDT-NW TFTs was ~10 $cm^2$ $V^{-1}$ $s^{-1}$ and the normalised contact resistance ($R_cW$) was ~230 Ω cm (**Figure S5**), which is a low value for OSCs without extra doping[6]; this implies a high effectiveness of carrier injection in the fabricated $C_9$-DNBDT-NW-based TFTs.

**Electrical performance of the hybrid inverters**

The electrical properties of the p- and n-channel TFTs were evaluated. A micrograph of a complementary inverter with channel width/channel length ($W/L$) of 200 μm/9 μm for the $C_9$-DNBDT-NW p-channel and 200 μm/13 μm for the IZO n-channel is shown in the inset of **Figure 2**(a). The output curves revealed that both the n- and p-channel TFTs exhibited a typical output with good pinch-off behaviour and negligible hysteresis (**Figure 2**(a)). The transfer characteristics of each TFT in the linear and saturation regions are illustrated in **Figure 2**(b)–(e). In the case of $C_9$-DNBDT-NW-based TFTs, transfer curves in the linear ($V_D$ = –1 V, **Figure 2**(b)) and saturation ($V_D$ = –10 V, **Figure 2**(d)) regions indicated a linear mobility ($\mu_{lin}$), saturation mobility ($\mu_{sat}$), on-off current ratio ($I_{on}/I_{off}$), off current ($I_{off}$), and turn-on voltage ($V_{on}$) of 5.8 $cm^2$ $V^{-1}$ $s^{-1}$, 5.1 $cm^2$ $V^{-1}$ $s^{-1}$, ~$10^8$, $10^{-12}$ A, and ~2 V,

respectively; the corresponding values in the IZO TFT were 2.9 $cm^2 V^{-1} s^{-1}$, 4.0 $cm^2 V^{-1} s^{-1}$, ~$10^8$, $10^{-12}$ A and ~0 V, respectively (**Figure 2**(c) and (e)).

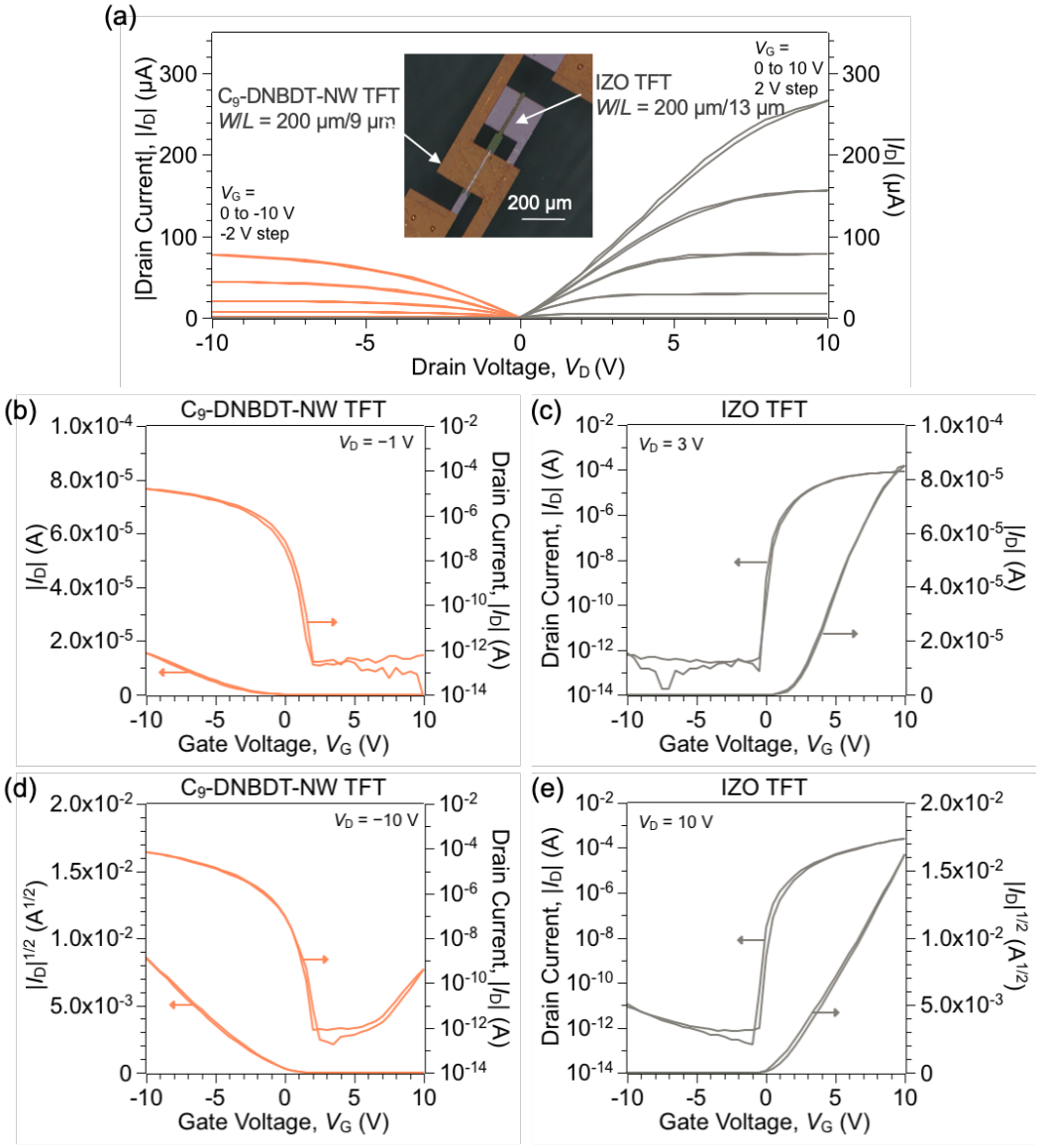


**Figure 2** Electrical performance of C9-DNBDT-NW- and IZO-based TFTs. (a) Output performance. The inset shows a micrograph of a complementary inverter with $W/L$ = 200 μm/9 μm for the C9-DNBDT-NW p-channel and 200 μm/13 μm for the IZO n-channel. (b)–(e) Transfer characteristics in the linear region and the saturation region

Due to contact resistance, the effective mobility ($\mu_{eff}$) is lower than $\mu_{int}$, especially in short-channel devices, as shown in Equation (1),

$$\mu_{\text{eff}} = \mu_{\text{int}} \frac{1}{1+\frac{R_C W}{L}\mu_{\text{int}} C_i (V_G - V_{\text{th}})} \quad (1)$$

where $C_i$ is the gate capacitance per unit area, $V_G$ represents gate voltage, and $V_{th}$ is the threshold voltage. The $\mu_{eff}$ of the C9-DNBDT-NW-based TFT was estimated to be ~5.9 $cm^2$ $V^{-1}$ $s^{-1}$, which is similar to the experimental value. In the case of the IZO-based TFT, $R_C$ was estimated to be 29 Ω cm and the effective resistance measured after the integration process is at similar to that of IZO TFTs before integration[40]. The good performance of C9-DNBDT-NW- and IZO-based TFTs can be attributed to the high performance of the semiconductor materials and the well-designed integration processes. Patterned gate electrodes and short channels lead to degraded performance[45], especially in TFTs with bottom-gate top-contact structures. This may be because 1) as the channel length decreases, contact resistance starts to dominate, 2) the S/D patterning process may damage the semiconductor layer, and 3) the uneven surface caused by patterned gate electrodes may affect the uniformity of the active layer in the solution-processed semiconductor. In this study, these problems were solved by using damage-free processes for both p- and n-channel TFTs, controlling the thickness and edge conditions of the gate electrode, and improving the process durability of IZO-based TFTs during p-channel TFT integration, which was processed with a bilayer PMMA/parylene passivation structure.

A hybrid complementary inverter was formed by connecting the gate electrodes of p- and n-channel TFTs as an input terminal and the corresponding drain electrodes as an output terminal, as shown in **Figure 3**(a). **Figure 3**(b) shows the voltage-transfer curves (VTCs) of the complementary inverter discussed in the previous section with applied voltage ($V_{DD}$) in the range of 2 to 10 V. Significantly, the inverter exhibited a good rail-to-rail performance with a full output-voltage swing and negligible hysteresis at each $V_{DD}$. The corresponding voltage gain and static current ($I_{supply}$) values are shown in **Figure 3**(c) and (d), respectively.

At a $V_{DD}$ of 7 V, a nearly symmetrical VTC with a midpoint voltage ($V_M$) of 3.42 V and maximum voltage gain of 38 V/V was observed. At $V_{in}$ = 0 V, $I_{supply} \sim 1.0 \times 10^{-9}$ A and this value increased to ~0.1 μA at $V_{in} = V_{DD}$ (2–10 V) (**Figure 3**(d)). Although the static current at a high $V_{in}$ was several orders higher than that at a low $V_{in}$, the static power consumption was still less than 0.76 μW at $V_{DD}$ = 7 V. Because the current ($I_D = 3 \times 10^{-7}$ A) of the p-channel TFT at $V_G$ = 0 V or $V_{in}$ = 7 V was 5 orders of magnitude higher than that ($I_D = 1 \times 10^{-12}$ A) of the n-channel TFT at $V_G$ = 0 V or $V_{in}$ = 0 V (**Figure S6**) higher static currents were observed at high $V_{in}$ values. Our future work will aim to control $V_{on}$ for p-channel TFTs to further lower the static power consumption of hybrid complementary inverters. **Figure 3**(e) shows the VTC obtained with a $V_{DD}$ of 7 V; the noise margins high ($NM_H$) and noise margin low ($NM_L$) are indicated by green rectangles ($NM_H$ = 2.7 V and $NM_L$ = 1.9 V).

It is particularly important to note that the hybrid complementary inverter exhibited a decent performance even after exposure to the ambient atmosphere (air) for 5 months (**Figure 3**(f)). The transfer characteristics of p- and n-channel TFTs before and after exposure to air for 5 months were recorded (**Figure S7**). In the case of both $C_9$-DNBDT-NW- and IZO-based TFTs, the off current increased slightly. This may be attributed to a self-healing effect in which the number of carrier traps decreased slightly over time [6,46]. One possible reason for the slight $V_{on}$ shift of the IZO TFT may be the diffusion of environmental molecules such as oxygen and water because the current passivation layer, PMMA/parylene, could not isolate the device completely. The passivation technique is being studied to further stabilise these devices.

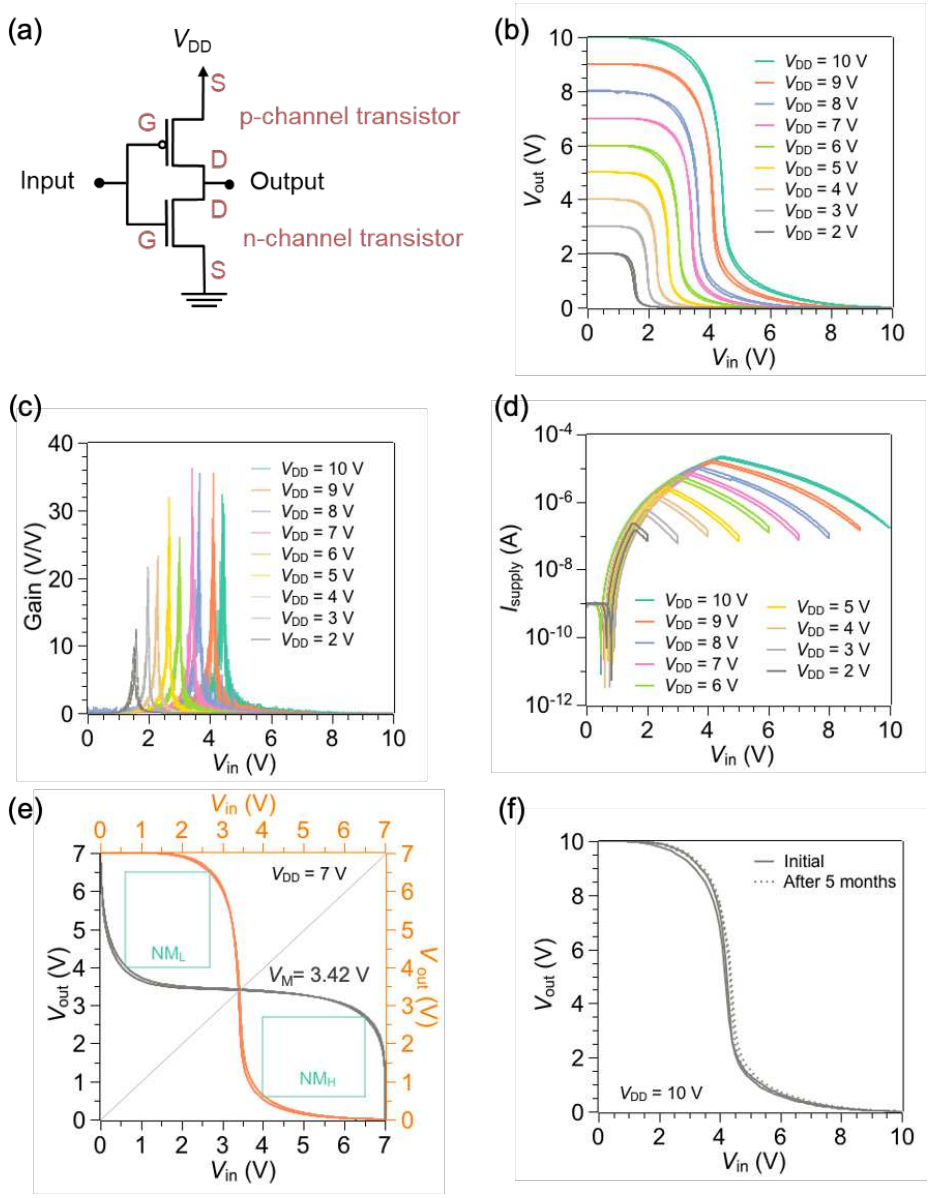


**Figure 3** Electrical performance of the hybrid inverter shown in Figure 2. (a) Circuit of a complementary inverter. (b) VTCs, (c) voltage gains, and (d) static current at $V_{DD}$ = 2–10 V. (e) VTCs at $V_{DD}$ = 7 V with noise margins represented by the green rectangles. $V_M$ = 3.42 V, $NM_H$ = 2.5 V, and $NM_L$ = 1.9 V. (f) VTCs before and after exposure to air for 5 months ($V_{DD}$ = 10 V)

**Flexibility of the hybrid inverters**

The PI substrate was delaminated from the glass support using a laser lift-off (LLO) method to evaluate the flexibility of the as-fabricated inverters. **Figure 4**(a) shows a photograph of the

ICs on a free-standing PI film and **Figure 4**(b) compares the VTCs obtained before and after delamination at $V_{DD}$ = 4, 6, 8, and 10 V. The overlap between the VTCs at each $V_{DD}$ indicated that the LLO process did not adversely affect the electrical performance of the inverter.

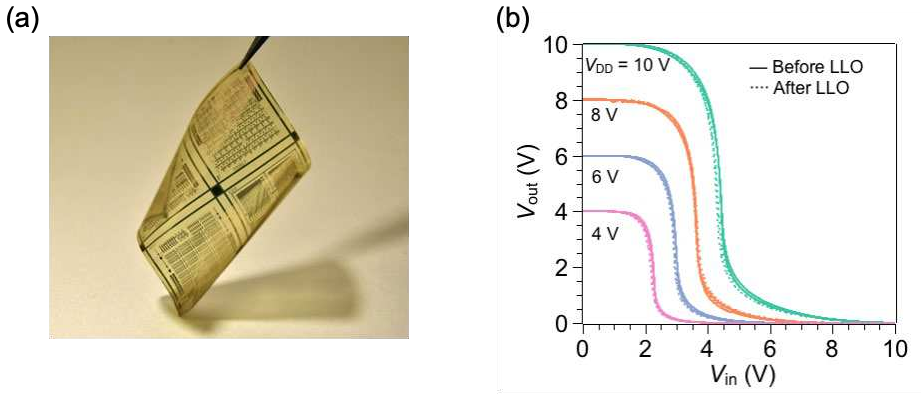


**Figure 4** Properties of the hybrid inverter before and after delamination from glass supports. (a) Photograph of the hybrid ICs on a free-standing PI film. (b) VTCs of the hybrid complementary inverter with p- and n-channel *W*/*L* values of 200 µm/9 µm and 200 µm/13 µm, respectively, before and after delamination

To further explore the potential of this hybrid technology for flexible applications, the VTCs of the fabricated inverters were recorded at different bending stresses with a supply voltage of 10 V. When the substrate was curved, the circuits were stretched or compressed. During measurement, the film substrate was attached to the cylindrical surfaces of different radii, which resulted in schematically curved substrates, as shown in **Figure 5**(a). For example, refer to the inset of **Figure 5**(b), which shows the flexibility-measurement setup with a bending radius of 6 mm. **Figure 5**(b) summarises the VTCs of a complementary inverter with p- and n-channel *W*/*L* values of 100 µm/19 µm and 50 µm/24 µm, respectively and flat and bent radii (17.5, 12.0, and 6.0 mm); no significant changes were observed even at a bending radius of 6 mm. The transfer characteristics of each of the fabricated TFTs were examined under similar bending conditions. As shown in **Figure 5**(c)–(f), both the p- and n-channel

TFTs exhibited decent transfer characteristics under the action of a bending stress. The slight $V_{on}$ shift is probably due to system error during measurement[40, 47].The bending stress applied on semiconductors depends not only on the bending radii but also device structure and substrate thickness. The corresponding surface strain ($\varepsilon$) can be calculated using the following equation[48]

$$\varepsilon = \frac{h_s}{2R} \times 100\% \quad (2)$$

where $R$ is the bending radius and $h_s$ is substrate thickness. In addition, when a substrate is bent, there is always a layer with zero bending stress and while the inner surface suffers compression stress, the outer surface suffers tensile stress. In this study, compared with the thickness of substrate PI (~10 μm), the total thickness of the other layers (<500 nm) was negligible; hence, the TFTs experienced a tensile force perpendicular to the channels. In other words, the tensile force was applied in the *c*-axis direction, *i.e.,* the preferred carrier-transport direction in the herringbone packing structure of the $C_9$-DNBDT-NW single crystal, which might decrease carrier mobility[48]. Meanwhile, amorphous IZO was isotopically stressed. Using Equation (2), the maximum tensile stress was estimated to be 0.08% with a bending radius of 6 mm, at which the decrease in mobility was small (1%)[48]; this observation is consistent with our results. In addition, the small tensile stress should have negligible effects on the amorphous IZO layer. Therefore, the identical electrical performance of the inverter under bending conditions suggests that this hybrid technology can enrich flexible electronic applications.

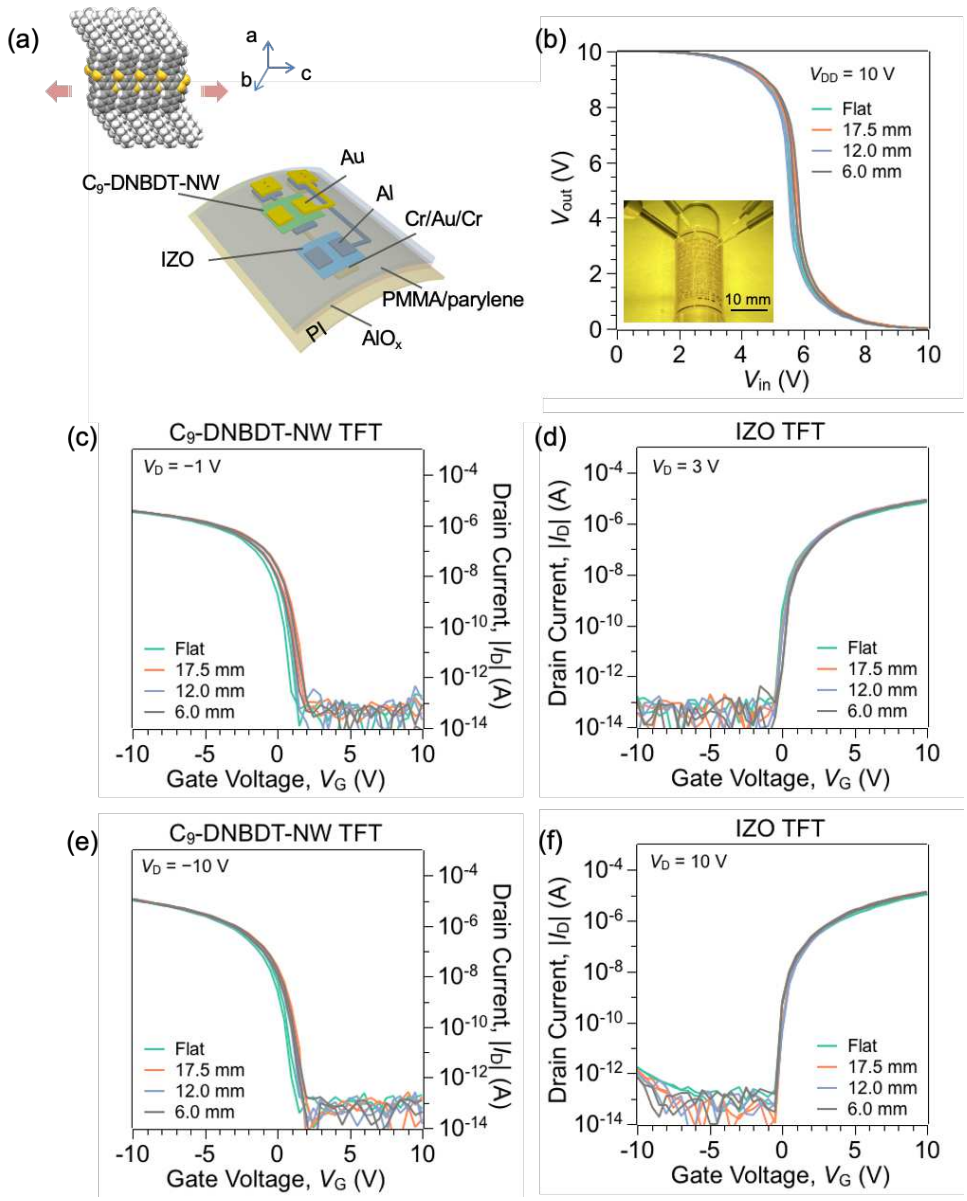


**Figure 5** Electrical performance of a hybrid complementary inverter under bending stress. (a) Schematic illustration of a device under bending stress. (b) VTCs of the inverter when flat and bent to tensile radii of 17.5, 12.0, and 6 mm. The inset shows the measurement setup with a bending radius of 6 mm. Transfer curves of TFTs based on (c and d) C9-DNBDT-NW and (e and f) IZO in the linear and saturation regions under different bending stresses

**Performance of hybrid ring oscillators**

Unlike direct calculation by propagation delay, ring oscillators provide a simple and effective way to evaluate the maximum switching speed of larger logic gates. In a ring oscillator, each

inverter delays the input signal for a specific time, which is defined as the stage propagation delay ($t_p$). To simplify, we assume that all inverters have the same property and the same delay time. The delay time at the output can hence be written as

$$T = 2nt_p \quad (3)$$

where $n$ is the stage number and $T$ is the period of the ring oscillator. By measuring the operation frequency of the ring oscillator ($f_{ROSC}$), $t_p$ can be calculated as shown in Equation (4).

$$f_{ROSC} = \frac{1}{T} = \frac{1}{2nt_p} \quad (4)$$

Five-stage ring oscillators were fabricated by connecting five inverters in a loop to study the propagation delay of the hybrid inverter and the availability of more complex circuits. An optical micrograph of the as-fabricated ring oscillator is shown in **Figure 6**(a). In each stage, the dimensions were $W/L$ = 200 μm/4 μm and $\Delta L$= 3 μm for the p-channel TFT and $W/L$ = 200 μm/8 μm and $\Delta L$= 1.5 μm for the n-channel TFT. The electrical performance of the p- and n-channel TFTs recorded under these conditions is shown in **Figure S8**. The p-channel TFT exhibited $\mu_{lin}$, $\mu_{sat}$, $I_{off}$, and and $I_{on}/I_{off}$ ratio of 4.4 $cm^2\ V^{-1}\ s^{-1}$, 1.1 $cm^2\ V^{-1}\ s^{-1}$, as low as $10^{-13}$ A, and $10^8$, respectively, while the corresponding values for the n-channel TFT were 1.6 $cm^2\ V^{-1}\ s^{-1}$, 1.9 $cm^2\ V^{-1}\ s^{-1}$, as low as $10^{-13}$ A, and $10^9$ respectively; additionally, for the n-channel TFT, $V_{on} \sim 0$ V. The $\mu_{sat}$ value observed for the p-channel TFT may be attributed to an early pinch-off phenomenon, which is often observed in short-channel TFTs based on OSCs[49].

The VTC of a single inverter with a supply voltage of 10 V (**Figure 6**(b)) suggests that even those inverters with short channel lengths exhibit a full rail-to-rail swing, symmetric transition of $V_M \sim 5$ V for both forward and backward voltage sweep, and a high noise margin with an

$NM_H$ of 3.2 V and $NM_L$ of 2.9 V. The output signal at a $V_{DD}$ of 10 V is shown in **Figure 6**(c). In this case, $f_{ROSC}$ = 77 kHz and the propagation delay per stage was estimated to be 1.3 µs. We compared several complementary ring oscillators based on solution-processed OSCs or MOSs with respect to propagation delay in terms of scalable fabrication and flexible circuits. As there only a few studies on flexible substrates, ring oscillators fabricated on rigid substrates were also added to the list **(Table 1**). Because the frequency of a ring oscillator is approximately proportional to $V_{DD}^{50}$, different devices were compared by converting $V_{DD}$ to 10 V and the corresponding propagation delay after conversion was defined as $t_{p(10V)}$. Notably, the hybrid ring oscillator described in this study exhibited the fastest operation speed when compared to all other compared oscillators.

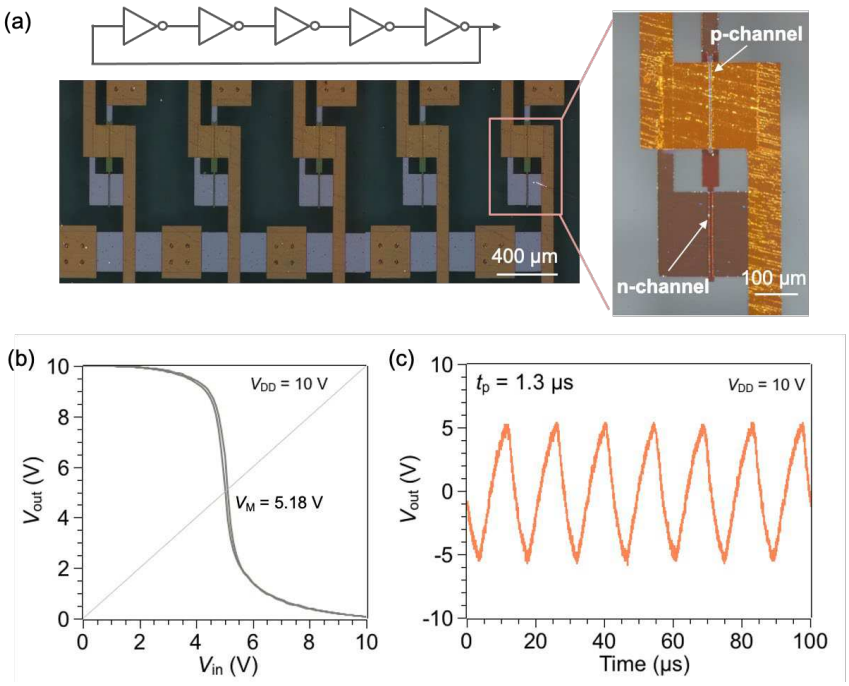


**Figure 6** Properties of a five-stage ring oscillator. (a) Optical micrograph of a hybrid ring oscillator. The magnified image shows one stage. $W/L$ = 200 µm/4 µm and $\Delta L$ = 3 µm for p-channel TFT and $W/L$ = 200 µm/8 µm and $\Delta L$ = 1.5 µm for n-channel TFT. (b) VTCs of the hybrid inverter with $V_{DD}$ = 10 V. (c) Output signal of the ring oscillator at $V_{DD}$ = 10 V

**Table 1** Comparison of the stage-propagation delay in ring oscillators based on solution-processed MOSs or OSCs

| Substrate | p-channel material | n-channel material | Stage No.* | $L_p/L_n$† (μm) | $V_{DD}$‡ (V) | $f_{ROSC}$§ (kHz) | $t_p$** (μs) | $t_{p(10\ V)}$†† (μs) | Ref. |
|---|---|---|---|---|---|---|---|---|---|
| PI | $C_9$-DNBDT-NW | IZO | 5 | 4/8 | 10 | 77 | 1.3 | 1.3 | This work |
| PEN | ActivInk P2100 | P(NDI2OD-T2) | 5 | 5/5 | 10 | 10 | 10 | 10 | 51 |
| PEN | TIPS-PEN | ActivInk N3300 | 19 | 5/5 | 10 | 1.0 | 25 | 25 | 52 |
| PEN | DPPT-TT | P(NDI2OD-T2) | 7 | / | 100 | 2 | 31 | 310 | 53 |
| PET | TIPS-pentacene | GSID 104031-1 | 5 | 70/70 | 100 | 0.134 | 746 | 7460 | 54 |
| Parylene | DiF-TES-ADT/PS | TU-3 | 3 | / | 10 | 0.217 | 768 | 768 | 27 |
| Si | P3HT | ZnO | 5 | 1/1 | 2 | 2.2 | 45 | 9 | 55 |
| Glass | $C_{10}$-DNBDT-NW | BASF GSID-104031-1 | 5 | 30/5 | 20 | 22 | 4.5 | 9 | 30 |
| Glass | IDT-BT | IZO | 3 | 5/5 | 10 | 3.2 | 52 | 52 | 34 |
| Glass | DiF-TES-ADT/PS | TU-3/PαMS | 5 | 10/10 | 10 | 1.465 | 68.2 | 68.2 | 56 |
| Glass | P($T_0T_0TT_{16}$) | P(NDI2OD-T2) | 7 | 2.5/2.5 | 1.5 | 0.14 | 500 | 75 | 57 |
| Glass | TIPS-PEN | PD18CN2 | 7 | 10/10 | 4 | 0.03 | 2246 | 898 | 26 |
| Glass | MOP-01 | TU-3 and /PαMS | 5 | 60/55 | 10 | 0.09 | 1065 | 1065 | 58 |

*Stage No.: Stage number
†$L_p/L_n$: Channel lengths for n-channel TFT and p-channel TFT
‡$V_{DD}$: Supply voltage
§$f_{ROSC}$: Frequency of ring oscillator
**$t_p$: Stage propagation delay
††$t_{p(10\ V)}$: Stage propagation delay at $V_{DD}$ = 10 V or converted $V_{DD}$ to 10 V

The output signals of devices with other dimensions (channel widths of 200 μm) are shown in **Figure S9**. For ROSC1 ($L$ = 19 μm and $\Delta L$ = 10 μm for the p-channel TFT and $L$ = 24 μm and $\Delta L$ = 8 μm for the n-channel TFT), ROSC2 ($L$ = 9 μm and $\Delta L$= 10 μm for the p-channel TFT and $L$ = 13 μm and $\Delta L$ = 8.5 μm for the n-channel TFT), and ROSC3 ($L$ = 4 μm and $\Delta L$ = 5 μm for the p-channel TFT and $L$ = 8 μm and $\Delta L$ = 3.5 μm for the n-channel TFT), the propagation delays in each stage were 3.8, 3.0, and 1.7 μs, respectively. These results imply that this technology is suitable for directly printing advanced commentary circuits on flexible substrates. We believe that the operation speed can be further improved by optimising the photolithography and semiconductor-deposition conditions.

**Discussion**

We demonstrated scalable hybrid complementary ICs on flexible substrates using solution-processed semiconductors. Using high-performance semiconductor materials, viz. p-type $C_9$-DNBDT-NW single crystals and n-type amorphous IZO, and carefully designed integration processes, we could fabricate hybrid inverters with excellent electrical characteristics, including an almost rail-to-rail swing, negligible hysteresis, voltage gain as high as 38 V/V, large noise margin, and superior long-term stability. A five-stage ring oscillator operating at 77 kHz with a supply voltage of 10 V proved the potential of this hybrid technology for high-speed operations and highly complex ICs. Furthermore, the hybrid complementary inverters worked well even under bending conditions at radii as high as 6 mm. To further improve the operation speed of these inverters, it is required to further improve their carrier mobility and reduce their dimensions. We are currently working on optimising the fabrication conditions to

achieve finer patterns and these results will be reported in near future. In addition, appropriate passivation is being studied to further improve the stability of this hybrid system. Finally, because the proposed technology enables the direct printing of advanced complementary circuits on flexible substrates, we envision that it will contribute significantly to IoT applications.

## Methods

### Substrate preparation

All the devices used in this study were fabricated on PI substrates. The PI substrate was prepared by spin-coating polyamic acid (Ube Industries, Ltd.) on a glass supporter ($5 \times 5$ $cm^2$) at 2000 rpm for 3 min, followed by thermal curing at 110 °C for 60 min, 150 °C for 30 min, 200 °C for 10 min, 250 °C for 10 min, and 430 °C for 10 min on a hot plate in the air. The PI film was attached to a glass support during fabrication and delaminated using an LLO technique to achieve free-standing films for flexibility evaluation.

### Fabrication of n-channel TFTs based on IZO

IZO films were fabricated using a sol-gel method. Initially, In and Zn precursor solutions (0.1 M) were prepared by adding $In(NO_3)_3 \cdot xH_2O$ (Aldrich) and $Zn(NO_3)_2 \cdot xH_2O$ (Aldrich) to 2-methoxyethanol, respectively, and stirring at room temperature in the air for more than 6 h. The IZO precursor was then prepared by mixing the In and Zn precursors at an In/Zn ratio of 3/2 and stirring under the conditions described above.

Both n- and p-channel TFTs exhibit a bottom-gate top-contact structure, as shown in **Figure S1**. Gate patterns of IZO-based TFTs were formed by photolithography with a photoresist (TLOR, Tokyo Ohka Kogyo Co., Ltd.). Cr/Au/Cr (5/25/5 nm) was deposited via thermal evaporation, followed by a lift-off process. An $AlO_x$ gate dielectric layer was formed by ALD. Before IZO deposition, the substrate was treated with a UV ozone cleaner (Filgen, Inc.,

UV253H) for 10 min to remove any organic residues and improve its wettability. The IZO precursor was then spin-coated on the substrate at 500 rpm for 5 s and 5000 rpm for 30 s, followed by soft baking at 150 °C for 5 min and hard baking at 370 °C for 1 h under ambient conditions. The IZO film was patterned with a PDM (Taiyo Ink Mgf. Co., Ltd.), and etched with oxalic acid. S/D electrodes for IZO-based TFTs and gate electrodes for $C_9$-DNBDT-NW-based TFTs (Al, 45 nm) were deposited by thermal evaporation and patterned by a lift-off process based on PDM[40].

**Fabrication of p-channel TFTs based on $C_9$-DNBDT-NW**

After the fabrication of n-channel TFTs, a PMMA/parylene bilayer was fabricated to act as a passivation layer for n-channel TFTs and it doubled as a gate dielectric for p-channel TFTs. The PMMA layer was formed by spin coating a PMMA solution (Mw = 120,000, 0.56 wt.% in butyl acetate) at 500 rpm for 5 s and then 4000 rpm for 30 s, followed by soft baking at 150 °C for 1 h. The parylene layer was deposited by chemical vapour deposition.

$C_9$-DNBDT-NW was synthesised and purified in-house; initially, a $C_9$-DNBDT-NW solution was prepared by dissolving 0.02 wt.% $C_9$-DNBDT-NW in 3-chlorothiophene. The $C_9$-DNBDT-NW single-crystal layer was printed by continuous edge casting on a super hydrophilic substrate and then transferred to the top of the PMMA/parylene dielectric layer. More details on the printing and OSC transfer methods can be found in our previous reports[8,41,42].

Fine patterns of OSC and Au S/D electrodes were achieved by a two-step patterning process based on a dry film resist with a thickness of 5 μm (PDM, Taiyo Ink Mfg. Co., Ltd.)[43,44]. This process is illustrated schematically in **Figure S10**. A PMMA layer (Mw = 120,000, 5 wt.% in butyl acetate) was formed by spin coating at 500 rpm for 5 s and 1000 rpm for 30 s, followed by baking at 80 °C for 10 min before being laminated with a PDM dry film. The PDM layer

was patterned by photolithography and PMMA was patterned using $O_2$ plasma with patterned PDM as a mask. After etching the OSC or S/D electrodes, PMMA and PDM were stripped together with acetonitrile. For OSC patterning, Au (30 nm) was deposited via thermal evaporation on the entire surface and it acted as a protection layer as well as S/D electrodes. Subsequently, a two-step photolithography process was conducted. Au was etched using an AURUM S-50790 (Kanto Chemical Co. Inc.) instrument and the OSC layer was etched using $O_2$ plasma. Subsequently, a solid-state laser (Delphi Laser, Inducer-6001-P, 355 nm) was used to create holes in the gate dielectrics for bottom electrodes. Next, Au (60 nm) was deposited by thermal evaporation and patterned by two-step photolithography to form S/D electrodes and conduction terminals for the bottom electrodes. Finally, the substrate was annealed at 110 °C for 1 h to remove the solvent used during fabrication.

**Device characterisation**

The electrical properties of the fabricated hybrid inverters were measured under ambient and dark conditions. The static properties of the TFTs and the VTCs of the inverters were measured using a semiconductor parameter analyser (Keithley, 4200-SCS). The output signals of the ring oscillators were recorded using an oscilloscope (Tektronix, MDO3014). Micrographs of the complementary inverter and ring oscillator were acquired using an optical microscope. An FIB-SEM (JEOL, JIB-4700F) was used to observe the edge conditions of the gate electrodes in p-channel TFTs.

Carrier mobility ($\mu$) and $V_{th}$ were determined by measuring the dependence of drain current ($I_D$) on $V_G$ and fitting with the following equations.

In the linear region,

$$I_D = \frac{\mu_{lin} W C_i}{L} V_D (V_G - V_{th}) \quad (5)$$

In the saturation region,

$$I_{\mathrm{D}} = \frac{\mu_{\mathrm{sat}} W C_{\mathrm{i}}}{2L} (V_{\mathrm{G}} - V_{\mathrm{th}})^2 \quad (6)$$

$C_{\mathrm{i}}$ is determined by capacitance–voltage measurements at 10 kHz. The values of $C_{\mathrm{i}}$ for the ring oscillators used in this study were 88.5 nF cm$^{-2}$ for n-channel ($AlO_x$, 80 nm) and 13.2 nF cm$^{-2}$ for p-channel (PMMA, ~10 nm; parylene, ~190 nm); for inverters discussed in other parts (excepted the ring oscillators, **Figure 6**, **Figure S8, and Figure S9**) 122.5 nF cm$^{-2}$ for n-channel ($AlO_x$, 63 nm) and 22.1 nF cm$^{-2}$ for p-channel (PMMA, ~10 nm; parylene, ~120 nm).

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**Author contributions**

J.T. and S.W. conceived the study. X.W. designed the integration process and carried out device fabrication, characterisation studies, and the related data analysis. S. K. contributed to the process design and data analysis of metal-oxide semiconductors and the passivation process. T.M. contributed to the fabrication and patterning of organic semiconductors. K.T. discussed the IZO preparation process. A.Y. contributed to the design of complementary circuits. All authors analysed and interpreted the data and wrote the manuscript.

**Competing interests**

The authors declare no competing interests.

# Figures

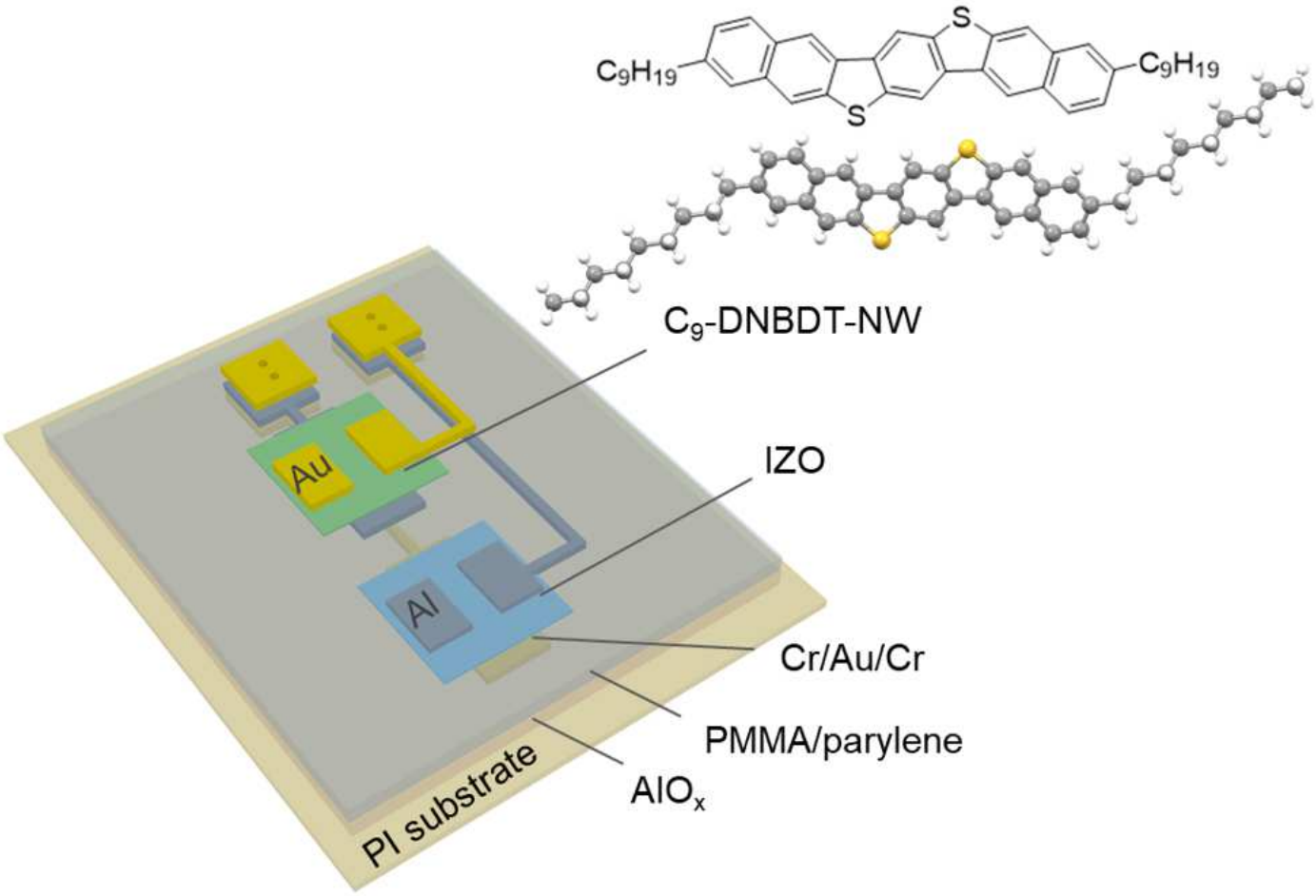
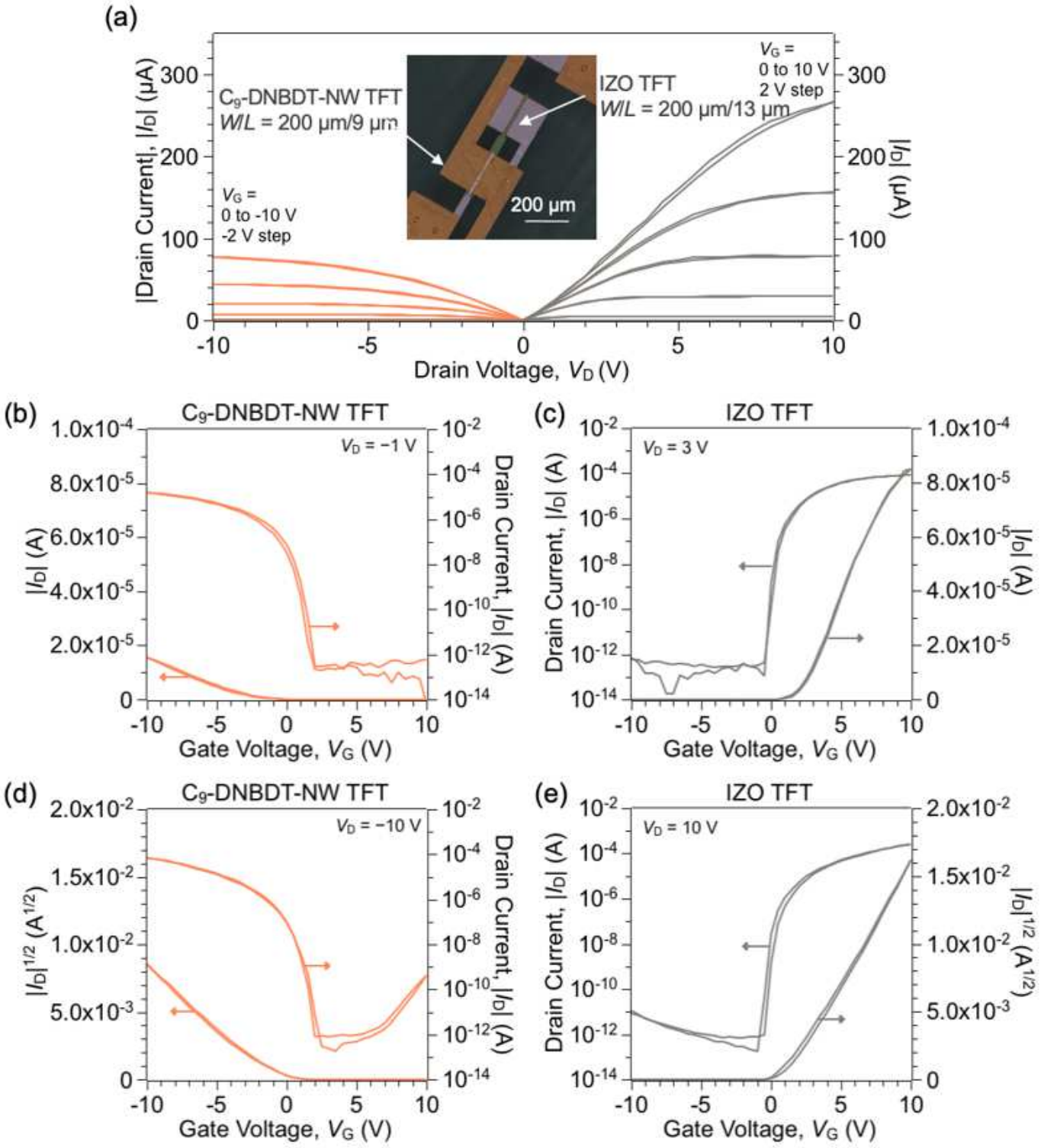



**Figure 1**

Schematic structure of a hybrid complementary inverter with IZO as the n-channel material and C9-DNBDT-NW single crystal as the p-channel material




## Figure 2

Electrical performance of C9-DNBDT-NW- and IZO-based TFTs. (a) Output performance. The inset shows a micrograph of a complementary inverter with W/L = 200 μm/9 μm for the C9-DNBDT-NW p-channel and 200 μm/13 μm for the IZO n-channel. (b)–(e) Transfer characteristics in the linear region and the saturation region

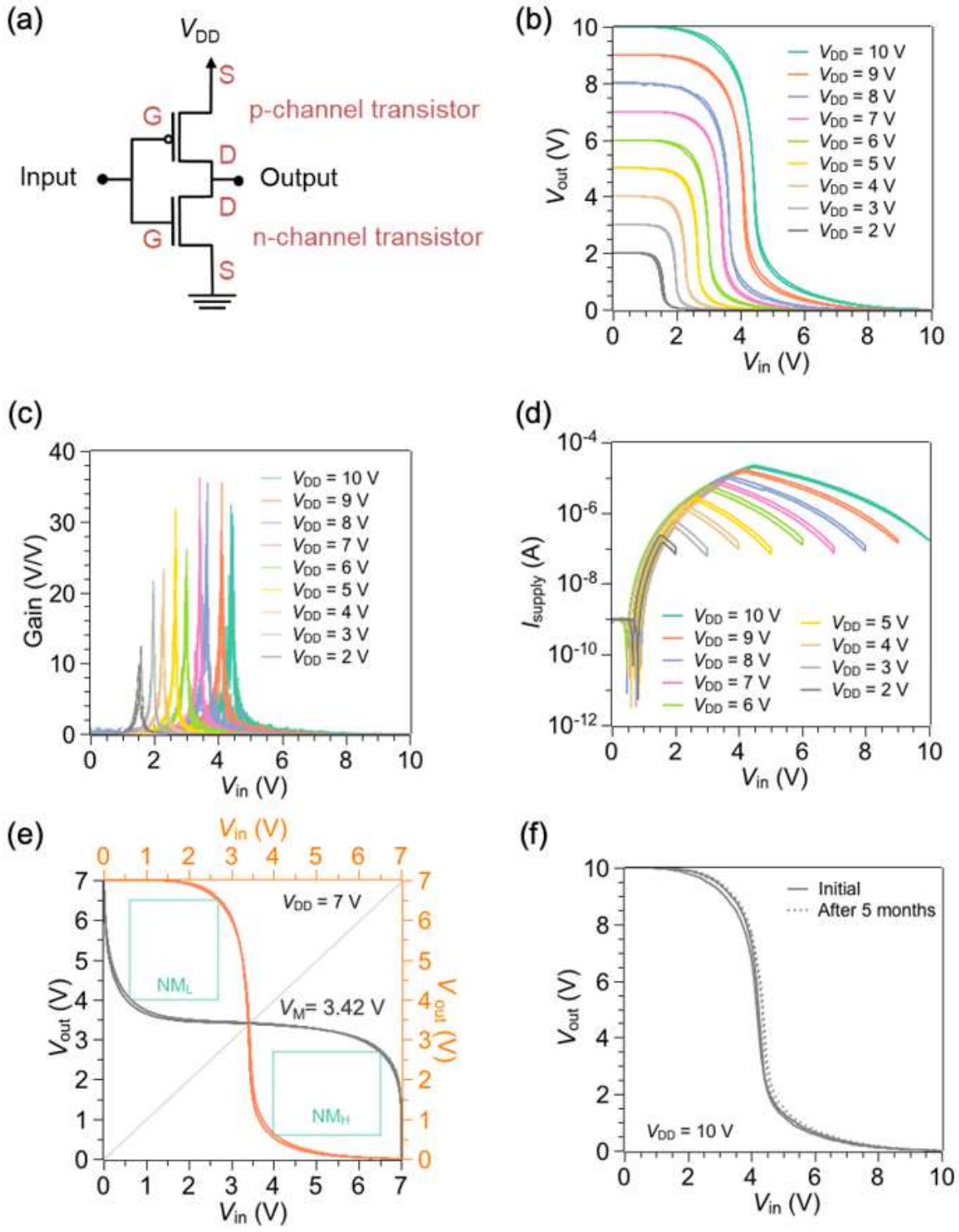



**Figure 3**

Electrical performance of the hybrid inverter shown in Figure 2. (a) Circuit of a complementary inverter. (b) VTCs, (c) voltage gains, and (d) static current at VDD = 2–10 V. (e) VTCs at VDD = 7 V with noise margins represented by the green rectangles. VM = 3.42 V, NMH = 2.5 V, and NML = 1.9 V. (f) VTCs before and after exposure to air for 5 months (VDD = 10 V)

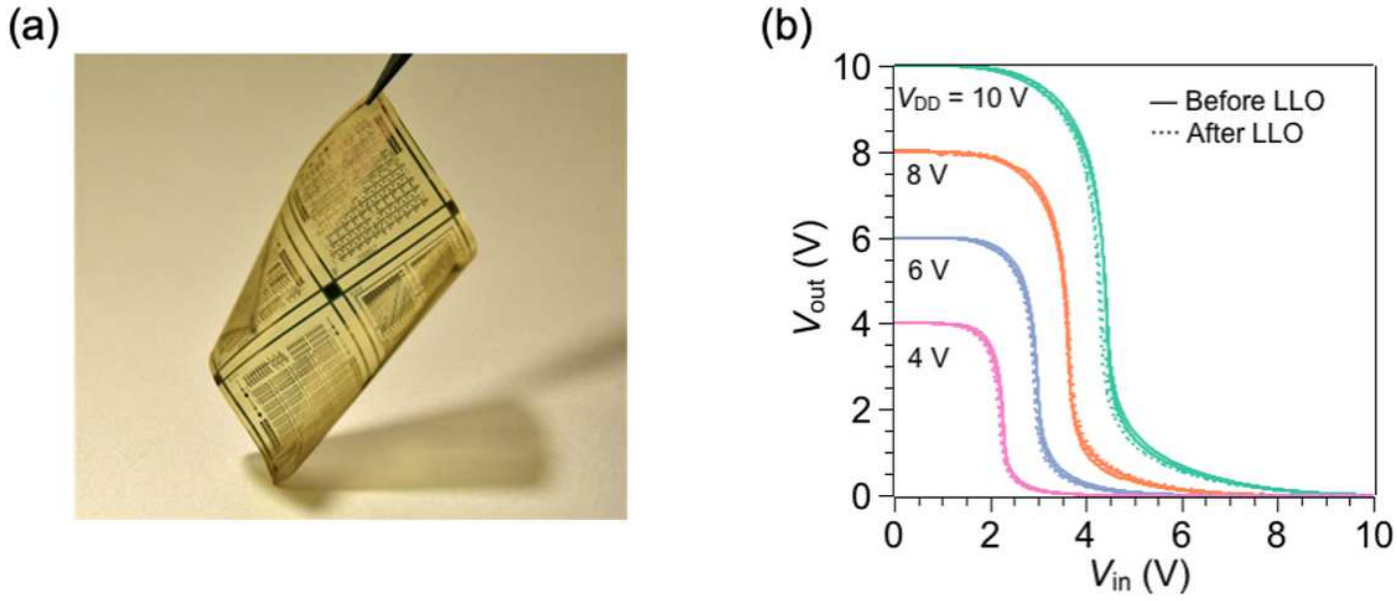
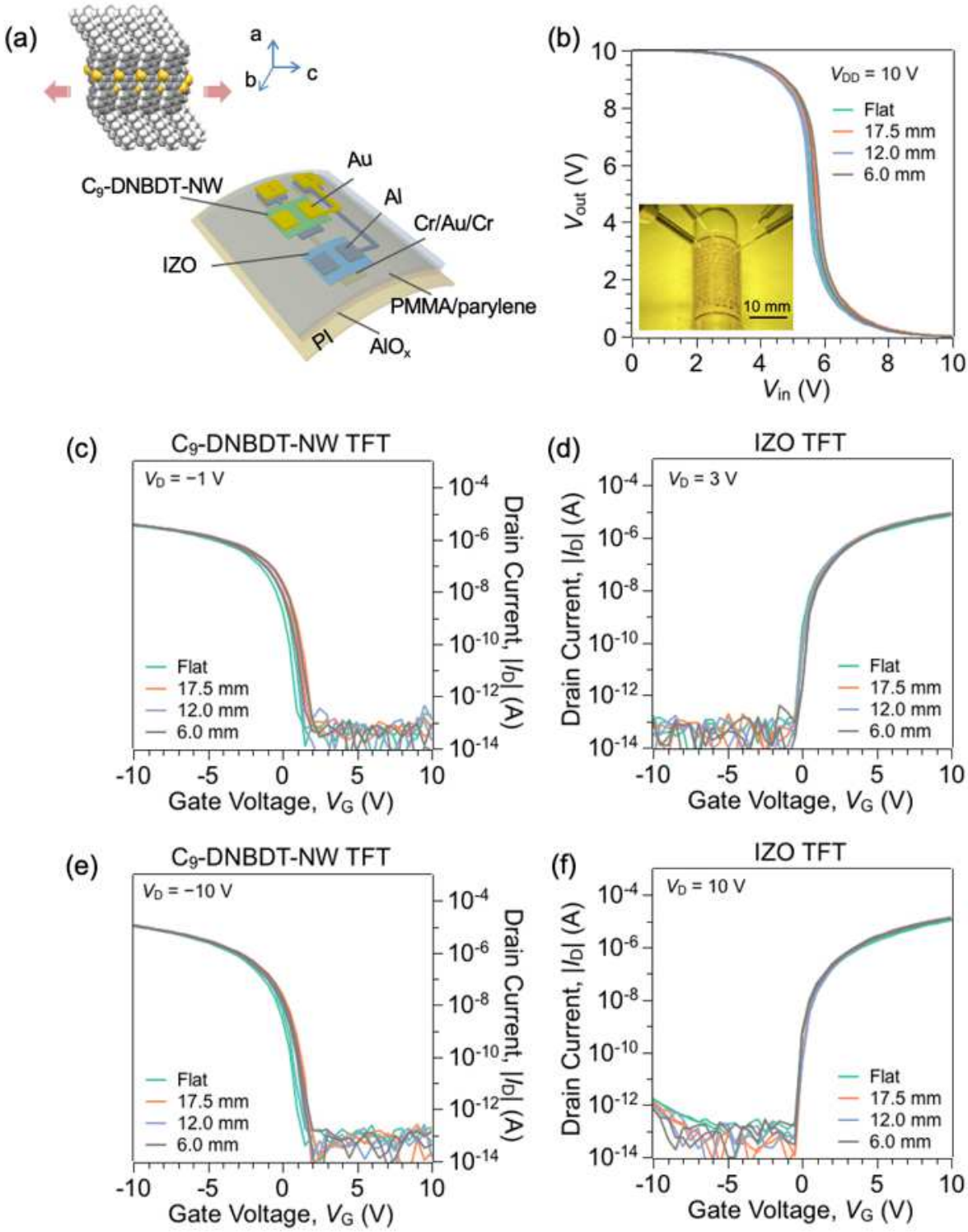



**Figure 4**

Properties of the hybrid inverter before and after delamination from glass supports. (a) Photograph of the hybrid ICs on a free-standing PI film. (b) VTCs of the hybrid complementary inverter with p- and n-channel W/L values of 200 μm/9 μm and 200 μm/13 μm, respectively, before and after delamination




## Figure 5

Electrical performance of a hybrid complementary inverter under bending stress. (a) Schematic illustration of a device under bending stress. (b) VTCs of the inverter when flat and bent to tensile radii of 17.5, 12.0, and 6 mm. The inset shows the measurement setup with a bending radius of 6 mm. Transfer curves of TFTs based on (c and d) C9-DNBDT-NW and (e and f) IZO in the linear and saturation regions under different bending stresses

## Supplementary Files

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