Physics Based Analytical Modeling of Asymmetric Elevated Source Tunnel FET (AES-TFET) for Better Tunnel Junction Device (TJD) Performance

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Physics Based Analytical Modeling of Asymmetric Elevated Source Tunnel FET (AES-TFET) for Better Tunnel Junction Device (TJD) Performance

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Abstract

In this paper, a two-dimensional analytical model for asymmetric elevated source tunnel field effect transistor (AES-TFET) has been developed to obtain better tunnel junction device performance. Device physics based analytical modelling is performed by solving 2-D Poisson's equation. Surface potential distribution, electric field variation and band-to-band tunneling (B2B) rate have been investigated by this numerical modelling. In our proposed structure, the source has been elevated (varied 2 nm to 6 nm) to incorporate corner effect; which boosts the carrier transport via thin tunneling barrier, with controlled ambipolar conduction. This eventually produces better source-channel interface tunneling for a *n*-channel AES-TFET structure. 2-D numerical device simulator (SILVACO TCAD) has been used for simulation work. The simulated graphical representations have been finally validated by analytical modelling of AES-TFET.

Keywords AES-TFET · Surface potential distribution · Electric field variation · B2B tunneling · TCAD · Numerical modelling.

1 Introduction

With the advent of nanoscience and nanotechnology in nano-scaled devices, the physical sizes of transistors have been scaled down categorically. By following the Moore's law prediction in 2022, the miniaturization has reached its limit for metal oxide field effect transistors (MOSFETs) [1]. In this connection, various scaling issues has been emerged in last two decades viz. short channel effects (SCE), drain induced barrier lowering (DIBL) [2]. To overcome these issues, continuous research is going on in novel structures of MOSFETs. But in present scenario, the limited subthreshold swing (SS) of MOSFETs at around 60mV/decade has been a major drawback for researchers.

Keeping all device parameter scaling issues in mind, a new device physics has been inculcated in nanodevice engineering. In this case quantum tunneling has been introduced as a solid replacement of earlier FETs [3]. The typical energy band structure with ultra-thin barrier helped researchers to develop tunneling junction devices (TJD) using band to band (B2B) tunneling phenomenon. In this paper, prior to this work, several literatures were surveyed based on structural and material engineering [4-14]. The effect of homogeneous and heterogeneous material in tunneling junctions [15], effect of pocket intrinsic doping on single as well as multi gate tunneling FETs [16-17], effect of device performance based on various high-*k* materials [18], stress-strain effects in source-channel (*n*-channel) and drain-channel (*p*-channel) TJDs [19], usage of carbon nano-tubes (CNT) in tunneling FETs [20], nano-wire tunneling FETs [21], capacitive effects in modified TJD structures [22], various symmetric and asymmetric tunneling device structures has been studied to meet the earlier mentioned scaling issues and device performance factors.

In our paper the typical elevated design of source region has been modelled to introduce corner effect in source-channel junction for *n*-channel TFET. The entire device structure details have been mentioned in section 2, where the typical device parameters are used based on recent established literature survey. The device physics based analytical modelling has been introduced in section 3. Here the two-dimensional Poisson's equation is used for numerical analysis. Parabolic approximation method is considered for potential distribution analysis across the

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channel region. In section 4, simulation and analytical results and discussion are compared for validation of our work. The energy band diagram analysis, surface potential distribution, electric field variation, transfer characteristics and transconductance analysis are graphically plotted. Finally, in section 5, the conclusion and future scope of our proposed AES-TFET structure has been discussed.

2 Device Structure

In this section, a typical elevated design of source region has been modelled to introduce corner effect in source-channel junction for n -channel TFET (figure 1). Unlike conventional symmetric single gate tunnel FET (figure 2), the asymmetric elevated source results better B2B

tunneling across ultra-thin tunneling barrier. The tunneling region is divided into five parts. Region 1 (length of R_1 , $L_1 = 5\text{nm}$) is made of Si-Ge material for better tunneling, Region 2 (length of R_2 , $L_2 = 10\text{nm}$), Region 3 (length of R_3 , $L_3 = 20\text{nm}$) and Region 4 (length of R_4 , $L_4 = 5\text{nm}$) to consider the potential distribution at drain side depletion region. Region 1 and 2 are considered unitedly as Region 5 (length of R_5 , $L_1+L_2 = L_5 = 15\text{nm}$). P^+ source side doping (N_S) = 10^{20} cm^{-3} , intrinsic channel doping (N_{ch}) = 10^{14} cm^{-3} and N^+ drain side doping (N_D) = 10^{18} cm^{-3} , body thickness (t_{si}) = 10nm and gate oxide thickness (t_{ox}) = 2nm is considered in our simulation work.

Fig. 1. Three-dimensional view of proposed AES-TFET device model

Fig. 2. Three-dimensional view of symmetric conventional TFET device model

3 Analytical Model

In order to investigate the electrostatic potential across the identified regions from R_1 to R_4 (figure 1), two-dimensional Poisson's equation is used as follows:

$$\frac{\partial^2 \psi_i}{\partial x^2} + \frac{\partial^2 \psi_i}{\partial y^2} = \frac{qN_i}{\epsilon_i} \quad \text{for } i = 1, 2, 3, 4 \quad 0 \leq x \leq L \quad \text{and} \quad 0 \leq y \leq t_{Si} \quad (1)$$

Where, ψ_i is electrostatic potential for all four regions (R_1 to R_4), q is charge, N_i is doping concentration of respective regions, ϵ_i is the dielectric constant. L is assumed as overall length of all four regions i.e. $L = L_1 + L_2 + L_3 + L_4$. The channel thickness is denoted as t_{Si} , used for numerical analysis.

Here in our work, parabolic approximation is assumed for solving the surface potential distribution across the regions. So, we can write:

$$\psi_i(x, y) = a_{0i}(x) + a_{1i}(x)y + a_{2i}(x)y^2 \quad (2)$$

Where, constant coefficients are denoted as a_{0i} , a_{1i} and a_{2i} which are the arbitrary functions of x . Now after assuming the arbitrary coefficients for all regions along x axis, their values can be calculated using following boundary conditions. So, from the planar device structure, it can be clearly understandable that the boundary conditions are completely based on continuity of surface potential profile and electric field distribution profile. Therefore, from gate oxide layer to semiconductor layer i.e. (SiO_2 to Si interface) the boundary conditions are set as $y = 0$ and $y = t_{Si}$.

$$\psi_i(x, y)|_{y=0} = \psi_{Si}(x) \quad (3)$$

$$\left. \frac{\partial \psi_i(x, y)}{\partial y} \right|_{y=0} = \frac{C_{ox}}{\epsilon_i} (\psi_{Si}(x) - V_G) \quad (4)$$

$$\left. \frac{\partial \psi_i(x, y)}{\partial y} \right|_{y=t_{Si}} = 0 \quad (5)$$

Where, $\psi_{Si}(x)$ is denoted for surface potential along lateral direction i.e. (x axis) and C_{ox} is denoted as gate oxide capacitance.

Here in our device model, the fringing field at channel-drain interface depletion region (i.e. region R_4) has been considered. Therefore, gate oxide thickness (C_{ox}) in equation 4 can be replaced by $\frac{2}{\pi} C_{ox}$ [23] and effective gate voltage (V_G) can also be written as:

$$V_G = V_{gs} - V_{fbi} \quad (6)$$

$$V_{fbi} = V_{gs} - \phi_m + \chi_i + \frac{E_{gi}}{2} + \phi_{fi} \quad (7)$$

Where, ϕ_m is metal work function and ϕ_{fi} is denoted as fermi potential. V_{fbi} is denoted as flat band voltage, χ_i and E_{gi} represents electron affinity and energy band gap of respective identified regions. In the region 1, in order to introduce stress – strain effect; Si-Ge combination is introduced. Due to which

the band gap energy of region R_1 (i.e. E_{g1}) can be written as [24]:

$$E_{g1} = 1.10 - 0.34x \quad \text{where, } x = \text{mole fraction of Ge} \quad (8)$$

Now using the above-mentioned boundary conditions equation 3 to 5 and equations 6 to 7, the co-efficient (equation 2) can be estimated as:

$$a_{0i}(x) = \psi_{Si}(x) \quad (9)$$

$$a_{1i}(x) = \frac{\epsilon_{ox}}{\epsilon_i t_{ox}} (\psi_{Si}(x) - V_G) \quad (10)$$

$$a_{2i}(x) = \frac{\epsilon_{ox}}{2 \epsilon_i t_{ox} t_s} (V_G - \psi_{Si}(x)) \quad (11)$$

Therefore, substituting these coefficient values from equation 9, 10 and 11 in equation 1; the surface potential from the regions R_1 to R_4 can be written as:

$$\psi_{Si}''(x) - k_i^2(x) \psi_{Si}(x) = k_i^2 \eta_i \quad (12)$$

$$\text{Where, } k_i = \sqrt{\frac{C_{ox}}{t_{Si} \epsilon_i}} \quad \text{and} \quad \eta_i = \frac{qN_i}{\epsilon_i k_i^2} - V_G$$

So, in general the equation 11 can be written as:

$$\psi_{Si}(x) = A_i e^{(k_i x_i)} + B_i e^{(-k_i x_i)} - \eta_i \quad (13)$$

Since, the device model is designed assuming n-channel AES-TFET, therefore the band-to-band tunneling regions i.e. R_1 and R_2 regions combinedly denoted as region 5 (R_5). Using Poisson's equation, we can write:

$$\frac{\partial^2 \psi_{s5}}{\partial x^2} = \frac{q N_2}{\epsilon_2} \quad (14)$$

Therefore, similarly the equation 13 can be written in general:

$$\psi_{s5}(x, y) = \frac{q \cdot N_2}{\epsilon_2} x^2 + C_{51} x + C_{52} \quad (15)$$

Finally, all these coefficients A_i , B_i , C_{51} and C_{52} can be solved using following boundary conditions. Here, the x is replaced by respective region lengths L_1 to L_4 .

$$V_{bis} = \psi_{s1}(0) = -\frac{\delta T}{q} \ln\left(\frac{N_1}{N_2}\right) \quad (16)$$

$$\psi_{s1}(L_1) = \psi_{s2}(L_1) \quad (17)$$

$$\therefore \frac{\partial \psi_{s1}(L_1)}{\partial x} = \frac{\partial \psi_{s2}(L_1)}{\partial x} \quad (18)$$

$$\psi_{s2}(L_2) = \psi_{s3}(L_2) \quad (19)$$

$$\therefore \frac{\partial \psi_{s2}(L_2)}{\partial x} = \frac{\partial \psi_{s3}(L_2)}{\partial x} \quad (20)$$

$$\psi_{s3}(L_3) = \psi_{s4}(L_3) \quad (21)$$

$$\therefore \frac{\partial \psi_{s3}(L_3)}{\partial x} = \frac{\partial \psi_{s4}(L_3)}{\partial x} \quad (22)$$

$$\text{Since, } \psi_{s5}(L_1 + L_2) = \psi_{s5}(L_3) \quad (23)$$

$$\therefore \frac{\partial \psi_{s5}(L_1 + L_2)}{\partial x} = \frac{\partial \psi_{s5}(L_3)}{\partial x} \quad (24)$$

Similarly, for region 4 at channel-drain interface, the drain-bias potential can be written as:

$$V_{bid} = \psi_{s4}(L_4) = V_{ds} + \frac{\delta T}{q} \ln\left(\frac{N_3}{N_2}\right) \quad (25)$$

$$\therefore L_4 = \sqrt{\frac{2 \varepsilon_i N_2 (V_G - V_{ds} - V_{bid})}{q N_3 (N_2 + N_3)}} \quad (26)$$

Now, from equation 13, 15 and (16 to 26), the coefficients A_i, B_i, C_{51} and C_{52} can be calculated as follows:

$$\begin{aligned} C_1 = & A_4 \left[Z_1(k_3 + k_4) e^{(k_4 L_3)} \right. \\ & \left. - Z_2(k_3 - k_4) e^{(k_4 L_3)} \right] \\ & + B_4 \left[Z_1(k_3 - k_4) e^{(-k_4 L_3)} \right. \\ & \left. - Z_2(k_3 + k_4) e^{(-k_4 L_3)} \right] \\ & + \left[Z_1 k_3 (\eta_3 - \eta_4) - Z_2 k_3 (\eta_3 - \eta_4) - 2 L_2 \frac{q N_5}{\varepsilon_i} \right] \end{aligned} \quad (27)$$

$$\begin{aligned} C_2 = & A_4 \left[D_2 R_1 + D_3 R_2 \right. \\ & + B_4 \left[D_2 R_3 + D_3 R_4 \right. \\ & + \left[D_2 R_5 + D_3 R_5 \right. \\ & \left. \left. - \eta_3 - D_1 \right] \right] \end{aligned} \quad (28)$$

$$B_4 = \frac{\{(V_{bis} + \eta_1) e^{(k_4 L_4)}\} - \{(V_{bid} + V_{ds} + \eta_4) (E_1 + E_3)\} - \{(G_1 + G_2) e^{(k_4 L_4)}\}}{(E_2 + E_4) e^{(k_4 L_4)} - (E_1 + E_3) e^{(-k_4 L_4)}} \quad (29)$$

$$A_4 = \frac{\{(V_{bis} + \eta_1) e^{(-k_4 L_4)}\} - \{(V_{bid} + V_{ds} + \eta_4) (E_2 + E_4)\} - \{(G_1 + G_2) e^{(-k_4 L_4)}\}}{(E_1 + E_3) e^{(-k_4 L_4)} - (E_2 + E_4) e^{(k_4 L_4)}} \quad (30)$$

$$A_3 = \frac{1}{2 k_3 e^{(k_3 L_3)}} \left[A_4(k_3 + k_4) e^{(k_4 L_3)} + B_4(k_3 - k_4) e^{(-k_4 L_3)} + k_3 (\eta_3 - \eta_4) \right] \quad (31)$$

$$B_3 = \frac{1}{2 k_3 e^{(-k_3 L_3)}} \left[A_4(k_3 - k_4) e^{(k_4 L_3)} + B_4(k_3 + k_4) e^{(-k_4 L_3)} + k_3 (\eta_3 - \eta_4) \right] \quad (32)$$

$$\begin{aligned} A_2 = & A_4 \left[Y_1(k_3 + k_4) e^{(k_4 L_3)} \right. \\ & + Y_2(k_3 - k_4) e^{(k_4 L_3)} \\ & + B_4 \left[Y_1(k_3 - k_4) e^{(-k_4 L_3)} \right. \\ & \left. + Y_2(k_3 + k_4) e^{(-k_4 L_3)} \right] \end{aligned} \quad (33)$$

$$+ \frac{1}{4 k_2 e^{(k_2 L_2)}} \left[O_6(k_2 + k_3) + O_7(k_2 - k_3) + O_8 \right]$$

$$\begin{aligned} B_2 = & A_4 \left[W_1(k_3 + k_4) e^{(k_4 L_3)} \right. \\ & + W_2(k_3 - k_4) e^{(k_4 L_3)} \\ & + B_4 \left[W_1(k_3 - k_4) e^{(-k_4 L_3)} \right. \\ & \left. + W_2(k_3 + k_4) e^{(-k_4 L_3)} \right] \end{aligned} \quad (34)$$

$$+ \frac{1}{4 k_2 e^{(-k_2 L_2)}} \left[O_6(k_2 - k_3) + O_7(k_2 + k_3) + O_8 \right]$$

$$A_1 = A_4 E_1 + B_4 E_2 + G_1 \quad (35)$$

$$B_1 = A_4 E_3 + B_4 E_4 + G_2 \quad (36)$$

Now, by differentiating the surface potential functions obtained from above numerical analysis; the lateral as well as vertical electric field can be achieved. Therefore, along (x - axis) channel length, the lateral e-field can be obtained as follows:

$$E_{xi} = -k_i [A_i e^{(k_i x_i)} - B_i e^{(-k_i x_i)}] \quad \text{for Region } R_1 \text{ to } R_4 \quad (37)$$

$$E_{x5} = - \left[2 \frac{q N_2}{\varepsilon_2} L_2 + C_1 \right] \quad (38)$$

Similarly, the vertical e-field along (y - axis) also can be achieved as follows:

$$E_{yi} = -[A_{1i}(x) + 2 y a_{2i}(x)] \quad \text{for Region } R_1 \text{ to } R_4 \quad (39)$$

$$E_{y5} = 0 \quad (40)$$

In our work, a new carrier transport phenomenon is introduced

i.e. band-to-band (B2B) quantum tunneling. Since n -channel AES-TFET is designed with introducing a thin ($L_1 = 5\text{nm}$) Si-Ge material for better tunneling at source – channel interface, so the drain current (I_d) can be obtained as:

$$I_d = q \int_{L_1}^{L_4} G_{BTBT} dv \quad (41)$$

for Region R_1 to R_4

$$\text{So, } G_{BTBT} = A \frac{|E^2|}{\sqrt{E_{gi}}} e^{(-B \frac{E_{gi}^{1.5}}{|E|})} \quad (42)$$

$$\text{Where, } |E| = |\sqrt{E_x^2 + E_y^2}|$$

As mentioned in equation 42, A and B are the model parameters, whose values are considered as $4 \times 10^{14} \text{ cm}^{-3} \text{ s}^{-1}$ and $1.9 \times 10^7 \text{ V cm}^{-1}$ respectively. After obtaining the drain current (I_d) i.e. ON-state current, the transconductance (g_m) can also be calculated as:

$$g_m = (dI_D/dV_{GS})_{V_{DS}} \quad (43)$$

4 Results and Discussion

4.1 Energy Band Diagram Analysis

Minute study of energy band diagram helps to assess the carrier transport across source channel interface for a n -channel tunnel FET. Unlike conventional TFET structures, our proposed AES-TFET offers a typical elevated source structure which eventually capitalizes the corner effect at the junction. Due this corner effect, the thin tunneling barrier can easily be tunnelled through by carriers from source to intrinsic channel regions of AES-TFET. Considering indirect B2B tunneling and other device model parameters, the simulation work is performed using 2D SILVACO TCAD device simulator. The dotted encircled area shown in figure 3 represents the improved tunneling window developed by proposed AES-TFET model at 0.5V of supply voltage.

Fig.3 Energy band diagram of AES-TFET at $V_{gs} = 1\text{V}$, $V_{DD} = 0.5\text{V}$

4.2 Surface Potential Distribution

The potential distribution along the surface of our proposed device AES-TFET structure is investigated based on the two-dimensional Poisson's equation. Across the source-channel interface region and due to its typical elevated structure, the variation of surface potential is substantially plotted in figure 4. The simulation is done using TCAD device simulator, keeping supply voltage (V_{DD}) fixed at 0.5V in order to utilize this device model for low power applications.

Therefore, by varying the gate-source voltage (V_{gs}) ranging from 1V to 0.5V, the potential distribution can be studied. In figure 4, it can be very well observed that the simulation data become almost in line with analytical dataset.

Fig.4 Surface potential distribution along the channel of AES-TFET for different gate-to-source voltages (V_{gs}) at $V_{DD}=0.5V$

4.3 Electric Field variation along the channel

Figure 5 shows the comparison between simulation and analytical values obtained from electric field variation. For different gate to source voltages (V_{gs}), the electric field (lateral and vertical) varies considerably. In our proposed structure, the source has been elevated to introduce corner effect at source – channel tunneling

interface. This further result large overlapping between the bottom edge of conduction band and top edge of valence band. Because of which, in this fig. 5, a spike has been identified at source-channel junction. However, electric field distribution remains same at rest of the channel region except a slight change near drain depleted region. Here, the analytical results almost match with the simulated graphical representations. This validates the work.

Fig.5 Electric field distribution along the channel of AES-TFET for different gate-to-source voltages (V_{gs}) at $V_{DD}=0.5V$

4.4 Transfer Characteristics

Although the tunnel FET structure with modified device models act as proper replacement of conventional MOSFET device structures, but the low ON state current has been major limitation in tunnel FET device modelling. Keeping these limitations in view, in this work the conventional source has been elevated to introduce the sharp corner deep inside the lessly doped intrinsic channel. In addition to this, at this tunneling junction *Si-Ge* material has been proposed to embed the stress-strain effect, which further helped to boost the drain current (I_{ON}). In figure 6, the transfer characteristics depicts

the improvement in drain current for better device performance.

4.5 Transconductance

Solving the equation 43, the analytical modelling of proposed asymmetric elevated source tunnel field effect transistor (AES-TFET) structure has been validated with simulation data of transconductance (g_m). Further the transconductance of AES-TFET has been compared with conventional TFET symmetric structures (figure 7).

Fig.6 Transfer characteristics (I_d vs V_{gs}) analysis between Conventional TFET and proposed AES-TFET at $V_{DD}=0.5V$

Fig.7 Transconductance (g_m vs V_{gs}) analysis between Conventional TFET and proposed AES-TFET at $V_{DD}=0.5V$

5 Conclusion

In this work a detail numerical analysis has been performed for our proposed asymmetric elevated source tunnel field effect transistor (AES-TFET). Analytical modelling of potential distribution along the channel surface, electric field variation, drain current and transconductance has been derived using 2-D Poisson's equation, considering parabolic approximation method. Besides this, using 2-D SILVACO TCAD device simulator, all device characteristics has been simulated and graphically plotted. The analytical model shows a substantial agreement in matching with simulation model dataset. These graphical representations validate our work. All D.C characteristics has been performed at 0.5V of supply voltage for low power device applications. The major challenge of improving sub-threshold swing (SS) has been taken care of by the proposed model, where $SS = 21.83$ mV/decade has been recorded as best compared to symmetric single gated conventional TFET structure. The ON state current and ambipolar current suppression has also been achieved at greater extent, shown in transfer function analysis of both device models.

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Figures

Figure 1

Three-dimensional view of proposed AES-TFET device model

Figure 2

Three-dimensional view of symmetric conventional TFET device model

Figure 3

Energy band diagram of AES-TFET at $V_{gs} = 1V$, $V_{DD} = 0.5V$

Figure 4

Surface potential distribution along the channel of AES-TFET for different gate-to-source voltages (V_{gs}) at $V_{DD}= 0.5V$

Figure 5

Electric field distribution along the channel of AES-TFET for different gate-to-source voltages (V_{gs}) at $V_{DD}= 0.5V$

Figure 6

Transfer characteristics (I_d vs V_{gs}) analysis between Conventional TFET and proposed AES-TFET at $V_{DD}=0.5V$

Figure 7

Transconductance (g_m vs V_{gs}) analysis between Conventional TFET and proposed AES-TFET at $V_{DD} = 0.5V$