Comparative Analysis of Different Figures of Merit for Algan/Gan and Si Surrounding-Gate Field Effect Transistors (SG-Fets)

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Abstract

The combination of better transport properties of III-V group semiconductors along with excellent electrostatic control of surrounding gate is a promising option for the future low power electronics. Accordingly in this brief, the major figures of merit (FOM) including output current, output conductance (g_d), transconductance generation factor (TGF), intrinsic gain (dB), and dynamic power dissipation are computed for surrounding-gate field effect transistors (SG-FETs) considering III-V group semiconductors and Si channel material respectively with respect to different device parameters. It is noticed that the center potential is higher in AlGaIn/GaN SG-FET than Si for different values of channel length (CL), channel height (H), oxide thickness (t_{ox}), and doping concentration (N_d). The AlGaIn/GaN SG-FET provides lower g_d than Si for different values of CL, H, t_{ox} , and N_d as required for MOS analog circuits to achieve higher gain. The peak value of TGF and intrinsic gain is higher in AlGaIn/GaN than Si SG-FET for different values of CL, H, t_{ox} , and N_d . In this work, we have analyzed the MOSFET structure for normally off operation of AlGaIn/GaN high electron mobility transistors (HEMTs) to reduce dynamic power dissipation (P_D). The magnitude of P_D is calculated to be lower in normally off AlGaIn/GaN SG-FET than Si for different values of CL, H, and t_{ox} .

1. Introduction:

Since the invention of IC technology, there has been quest for integrating more and more functionalities on a single IC which led to miniaturization of the transistors [1]. The major problem associated with the conventional Si Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) is the parasitic capacitance and the corresponding resistance that enhances as device dimensions reduce [2]. The utilization of III-V compound semiconductor as channel material with improved electron mobility and lower effective mass than Si offers the promising option for device scaling to nano-meter regime [3][4][5]. The improved scalability of MOSFET over what single gate devices can deliver required 3D or multigate device designs [2] [6] [7]. The III-V channel material based multi-gate field effect transistor represents the recent committing technology for very high power, high temperature, high frequency, and high linear conditions [8] [9] [10]. The scaling down the size of field effect transistors (FETs) also introduces short-channel effects (SCEs), that can be mitigated by enhanced gate control over the channel [11]. The international technology roadmap for semiconductors (ITRS) roadmap also depicts the fact that for sub 100 nm device sizes the multiple gate MOSFETs are to be used due to reduced SCEs [12] [13]. The capability of the III-V semiconductors to integrate with the conventional Si CMOS makes them a potential contender for the realization of n-MOSFETs [14]. S. Takatani et al. [15] reported that the III-V channel material field effect transistors have significant potential for the realization of antenna switches in microwave communication systems due to their low on resistance (R_{ON}).

2. Structure Description:

The multigate geometry allows the reduction in SCEs. The several types of multiple gate transistors e.g., double, triple, Ω , Π , surround gate etc. have been proposed out of which SG-FET is being extensively explored presently. The surrounding gate structure is very committing and provides the best control over the channel. Fig. 1 (a) and (b) represents the structure of surrounding gate field effect transistor (SG-FET) for Si and III-V channel material respectively. Table 1 and 2 represents the different device parameters and relations used in the present work [13]. Table 3, 4, 5, and 6 represents the computation of center potential for different channel length (CL), channel height (H), oxide thickness (t_{ox}), and doping concentration (N_d) respectively. The simulations have been performed using the commercially available Silvaco ATLAS device simulator [16], which is commonly used to characterize the electrical properties of different semiconductor devices. The simulated results for center potential have been validated against analytical modeling for the Si channel material in our previous work [13]. After validation of the results for Surrounding-Gate FET having Si as channel material we have approached further in the present work with GaN as the channel material. GaN based electronic devices are considered very promising for power switching applications because of their excellent material properties such as high breakdown electric field and high electron conductivity of the two-dimensional electron gas (2DEG). Conventional AlGaN/GaN HEMT is a normally ON device because of its strong polarization effect and 2DEG density at the heterointerface. However, for power electronics applications, normally OFF operation is required to reduce power consumption and simplify circuit configuration [17]. In AlGaN/GaN field effect transistor, the electron mobility is higher than in comparably doped bulk material because the high sheet electron density screens the ionized impurities and diminishes the scattering [18].

Table 1: Parameters used in present work

Parameter	Value
SiO ₂ layer thickness (t_{ox} , nm)	2
Channel length (CL, nm)	20
Atomic Composition of Al	0.28
Work function of Gate (eV)	4.3
Doping conc. of barrier (N_d , cm ⁻³)	1x10¹⁹
Channel height (H, nm)	10

Table 2: Relations used

Symbol	Quantity	Unit	Relations Used
TGF	Transconductance generation factor	V^{-1}	
g_d	Output conductance	$A/\mu mV$	
A_v	Intrinsic gain	dB	

Table 3: Computation of Center Potential w.r.t. channel length for different position along the channel from the source to drain side (X)

CL (nm)	X (nm)	Center Potential (V) for Si material		Center Potential (V) for III-V material
		Simulation	Model [13]	Simulation
20	0	0.526	0.525	2.115
	5	0.139	0.127	1.192
	10	0.009	0.012	1.006
	15	0.139	0.127	0.984
	20	0.526	0.526	1.006
30	0	0.526	0.526	2.115
	5	0.114	0.121	1.193
	10	-0.078	-0.063	1.010
	15	-0.123	-0.116	0.971
	20	-0.077	-0.063	0.966
	25	0.114	0.121	0.972
	30	0.526	0.526	1.015
40	0	0.526	0.526	2.114
	5	0.112	0.129	1.189
	10	-0.087	-0.066	1.050
	15	-0.152	-0.156	0.961
	20	-0.167	-0.182	0.963
	25	-0.152	-0.156	0.971
	30	-0.087	-0.066	0.973
	35	0.111	0.129	0.975
	40	0.526	0.526	0.999

Table 4: Computation of Center Potential w.r.t. channel height for different position along the channel from the source to drain side (X)

H (nm)	X (nm)	Center Potential (V) for Si material		Center Potential (V) for III-V material
		Simulation	Model [13]	Simulation
10	0	0.526	0.526	2.115
	5	0.139	0.129	1.191
	10	0.009	0.013	1.006
	15	0.139	0.129	0.983
	20	0.526	0.526	1.029
18	0	0.526	0.526	2.115
	5	0.292	0.283	1.254
	10	0.195	0.201	1.090
	15	0.291	0.283	1.067
	20	0.526	0.526	1.123

Table 5: Computation of Center Potential w.r.t. SiO_2 thickness for different position along the channel from the source to drain side (X)

tox (nm)	X (nm)	Center Potential (V) for Si material		Center Potential (V) for III-V material
		Simulation	Model [13]	Simulation
1	0	0.526	0.526	2.115
	5	-0.006	-0.005	1.056
	10	-0.157	-0.158	0.904
	15	-0.006	-0.005	0.890
	20	0.525	0.526	0.904
1.5	0	0.526	0.526	2.115
	5	0.139	0.067	1.137
	10	-0.068	-0.067	0.962
	15	0.067	0.073	0.942
	20	0.526	0.526	0.962
2	0	0.526	0.526	2.115
	5	0.139	0.128	1.200
	10	0.009	0.008	1.010
	15	0.139	0.128	0.987
	20	0.526	0.526	1.010
2.5	0	0.526	0.526	2.115
	5	0.195	0.179	1.259
	10	0.078	0.072	1.060
	15	0.195	0.179	1.034
	20	0.525	0.526	1.060

Table 6: Computation of Center Potential w.r.t. doping concentration for different position along the channel from the source to drain side (X)

Nd (cm ⁻³)	X (nm)	Center Potential (V) for Si material		Center Potential (V) for III-V material
		Simulation	Model [13]	Simulation
5x10¹⁸	0	0.508	0.508	2.096
	5	0.023	0.018	1.079
	10	-0.128	-0.129	0.930
	15	0.023	0.018	1.079
	20	0.508	0.508	1.877
1x10¹⁹	0	0.526	0.526	2.029
	5	0.139	0.130	1.094
	10	0.009	0.010	1.019
	15	0.139	0.130	1.234
	20	0.526	0.526	1.890

3. Results And Discussions:

Fig. 2(a)-(d) depicts the numerical computation of drain current, output conductance, transconductance generation factor, and intrinsic gain respectively for different values of t_{ox} . It is obvious from Fig. 2(a) that in weak inversion region of III-V channel material FET for lower values of (gate-source voltage) V_{GS} as t_{ox} is reduced; drain current is also reduced due to the reduction in gate capacitance caused due to the influence of quantum capacitance. Fig. 2(b) depicts the computation of output conductance (g_d) in respect of different thickness of the oxide layer. As oxide thickness increases output conductance increases resulting in lower output resistance thereby reducing the gain of the device. Fig. 2(b) indicates that the pinnacle value of g_d decreases by 15.21% when t_{ox} is reduced to 1 nm from 2.5 nm for Si channel material at (drain-source voltage) $V_{DS}=0$ V. The pinnacle value of g_d shifts from $V_{DS}=0.66$ to $V_{DS}=0.64$ V and pinnacle value enhances by 6.73% when t_{ox} is reduced from 2.5 nm to 1 nm for III-V channel material SG-FET. Fig. 2(c) depicts the computation of TGF in respect of gate voltage for different values of t_{ox} . Fig. 2(c) indicates that TGF is higher at lower values of t_{ox} for both III-V and Si channel material SG-FET. The magnitude of transconductance (gm_1) and drain current (I_D) increases when oxide thickness (t_{ox}) is reduced for III-V channel material surrounding-gate FET. The transconductance generation factor (TGF) is expressed as the ratio of gm_1 and I_D . So, TGF increases when t_{ox} is reduced. The pinnacle value of TGF reduces by 13.96% when t_{ox} is enhanced from 2.5 nm to 1 nm oxide thickness for Si channel material based SG-FET. Fig. 2(d) depicts the computation of intrinsic gain (dB) and it is obvious that intrinsic gain is higher at lower values of t_{ox} for both devices. The pinnacle value of intrinsic gain reduces by 27.6%

when thickness of oxide layer is enhanced from 1 to 2.5 nm for Si channel material SG-FET. The lower value of output conductance is desirable to achieve higher gain.

Fig. 3(a) depicts the variation of drain current in respect of V_{GS} , and it is obvious that the pinnacle magnitude of drain current enhances by 5.31% and 78.39% when CL decreases from 50 to 20 nm for III-V and Si channel material respectively at $V_{GS}=1.08$ V. The drain current is proportional (inversely) to CL, hence it is noticed that as CL reduces, the drain current increases for both Si and III-V channel material devices. So, lower channel length yields a higher drain current. Fig. 3(b) depicts the calculation of g_d in respect of V_{DS} for different channel length. As channel length reduces, output resistance decreases and output conductance increases. It is obvious from Fig. 3(b) that g_d is higher for lower values of channel length for both III-V and Si channel material SG-FET. Fig. 3(c) depicts the calculation of TGF in respect of V_{GS} for different channel length. As CL reduces, the drain current and transconductance increases and consequently TGF reduces. It can be concluded from Fig. 3(c) that as channel length enhances, TGF is also increased. It is evident from Fig. 3(c) that the pinnacle value of TGF reduces by 2.19% at $V_{GS}=0.14$ V and 9.17% at $V_{GS}=0$ V when the channel length is decreased from 50 to 20 nm for III-V and Si channel material respectively. Fig. 3(d) depicts the computation of intrinsic gain (dB) for different channel length. As CL reduces, the transconductance and output conductance increases. It is evident against Fig. 3(d) that higher channel length results in a greater magnitude of intrinsic gain.

The variation of the drain current in respect of V_{GS} for dissimilar magnitudes of channel height at V_{DS} of 1 V is represented by Fig. 4(a). The drain current reduces due to the reduction in the cross-sectional area for the flow of charge carriers when the height of the channel is reduced. It is obvious from Fig. 4(a) that the pinnacle magnitude of drain current reduces by 46.57% and 32.9% when H is reduced from 18 to 10 nm for III-V and Si channel material respectively at $V_{GS}=1.08$ V. Fig. 4(b) depicts the variation of g_d in respect of V_{DS} for dissimilar channel height. The output conductance enhances as channel height increases causing a decrease in the output resistance. It is obvious from Fig. 4(b) that higher channel height yields higher output conductance for both III-V and Si channel material SG-FET. Fig. 4(c) depicts the calculation of TGF in respect of V_{GS} for dissimilar magnitude of H. It is obvious from Fig. 4(c) that the lower magnitude of H yields a higher value of TGF. TGF is almost constant at lower values of V_{GS} and reduces as V_{GS} reduces. Fig. 4(d) depicts the computation of intrinsic gain (dB) for dissimilar channel height, and it is obvious that lower channel height yields higher intrinsic gain in III-V and Si channel material SG-FET.

Fig. 5(a) depicts the variation of drain current in respect of V_{GS} , and it is obvious that the pinnacle value of drain current reduces by 22.83% and 44.52% when N_d is decreased from 1×10^{19} to $5 \times 10^{18} \text{ cm}^{-3}$ for III-V and Si channel material SG-FET respectively at $V_{GS}=1.08$ V. Fig. 5(b) depicts the computation of output conductance in respect of V_{DS} for dissimilar magnitude of N_d . As N_d increases output conductance also enhances resulting in decreasing output resistance. Fig. 5(c) depicts the calculation of TGF in respect of V_{GS} for dissimilar magnitude of N_d . The intrinsic gain and TGF both reduces with increase in magnitude of N_d . The pinnacle value of TGF is reduced by 21.96% when doping concentration is increased from

5×10^{18} to $1 \times 10^{19} \text{ cm}^{-3}$ for Si channel material SG-FET. Fig. 5(d) depicts the calculation of intrinsic gain in respect of V_{GS} for dissimilar magnitude of N_d .

The dynamic power dissipation (P_D) is the product of clock frequency (f_p), load capacitance (C_L), and square of the supply voltage (V_{DD}). The P_D can be reduced by reducing any of the three parameters among f_p , C_L , and V_{DD} . The problem associated with the reduction of f_p is increased time delay. The second approach is to reduce C_L , but it involves system design so that system components such as wires and the number of pins are reduced, and fan-out is minimized. Another generic approach is to reduce the supply voltage V_{DD} ; which is possible only through device technology.

Fig. 6 depicts the computation of dynamic power dissipation at $V_{DS}=1 \text{ V}$ and 1 MHz frequency. Fig. 6(a) depicts the variation of P_D in respect of V_{GS} for different magnitudes of C_L . The pinnacle magnitude of P_D reduces by 65.35% when C_L is decreased from 50 to 20 nm for III-V channel material at $V_{GS}=1.08 \text{ V}$. The pinnacle magnitude of P_D shifts from $V_{GS}=1.08 \text{ V}$ to $V_{GS}=1.02 \text{ V}$ and pinnacle magnitude decreases by 69.50% when C_L is decreased from 50 to 20 nm for Si. The magnitude of P_D in Si is noticed to be higher than III-V channel material for 50 nm and 20 nm channel lengths. Fig. 6(b) depicts the variation of P_D in respect of V_{GS} for different channel height. The magnitude of P_D in III-V channel material is less as compared to Si for 18 nm and 10 nm channel height. Fig. 6(c) depicts the variation of P_D in respect of V_{GS} for different values of t_{ox} . The magnitude of dynamic power dissipation in III-V channel material is less than Si.

4. Conclusion:

The major figures of merit (FOM) including output current, output conductance (g_d), transconductance generation factor (TGF), intrinsic gain (dB), and dynamic power dissipation are computed for different device parameters. It has been noticed that the intrinsic gain and TGF enhances with increment in channel length. On the other hand, intrinsic gain and TGF decreases with increase in oxide thickness, channel height, and doping concentration. The center potential is higher in III-V channel material than Si for different C_L , H , t_{ox} , and N_d . It is also noticed that the intrinsic gain in III-V surrounding gate FET is higher than Si channel material. It can be concluded on the basis of the analysis performed in this work that for optimum performance it is advisable that the magnitude of C_L , H , t_{ox} , and N_d should be less. It has been analyzed that the magnitude of dynamic power dissipation in III-V channel material is less than Si for 2.5 nm and 1 nm oxide thickness.

Declarations

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Figures

Figure 1

(a): 3-D View of Si channel material surrounding-gate FET (b): 3-D View of III-V channel material surrounding-gate FET

Figure 2

Computation of (a) Drain Current (b) Output-conductance (c) TGF (d) Gain; w.r.t. different tox

Figure 3

Computation of (a) Drain Current (b) Output-conductance (c) TGF (d) Gain; w.r.t. different CL

Figure 4

Computation of (a) Drain Current (b) Output-conductance (c) TGF (d) Gain; w.r.t. different H

Figure 5

Computation of (a) Drain Current (b) Output-conductance (c) TGF (d) Gain; w.r.t. different N_d

Figure 6

Power dissipation in reference of different (a) Channel length (nm) (b) Channel height (nm) (c) Oxide Thickness (nm)