

Assessment of Interface Trap Charges on Proposed TFET for Low Power High-frequency Application

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Assessment of Interface Trap Charges on Proposed TFET for Low Power High-Frequency Application

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Abstract Accumulation of trap charges at the semiconductor and oxide interface is the most dominating factor and cannot be neglected as it degrades device performance and reliability. This manuscript, presents detailed investigation to analyze the impact of interface trap charges (ITCs) on the performance parameters of the proposed device i.e., heterogeneous dielectric dual metal gate step channel TFET (HD DMG SC-TFET). The comparative study is conducted with dual metal gate step channel TEFT (DMG SC-TFET). The proposed device shows improved current carrying capability, suppressed ambipolar behaviour with steeper sub-threshold swing. The purpose of this study to determine the ITCs impact on DC characteristics and analog/RF electrical performance parameters of the proposed device. It further observed that the proposed device exhibit superior performance due to dielectric engineering at oxide layer. Moreover, advanced communication devices must respond linearly therefore, the impact of ITCs on linearity parameters is also studied. From this brief comparative investigation, it is observed that the proposed TFET exhibits negligible distortion in linearity parameters with little or no impact of trap charges as compared to DMG SC-TFET. Thus, proposed TFET is appropriate for ultra-low power high-frequency electronic devices.

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1 Introduction

The semiconductor industry shows rapidly growth in 20th century. The reason behind this is MOSFETs. Nowadays, billions of transistors are inter-connect on single microprocessors for enhanced device performance. Today's transistors are the building block for low power electronic devices. So, MOSFETs is scaled down to increase device performance in term of switching speed, power consumption, and package density per unit area constant with reduced fabrication cost. This continuous down-scaling of MOSFETs has also lead to adverse impact on a device due to unacceptable enhancement in the leakages current that creates major problems at room temperature such as sub threshold leakage current, short circuit effect (SCE), mobility degradation, drain induced barrier lowering (DIBL), impact ionization, hot carrier effects (HCE) and static power consumption [1–3]. In addition to this MOSFET limits the subthreshold slope to 60mV/decades [4].

In this concern, the tunnel field-effect transistor (TFET) shows very promising behavior to overcomes the aforementioned limitation of MOSFET [5]. It offers sharper turn-on devices compared to MOSFET and shows better performance for low-power electronic device. TFET works on phenomena of quantum tunneling of charge carrier from source to channel which benefits steeper switching characteristics and reduced power consumption [6]. Apart from these advantages it also suffers from several limitations such as low current driving capability and ambipolar current behavior that degrades the

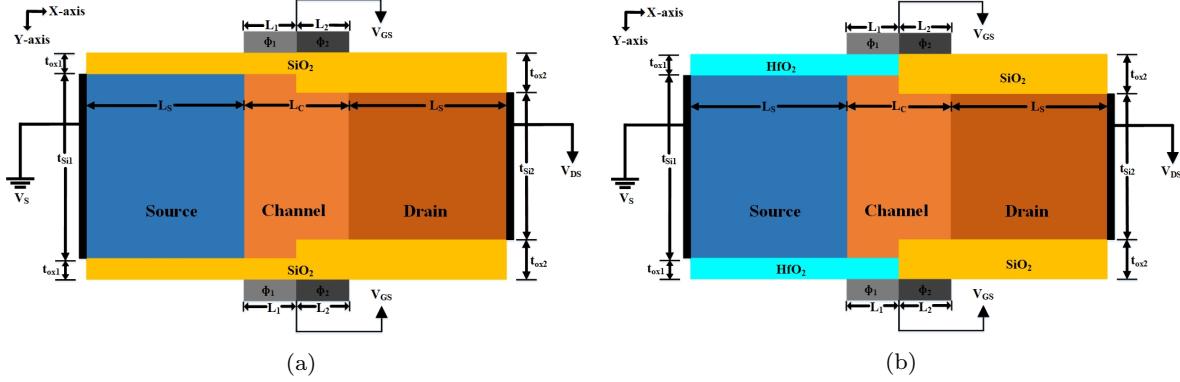


Fig. 1: Device Schematic view of (a) DMG SC-TEFT (b) HD DMG SC-TEFT

device analog/RF performance [7]. In order to overcome these limitations of conventional TFET various techniques are introduced such as gate engineering [8], dielectric engineering [9], doping engineering [10], material engineering [11] and many more.

In order to solve issues related to conventional TFET a novel combination of gate engineering with step channel structural modification [12] are implemented in this manuscript as dual metal gate step channel TFET (DMG SC-TFET). Due to this an intense improved ON-state current with steeper subthreshold swing is noticed. For further reducing threshold voltage and increase current driving capability implementation of dielectric engineering followed with gate engineering and step channel structural modification leads to our proposed device heterogeneous dielectric dual metal gate step channel TFET (HD DMG SC-TFET).

However, during fabrication process ITCs are generally accumulated at semiconductor/oxide interface due to damage induced by bond breaking, oxidation, radiation, and stress which are responsible for degrading the life span of the devices [13, 14]. These traps charges are categorized as donor trap charges and acceptor trap charges. Donor trap charges are presented above the valance energy band which acts as a positive ITCs when it denotes an electron whereas acceptor trap charges are present below the conduction energy band and it acts as a negative ITCs when it accepts an electron [15, 16].

In TFETs these trap charges are accumulated because of missive electric field at the tunneling junction which excited silicon body surface that leads to modification of the electric field at source/channel junction (SC-junction) [17]. In addition, the output current is exponentially dependent on the electric field at junction [18] that results in a change in the current-carrying capability of devices. So, it is mandatory to determine the impact of trap charges on performance parameters of device.

This manuscript is arranged into different sections as follows: Section 2 discussed device structure, simulation parameters, and device specification. Whereas, Section 3 investigates the impact of ITCs on physical characteristics, analog/RF and linearity performance parameters. Finally, Section 4 concludes the important finding of this brief study.

2 Devices Structure

Previously various research works have been conducted to show the impact of oxide thickness on I_{on} and sub-threshold swing [19, 20]. These works particularly conclude that reduced oxide thickness provides higher oxide capacitance with improves gate control capability which allows faster transition of charge carrier through tunnel barrier that results in enhance I_{on} with steeper subthreshold swing [21]. However, to avoid high leakage current, oxide thickness is practically limited to not less than 1nm [22]. Therefore to maintain lower leakage current that make a power efficient device we have made oxide layer of 2nm thickness [23, 24] at the drain-channel junction and to enhances I_{on} with steeper sub-threshold swing the oxide thickness is kept as 1nm [25] at the source-channel junction that allows a greater number of fanouts with higher switching rate. This leads to step channel structure.

To overcome the challenges of conventional TFET, we have proposed a novel schematic of TFETs which are illustrated in Fig.1. Fig.1a and Fig.1b portrayed the device schematic cross-section view of DMG SC-TFET and HD DMG SC-TFET. For DMG SC-TFET gate engineering is employed on the gate electrode with decreased oxide layer thickness at SC-junction. This allows better subthreshold swing and high current driving capability in the range 10⁻⁵ with suppressed ambipolar behavior in the range 10⁻¹⁵. For HD DMG SC-TFET oxide layer at SC-junction is deposited with hafnium

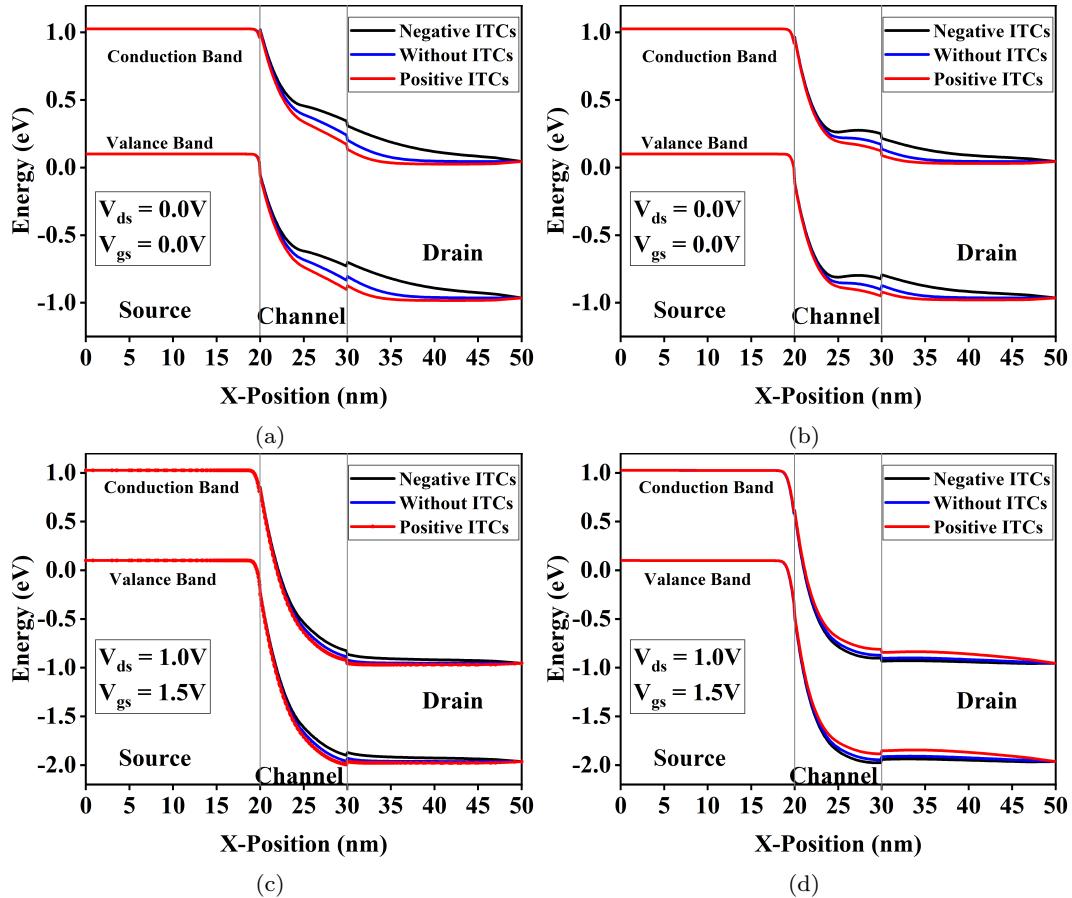


Fig. 2: Impact of ITC on (a) Energy Band of DMG SC-TFET under Thermal Equilibrium (b) Energy Band of HD DMG SC-TFET under Thermal Equilibrium (c) Energy Band of DMG SC-TFET under ON-State (d) Energy Band of HD DMG SC-TFET under ON-State

Table 1: Structural parameters value

Parameters (Notation)	Value & Unit
Source (p-type) doping (N_S)	$5 \times 10^{20} \text{ cm}^{-3}$
Channel doping (N_C)	$1 \times 10^{17} \text{ cm}^{-3}$
Drain (n-type) doping (N_D)	$5 \times 10^{18} \text{ cm}^{-3}$
Source length (L_S)	20nm
Oxide thickness at SC-junction (t_{ox1})	1nm
Channel length (L_C)	10nm
Oxide thickness at DC-junction (t_{ox2})	2nm
Drain length (L_D)	20nm
Source thickness (t_{si1})	8nm
Drain thickness (t_{si2})	6nm
Tunnel gate length (L_1)	5nm
Auxiliary gate length (L_2)	5nm
Tunnel gate work function (ϕ_1)	4.02eV
Auxiliary gate work function (ϕ_2)	4.50eV

oxide (HfO_2) that increases the tunneling probability of charge carrier at SC-junction. This leads to a reduc-

tion in threshold voltage and enhances current driving capability in the range of 10^{-4} .

The simulation is carried out using TCAD software called Silvaco Atlas Simulator. Since, TFET is works on phenomena of quantum tunneling of charge carrier through potential barrier, bandgap narrowing (BGN) model and band to band tunneling (BTBT) models are used for simulation. In addition to these models some more physical models are used in this study such as Shockley read hall (SRH) model, concentration depended on mobility (CONMOB) model, field depended on mobility (FLDMOB) model, and Auger recombination (Auger) model. Also newton methods are employed for mathematical calculation. To investigates the impact of ITCs on electrical performance parameters of proposed TFET interfacial charge density are taken as $1 \times 10^{12} \text{ cm}^{-3}$. Further, Table 1 depicted device specification and parameters that we used in the simulation of both TFETs.

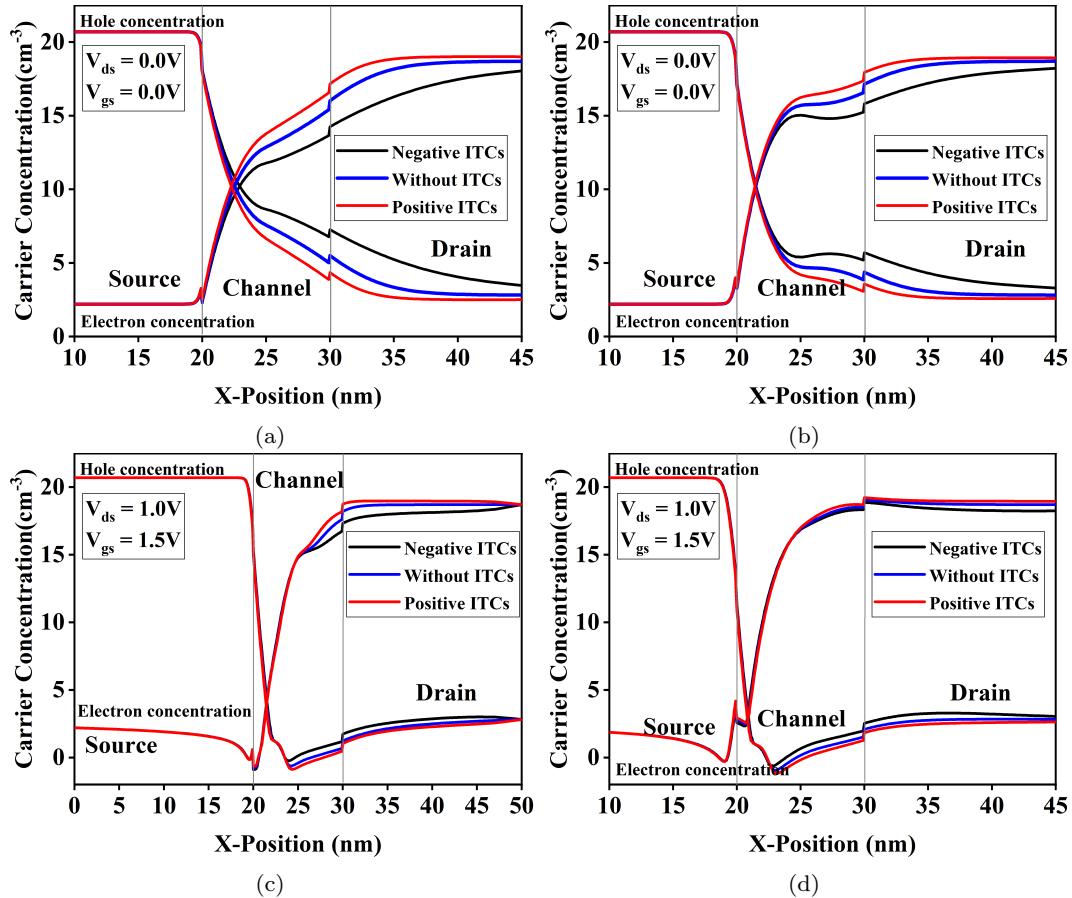


Fig. 3: Impact of ITC on (a) Carrier Concentration of DMG SC-TFET under Thermal Equilibrium (b) Carrier Concentration of HD DMG SC-TFET under Thermal Equilibrium (c) Carrier Concentration of DMG SC-TFET under ON-State (d) Carrier Concentration of HD DMG SC-TFET under ON-State

3 Result and discussion

In this section, an investigation is carried out to examine the impact of ITCs on physical characteristics, DC characteristics and analog/RF parameters for both simulated TFETs. Moreover, advance wireless communication system devices must behave linearly towards applied voltage. Hence, a comparative study of the linearity parameter is also carried out to determine device susceptibility toward reliable communication.

3.1 Physical Characteristics

This section discuss the physical characteristics of device illustrated in Fig 1. The study have been done under thermal equilibrium and ON-state with impact of positive ITCs, without ITCs and negative ITCs.

3.1.1 Energy Band

The impact of ITCs on energy band as function of device length are illustrated in Fig.2. Under thermal equilibrium, it is clearly observed from Fig. 2a,2b, tunneling width for charge carrier is wider that not allows to tunnel the majority carrier through junction. Also due to positive ITCs there is accumulation of electron above the valence band that allows downward shift of band, where as due to negative ITCs there accumulation of electron below the conduction band that allows upward shift of energy bands. Under ON-state, when we applied proper biasing to device, tunneling barrier for the charge carrier gets reduces as shown in Fig. 2c,2d. Moreover, it noticed that tunneling barrier of proposed TFET is lower then DMG SC-TFET because of the heterogeneous dielectric at the oxide layer which enhance the tunneling operation of the dominate charge carrier at the junction.

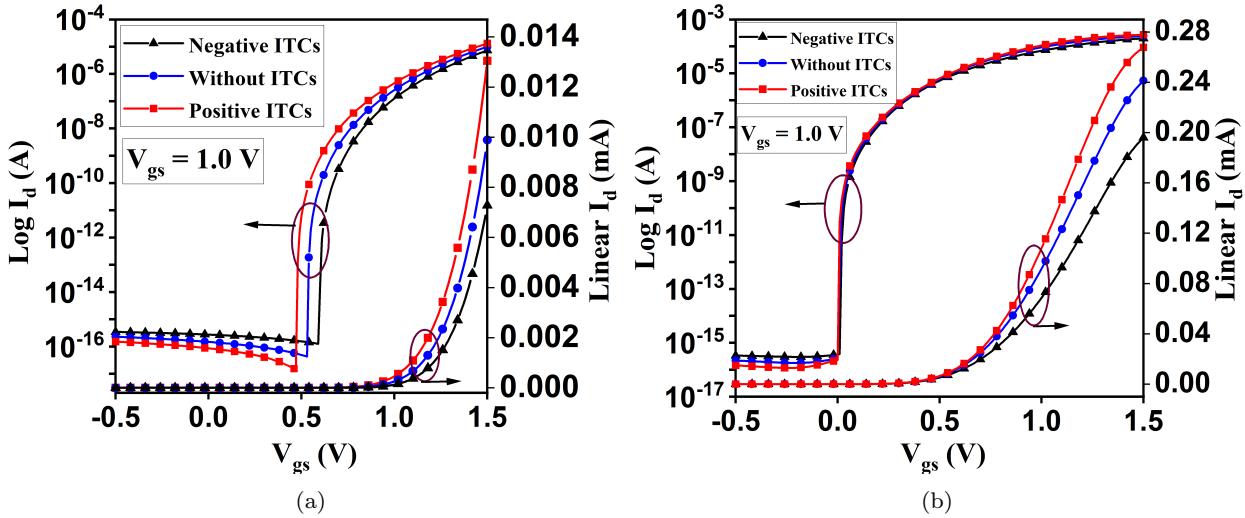


Fig. 4: Impact of ITCs on transfer characteristics (a) DMG SC-TEFT (b) HD DMG SC-TEFT

3.1.2 Carrier Concentration

Under thermal equilibrium, Fig. 3a ,3b shows the carrier (i.e, electron and hole) concentration along with channel direction where it is observed that symmetric carrier concentration in channel region with no accumulation of electron concentration in channel. Due to impact positive (negative) ITCs carrier (i.e, electron and hole) concentration get increases (decreases) in channel region as discuss earlier. Also it is notices that HD DMG SC-TFET exhibits more no number of carrier concentration in channel region as compared to DMG SC-TFET which is due to present of high- κ dielectric material at the SC-junction oxide layer. Under ON-state condition, carrier concentration in channel region is observed from Fig 3c,3d. This is due to narrowing of tunneling barrier width across the junctions that enhance the flow of charge carrier and hence charge concentration gets accumulates that leads to output current.

3.2 DC Characteristics

3.2.1 Transfer Characteristics

It represent the relationship between input voltage (i.e, V_{gs}) and output current (i.e, I_d). Fig.4 illustrates the impact of the ITCs on transfer characteristics for both TFETs on logarithmic and linear scale. Due to positive (negative) ITCs current driving capability (i.e, I_d) of both TFET devices increases (decreases). Because it improves (reduces) the energy band bending of the conduction band and valence band which results in decreased (increased) tunneling barrier. So, the probability of tunneling charge carriers gets improved (reduced) which results in a increase (decrease) in current-carrying capability. It is further observed that HD DMG SC-TFET achieves higher value I_d . This is due to the presence of HfO₂ oxide layer at SC-junction which provides better gate coupling that leads to increased tunneling probability of majority charge carrier at the junctions. Moreover, the transfer characteristics of HD DMG SC-TFET are lesser influence by trap charges as compared to DMG SC-TFET because of high tunneling rate of charge carriers.

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3.2.2 Threshold Voltage (V_{th})

For low power, high-frequency application, V_{th} of the device must be as low as possible. It is the minimum amount of voltage that is required to start tunneling phenomena at the junction that results in the current carrying capability of the device. Table 2 shows the comparison of V_{th} for both device and it is notice the proposed device shows lower V_{th} due to high- κ dielectric at the SC-junction which provides superior gate coupling at the junction with enhanced tunneling phenomena of the charge carrier that results in low V_{th} . Moreover, due to positive (negative) ITCs V_{th} of the devices decreases (increases) due to degradation (enhancement) of tunneling width at the junction.

3.2.3 Subthreshold Swing

To achieves high switching speed, the device must have steeper subthreshold swing that results in high fan-outs with reduced power consumption. The impact of ITCs on the subthreshold swing is depicted in Table 2

Table 2: Impact of ITCs on Threshold Voltage, Subthreshold Swing and I_{on}/I_{off} Ratio

Parameters	Device	+ve ITCs	without ITCs	-ve ITCs
Threshold Voltage	DMG SC-TFET	0.78V	0.80V	0.81V
	HD DMG SC-TFET	0.23V	0.24V	0.28V
Subthreshold Swing	DMG SC-TFET	2.51mV/decade	2.75mV/decade	4.58mV/decade
	HD DMG SC-TFET	1.95mV/decade	3.09mV/decade	2.38mV/decade
I_{on}/I_{off} Ratio	DMG SC-TFET	1.52×10^{11}	6.68×10^{10}	2.65×10^{10}
	HD DMG SC-TFET	1.16×10^{12}	9.05×10^{11}	5.28×10^{11}

and it notices proposed devices have high subthreshold swing as compared to DMG SC-TFET. Moreover, due to positive (negative) ITCs its values get decreases (increases) for HD DMG SC-TFET. Thus, the positive (negative) trap charge improves (degrades) the device performance.

3.2.4 I_{on}/I_{off} Ratio

In order to achieves high switching speed, device must have high I_{on}/I_{off} ratio. For this, device must have high ON-state current (I_{on}) and low OFF-state current (I_{off}). Table 2 manifest the impact of ITCs on I_{on}/I_{off} ratio and it is observe due to positive (negative) ITC I_{on}/I_{off} ratio result in increases (decreases) in value. Moreover, proposed device shows higher I_{on}/I_{off} ratio and lesser impact of ITCs in comparison to DMG SC-TFET. This makes appropriate device for ultra-low power high frequency application.

3.3 Analog/RF Parameters

In this section, a detailed comparative studies are carried out to investigates the impact of trap charges on analog/RF parameters of both the simulated TFET. These parameters play a most important role in determining device performance at high-frequency. For better reliability and good life spam, these parameters should have less impact on ITCs.

3.3.1 Gate-to-Drain capacitance (C_{gd})

C_{gd} is dominating parasitic capacitance that determines analog/RF performance parameters like cut-off frequency. Expression for C_{gd} is given by equation 1 [26]. Fig. 5 manifests a graphical representation of C_{gd} with respect to V_{gs} at different traps charges. C_{gd} of devices increase with V_{gs} due to decrease drain-channel barrier. Moreover, due to positive (negative) traps charges C_{gd} increases (decreases) because it increases (decreases) inversion layer in the channel region from drain to source. From these results, it observed that proposed TFET

shows lesser influences of trap charges due to heterogeneous dielectric material at the oxide layer which provides proper gate coupling at the junctions.

$$C_{gd} = \frac{\partial Q_g}{\partial V_{gd}} \quad (1)$$

3.3.2 Transconductance (g_m)

g_m is an essential parameter for examining device performance which is express by equation 2 [27]. g_m shows the electrical characteristics of the device that relates the I_d to applied V_{gs} and determine the current driving capability of the device. For better device performance we required high value of g_m . Fig 6 illustrate the impact of ITCs on g_m with respect to V_{gs} . Since g_m is directly proportional to I_d , therefore it increases with applied V_{gs} for both the devices but for the HD DMG SC-TFET it starts to decrease after achieves maximum peak due current saturation. Moreover, due to impact of positive (negative) ITCs plots of g_m shift upward (downward) because value of I_d increases (decreases) that leads to upgradation (degradation) analog/RF performance parameters.

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \quad (2)$$

3.3.3 Cut-off Frequency (f_T)

f_T is the most dominant performance parameter for high-frequency low power devices. According to equation 3 [28] f_T of device is directly dependent to g_m and inversely dependent to total parasitic capacitance (i.e, C_{gd} , C_{gs}) where g_m is dominating factor. Fig. 7 depicts proposed device have higher value as compared to DMG SC-TFET which is due to HfO_2 present at SC-junction which enhance tunneling phenomena. As V_{gs} increases, f_T of the both devices increases due to increment in g_m and for proposed device after attain maximum peak it start to decrease due increase in C_{gd} and mobility saturation of charge carrier. Moreover, we have observed impact of ITCs and notice f_T of the devices increases

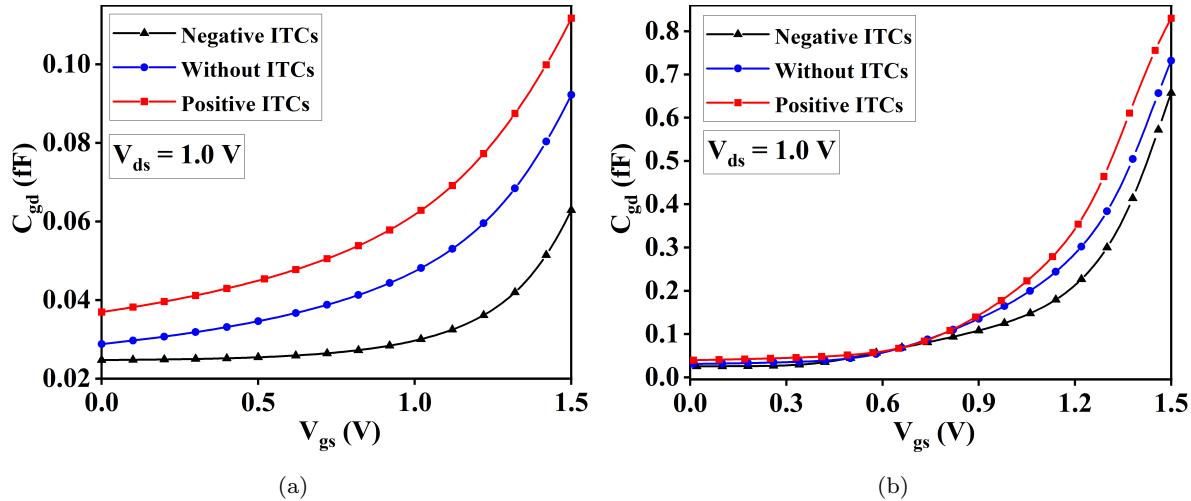


Fig. 5: Impact of ITCs on C_{gd} (a) DMG SC-TEFT (b) HD DMG SC-TEFT

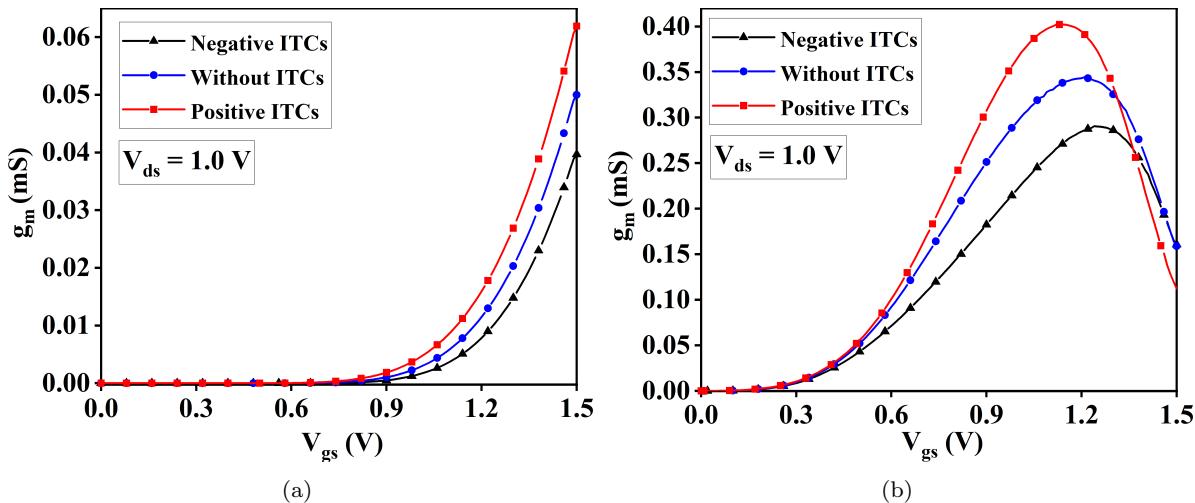


Fig. 6: Impact of ITCs on g_m (a) DMG SC-TEFT (b) HD DMG SC-TEFT

(decreases) with positive (negative) ITCs similar to g_m curve.

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \quad (3)$$

3.3.4 Gain Bandwidth Product (GBP)

GBP is also most essential performance parameter to examine the device performance. Expression of GBP is given by equation 4 [28] which shows GBP is directly dependent to g_m and inversely dependent to C_{gd} . The impact of ITCs on GBP illustrates in Fig. 8 where proposed device exhibit the higher value of GBP and it increases with V_{gs} due to high- κ dielectric material at SC-junction that reduces the tunneling barrier and enhance the tunneling phenomena of charge carrier which results in higher g_m and after attaining maximum peak

it starts to decreases due to scattering mechanism of charge carrier at high V_{gs} . Moreover, due to the positive (negative) ITCs it achieves higher (lower) peak similarly to g_m due to a direct relationship.

$$GBP = \frac{g_m}{2\pi C_{sd}} \quad (4)$$

3.3.5 Transconductance Generation Factor (TGF)

TGF is the performance parameter that determines device efficiency to convert I_d into g_m which measures the ability to convert power into speed. For better performance and low power consumption we required a higher value of TGF. The expression for TGF is given by equation 5 [29]. Fig. 9 manifest comparatives plot for the

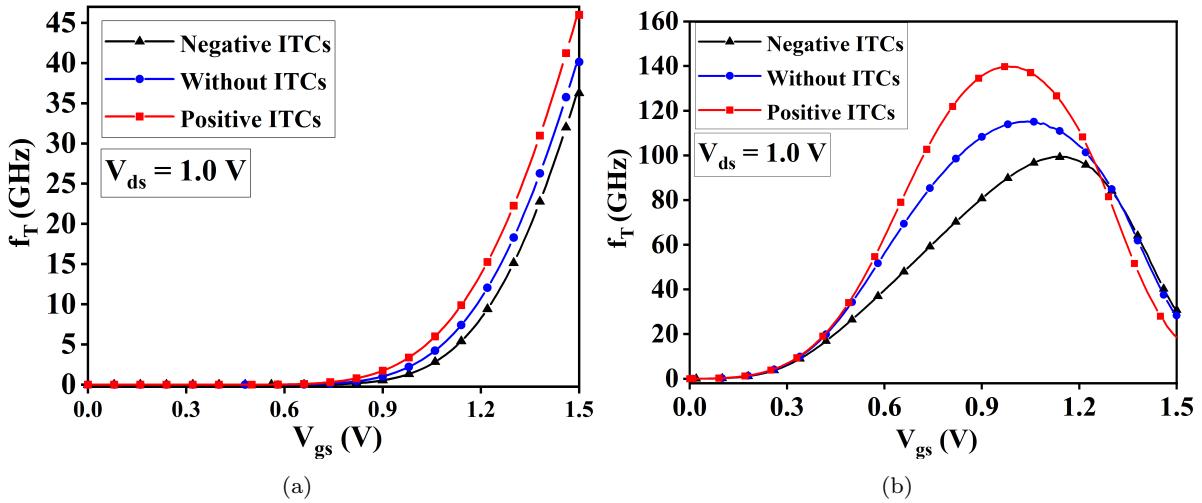


Fig. 7: Impact of ITCs on f_T (a) DMG SC-TEFT (b) HD DMG SC-TEFT

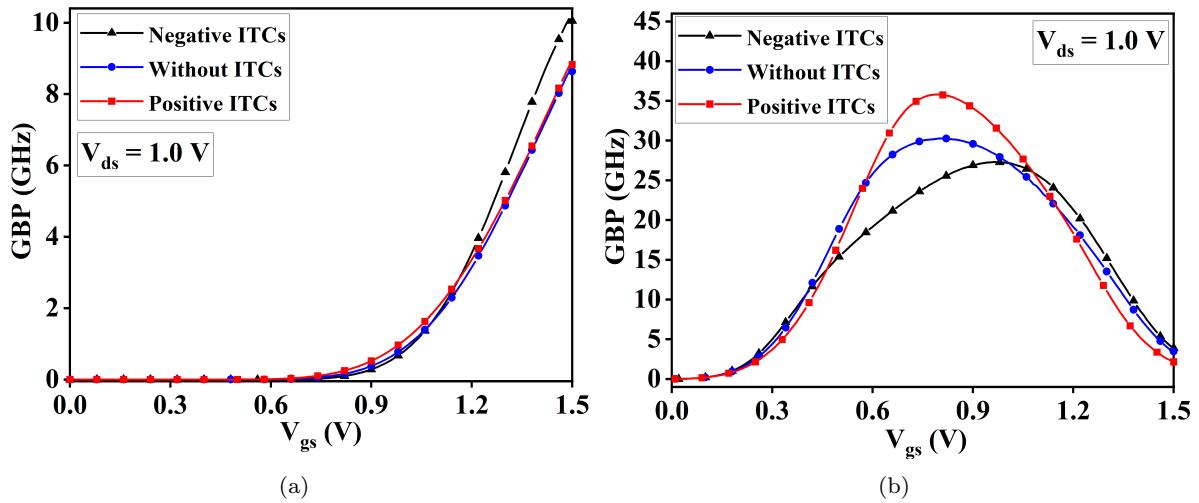


Fig. 8: Impact of ITCs on GBP (a) DMG SC-TEFT (b) HD DMG SC-TEFT

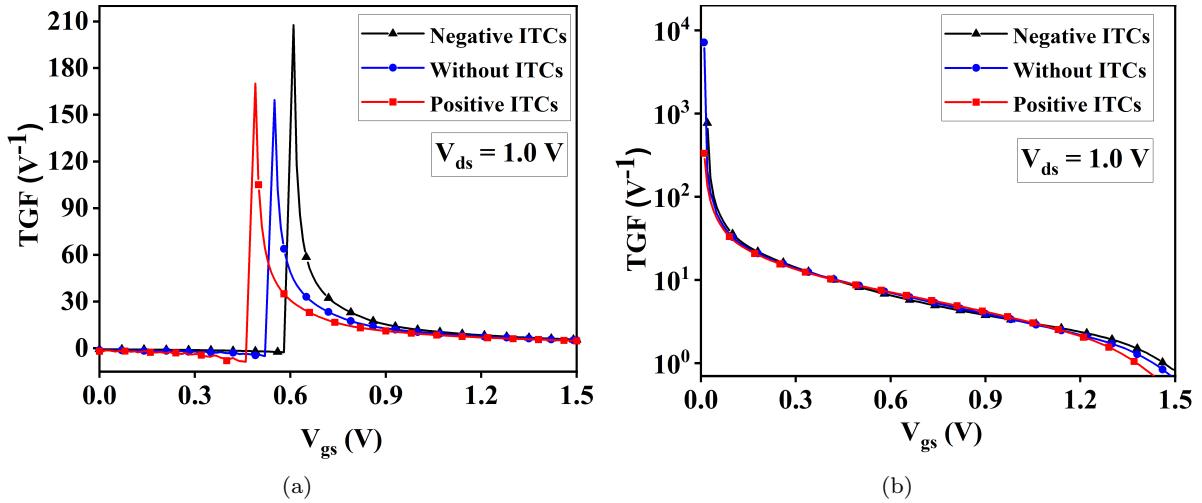


Fig. 9: Impact of ITCs on TGF (a) DMG SC-TEFT (b) HD DMG SC-TEFT

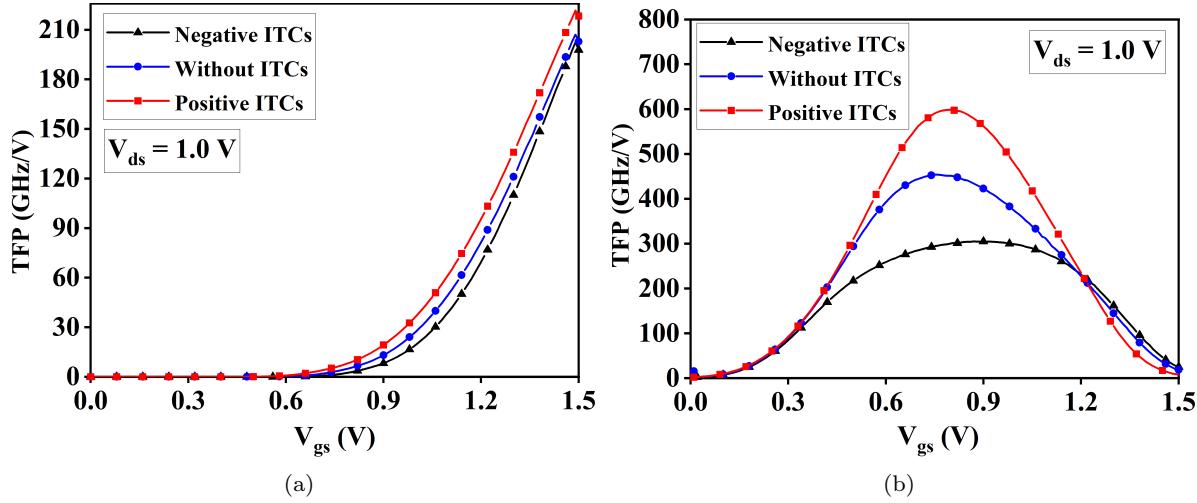
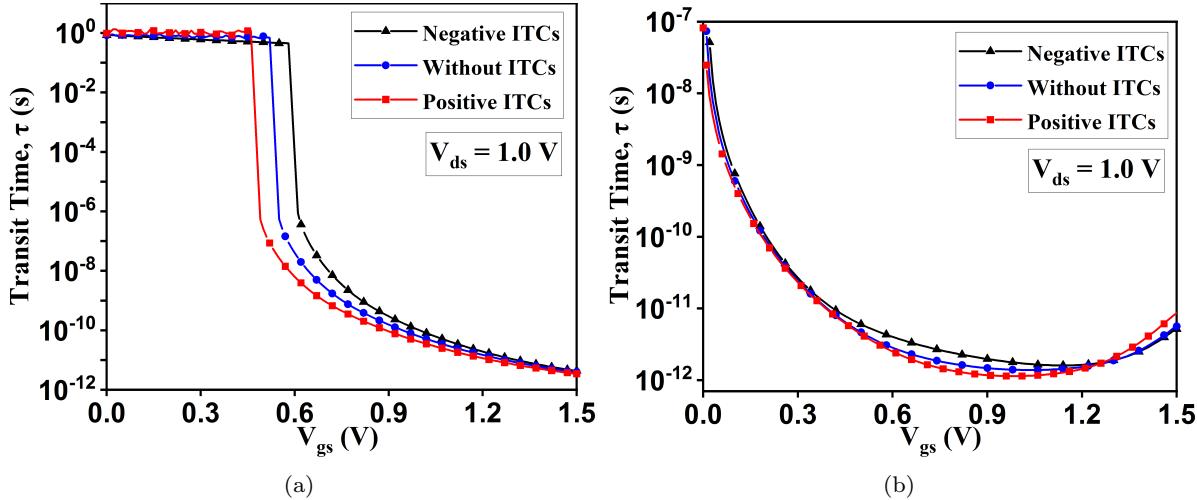


Fig. 10: Impact of ITCs on TFP (a) DMG SC-TEFT (b) HD DMG SC-TEFT

Fig. 11: Impact of ITCs on τ (a) DMG SC-TEFT (b) HD DMG SC-TEFT

impact of ITCs on TGF with a change in V_{gs} . It is observed proposed devices show higher TGF and almost negligible impact of ITCs due to the presence of HfO₂ oxide layer at SC-junction which reduces the barrier width for charge carrier and result in increase tunneling probability at the junction. In general, TGF gets decreases with increases in V_{gs} but DMG SC-TFET shows significant behavior for the lower value of V_{gs} due to high value of V_{th} .

$$TGF = \frac{g_m}{I_d} \quad (5)$$

3.3.6 Transconductance Frequency Product (TFP)

TFP is another most crucial parameter that determines device performance at the operating frequency. It shows the relationship between power and bandwidth for high-speed device applications. For better device performance

it must be high as possible. Expression for TFP is given by equation 6 which shows direct relationship with f_T [29]. The impact of ITCs on TFP with applied V_{gs} is illustrated in Fig. 10. It is clearly noticed that TFP of the proposed device is higher than DMG SC-TFET and it increases with increases value of V_{gs} . And once it attain maximum peak it starts to decreases due to degraded mobility of charge carrier at high V_{gs} . Moreover, due to impact positive (negative) ITCs it attains a higher (lower) peak similar to f_T .

$$TFP = \frac{g_m f_T}{I_d} \quad (6)$$

3.3.7 Transit Time (τ)

It is the most important parameter for examining the device speed to evaluate circuit performance. For high-

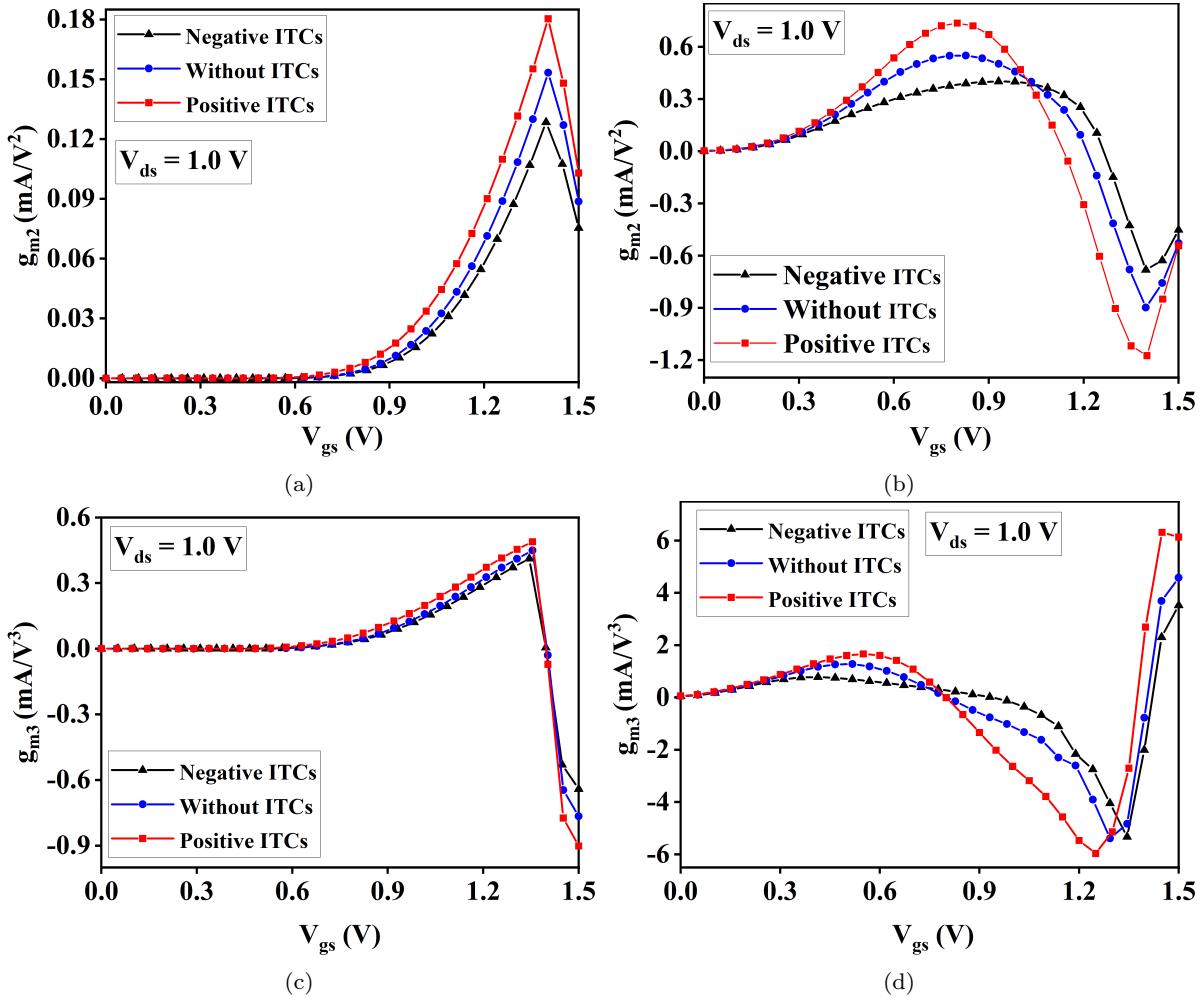


Fig. 12: Impact of ITCs on (a) g_{m2} of DMG SC-TEFT (b) g_{m2} of HD DMG SC-TEFT (c) g_{m3} of DMG SC-TEFT (d) g_{m3} of HD DMG SC-TEFT

speed performance we require less τ for less delay in performance speed. Expression for τ is given by equation 7 which shows inverse relationship with f_t [30]. The impact of ITCs on τ is illustrated in Fig. 11 where it noticed the proposed device shows lesser τ as compared to DMG SC-TFET due to higher value of f_t . Moreover, due to positive (negative) ITCs it gets decreases (increases) and HD DMG SC-TFET shows the negligible effect of ITCs due to presence of HfO_2 oxide layer at SC-junction which increases the flow of charge carrier due to proper gate coupling at the junction. This makes a very promising TFET for low power high-frequency devices.

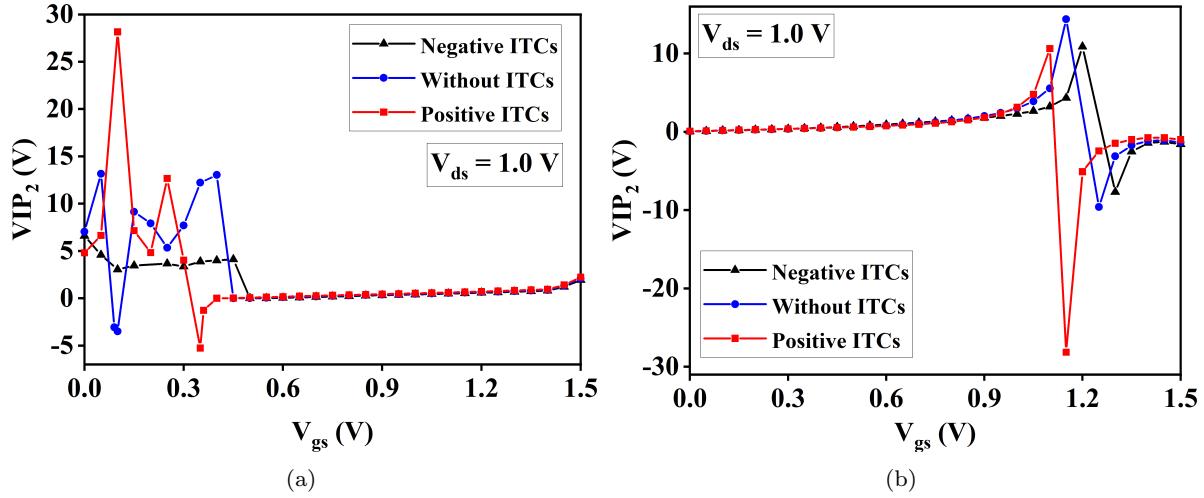
$$\tau = \frac{1}{2\pi f_T} \quad (7)$$

3.4 Linearity Analysis

In this scenario, along with high-speed wireless communication systems needs a device that has less noise and high signal to noise ratio to attains maximum linearity performance with reduces power consumption. Higher linearity performance means low distortion at the output with applied V_{gs} . If the linearity performance is not maintained by the system then non-linearity behavior induced noise/distortion at the output. And it is seen in many studies that ITCs widely influence the linearity performance of the TFET. So, it is important to assessment the impact of ITCs on the linearity parameters of the devices.

3.4.1 Higher Order Transconducance

Non-linearity behavior of device examine from higher order transconducance that are 2nd order and 3rd or-

Fig. 13: Impact of ITCs on VIP₂ (a) DMG SC-TEFT (b) HD DMG SC-TEFT

der derivative of I_d with respect to V_{gs} i.e., g_{m2} and g_{m3} which are given by equation 8 and 9 respectively [31]. For better linearity performance they must have low peaks with applied V_{gs} . The impact of ITCs on higher-order transconductance is illustrated in Fig 12 and it observed the proposed device shows lower peaks. Due to positive ITCs zero crossover frequency moves toward higher peaks that implies higher V_{gs} is required to maintain linear behavior of the device. The degradation of the linearity parameter for positive ITCs is due to enhancement in SCE characteristics of device which increases with positive ITCs. Moreover, due to negative ITCs zero crossover frequency shifts downward that increase the device performance.

$$g_{m2} = \frac{\partial^2 I_d}{\partial^2 V_{gs}} \quad (8)$$

$$g_{m3} = \frac{\partial^3 I_d}{\partial^3 V_{gs}} \quad (9)$$

3.4.2 Second Order Voltage Intercept Point (VIP₂)

VIP₂ examine mathematically input voltage (i.e. V_{gs}) at which first and second order harmonic voltages become equal. Expression for VIP₂ is given by equation 10 [32]. For better performance peaks of VIP₂ must be high. Fig. 13 manifests the impact of ITCs on VIP₂ and it noticed the proposed device shows high peaks in comparison to DMG SC-TFET. This is due to HfO₂ oxide layer at the SC-junction that's allow higher tunneling phenomena at the junction. However due to positive (negative) trap charges VIP₂ of HD DMG SC-TFET achieves a higher peak earlier (later) as compared to

without ITCs. And DMG SC-TFET shows some random peaks at low V_{gs} due to high V_{th} .

$$VIP_2 = 4 \left(\frac{g_m}{g_{m2}} \right) \quad (10)$$

3.4.3 Third Order Voltage Intercept Point (VIP₃)

VIP₃ examine mathematically input voltage (i.e. V_{gs}) at which first and third order harmonic voltages become equal. Similarly to VIP₂ peaks of VIP₃ needs to high for distortion-less output. Expression for VIP₃ is given by equation 11 [32]. The impact of ITCs on VIP₃ is illustrated in Fig. 14 and it is noticed the proposed device have high peaks in comparison to DMG SC-TFET. And DMG SC-TFET shows random peaks at low applied V_{gs} . Moreover, due to positive ITCs proposed device shows the maximum peak which is clearly shown in plots. Also, due to negative ITCs it shows a higher peak as compared to without interface trap charges. Hence, due to the impact of trap charges device performance gets improved.

$$VIP_3 = \sqrt{24 \left(\frac{g_m}{g_{m3}} \right)} \quad (11)$$

3.4.4 Third Order Input Intercept Point (IIP₃)

IIP₃ examine mathematically input power at which first and second order harmonic powers become equal. Expression for IIP₃ is given by equation 12 [32]. For reliable communication IIP₃ peaks should be high as possible. Fig. 15 illustrated the ITCs impact on IIP₃ with applied V_{gs} and it observed the proposed device shows higher peaks at low applied V_{gs} in comparison to DMG

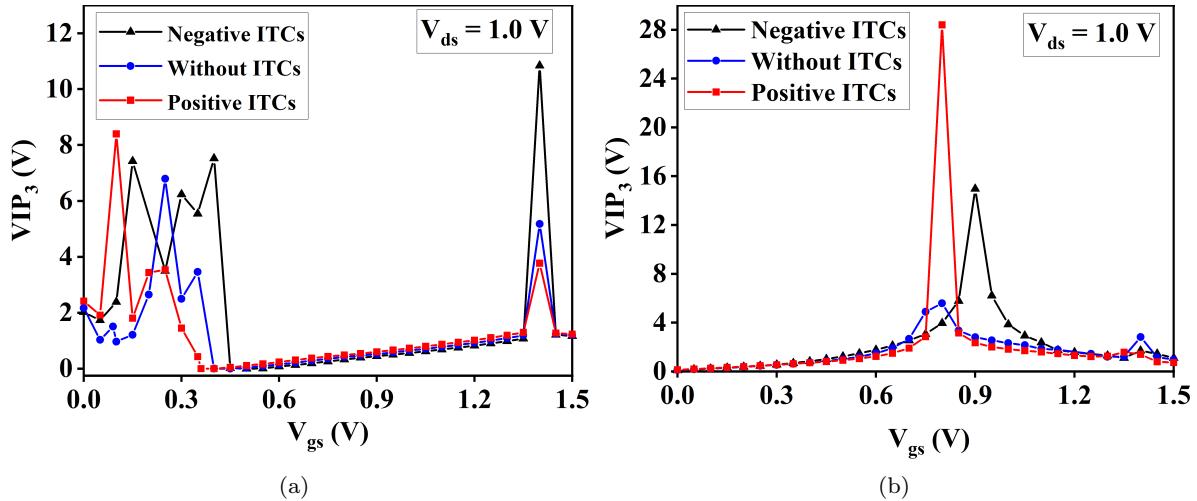


Fig. 14: Impact of ITCs on VIP_3 (a) DMG SC-TEFT (b) HD DMG SC-TEFT

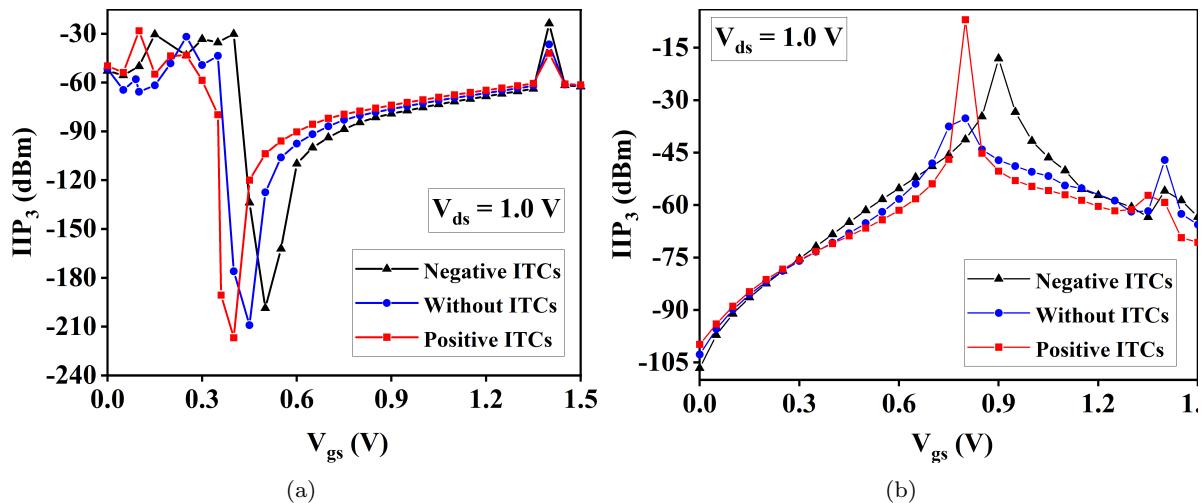


Fig. 15: Impact of ITCs on IIP_3 (a) DMG SC-TEFT (b) HD DMG SC-TEFT

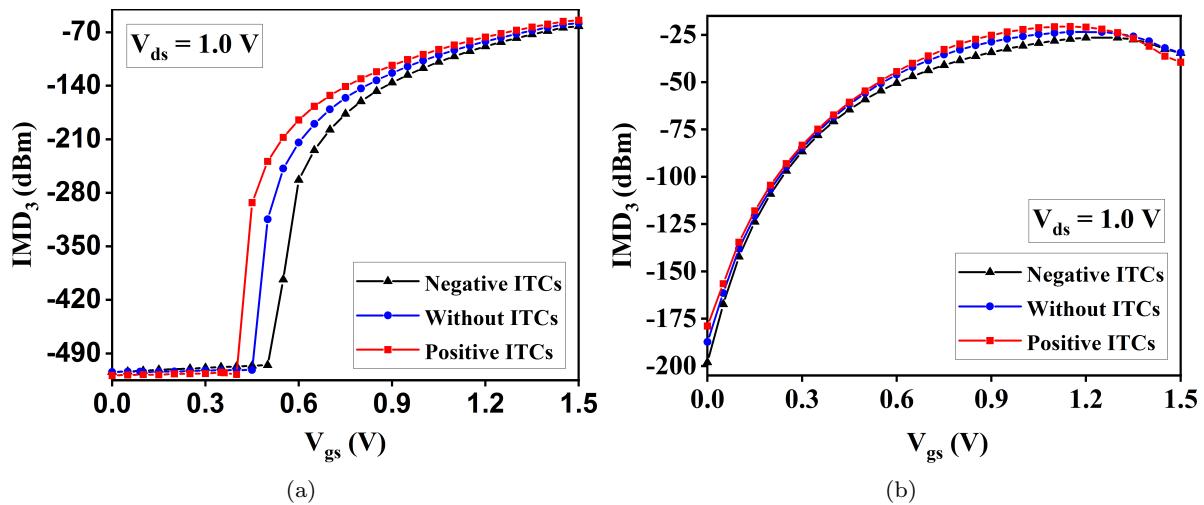


Fig. 16: Impact of ITCs on IMD_3 (a) DMG SC-TEFT (b) HD DMG SC-TEFT

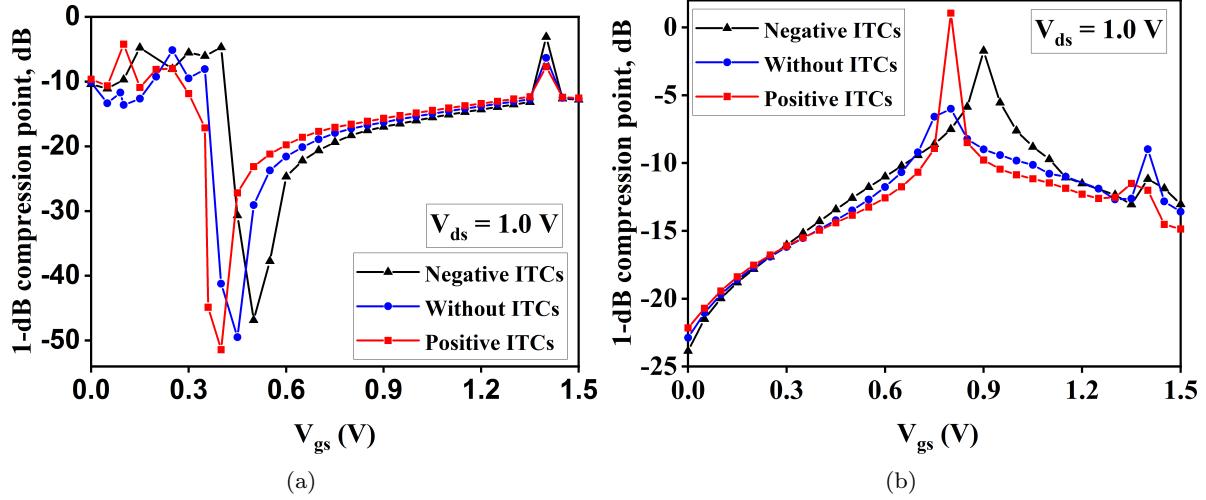


Fig. 17: Impact of ITCs on 1dB compression point (a) DMG SC-TEFT (b) HD DMG SC-TEFT

SC-TFET due to HfO₂ oxide layer at SC-junction which increases tunneling of charge carrier. It is further noticed, due to the impact of ITCs peaks of IIP₃ increases because of increased tunneling phenomena at the junction and DMG SC-TFET shows some random peaks at low V_{gs} due to high V_{th}.

$$IIP_3 = \frac{2}{3} \left(\frac{g_m}{g_{m3} R_s} \right) \quad (12)$$

where, R_s=50 Ω for RF/analog application

3.4.5 Third Order Intermodulation Distortion (IMD₃)

IMD₃ generally determines intermodulation distortion which occurs due to the non-linearity response of the device. Expression for IMD₃ is given by equation 13 [32]. For distortion-less communication IMD₃ values should be low with applied V_{gs}. The impact of ITCs on IMD₃ is portrayed in Fig. 16 where it is noticed that proposed TFET shows higher value as compared to DMG SC-TFET. Also, due to positive (negative) ITCs it increases (decreases) and the proposed device shows the almost negligible impact of ITCs. Moreover it also observed, at low V_{gs} the value of IIP₃ is higher as compared to IMD₃ which ensures that proposed device has superior linearity behavior with low distortion at applied V_{gs} that makes a very promising device for the reliable communication system.

$$IMD_3 = \left[\frac{9}{2} (VIP_3)^2 g_{m3} \right]^2 R_s \quad (13)$$

3.4.6 1dB Compression Point

It is another most significant parameter to determine the linearity performance of the device. It defines input

power level at which causes output power level shifts linearly from 1dB which is given by equation 14 [32]. It used to determine maximum input power after which the gain of the device degraded. Fig 17 manifests the impact of trap charges on 1dB compression point, revealing higher peak of proposed device in comparison to DMG SC-TFET. Moreover, due to positive and negative ITCs there are increases in 1dB compression point that result in upgrade linearity performance. And DMG SC-TFET shows some random peaks at low applied V_{gs} due to high V_{th} of the device.

$$1dB \text{ compression point} = 0.22 \sqrt{\frac{g_m}{g_{m3}}} \quad (14)$$

4 Conclusion

This research work present a novel TFET to overcome the shortcomings of conventional TFET. The proposed device employed combines benefits of both heterogeneous dielectric material and gate engineering which result in low V_{th}, high I_{on} in the order 10⁻⁴ with 3.09 mV/decade subthreshold swing. In addition to it I_{on}/I_{off} ratio in the order of 10¹¹. This makes a very promising device for digital circuit applications. Generally, trap charges are induced at the interface of the semiconductor/oxide layer during the fabrication process and these ITCs degrades the device performance. So, to assessment of the impact of positive and negative ITCs a comparative investigation is done between DMG SC-TFET and proposed device. This study shows that HD DMG SC-TFET has higher C_{gd} which is due to HfO₂ material at SC-junction. But, at the same times it shows large increment in g_m that enhance the current capability of the device which shows very significant improvement

in all other analog/RF parameters such as f_T , GBP, TGF, TFP, f_{max} and τ . Due to the impact of positive (negative) ITCs proposed TFET shows enhance (de-grade) device performance and also exhibit better immunity towards trap charges in comparison to DMG SC-TFET. Since the linearity behavior of the device plays a very crucial role for distortion-less and noise-free wireless communications. Therefore, impact of trap charges on linearity parameters is also examine and it observed proposed device has better response in comparison to DMG SC-TFET that makes very promising device for advance communication system. These results prove that our proposed TFET is suitable for low power high-frequency electronic devices.

Declarations

The manuscript follows all the ethical standards, including plagiarism.

– **Funding statement :** Not applicable.

– **Conflict of interest :** No conflicts of interest.

– **Authors contributions :**

- Sachin Kumar: Conceptualization, data curation, formal analysis, methodology, investigation, writing – original draft.
- Dharmendra Singh Yadav: Supervision, validation, visualization, writing – review & editing

– **Availability of Data and Material :** The data and material concerned to the manuscript may be made available on request.

– **Consent for Publication :** Yes.

– **Consent to Participate :** Yes.

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Figures

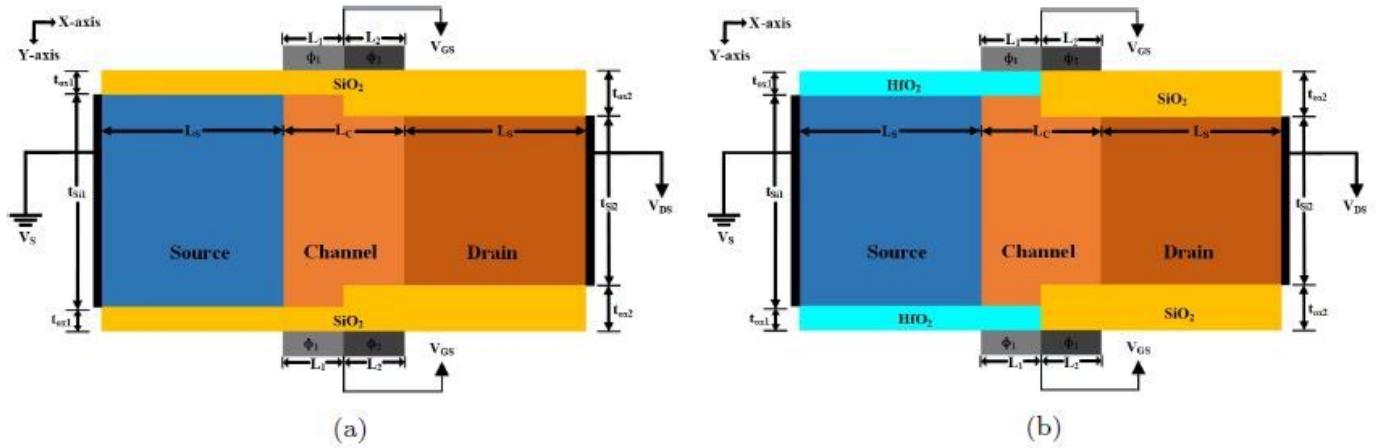


Figure 1

Device Schematic view of (a) DMG SC-TEFT (b) HD DMG SC-TEFT

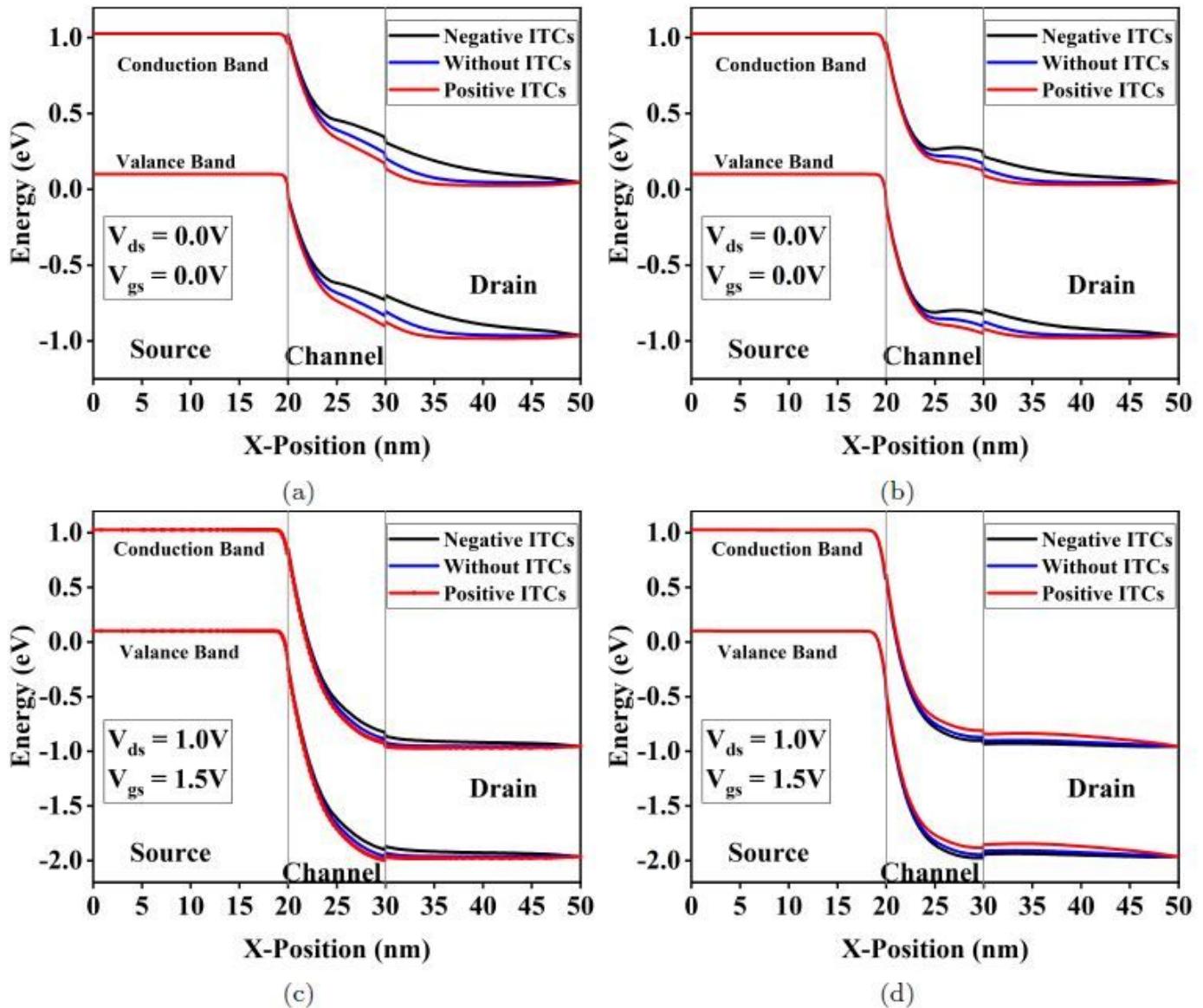


Figure 2

Impact of ITC on (a) Energy Band of DMG SC-TFET under Thermal Equilibrium (b) Energy Band of HD DMG SC-TFET under Thermal Equilibrium (c) Energy Band of DMG SC-TFET under ON-State (d) Energy Band of HD DMG SC-TFET under ON-State

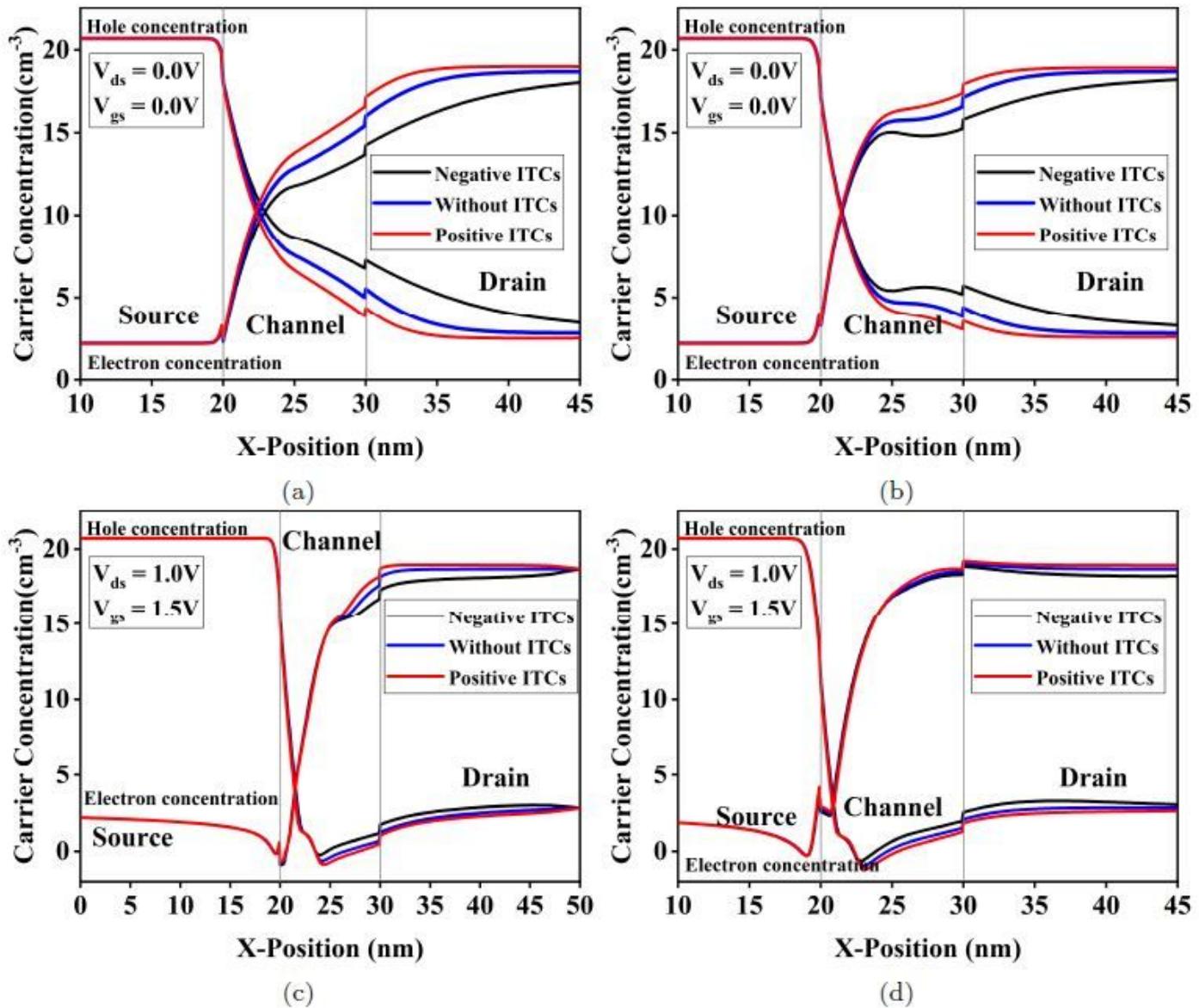


Figure 3

Impact of ITC on (a) Carrier Concentration of DMG SC-TFET under Thermal Equilibrium (b) Carrier Concentration of HD DMG SC-TFET under Thermal Equilibrium (c) Carrier Concentration of DMG SC-TFET under ON-State (d) Carrier Concentration of HD DMG SC-TFET under ON-State

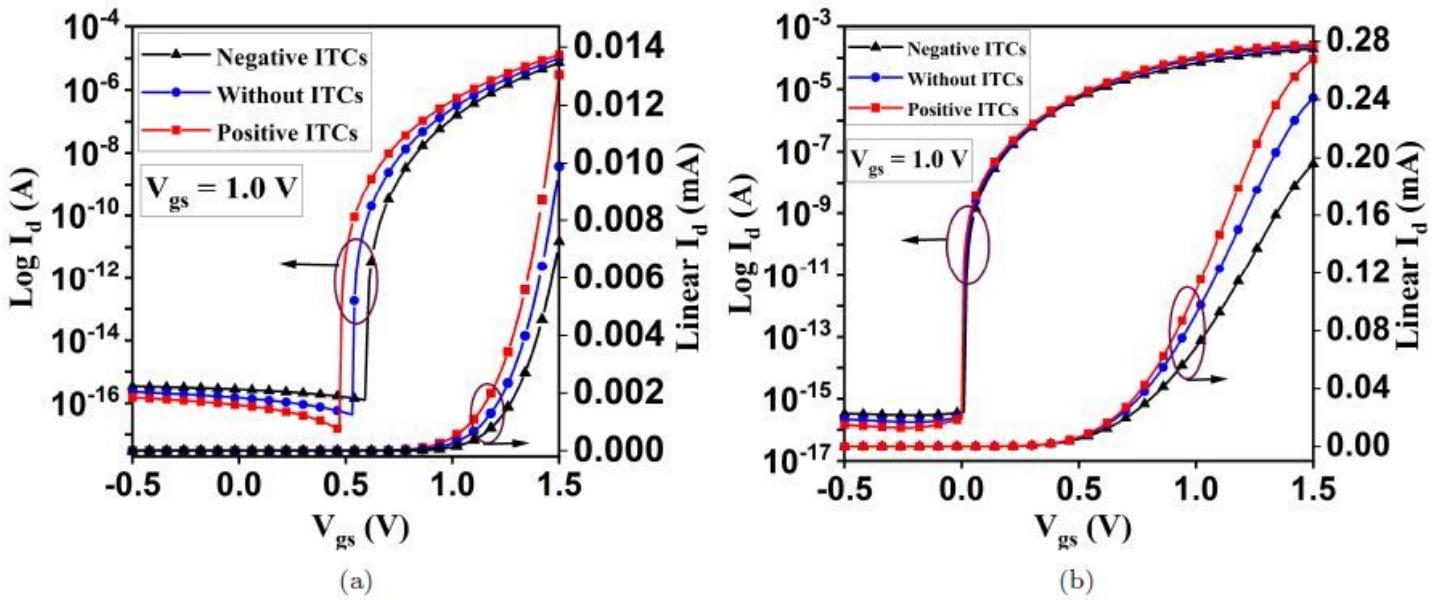


Figure 4

Impact of ITCs on transfer characteristics (a) DMG SC-TEFT (b) HD DMG SC-TEFT

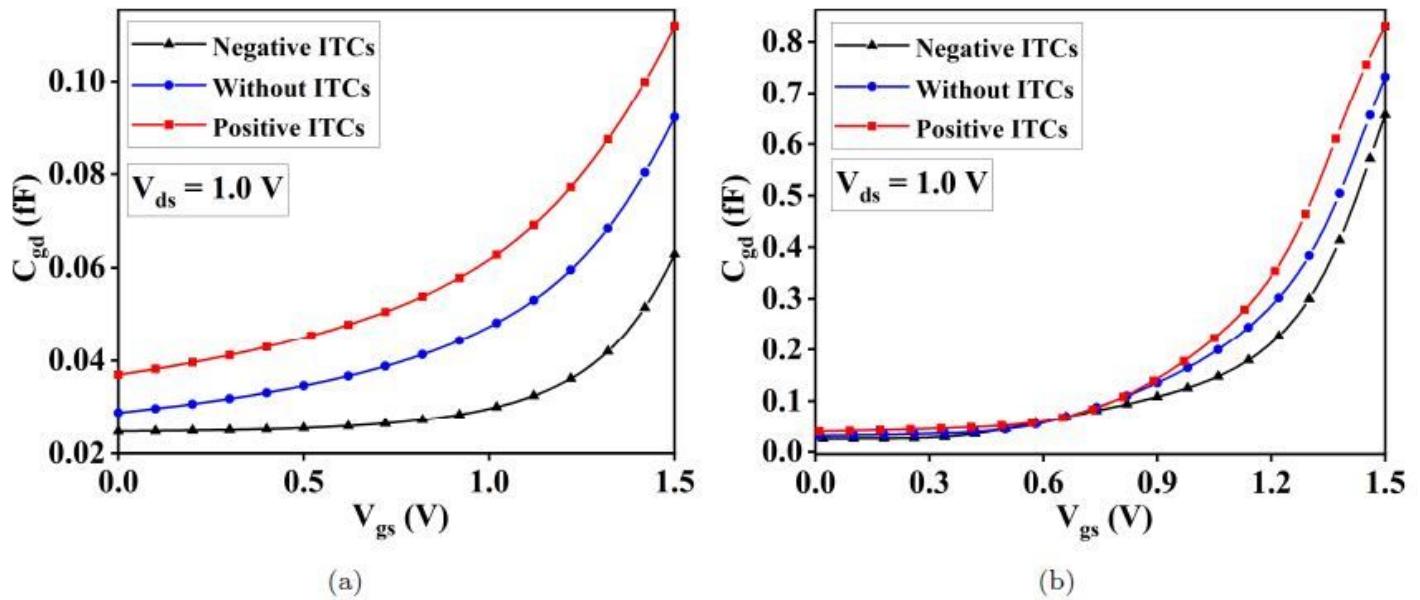


Figure 5

Impact of ITCs on C_{gd} (a) DMG SC-TEFT (b) HD DMG SC-TEFT

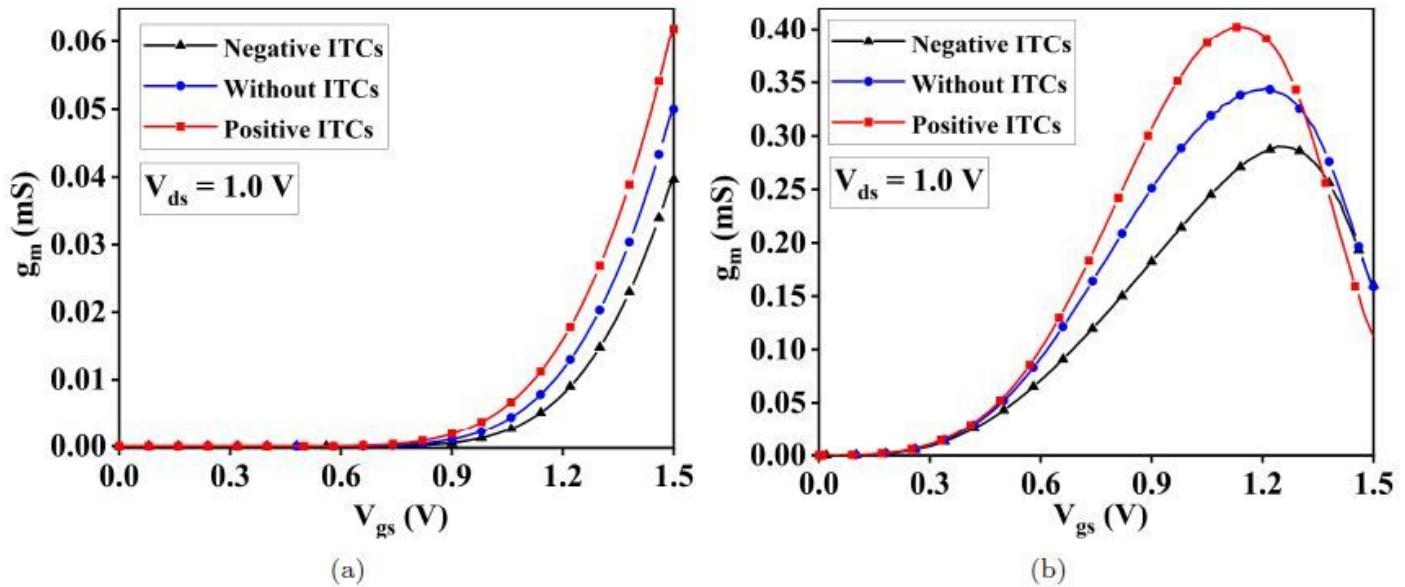


Figure 6

Impact of ITCs on g_m (a) DMG SC-TEFT (b) HD DMG SC-TEFT

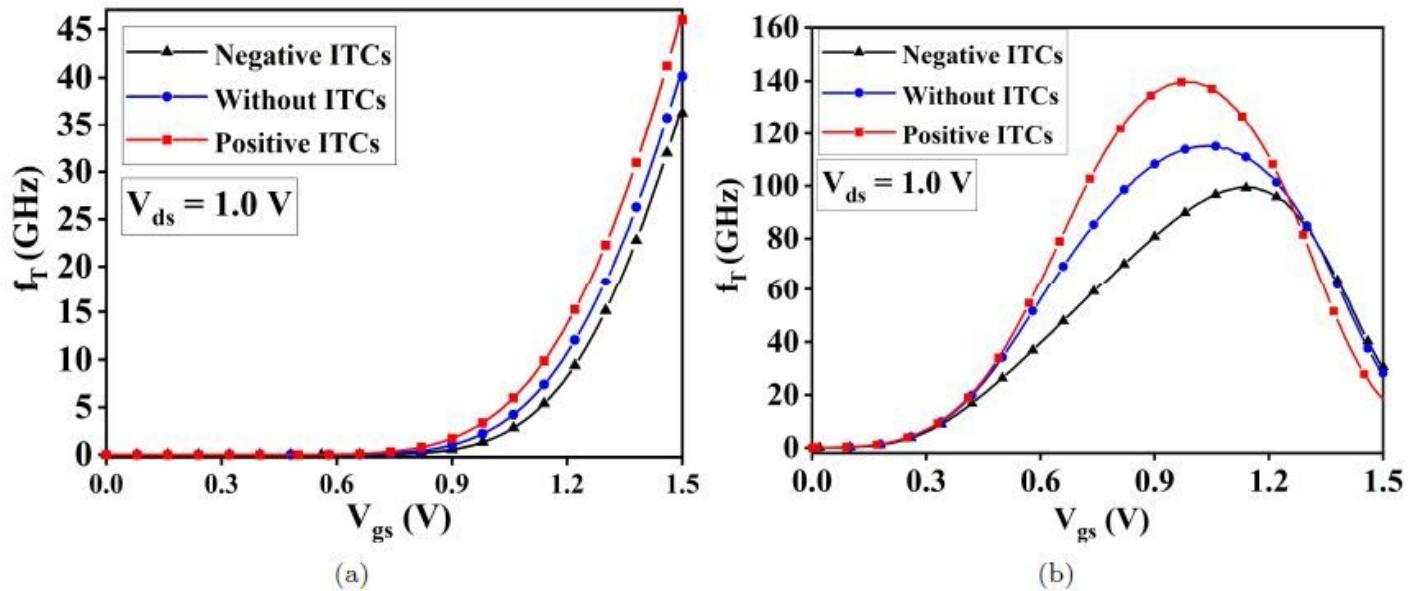


Figure 7

Impact of ITCs on f_T (a) DMG SC-TEFT (b) HD DMG SC-TEFT

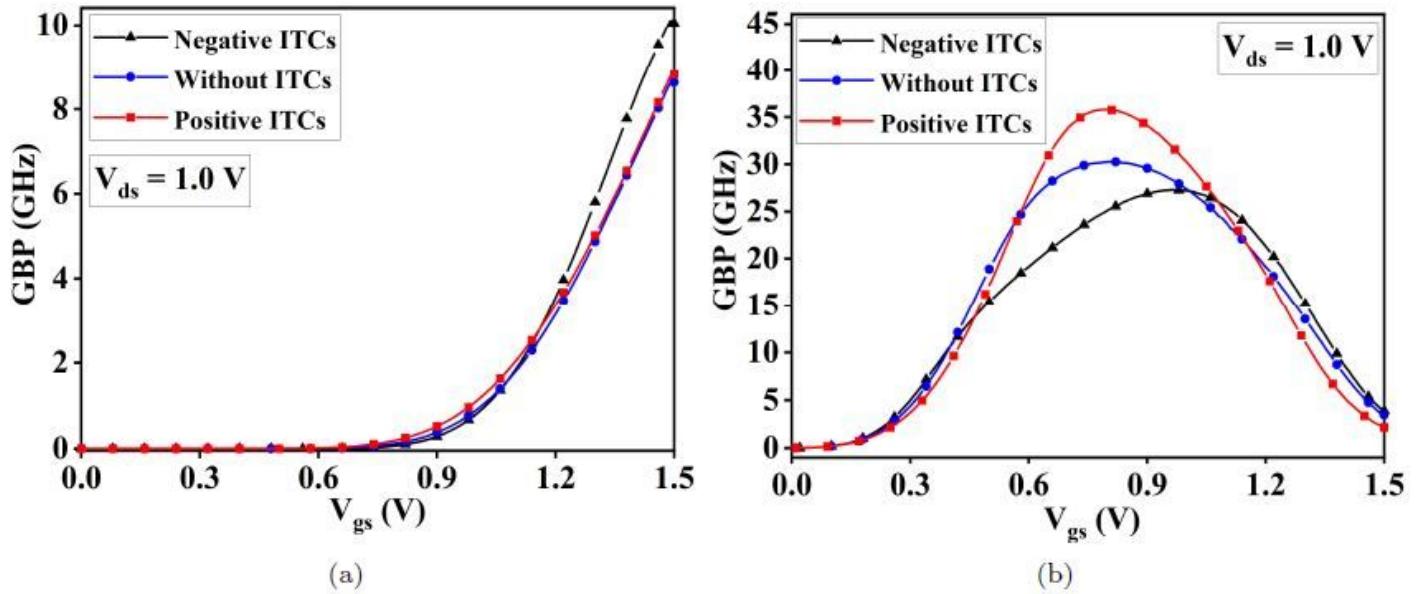


Figure 8

Impact of ITCs on GBP (a) DMG SC-TEFT (b) HD DMG SC-TEFT

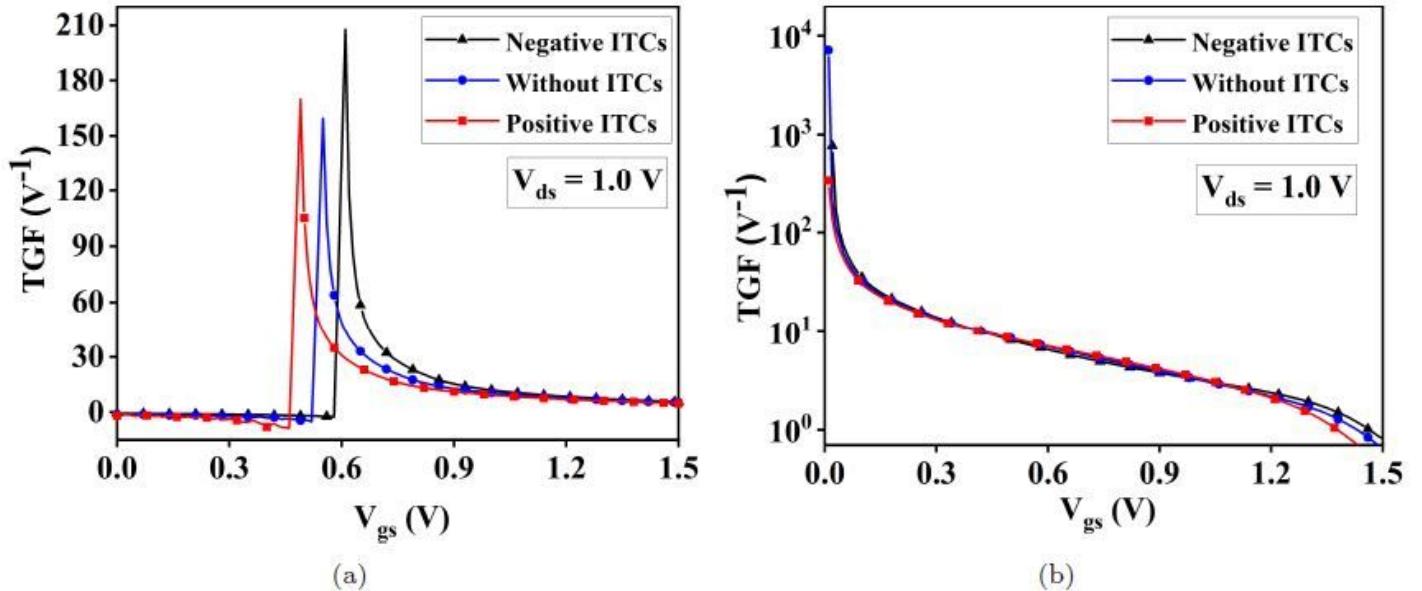


Figure 9

Impact of ITCs on TGF (a) DMG SC-TEFT (b) HD DMG SC-TEFT

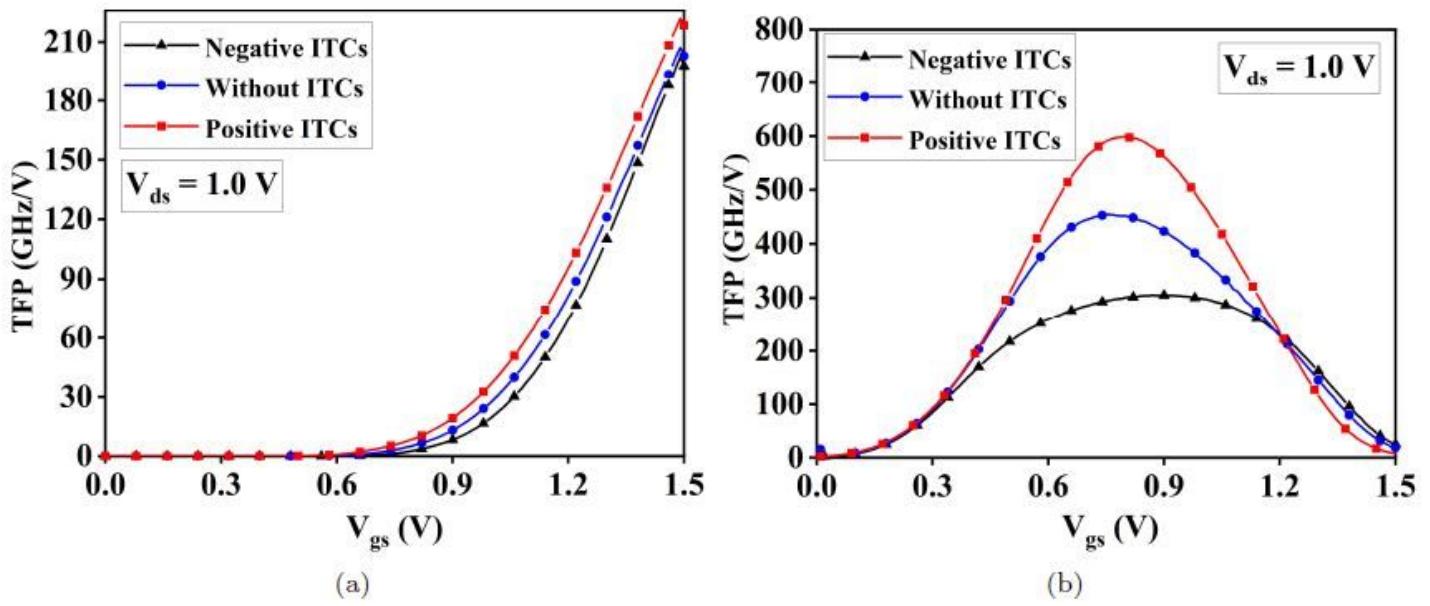


Figure 10

Impact of ITCs on TFP (a) DMG SC-TEFT (b) HD DMG SC-TEFT

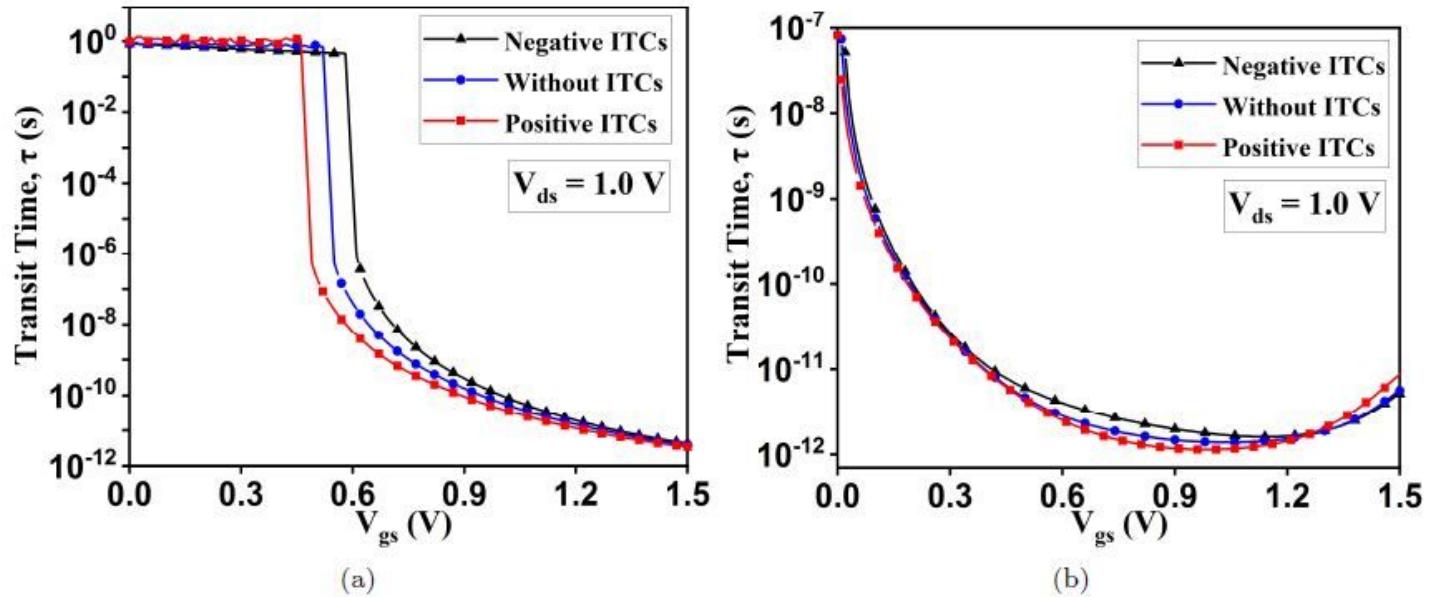


Figure 11

please see the manuscript file for the full caption

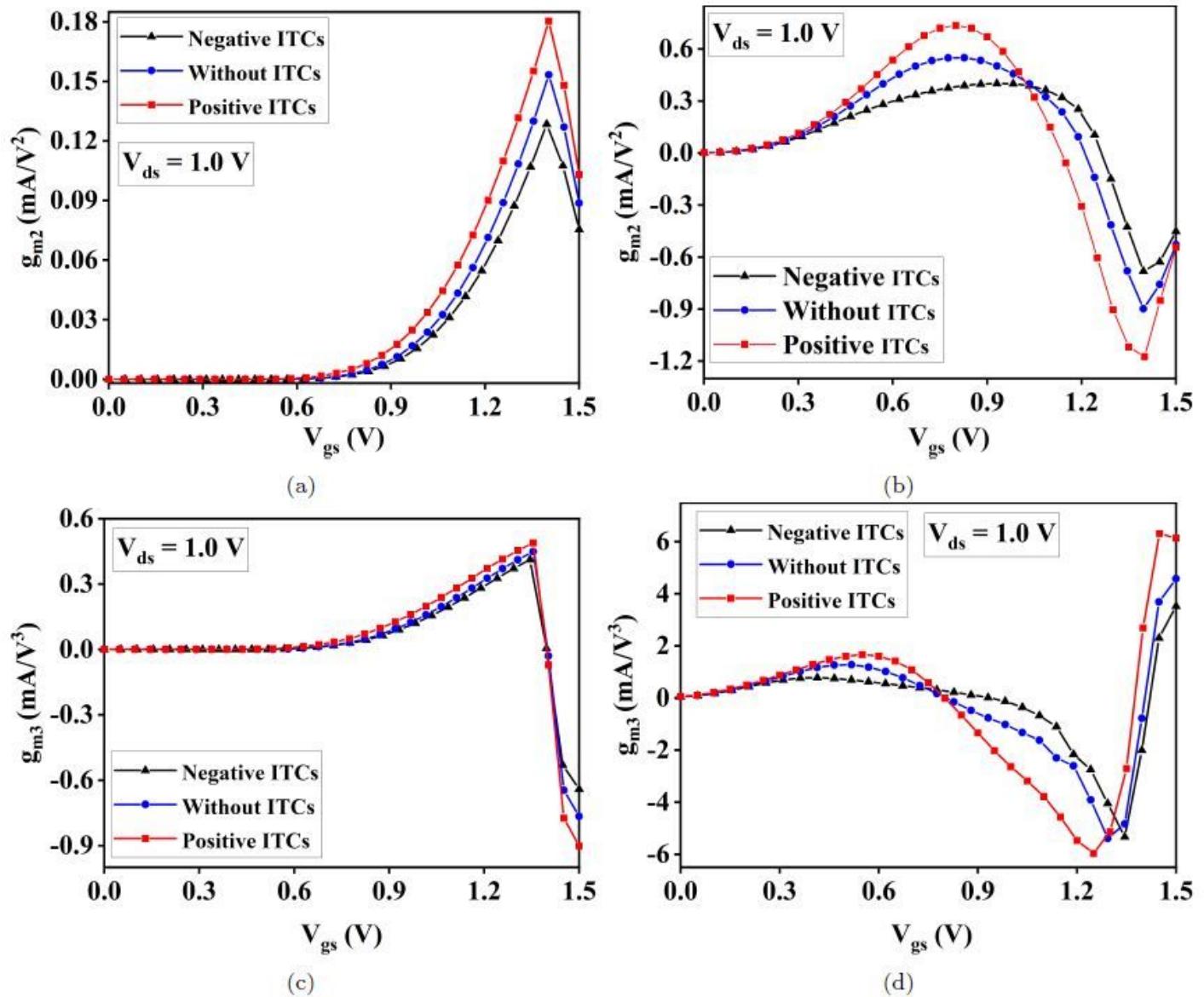


Figure 12

Impact of ITCs on (a) g_{m2} of DMG SC-TEFT (b) g_{m2} of HD DMG SC-TEFT (c) g_{m3} of DMG SC-TEFT (d) g_{m3} of HD DMG SC-TEFT

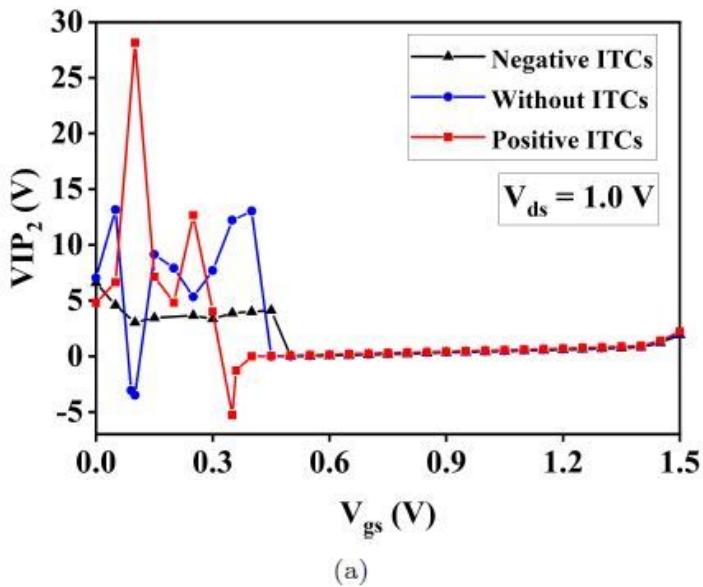


Figure 13

Impact of ITCs on VIP2 (a) DMG SC-TEFT (b) HD DMG SC-TEFT

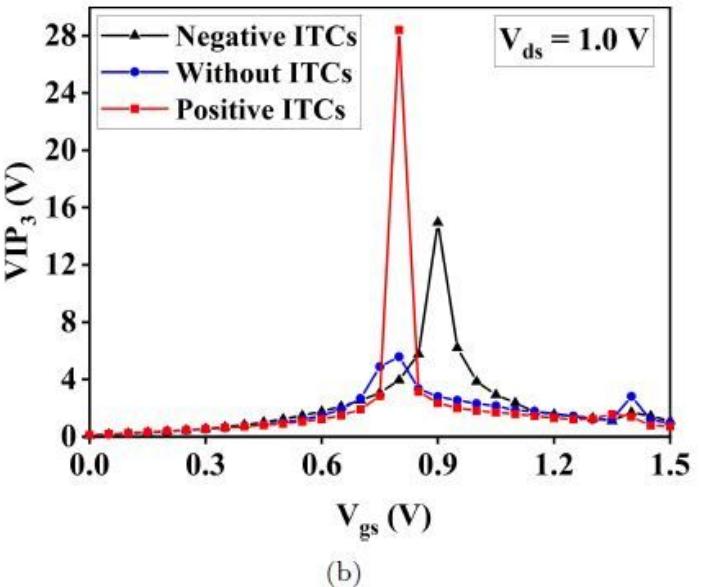
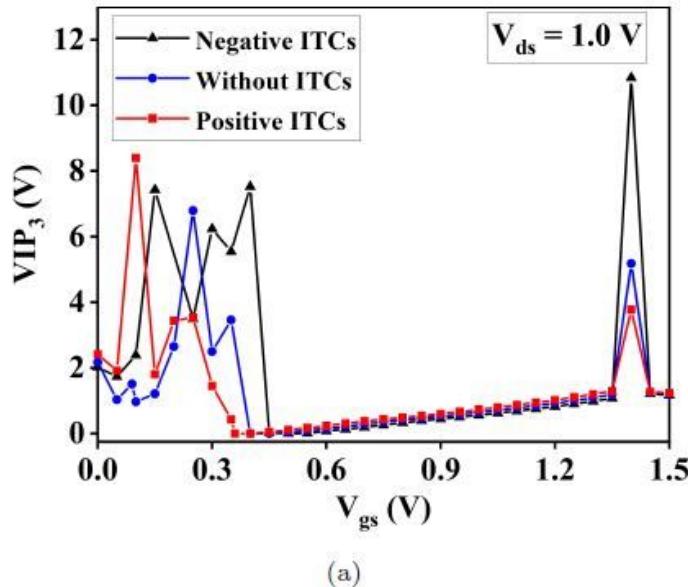


Figure 14

Impact of ITCs on VIP3 (a) DMG SC-TEFT (b) HD DMG SC-TEFT

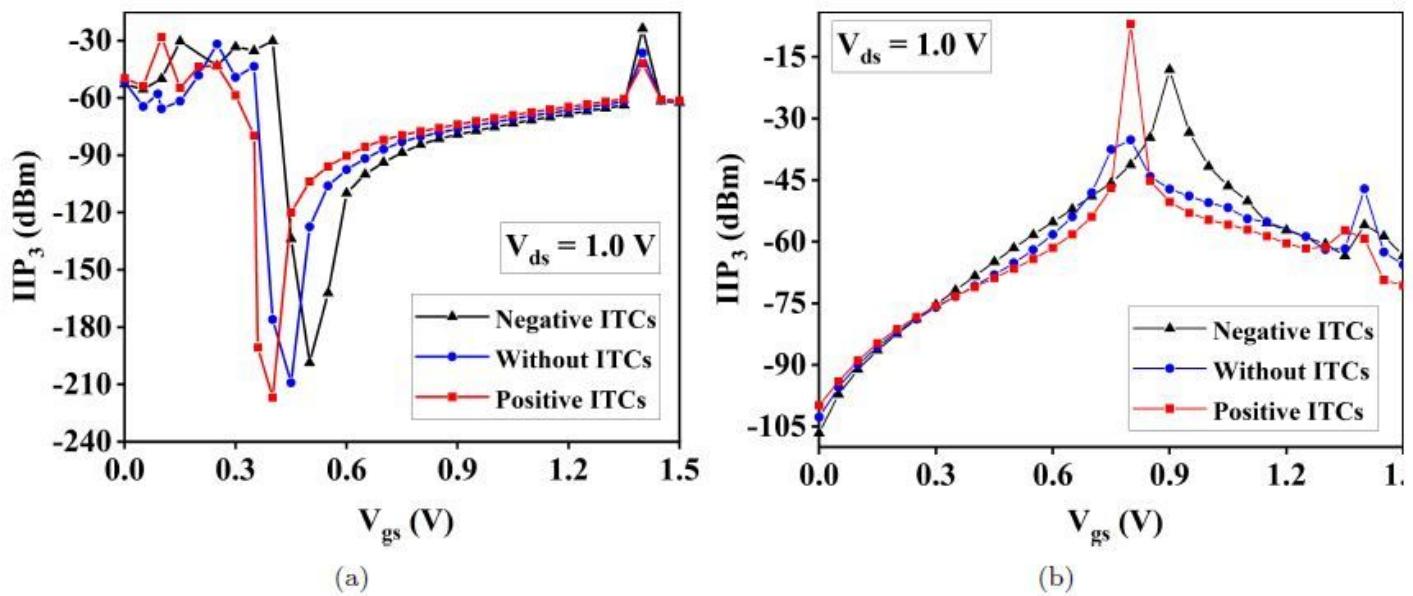


Figure 15

Impact of ITCs on IIP₃ (a) DMG SC-TEFT (b) HD DMG SC-TEFT

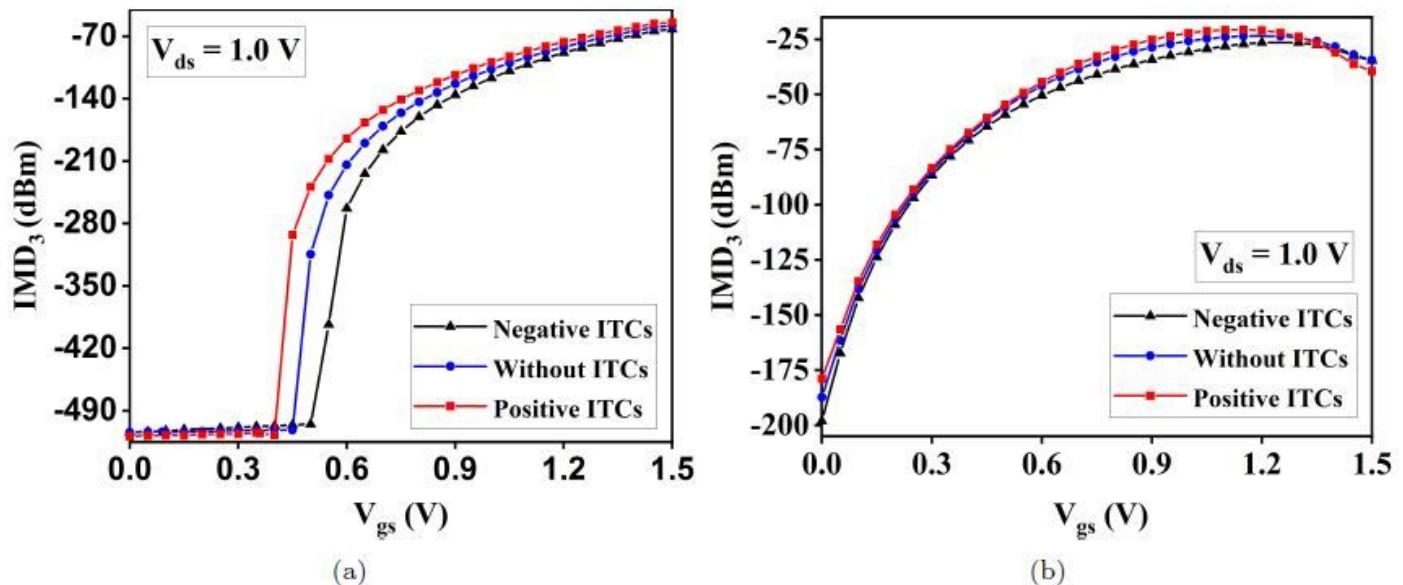


Figure 16

Impact of ITCs on IMD₃ (a) DMG SC-TEFT (b) HD DMG SC-TEFT

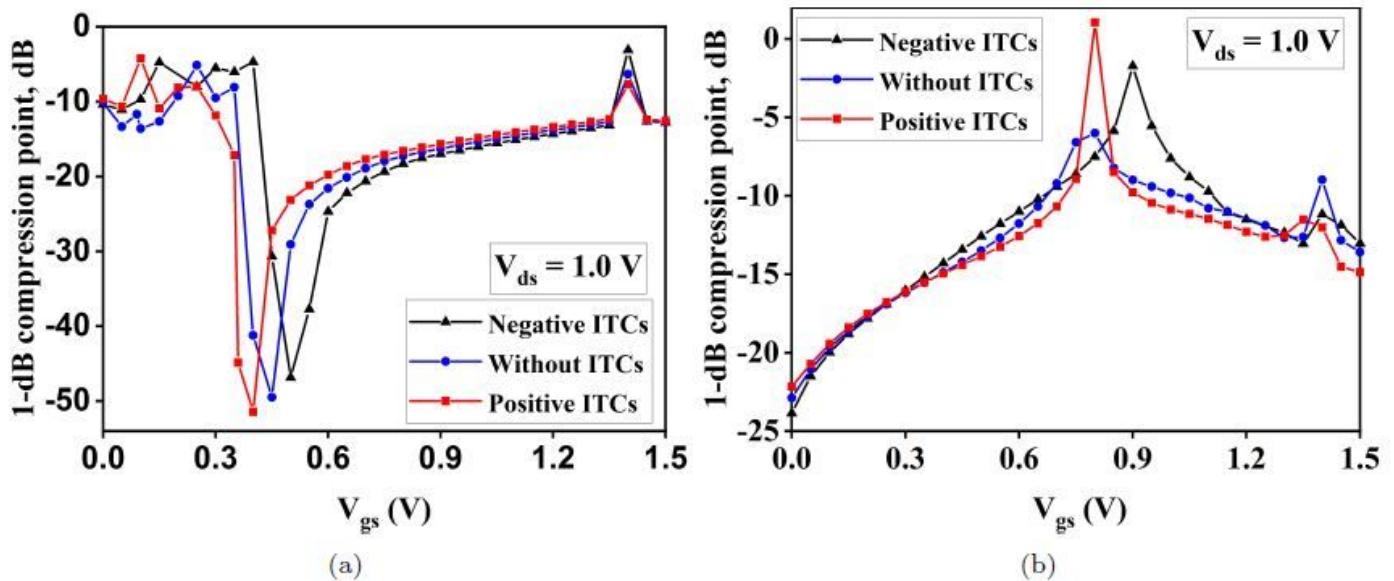


Figure 17

Impact of ITCs on 1dB compression point (a) DMG SC-TEFT (b) HD DMG SC-TEFT