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Design and Introduction of Thermal Collection Network (TCN) for the Thermal Management in 3-D IC Structures

Chandrashekhar V. Patil, *Ph.D. Scholar, B.M.S. College of Engineering*, and Dr. Suma M. S, Professor, *B.M.S. College of Engineering, Bangalore, India.*

Abstract - Power in Watts of the chip, per unit area is growing exponentially in the electronic industry. At the same time, thermal problems becoming side effects of huge power consumption. Continuous efforts are getting made to remove the thermal problems of electronic packaging and systems. Thermal problems if not alleviated or suppressed, will lead the dielectric breakdown, electromigration, material creep, thermal cycling, chemical reactions, board warpage, performance drift, indirect heating, and many more problems. Likewise, a dedicated Power Delivery/distribution Network (PDN), can deliver the power to the chip base, this paper has introduced a new methodology of a dedicated Thermal Collection Network (TCN) in the same Back End Of Line (BEOL) area of the System in Package (SiP), System on Chip (SOC) and any other power-consuming chips. Adding a Thermal Through Silicon Via (TTSV) is another advantage in it. Using such an apparatus or methodology connected to TTSV will quickly pump-up the thermal energy to the heat-sink-fan assembly. Hence, preempting of heat from its sources can manage the thermal problems inside the chips or 3-D IC structures. The methodology uses the same copper metal stripes inside the Inter-Layer/Level-Dielectric (ILD), which will not lead to any extra copper to introduce more Coefficient of Thermal Efficiency (CTE) mismatch problems. It would be considered as one among the other metal stripes. The experimental results using the Finite Element Method (FEM) tool shown that 32% heat suction occurs in the TCNs, in monolithic ICs, and 11% in 3-D IC structures, compared to without such an approach. The junction temperature remained at 35%, with and without such an approach, in 3-D IC structures. This might lead to a new methodology for designing electronic chips and 3-D IC structures, in the future.

Keywords— *Coefficient of thermal efficiency, Monolithic 3-D IC, Thermal collection network, Thermal resistance.*

I. INTRODUCTION

WHILE designing a chip, a typical power grid, and power switches (especially the count and distribution) are designed to meet the static IR ($I \cdot R = \text{Current} \cdot \text{Resistance}$) drop targets and not for dynamic IR drop of the chip. The robust design of the power grid is never met, even using with the usage of module-based De-Coupling Capacitor (DCAP/decap) cells and the module-based power switches, some of the other techniques need to be employed to overcome this problem. Based on the switching activity of logic for a particular period, the dynamic current is hugely drawn, by these localized logic areas. Therefore, a localized hot spot will appear. These hotspots would be presently fixed with decap cells, with a set

value, constrained in a particular percentage of targeted voltages. Hence, these are major candidates of the thermal energy accumulators. Such hotspots lead to accumulating thermal energy. Finally transfer it to wires and substrates of the chip, leading to indirect heating of other logic and other components of the chip. On the advanced nodes, the IR drop improvement targeted with decap cells going to be very minimal.

Shiv Govind Singh and Chuan Seng Tan [1], have shown a reduction of 54°C - 62°C in the maximum temperature of the chip, using TTSV inside 3 stacked assemblies. Nithin S K, *et al.* [2], discussed various techniques in reducing the dynamic voltage drop practiced in the industry. Especially, haloing of clock tree cells and padding decaps next to these cells. This will help in reducing the voltage drop in clock tree cells due to high switching. Another technique discussed is, power/ground metal fill. These inserted metal floating straps can also be connected to power or ground, which might be called augmentation. By doing this, the power and ground grid becomes stronger. Hence, would help in reducing the dynamic voltage drop. John H. Lau, and Tang Gong Yue [3], used Computational Fluid Dynamics (CFD) tools and different experiments show that a reduction in chip temperatures using TSVs, and also shown an increase in junction temperatures if a greater number of TSVs were used in 3-D stacked systems. Ayed Al Qahtani *et al.* [4], taken a case study of an industry-standard design and did a hotspot validation and thermal analysis. This has helped to make the presented proposal, on how to design TCNs. Jingrui Chai, *et al.* [5], studied an effective approach of thermal performance in a stacked IC system. Also studied the thermal conductivity in comparison with various publications. Yann Civalé, *et al.* [6], Sergii Osmolovskyi, and Jens Lienig Dresden [7], discussed various packaging schemes available in 3-D IC structures. Wherein they have shown Wafer Level Packaging (WLP) and physical design challenges in 3-D IC packages using TSVs. The study shows, the direction of Electronic Design Automation (EDA) tools that need to help in designing such packages. This gives an idea of how to look towards physical design aspects while designing proposed TCNs. Shabaz Basheer Patel, *et al.* [8], studied the Von Mises stress generated on such TTSV, which can be reduced by 40mpa, using carbon nanotube insertion inside the filler material. Hence making the chip more reliable. Pramod Kaddi, *et al.* [9], proposed an active cooling technique with a Peltier element, inside the TTSV, which could be the better solution for heat removal in 3-D ICs compared to

passive techniques used so far. Aditya Agrawal, *et al.* [10], take a complete case study on the Xylem chip by the placing of TTSVs and analyzed temperatures inside the stack. Zongqing Ren *et al.* [11], considered the different case studies with multiple memory chips. They have shown that, the most optimized stack in reducing the peak temperature was based on the TTSV and power-consuming areas of the die.

With presently available literature reviews, disadvantageously or unfortunately others have not attempted in the direction of making thermal runaway paths for the heat absorption quickly and efficiently, inside a chip or in 3-D IC structures in a more efficient way. The present paper proposes such methodology and device to make thermal management, by careful study of root cause and area of heat sources of the chips. The present paper also coined the word ‘‘Thermal Collection Network’’ (TCN).

Following section II will be discussing designing the widths of TCN. Section III explains the experimental setup. Section IV focuses on the results and discussion. Especially thermal performance of the thermal collection network, parameters, with various results, observed using computations and FEM tool readings. Relevant conclusions and summary are drawn in section V.

Nomenclature:

Subscripts and Symbols

A_0 = Footprint of the experimental area (um^2)

$g(n)$ = Normalized conductivity of n^{th} metal layer (W/m.K)

∂_{IR} = IR drop budget (Volts)

V_{DD} = Power supply voltage to the chip (Volts)

V_{SS} = Ground supply voltage to the chip (Volts)

J_{EM} = Electromigration current limit of n^{th} metal layer (Amps)

I_{EM} = Minimum current drawn as per electromigration (Amps)

I_{chip} = Minimum current drawn by the chip (Amps)

W_{EM} = Width of the metal, calculated as per EM (um)

W_{IR} = Width of the metal, calculated as per IR drop (um)

R_T = Thermal resistance (Ohm)

F_H = Heat flow/flux (W/m^2)

ΔT = Temperature differences ($^\circ\text{C}$)

Q_{in} = Inflow positive heat flux (W/m^2)

Q_{out} = Outflow positive heat flux (W/m^2)

P = Pitch of TSV cell (um)

T = Thickness/height of the TSV cell (um)

H_{cold} = Average temperature of hot surfaces ($^\circ\text{C}$)

H_{hot} = Average temperature of hot surfaces ($^\circ\text{C}$)

R_{therm} = Thermal resistance of the stack (Ohm)

H_{flow} = Generated heat of the stack (W/m^2)

T_{junct} = Junction temperature of the stacks ($^\circ\text{C}$)

T_{ambi} = Ambient temperature ($^\circ\text{C}$)

$k_{eqv,Z(chip)}$ = Thermal conductivity of chip in Z (W/m.K)

$k_{eqv,X/Y(chip)}$ = Thermal conductivity of chip in X/Y (W/m.K)

II. DESIGN AND THERMAL MODELS OF THE TCNS

Rishi Bhooshan [12], developed power models based on IR drop as well with the electromigration calculations. Herein a similar fashion calculating the width of the thermal collection

metal could be developed by sustaining currents, (by taking a resistance as the thermal representation) in each thermal budget. Here, via resistances taken negligible, and core ring concept is made. TCN can also be connected to the ground, intern TTSV could be connected to ground paths of current, to alleviate another capacitance of the metals.

$$W_{IR} = \frac{\min(I_{chip}, I_{EM}) L}{2 \partial_{IR} V_{DD} G \sum_{n=1}^{\infty} g(n)} \quad (1)$$

and,

$$W_{EM} = \max \left\{ \frac{\min(I_{chip}, I_{EM}) g(n)}{2 [\sum_{n=1}^{\infty} g(n)] J_{EM}(n)} \right\}, \forall_n \quad (2)$$

Here, n is the number of metal layers used in the core rings. Let $J_{EM}(n)$ be the Electromigration (EM) current density limit of the n^{th} metal layer. The minimum current of (I_{chip} or I_{EM}) carried to meet the IR drop budget ∂_{IR} .

As said above, TTSVs can also be electrically grounded to prevent charge accumulation. If TCNs are connected to power or ground supplies of the chip (augmentation), then need to consider the above equations (1)-(2). In such cases, whichever gives the bigger width values, that can be taken for actual widths of TCN rings. Budgeting the thermal energy in terms of resistance models and solving for widths of metals would be the scope of the project.

III. EXPERIMENTAL SETUP

The finite element method is a simulation technique that mathematically simulates fluid flow and heat transfer. Ansys® Workbench 2.0 software, 2020-R1, [13] uses partial differential equations to solve for quantitative and qualitative predictions on heat transfer flow and many other phenomena using FEM. The steady state-thermal analysis is done using this tool. Firstly, the process of simulations is, made by drawing geometries of the system. Secondly, material assignments are followed by constraining boundary conditions. The final step involved meshing, then computed/simulated. The geometries were drawn using Solid works®, 2020 [14]. This is a tool used to draw 2-D/3-D computer-aided designs (CAD).

Heng-Chieh Chien, *et al.* [15], did a thermal evaluation on the copper-filled TSV considering as a unit cell, with a thickness of ‘‘T’’ and a pitch ‘‘P’’. They derived the equivalent thermal conductivity of this TSV cell. The thermal conductivities to be calculated, include planes of k_{xy} (left to the right wall, i.e, horizontal thermal flow) and k_z (top to bottom, i.e vertical thermal flow) in the cross-section of the die or interposers. The positive heat flux Q_{in} is applied to one of its side surfaces (left wall). $-Q_{out}$ a negative flux is applied to its opposite side of the surface (right wall). Applying Fourier's law, the equivalent thermal conductivity in k_{xy} direction can be obtained as further, in equation (3).

$$Q_{in} = k_{xy} \left\{ \frac{H_{hot} - H_{cold}}{P} \right\} \quad (3)$$

Where, H_{hot} and H_{cold} are the average temperature of the left wall and right wall, respectively. P is the pitch of the TSV cell. Similarly, equivalent thermal conductivity in k_z direction of copper-filled TSV could be calculated further. H Considering heat flux entering on the top-side of TSV and exit at bottom-side of the TSV. Using Fourier's law, the equivalent thermal conductivity in k_z direction can be obtained as below in equation (4).

$$Q_{in} = k_z \left\{ \frac{H_{hot} - H_{cold}}{T} \right\} \quad (4)$$

Where, H_{hot} and H_{cold} are the average temperature of the top surface and bottom surfaces, respectively. T is the thickness of the TSV cell. Note that, thermal conduction along the vertical length of copper of TSV/TTSV is isothermal, where the conductivity of copper is uniform. Whereas horizontal flow of thermal energy is anisotropic as it hits many barriers like liner material and silicon substrates.

Weijun Zhu, *et al.* [16], studied with an example of a unit cell of a power distribution network. They studied effective thermal conductivity and temperature variations with different pitches of PDN and TSVs in a 3-D IC stack. The influence of TCN layers on heat conduction introduced the following equations (5) and (6),

$$\Delta T = F_H \cdot R_T \quad (5)$$

$$R_T = \frac{l}{kA} \quad (6)$$

Where ΔT , F_H , and R_T are temperature differences, heat flow, and thermal resistance, respectively. l , A , and k are the length of the object, cross-sectional area, and thermal conductivity of copper, respectively.

Weijun Zhu, *et al.* [16], also concluded important results that, as the number of PDN layers increases, thermal conduction of the ILD/BEOL in vertical direction deteriorates. But, thermal conduction in horizontal direction increases, due to change of cross-sectional areas of the PDN. Hence, larger PDN layers enhance thermal conduction in-plane, while reducing vertical thermal conduction. The larger PDN layers do not reduce the maximum temperature of the chip or 3-D stacked assembly. But can cause the horizontal temperature to be uniform. They declared each chip, which can improve temperature results by 15% compared with the case without on-chip PDN. This helped to look around the problem, applying thoughts into alleviating such thermal sources.

In 7nm and still below deep submicron chip design technology, the number of metal layers increasing as high as 16 to 20 layers. Because of the reason that, need more metal density in PDN due to increase in resistances of metal layers of narrow widths. Hence, need to take BEOL or ILD thickness as 10um in the experimental setup. Considered all Fin Field Effect Transistors (FinFET) base layer devices with a 20um thickness, in substrate area. For BEOL/ILD layers, low-k-dielectrics are usually used. For simplicity used low-k-dielectric as Corban Doped Oxide (CDO) with $k=0.39$ W/m.K. CTE, mismatches

will not be a problem, as copper itself is used as TCNs, inside BEOL/ILD layer. These low-k dielectrics will reduce the CTE. Experiments consider very thin dies, referring to various design thicknesses as mentioned in the literature survey [10]. There can be still a thinner base layer in some particular foundries. In the present paper, an experiment is carried out in 4 such chip dies, stacked in 'face top' fashion. These chip dies connected with a vertical TTSV with a diameter of 10um, with liner material of 0.2um (0.1nm each side), in a monolithic IC structure, with a total height of 30um, for a single die. The footprint area A_0 is considered as in large SOCs. The die size is considered 1000um x 1000um. Industry-standard network processing units or the routing chips would be of size 500mm-1200mm in its dimensions. Hence, this paper selected a 10mm x 10mm area (with a total die thickness of 30um), for the analysis and discussion. Fig. 1.a shows the structure of the experimental setup carried out throughout, all the experiments. This also shows, how TTSV is connected to the TCNs. Fig. 1.b shows 4 stacked 3-D IC structures. In this paper for the concept of these 2-D/2.5-D/3-D IC structures, it has been assumed that heat sink and fan assemblies are very efficient enough to empty the heat transferred to it, in all the various types of the experiments, in later stages of thermal paths.

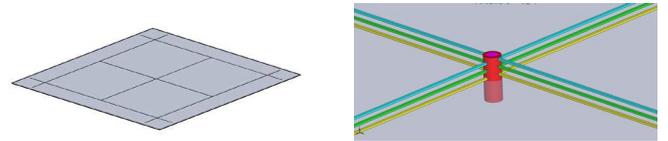


Fig. 1.a. The Thermal Collection Grid (TCN) in a 2-D IC structure.

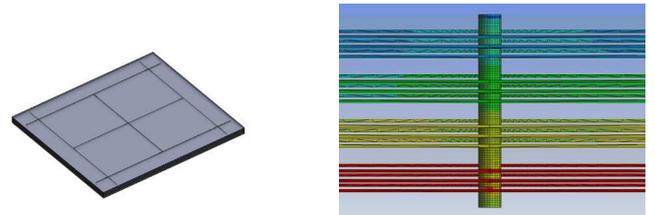


Fig. 1.b. Schematic of multiple stacked 3-D IC structures, connected to TTSV.

The boundary condition of heat flux $5W/m^2$ is applied on top of each die/stack. Considering the heat sink is located, on top of a silicon die, coupled with the fan to cool the heat sink. The bottom die/stack is applied with $10W/m^2$ heat flux. This has been considered that, air flows downwards to the bottom of the die/stack. Physically, this means the SiP has an air-cooling heat sink on the top-side and a natural convection cooling on the bottom side. Because of flip-chip packaging, the bottom layer

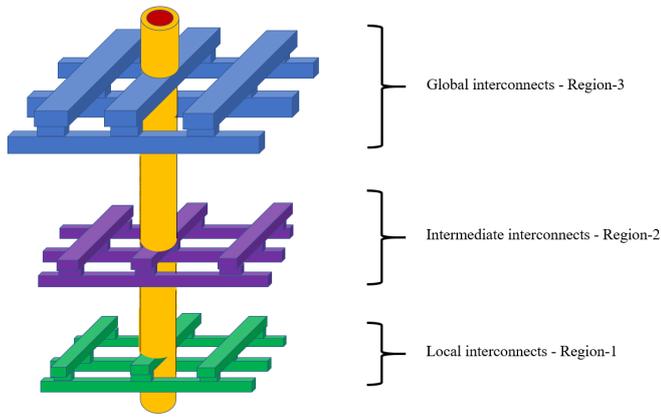


Fig. 2.a. Schematic of TCN rings connected to TTSV, in single die/chip.

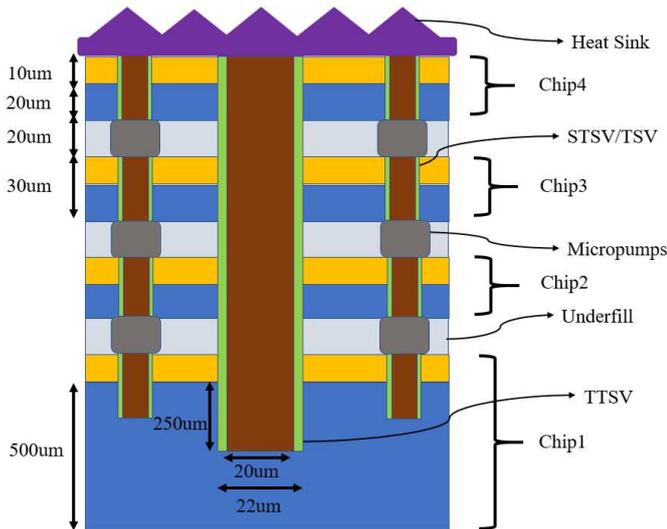


Fig. 2.b. The Thermal Collection Network in a 3-D IC stack of 4 dies.

Table I
THE PROPERTIES AND DIMENSION OF MATERIAL SUMMARY

Parameter	Material	Size/Conductivity
TSV diameter	Copper	10um
Filler thickness	Copper	8um
Liner thickness	SiO ₂	0.2um
Die dimensions	Silicon	10x10um
Substrate height	Silicon	20um
Underfill height	Polymer	20um
ILD Layer (CDO)	Corban Doped Oxide	10um
TSV filler conductivity	Copper	400W/m.K
TSV liner conductivity	SiO ₂	1.4W/m.K
ILD layer conductivity	Corban Doped Oxide	0.39W/m.K
Silicon Conductivity	Si	130W/m.K
Silicon dioxide Conductivity	SiO ₂	1.4W/m.K
Underfill Conductivity	Polymer	0.5W/m.K

of the 4-die stack has a maximum temperature near 110°C, and the minimum temperature on the top layer is 26°C applied. Assumed a uniform heat flux generated by base layer devices and interconnects joule heating occurs in each of the die and across the entire stack. Device power density is applied at top

of each Si layer and interconnects heat flux is applied in BEOL/ILD layer. Besides, an ambient temperature is kept at 25°C. Material sizes and conductivities used in FEM analysis are summarized in Table I. All four sidewalls of the stack applied adiabatic thermal isolation. Heat flux is uniform and normal to surfaces. Interlayers are isometric in nature. Made sure that each of the components in the die/stack, will have enough mesh points. In coarse meshing, it has been made sure that at least 25,000 mesh points are present in each die of the stack while using the FEM tool.

Fig. 2.a is a schematic of the TCN rings, with horizontal and vertical metal shapes, connected to TTSV. Fig. 2.b shows four stacked 3-D IC, with chip1 to chip4. This paper considers underfilling polymer material, with thermal conductivity of 0.5W/m.K.

For the placement of TCN metals, need to choose 3 regions in the BEOL/ILD area, as in Fig. 2.a. The reasons for choosing selected metal layers are explained further. For simplicity, it has been considered a pair of metals. For example, Metal#3 and Metal#4 are local interconnects. Usually, SRAMS will have blockages till Metal#4. To capture such physical memory activity heat, as well standard cell heat, the study chose Metal#3&4, in Region-1 as in Fig 2.a. Metal#1 and Metal#2 would be dedicated power meshes, to supply power/ground to standard cells of the die. The reason for choosing Metal#7 and Metal#8 is, these are middle/intermediate level interconnects, in Region-2 as shown in Fig 2.a. The reason for choosing Metal#11 and Metal#12 is, these are higher/global level interconnects, in Region-3 as shown in Fig 2.a. To capture any thermal energy developed by some of IP like TCAMS (Ternary Content-Addressable Memory), other IPs. These might have been blocked the metals till Metal#11 and Metal#12. Further metal#12 and above would be dedicated power mesh, would get lesser empty tracks of the metals. Since there could be many partitions and sub-blocks inside the whole chip. Complete designing of the width of TCN beyond scope of this paper. This it is indicatively mentioned how to calculate widths, as per given equations in (1) and (2), for a block/partition. For simplicity, the widths of TCNs considered as explained further. Looking from the top level of the chip. Metal#11 and Metal#12 with a metal width of 4um, Metal#7 and Metal#8 with a width of 2um, and Metal#3 and Metal#4 with a width of 1um. In industry-standard foundries, the pitches and widths of the above-mentioned metals will be still lessor, in the case of 7nm or 5nm. Usually, vias will be almost the same height and widths of top metal, connecting to the bottom metal in a pair. It is because lower to higher material widths will increase in common practices of chip designing protocols. Hence, this study keeps the height of vias as same as the width of metal pairs. Pitches of metals pairs in the same plane are taken almost the 200um distance from the boundaries of the chip. Coming to the stacking of 4 dies, it has been kept 20um as a gap between 2 dies, considering ETSVS/TSVs (Electrical TSV/TSV), would connect through them, with micro bumps, in heterogeneous 3-D IC structures. There could be dummy micro bumps (bumps) that will also be present in such an area, with an air gap, or polymers to give mechanical supports.

IV. RESULT ANALYSIS AND DISCUSSION

The thermal performance of various TCN rings along with TTSV stacked systems are studied, by FEM simulations. Respective graphs and data are analyzed in further sections.

A. Thermal performance of TCNs, in 2-D/2.5-D ICs:

The thermal performance of TCNs can be studied on 2-D/2.5-D IC structures, as shown in Fig. 3. The power dissipation in the substrate/base layer of the active region of ICs heat flux is $10W/m^2$ as a major heat source. Basically, to make the thermal runway for base layers, where switching of standard cell power could be $10W/m^2$ as a major heat source. This could include peak dynamic power. On-chip PDN is a minor heat generator; hence, their power dissipation heat flux is $5W/m^2$. Fig. 3 showing TCNs with dimensions mentioned as in computation setup. These were placed in 3 places of 2-D IC. These 5 types are shown with titles "0TCN + 0TTSV" till "3TCN + 1TTSV". The TTSVs are built, on the base of the substrate with a normal etching process, as in metallization methods. The presented paper's goal is to show the TCNs, hence the increased number of TCNs in 3 different regions. To make the first level of the experimental study, uniform thermal generation was applied. In real cases of chip design, designers can make more dedicated or more localized TCNs, to make more thermal runways, around known peak power consumption areas or hot-spot areas. These are easily identified and analyzed by IR drop analysis tools. To maximize heat transfer in a vertical direction, a greater number of TCNs were added with more metal staples in a vertical direction. The larger the TCNS more uniform heat in the horizontal direction.

Fig. 4, shows that when there are no TCN and no TTSV present in a single die, the maximum thermal energy accumulated inside the ILD/BEOL area is high as $68^\circ C$. That means most of the thermal energy is liberated inside the substrate, with $110^\circ C$, applied at the base. When a single TTSV is introduced, the ILD temperature suction increase by $71^\circ C$. By adding TCNs at lower layers of the chip maximum average temperature of the ILD increases to $75^\circ C$. When TCN rings are added in 2 more places, like intermediate and top layers of the chip, the maximum temperature suction goes up to $83^\circ C$. It clearly shows that if dedicated thermal runways are used, could be the solutions to the thermal mitigation inside 2-D ICs. This must be sucked into the heat sink and fan assembly, in further stages.

B. Thermal performance of multiple TTSVs and multiple TCNs in 2-D/2.5-D ICs:

The schematic of 2-D IC with multiple TTSVs along with multiple TCN rings, is shown in Fig. 5. Wherein, when there is no TTSV, later introduction of single TTSV, followed by 2, 4, and 5 TTSVs along with 3 rings of TCNs, are shown.

The empirical equations (7)-(8) represent the equivalent thermal conductivities inside the chip, when multiple TTSVs are used [3].

$$k_{eqv,z(chip)} = 150 + 180 (D^{-2}P^{-2}) \quad (7)$$

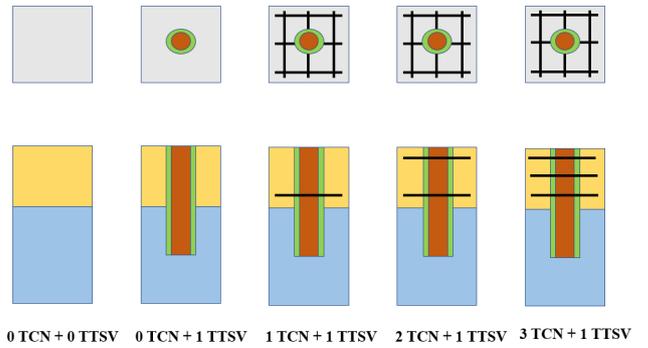


Fig. 3. The schematic of the 2-D IC with multiple TCNs and single TTSVs.

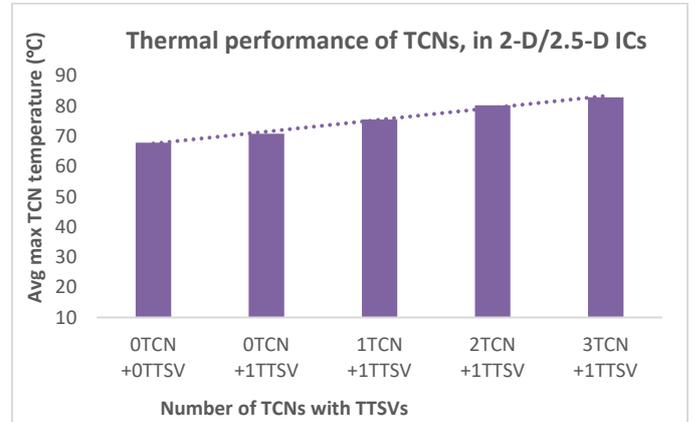


Fig. 4. Thermal performance of multiple TCNs with multiple TTSVs, in 2-D/2.5-D-IC structures.

$$k_{eqv,x(chip)} = k_{eqv,y(chip)} = 150 + 105 (D^{-2}P^{-2}) \quad (8)$$

Where, P is the pitch of the TTSVs and $D = (D_1 + D_2)/2$ is the diameters of the top (D_1) and bottom (D_2) of the TTSV. By considering the practical tapered width of the TTSVs.

Observing the equations shows that, the thermal conductivity of the chip in the Z (vertical) direction is faster than the thermal conductivity of the chip in X and Y directions (horizontal) when multiple copper-filled TTSVs are used.

Fig. 6, shows that the ILD temperature of the chip was $68^\circ C$ when there was no TTSV and no TCN ring grid. By introducing 1, 2, 4, and 5 TTSVs along with increasing TCN grids up to 3, in each of such 2-D IC, an average ILD temperature drastically increases to $89^\circ C$. This accumulation of heat should now be moved into the heat sink and fan assembly in later stages. This is the reason behind having more TTSVs, in 2.5-D structures. An example of such ICs is a network routing chip. These may go up to $500mm^2$ - $900mm^2$ in the area. These chips might be integrated with HBM (High Bandwidth Memory) stacks. Hence, thin-sliced dies, with broader widths defiantly need such TTSVs.

C. Thermal performance of TCNs in 3-D IC systems:

After a brief study in a single 2-D or 2.5-D IC structure, more light had been put towards 3-D IC structures, where thermal

mitigation is very crucial. Chip1 to 4, have been bonded in ‘face top’, fashion as shown in Fig. 7. Bonded 4 stacked dies, to form 3-D IC structures, with a single TTSV along with 5 TTSVs. Note that, the structure shown in the stacked TTSV can be a single structure built when manufacturing monolithic 3-D-IC, and not limited to that when building non-monolithic. These TTSV structures can also be formed to look like a single vertical rod, connecting with micropumps. Hence, micropump material would come into considerations. Where inside the TSVs these have a negligible impact on thermal mitigation as per [1] and [15].

Fig. 8. shows, single TTSV with 3 rings of TCNs versus 5 TTSVs with 3 rings of TCNs, inside the whole 4 dies stacked structure. The results show that, the average temperature raised inside the TCNS is 91°C. Without such structures, an average temperature is at 82 °C. As said earlier this heat must be passed onto the heat sink in later stages. Therefore, this could be complete and novel solutions towards the thermal mitigation problem of 3-D ICs, without expensive capillary fluidic solutions inside 3-D IC stacks.

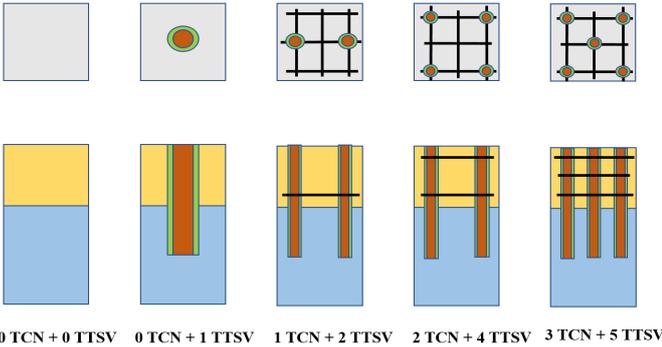


Fig. 5. The schematics of the 2-D IC with multiple TCNs and multiple TSVs.

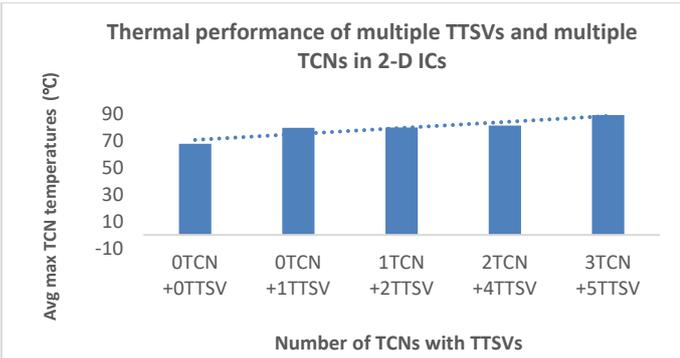


Fig. 6. Thermal performance of multiple TCNs with multiple TTSVs in the 2-D/2.5-D IC structures.

D. The junction temperature of TTSVs in 3-D IC systems:

The junction temperature is an important study when multiple TTSVs and TSVs are used in 3-D IC stacks. If junction temperature increases more than the maximum/budgeted

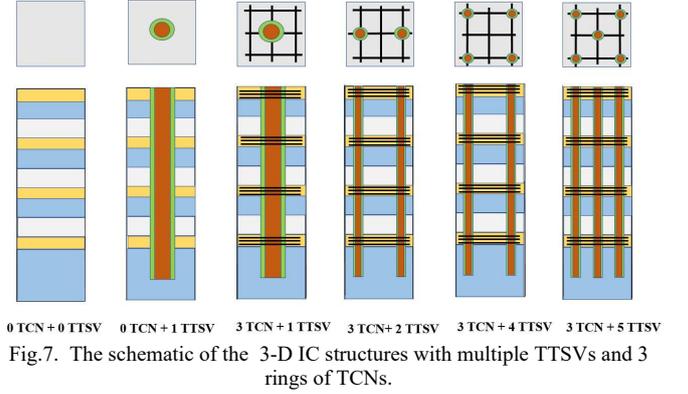


Fig. 7. The schematic of the 3-D IC structures with multiple TTSVs and 3 rings of TCNs.

allowable temperature, then it could be a disaster inside stacked systems. The junction temperatures can be described as below in equation (9).

$$R_{therm} = \frac{T_{junct} - T_{ambi}}{H_{flow}} \quad (9)$$

Where, R_{therm} is the thermal resistance of the stack. H_{flow} is generated heat of the stack. T_{junct} and T_{ambi} are the stack junctions and ambient temperatures, respectively.

From the graph, in Fig. 9, it is evident that temperature distribution for different TTSVs of the stacked fashion is uniform. If the comparison is done on a 3-D stack without any of the TCNs and TTSVs an average junction temperature is 68 °C. The maximum average junction temperature inside the TTSVs is 92°C, when introduced all 5 TTSVs. Because of the reason that TTSV is continuous and uniform in the vertical direction of heat flow. Whereas in case of TSVs junction will appear, soon after each of dies, through which signals/power must enter in different media/barriers, then junction temperature will start playing a major role. As a design constraint, the maximum junction temperature of the stack must be predefined. As per that, the maximum of a few dies’ integrations can only be possible for 3-D IC stacks. But, since this suction is attached to the next level of the heat distribution, if preempted successfully, then a greater number of the stacking is also possible, than the present limitations depending on junction temperatures. The total summary of all the experiments with the benefits of thermal runways is shown in Table II, in comparison with no TCNs and no TTSVs.

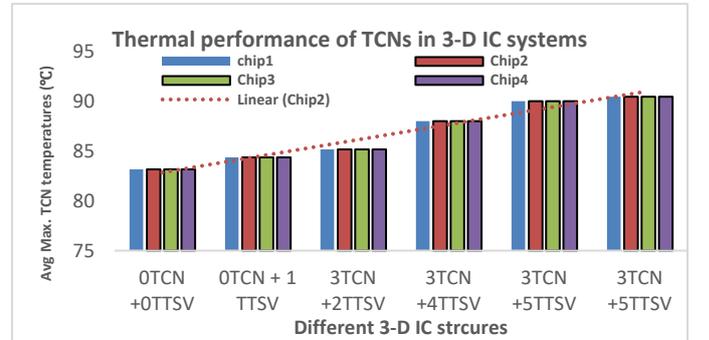


Fig. 8. Thermal performance of TCNs along with multiple TTSVs in 3-D IC structures.

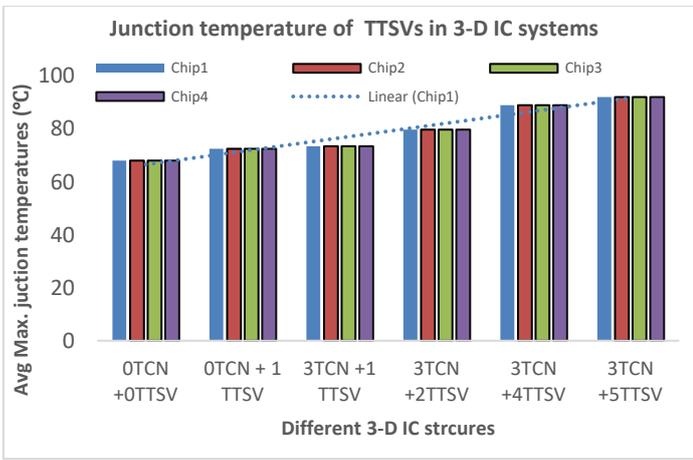


Fig. 9. Junction temperatures for 4 stacked TSV chips (uniform heat sources).

Table II
THE EXPERIMENTAL SUMMARY

Experiment names	Benefits compared to no TCN and no TTSV
Thermal performance of TCNs, in 2-D/2.5-D ICs	22.13%
Thermal performance of multiple TTSVs and multiple TCNs in 2-D/2.5-D ICs	31.62%
Thermal performance of TCNs in 3-D IC systems	11.36%
The junction temperature of TTSVs in 3-D IC systems	35.35%

V. CONCLUSION

This paper proposed a thermal collection network grid, and its models in designing optimal thermal collection/reception network for N metal layer system, with a given design constraint such as power, IR drop budget, and supply voltage for all type of SOCs, SiP packages, non-monolithic, and monolithic 2-D/2.5-D/3-D IC structures.

Using FEM simulations, it has been shown that, 22.13% more thermal energy was sucked when used 3-rings/layer of TCNs inside BEOL of a single die chip. When introduced up to 5 TTSVs along with the same 3 layer/rings of TCN grid, the thermal suction was up to 31.62%, for the same monolithic ICs. The same TCN when introduced in monolithic, 3-D IC system the thermal energy suction, was up to 11.36% of the total system package. Junction temperature study has shown that, 35.35% of heat suction could happen inside the TTSVs, junctions.

In the physical design world, laying of TCNs in 2-D IC chips could be done soon after PDNs or pre routes are created in floorplan designs. Later same design could be taken to the placement of cells followed by Clock Tree Synthesis (CTS) and route, chip finish, etc. Fabrication of TCNs inside 3-D ICs structures could also follow the conventional methods and procedures. But, need to connect to TTSVs, by penetrating the liner material of TTSVs.

The detailed foundry process procedures could be beyond the scope of the present paper. Thus, the presented paper coins new dedicated TCN rings/grids. This paper proposed dedicated thermal runway paths for the thermal absorptions, in a quick and efficient manner to preempt the thermal energy, to alleviate thermal problems of 2-D/2.5-D IC and 3-D IC structures.

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Figures

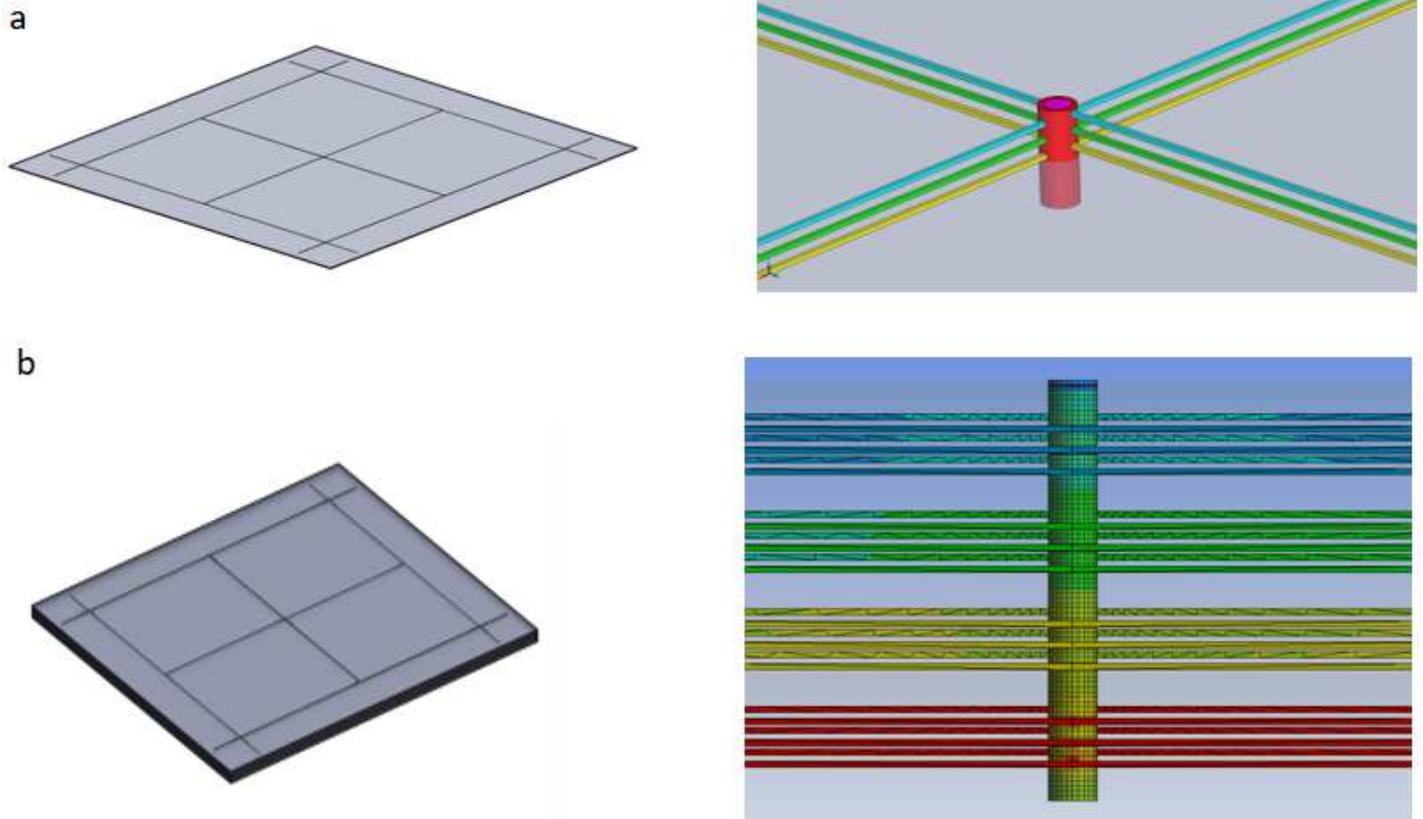


Figure 1

a. The Thermal Collection Grid (TCN) in a 2-D IC structure. b. Schematic of multiple stacked 3-D IC structures, connected to TTSV.

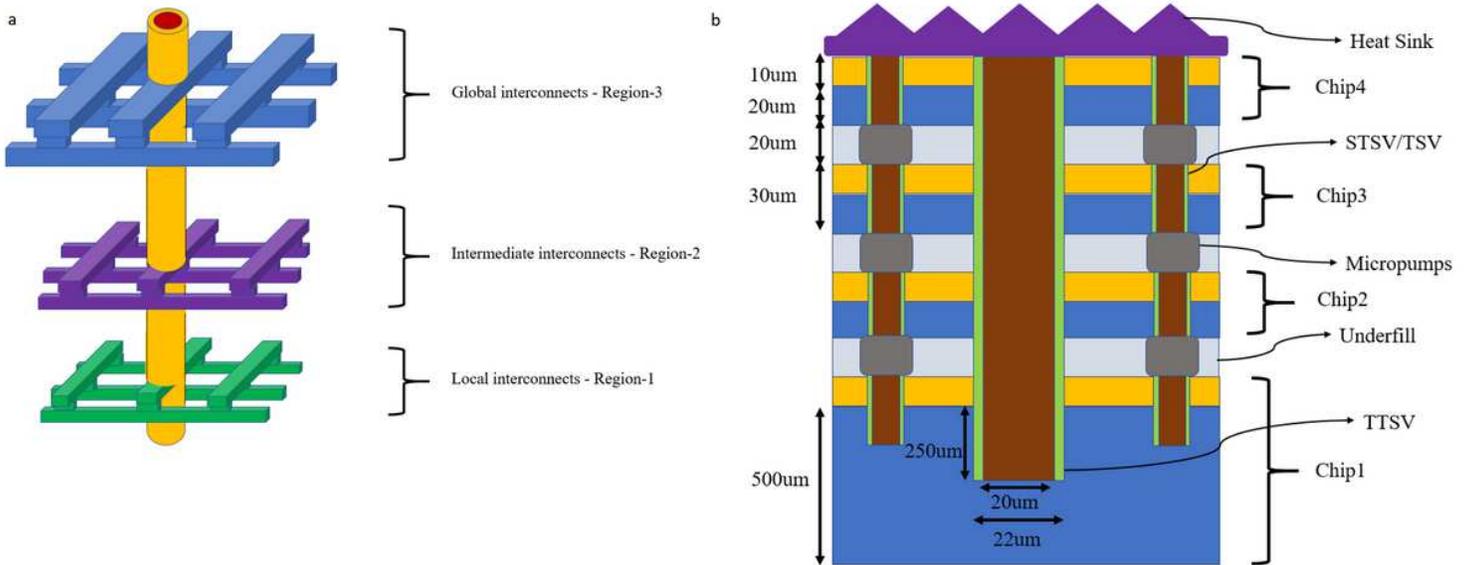


Figure 2

a. Schematic of TCN rings connected to TTSV, in single die/chip. b. The Thermal Collection Network in a 3-D IC stack of 4 dies.

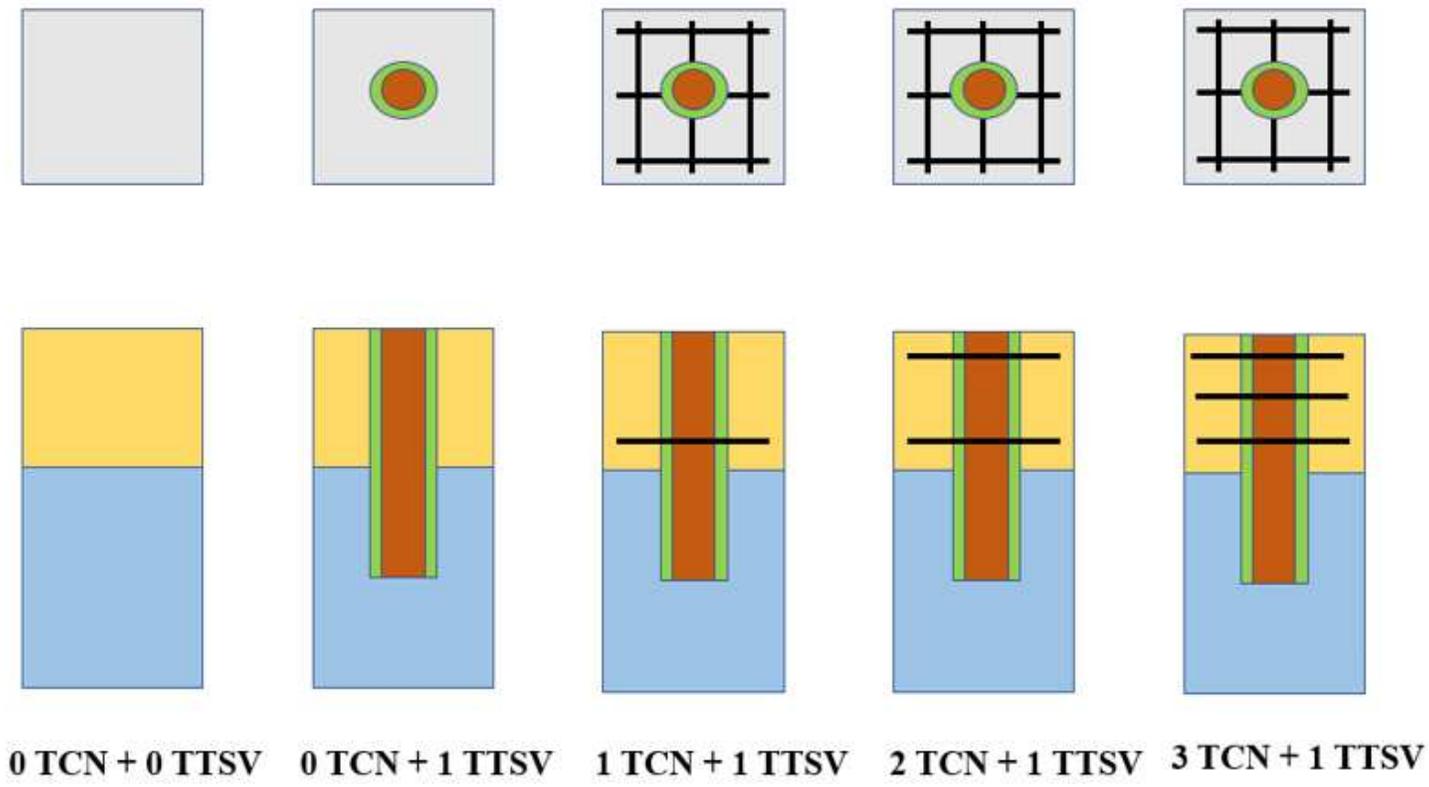


Figure 3

The schematic of the 2-D IC with multiple TCNs and single TTSVs.

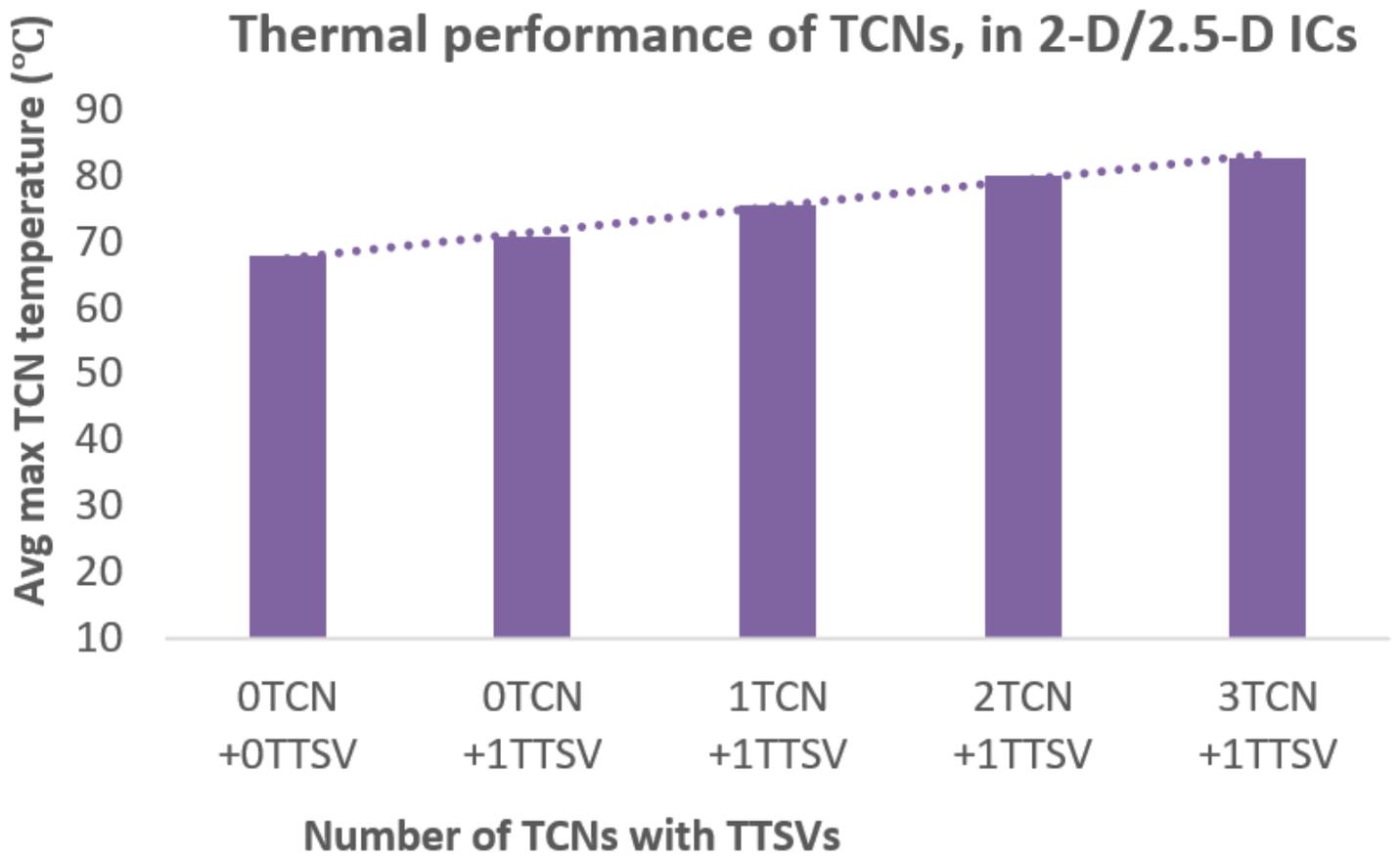


Figure 4

Thermal performance of multiple TCNs with multiple TTSVs, in 2-D/2.5-D-IC structures.

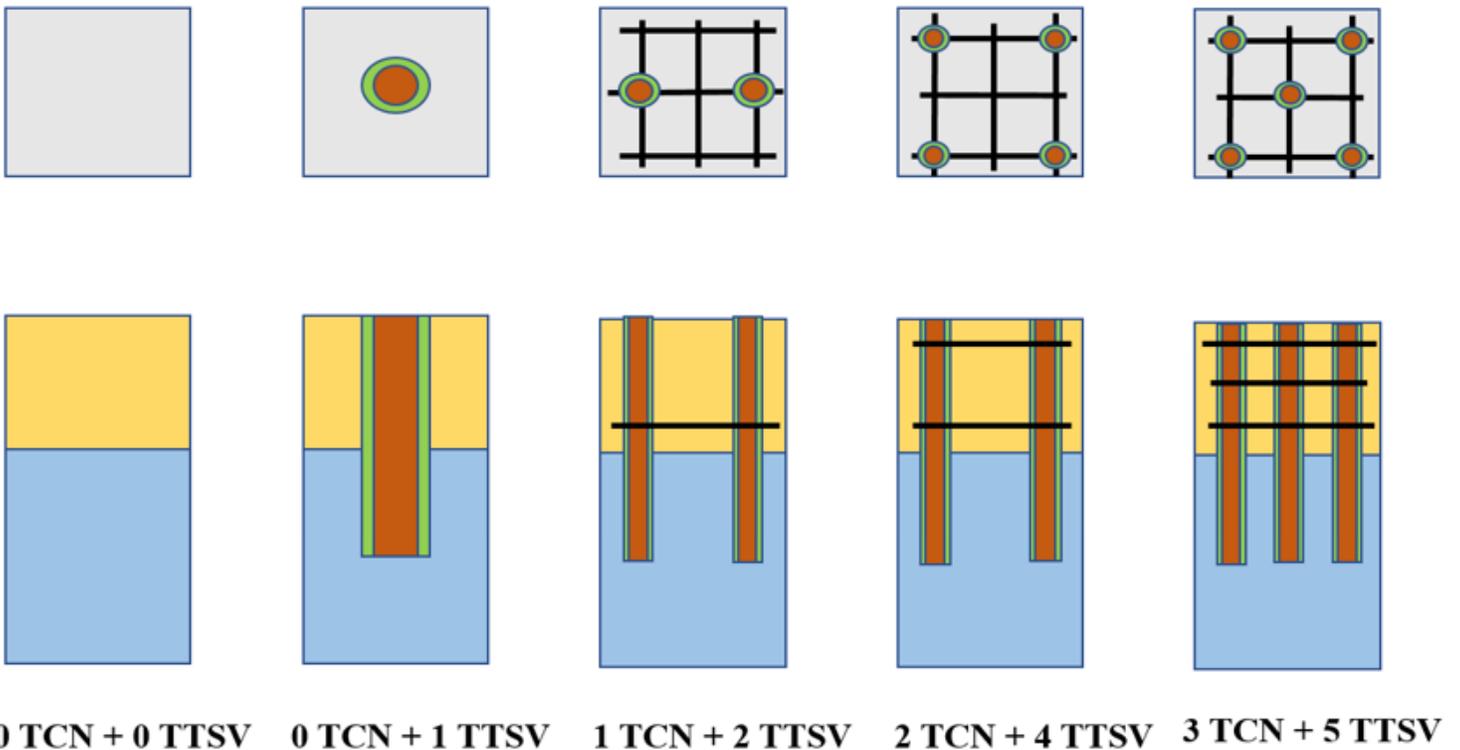


Figure 5

The schematics of the 2-D IC with multiple TCNs and multiple TSVs.

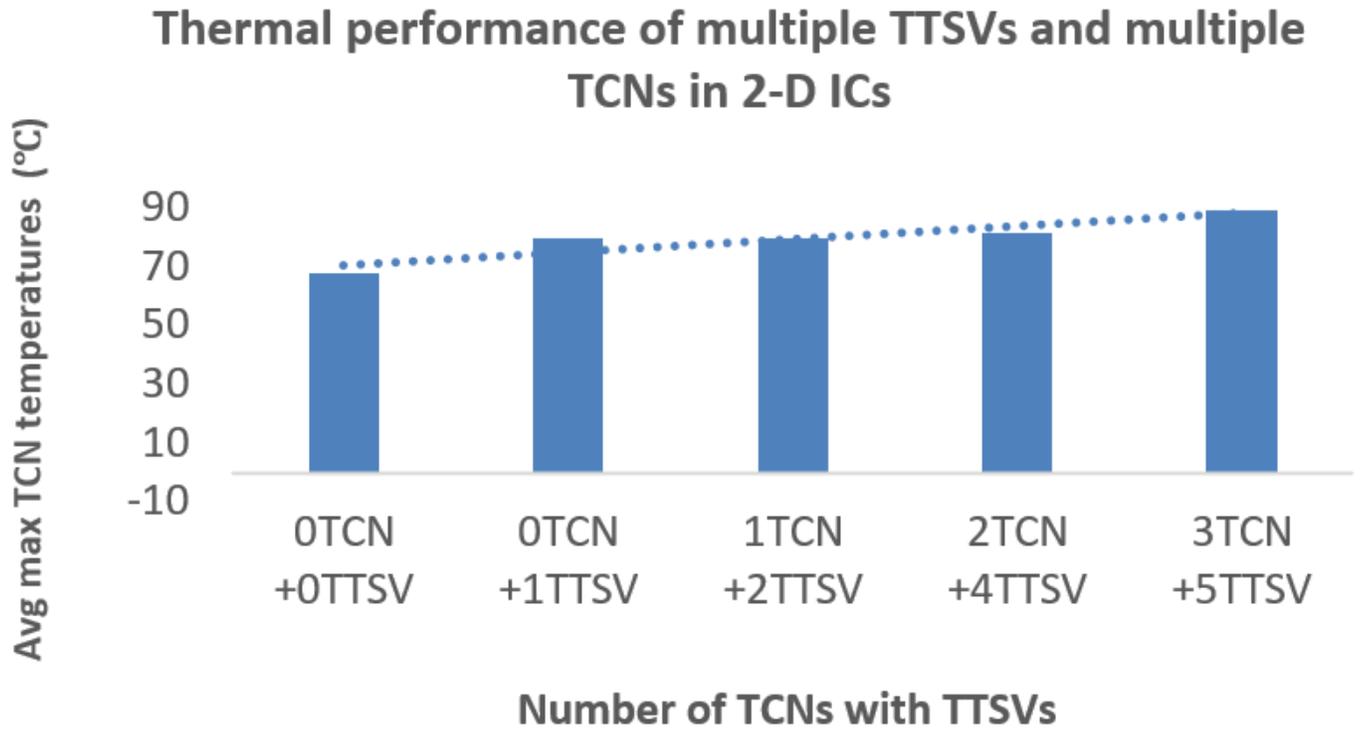


Figure 6

Thermal performance of multiple TCNs with multiple TTSVs in the 2-D/2.5-D IC structures.

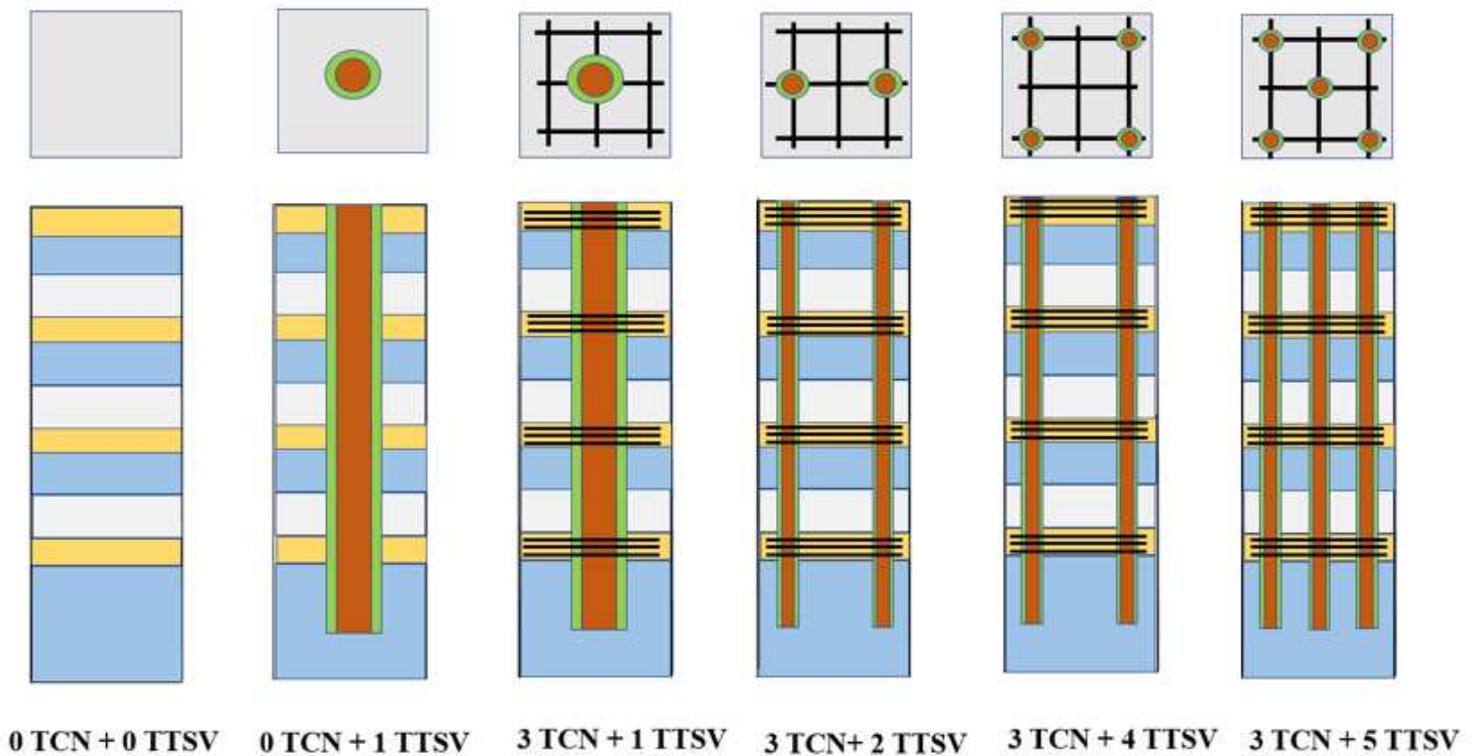


Figure 7

The schematic of the 3-D IC structures with multiple TTSVs and 3 rings of TCNs.

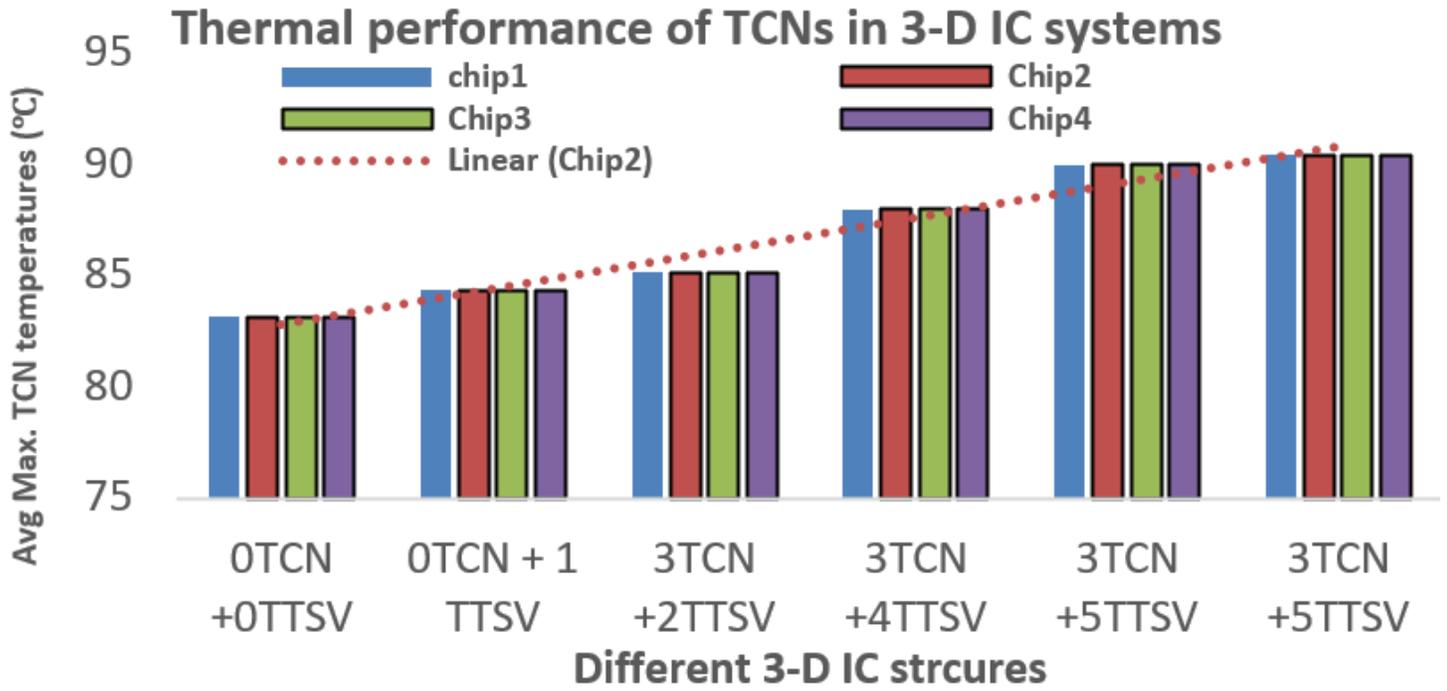


Figure 8

Thermal performance of TCNs along with multiple TTSVs in 3-D IC structures.

Junction temperature of TTSVs in 3-D IC systems

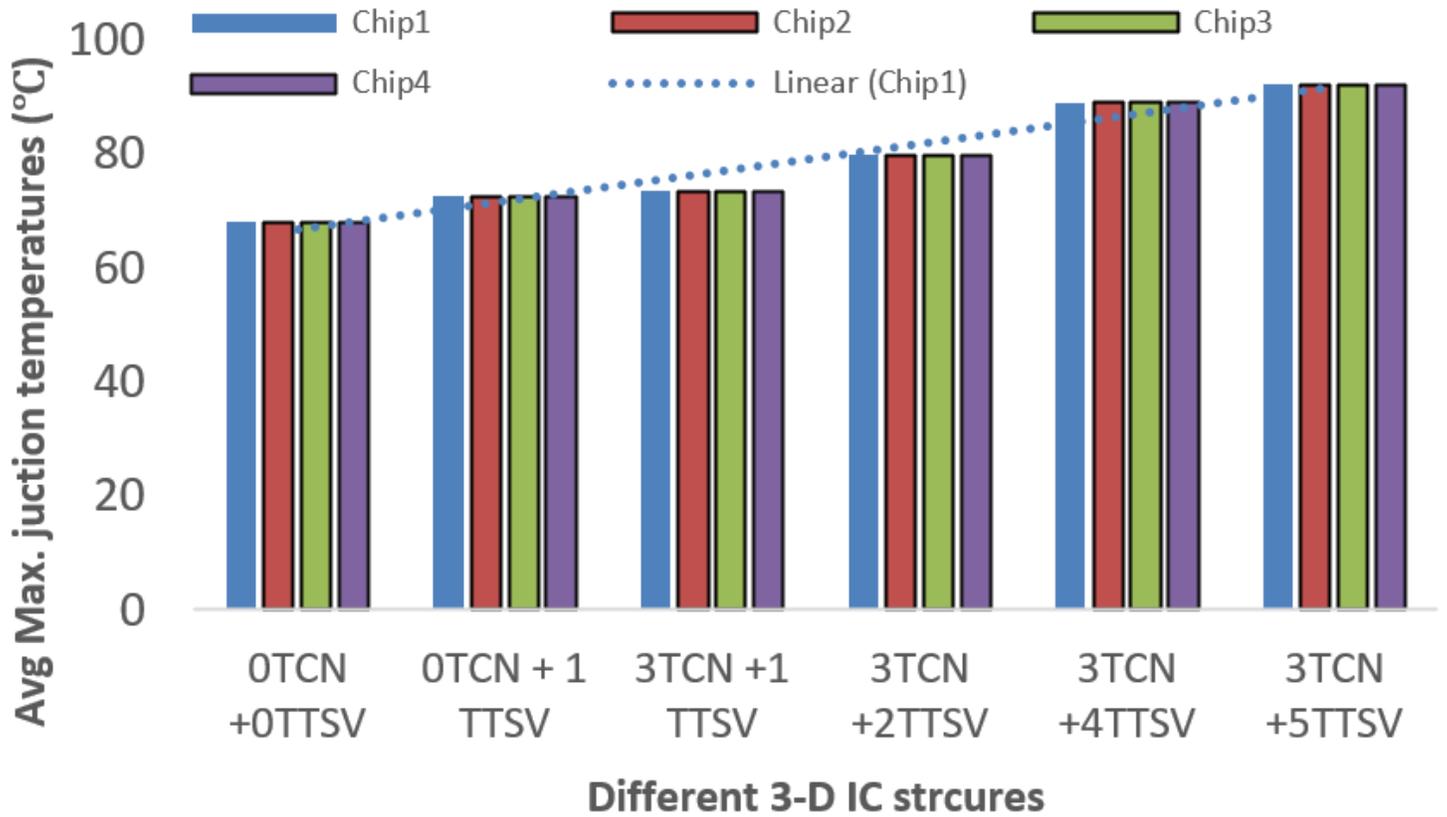


Figure 9

Junction temperatures for 4 stacked TSV chips (uniform heat sources).