Analog/RF Performance Analysis of Heterojunction Tunnel FET with Temperatute

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Research Article

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***Abstract*—In this paper, the analog/RF analysis of SiGe source-based heterojunction Tunnel FET is reported. The parameters like transconductance (g_m), device efficiency (g_m/I_D), gate-source capacitance (C_{GS}), gate-drain capacitance (C_{GD}), cut-off frequency (f_T) and gain-bandwidth product (GBP) are studied. DC, as well as AC simulations, have been performed on the proposed device. We have achieved an ON current of 0.537 µA/µm and OFF current of 13 fA/µm, thus achieving I_{ON}/I_{OFF} ratio as 3.72×10^{10}. We have also performed temperature analysis of the analog/RF parameters. We have also investigated the device for the temperature analysis concerning the drain current and the capacitance calculations. We have observed that the OFF currents are strongly dependent on the temperature. All the simulations have been performed on Visual TCAD (licensed version 1.9.2-3).**

***Keywords*—Tunnel FET; band to band tunneling; subthreshold swing; Miller capacitance; transconductance; cut-off frequency**

Declarations

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I. INTRODUCTION

With continuous scaling of transistors in CMOS technology, it has been made possible to attain high drive currents with a high-frequency performance of conventional MOSFET. However, due to the shrinking of the device with scaling, short channel effects and leakage currents put a constraint on its use [1-5]. Thus, extensive research has been made to develop novel devices that can overcome the scaling limitation in a MOSFET. Moreover, due to the thermionic emission mechanism, the subthreshold swing of a MOSFET cannot achieve less than 60 mV/decade at room temperature. In the recent past, Tunnel Field Effect Transistors (TFETs) have been proposed as a substitute for the conventional MOSFET structures [6-9]. The physics involved in the current transport mechanism of a TFET is based on the band to band tunneling (BTBT) rather than a thermal injection of electrons as in case of a MOSFET. So, it is possible to achieve steeper subthreshold swing and a high I_{ON}/I_{OFF}ratio, while operating at a supply voltage lesser than 1 Volt. Hence, TFETs are seen as promising devices for low power applications such as smartphones, laptops, etc.

Despite the given advantages, it has been seen that TFETs based on silicon material suffers from low ON current and high subthreshold swing (SS) thus rendering it unsuitable for practical use. Poor characteristics of a conventional TFET structure has been attributed to the larger energy band gap of the silicon material. Researchers have presented various performance booster techniques such as dual gates, gate all around, high-k dielectric material, use of low energy band gap, etc. to boost the ON current and to achieve sub 60 mV/decade subthreshold swing [10-15] However, seldom papers have been reported regarding the analog/RF performance of TFET structure [16-21].

In this paper, we have analyzed SiGe source-based heterojunction TFET device on the basis of the following analog/RF parameters: transconductance (g_m), device efficiency (g_m/I_D), gate source capacitance (C_{GS}), gate drain capacitance (C_{GD}), cut-off frequency (f_T) and gain-bandwidth product (GBP). Further, we have analyzed the device for the temperature variations from 200 Kelvin to 400 Kelvin.

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II. DEVICE DETAILS AND SIMULATION

The schematic structure of the device is given in Fig. 1. The structure uses $Si_{1-x}Ge_x$ as the source material, where x represents the amount of the molar fraction of Germanium added to the compound SiGe.

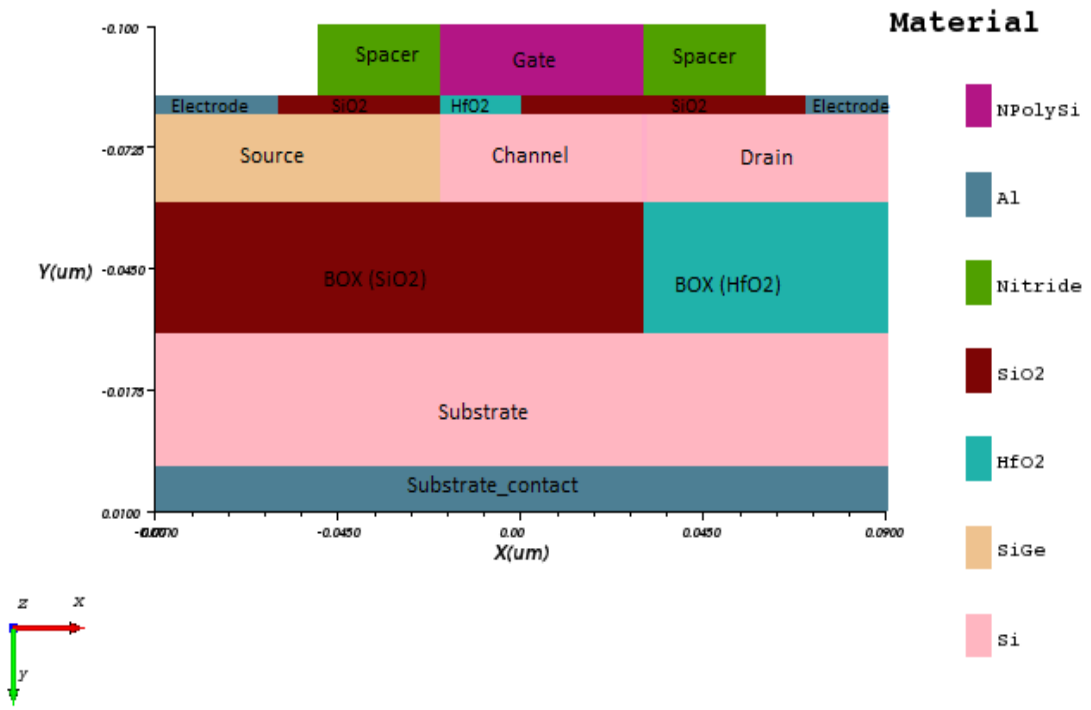

Fig.1. Proposed Device Structure

Germanium has a smaller energy band-gap compared to the silicon. Thus, it helps in boosting the ON current of a device [22-26].However, the sole used of a Germanium also increases the OFF current at the same time, which is not desirable. While as, the leakage current in silicon is around 1000 time lesser than that of a Germanium. Thus, to combine excellent features of both materials, SiGe has been used in the source region. The values of molar fraction, work function and spacer lengths have been optimized for better I_{ON}/I_{OFF} and SS [27-29]. The values of the device parameters have been provided in Table 1. Silicon on Insulator (SOI) has been utilized to suppress short channel effects [30-32].

All the simulations have been performed on Visual TCAD. Kane's local band to band tunneling model has been enabled while running the simulation. Lombardi Model has also been used in order to take high field mobility into consideration. The electron-hole tunneling current is calculated by WKB integral.

TABLE I
VALUES OF PARAMETERS

Parameters Used	**SiGe-TFET**
Gate Length	50 nm
Doping at Source	1×10^{20} cm^{-3}
Doping at Channel	1×10^{15} cm^{-3}
Doping at Drain	5×10^{18} cm^{-3}
Oxide Thickness	2 nm
Gate Work Function	4.7 eV
Substrate Doping	1×10^{19} cm^{-3}
Molar Fraction	$x = 0.65$

III. Investigation Results And Discussion

Fig. 2 represents the energy band diagram of a device in OFF and the ON state. When gate-source voltage V_{GS}= 0 Volt, the valence band of the source lies above the conduction band of the channel, hence band to band tunneling is inhibited.

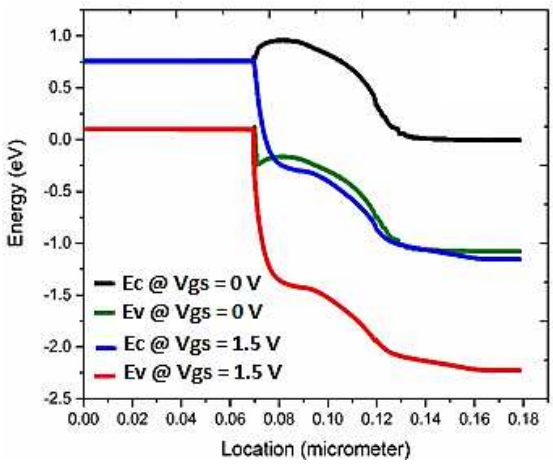

Fig.2. Energy Band Diagram for the proposed device

When the gate-source voltage is increased gradually, the electrical field around the gate-source region increases, thus enabling the band to band tunneling. This results in an increase in the drain current. Kane's model gives the rate of the tunneling as:

$$G^{BB} = A.BTBT.\frac{E^2}{\sqrt{E_g}}.\exp\left(-B.BTBT.\frac{E_g^{3/2}}{E}\right) \qquad (1)$$

Here A.BTBT and B.BTBT are empirical fitting parameters, E is the electrical field and E_g is the energy band-gap. From (1), it is clear that the tunneling rate increases with an increase in the electrical field. A

Fig. 3 shows the variation of an electrical field with the application of gate-source voltage. As the gate voltage is increased from V_{GS}= 0 V to V_{GS}= 1.5 V, the electrical field increases. Fig. 4 shows the surface potential of the device. It is clear from the figure that the potential is low at the source junction. As we proceed toward the drain junction, the surface potential increases. Moreover, the graph indicates that as the gate-source voltage is increased, the surface potential increases.

Fig. 5 shows the drain current transfer characteristics of the device. The device shows an excellent subthreshold swing of 28.57 mV/decade and maintains I_{ON}/I_{OFF} ratio of 3.72×10^{10}. The threshold voltage of a device has been found out by using

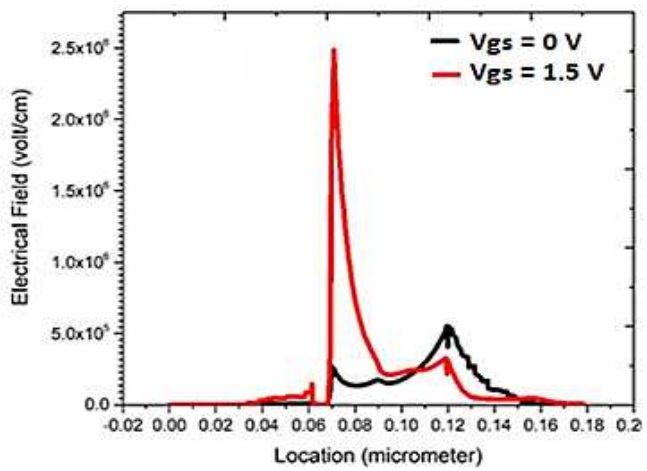

Fig. 3. Electric Filed Variations at the source

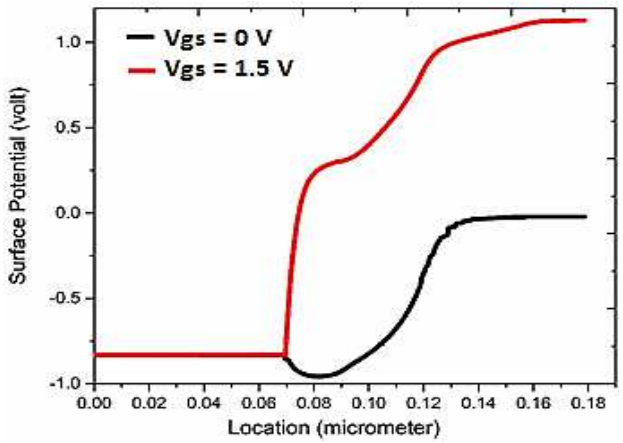

Fig. 4. Surface Potential of a device

a constant current method, and the gate voltage has been noted at the drain current value of 10^{-7} A/µm. Furthermore, drain induced barrier lowering (DIBL) has been calculated by observing the linear I_D vs V_{GS} curve at the linear and the saturation mode.

DIBL is basically a short channel effect phenomenon in short channel devices, where the larger drain voltage widens the depletion region hence lowering the potential barrier at the source. The value of DIBL obtained in our device is 3.636 mV. Thus, it can be said that the short channel effect of DIBL is greatly restrained in our proposed design. The equation used for DIBL calculation is given as:

$$\mathrm{DIBL} = \frac{V_{T_{LIN}} - V_{T_{SAT}}}{V_{D_{SAT}} - V_{D_{LIN}}} \qquad (2)$$

Where $V_{D_{SAT}}$ and$V_{D_{LIN}}$ are the supply voltages at the saturation and the linear mode. $V_{T_{LIN}}$and$V_{T_{SAT}}$ are the threshold voltages obtained using the constant current method at the linear and the saturation mode, respectively.The variations with temperature from a range of 200 K to 400 K are performed on the drain current. It can be observed from the Fig.6 and Fig. 7 that the ON current is not affected with temperature variations. It is because the band to band tunneling is weakly dependent on temperature. However, it can be seen that the OFF current strongly varies with temperature.Transconductance plays an important role in terms of analog performance. It represents

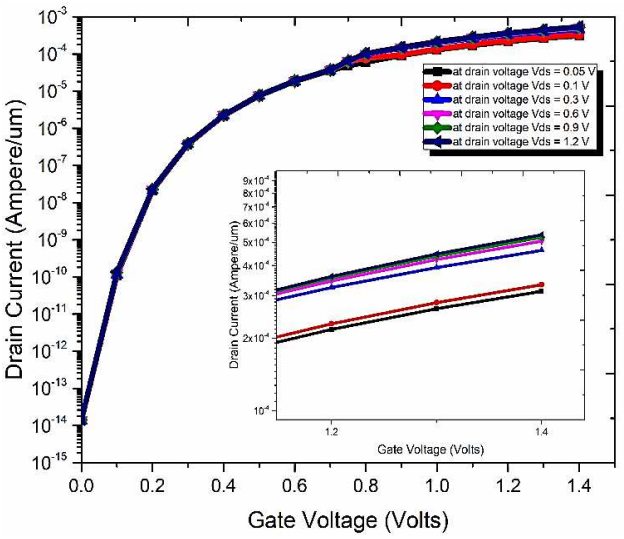

Fig. 5. I_D-V_{GS} Transfer characteristics curve

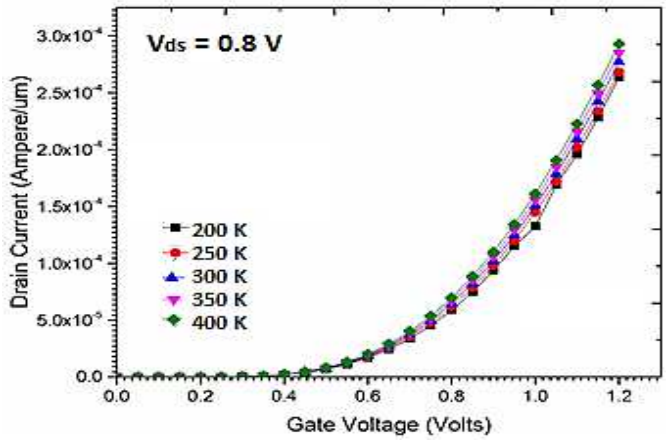

Fig. 6. Temperature variations in I_D-V_{GS} Transfer characteristics curve

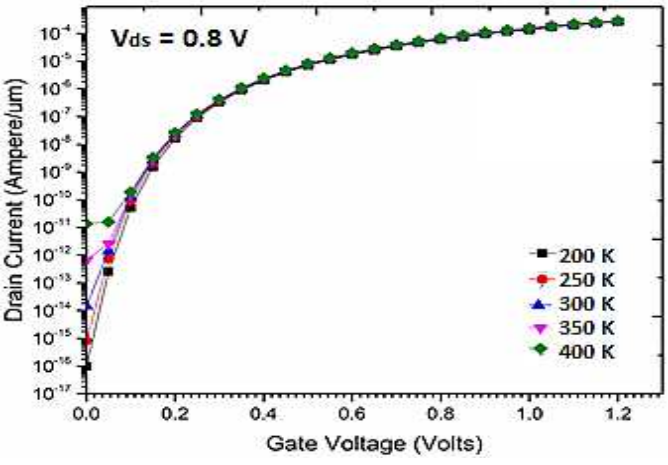

Fig. 7. Temperature variations in logI_D-V_{GS} Transfer characteristics curve

the change in the output drain current with respect to the variations in a gate voltage. It is clear from Fig. 8 that at the lower voltages, the transconductance increases with the increase of a gate voltage. However, at the higher voltages, it is observed that g_m decreases due to the mobility degradation.

Mathematically, transconductance is defined as:

$$g_m = \frac{dI_D}{dV_{GS}} \text{ (at Constant } V_{DS}) \qquad (3)$$

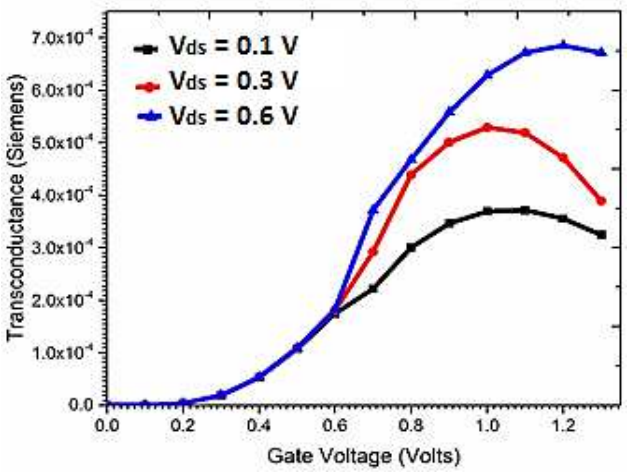

Fig.8. Transconductance vs Gate voltage curve

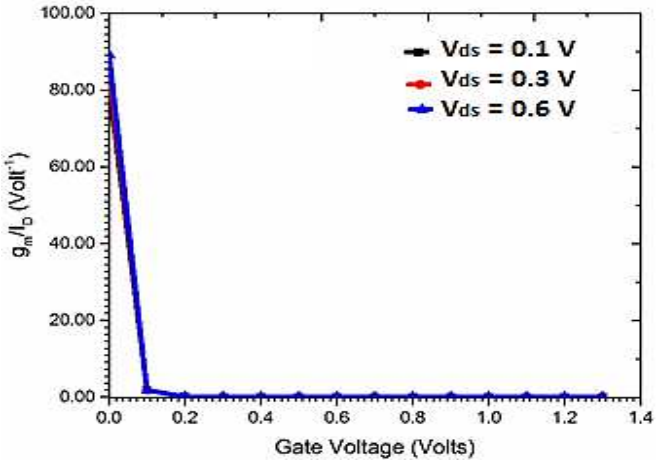

Fig. 9. Device Efficiency (g_m/I_{DS}) vs Gate Voltage curve

Transconductance to output drain current (g_m/I_{DS}) or device efficiency is another useful parameter for analog/RF applications—Fig. 9 plots device efficiency of the device against the drain current for the device. The improvements in the device efficiency are attributed to the increase in the transconductance of the device. g_m/I_{DS} ratio obtained shows that the device is capable of providing high energy efficiency at lower gate voltages, which is an essential parameter for low power analog/RF applications (Chander et al., 2017; Sarkar & Sarkar, 2013).

From equation (2), g_m/I_{DS} can be expressed as:

$$\frac{g_m}{I_{DS}} = \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}}$$

and subthreshold swing (SS) is given by:

$$\frac{1}{SS} = \frac{\partial \ln(I_{DS})}{\partial V_{GS}} = \frac{1}{\ln 10}\frac{\partial \ln(I_{DS})}{\partial V_{GS}}$$

$$= \frac{1}{\ln 10}\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{1}{\ln 10}\frac{1}{I_{DS}}g_m$$

$$\frac{1}{\mathrm{SS}} = \frac{1}{\ln 10}\frac{\mathrm{g_m}}{\mathrm{I_{DS}}} \qquad (4)$$

Therefore,

$$\frac{\mathrm{g_m}}{\mathrm{I_{DS}}} = \frac{\ln 10}{\mathrm{SS}} \qquad (5)$$

Hence, from Eq. (5), the theoretical limit of g_m/I_{DS} is about 38.3 V^{-1}. However, since TFET based structure has been employed in this paper with an excellent subthreshold swing of 28.57 mV/decade, thus increasing the device efficiency tremendously. From equation (5), by substituting the value of the average subthreshold swing, the value of device efficiency g_m/I_{DS} comes out to be 80.59 V^{-1}, which is more than twice the value achievable with the MOSFET structure. Thus, larger values of g_m/I_{DS} than that of a MOSFET is achievable with TFET structure Also, there is no noted difference with the variations in the drain voltage.

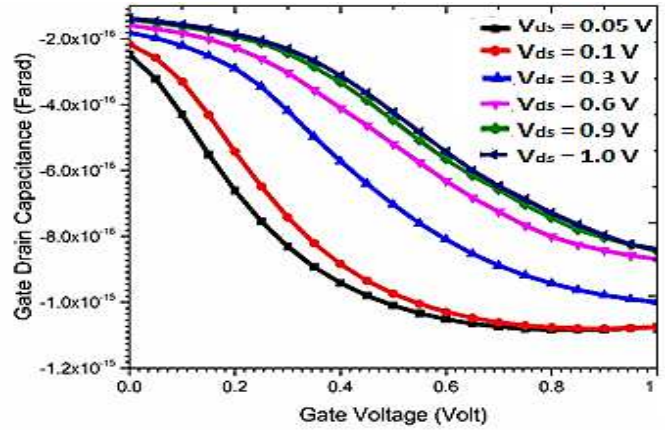

Fig. 10. Gate-Drain capacitance curve

Parasitic capacitances play a vital role in the determination of the propagation delay and the high-frequency response of the device. For complete insights, both gate-source capacitance (C_{GS}) and gate-drain capacitance (C_{GD}) are taken into consideration. For a heterojunction TFET, C_{GD} dominates overall capacitance (Mookerjea, Krishnan, Datta, & Narayanan, 2009). Fig. 10 shows the variation of the gate-drain capacitance as a function of the gate voltage. It is clear from the figure that C_{GD} increases with the increase of V_{GS}due to the development of the inversion layer from the drain towards the source region.

Fig. 11 shows gate-source capacitance variations with gate voltage. C_{GS}depends on the electron concentration of the source side. It can be observed that C_{GS}decreases with an increase in gate voltage V_{GS}. It is because the coupling between the gate and the source decreases because of the increased inversion

layer. C_{GS}values obtained are lesser than that ofC_{GD}. The total gate capacitance can be calculated by summing up gate-source (C_{GS}) and gate-drain capacitances (C_{GD}).nThe values of the capacitance obtained lies in the range of 0.1 to 1 femto Farads. Furthermore, we have also performed a temperature analysis of the capacitance parameters. It can be observed from Fig. 12 and Fig. 13 that both the capacitances remain weakly dependent on the temperature at lower voltages, and shows a slight increase in the values at higher

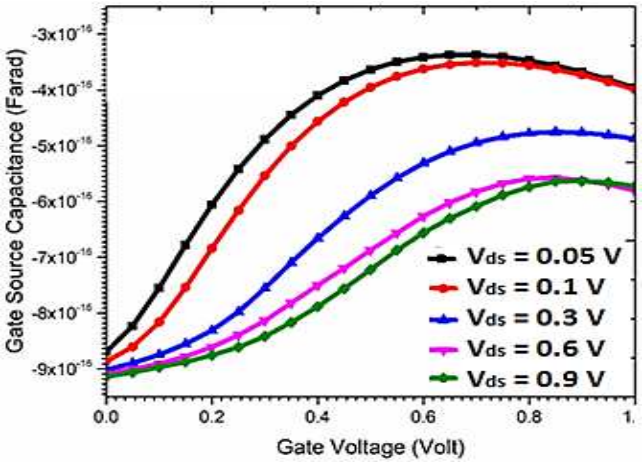

Fig. 11. Gate-Source capacitance curve

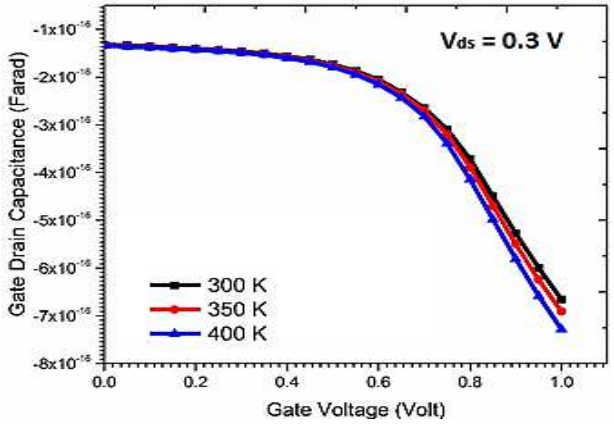

Fig. 12. Temperature variations in Gate-Drain capacitance curve

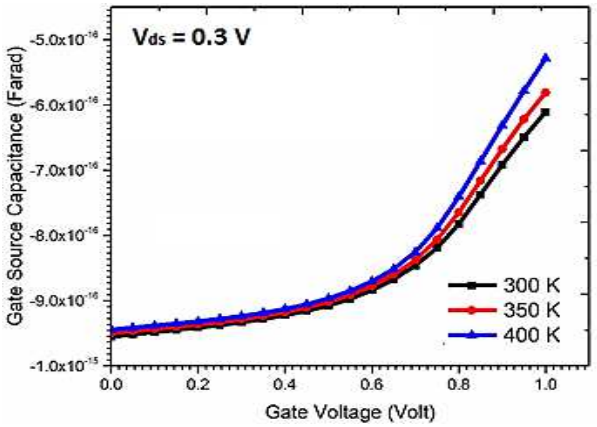

Fig. 13. Temperature variations in Gate-Source capacitance curve

gate voltages. Overall, it can be deduced that C_{GS} and C_{GD} have a negligible effect on temperature variations.The cut-off frequency (f_T) is another important parameter of interest, that represents the frequency range up to which a device can be amplified. It is defined as the frequency at which gain becomes unity. For better RF applications, f_T must be as high as possible. The value of cut-off frequency is given by:

$$f_T = \frac{g_m}{2\pi C_{GD}\sqrt{1+\frac{2C_{GD}}{C_{GS}}}}$$

$$\cong \frac{g_m}{2\pi(C_{GS}+C_{GD})}$$

$$f_T \cong \frac{g_m}{2\pi C_{GG}} \qquad (6)$$

Thus, an increase in parasitic capacitances would decrease the cut-off frequency. It can also be deduced from the given equation with an increase in g_m, the cut-off frequency increases as well. This is mainly attributed to the injection of charges from the source and the increase in the band to band tunneling. The higher mobility for a device can be achieved if a drain voltage is increased. This, in turn, improves the transconductance of the device. Similarly, the gate capacitance C_{GG} also reduces with an increase in drain-source voltage. Thus, the increase of g_m and the decrease of C_{GG} leads to the higher cut-off frequency for the device.

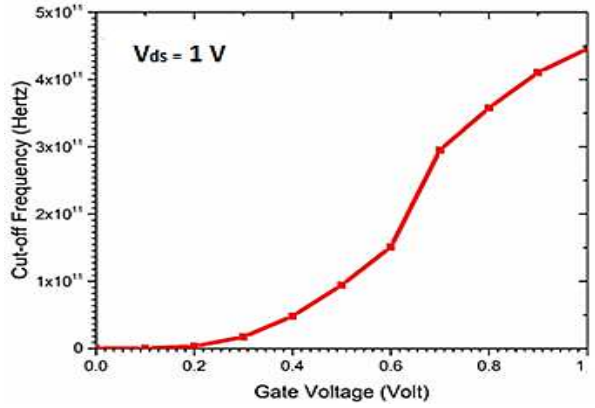

Fig. 14. Cut-off frequency curve

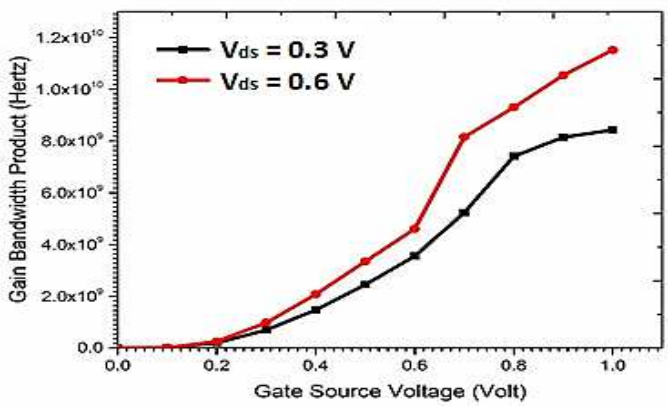

Fig. 15. Gain Bandwidth Product Plot

Fig. 14 indicates that the cut off frequency of the device lies in the Gigahertz (GHz) range. Fig. 15 demonstrates the gain-bandwidth product of the device. This parameter represents the trade-off between the bandwidth and the gain, and is calculated as follows:

$$GBP = \frac{g_m}{2\pi C_{GD} \times 10}$$
$$GBP = \frac{g_m}{20\pi C_{GD}} \quad (7)$$

The values obtained can be compared with the work of others in Table II.

TABLE II
COMPARATIVE ANALYSIS

Device Parameters	This work	Chen et al. [9]	Anand & Sarin [3]	Chander et al. [7]
ON current, $\boldsymbol{I_{ON}}$ (mA/μm)	0.537	0.081	0.0488	0.01
OFF current, $\boldsymbol{I_{OFF}}$ (fA/μm)	13	-	0.007	0.006
$\boldsymbol{SS}$ (mV/dec)	28.57	51.5	64.79	28
DIBL (mV)	3.636	-	98.22	11
Threshold voltage, $\boldsymbol{V_{TH}}$ (V)	0.256	-	0.66	0.41
Transconductance, $\boldsymbol{g_m}$(mS)	0.68	0.232	0.4	0.11
Cut-off frequency, $\boldsymbol{f_T}$(GHz)	446	11.9	≅500	7.6
Gate-Source capacitance, $\boldsymbol{C_{GS}}$ (fF)	0.387	0.7	-	0.3
Gate-Drain capacitance, $\boldsymbol{C_{GD}}$ (fF)	0.964	3.7	-	2
Gain Bandwidth Product, $\boldsymbol{GBP}$ (GHz)	126	2.3	15	0.87

IV. CONCLUSION

In this paper, the analog performance of $SiGe$ has been studied and demonstrated. The proposed device shows enhanced improvements in the parameters of the drive current, transconductance, device efficiencyg_m/I_D, gate-drain capacitance (C_{GD}), gate-source capacitance (C_{GS}), cut-off frequency (f_T), and gain-bandwidth product (GBP). The maximum I_{ON} and I_{OFF} values obtained for the device are 0.537 μA/μm and 13 fA/μm respectively, thus achieving I_{ON}/I_{OFF} ratio of around 3.72×10^{10}. The maximum transconductance value for the device is 0.68 milli Siemens/μm at the drain-source voltage, V_{DS}= 1V. The best device efficiency g_m/I_{DS} being obtained is 80.59 V^{-1}. The maximum cut-off frequency obtained for the device is around 446 GHz at the drain-source voltage, V_{DS}= 1V. For studying the high-frequency response, Miller capacitances ($C_{GS}$and C_{GD}) have been studied, and it was found that the gate-drain capacitance (C_{GD}) is the dominant factor in the Miller capacitance. The results obtained have also been compared to the existing TFET structures, and it is evident that the device shows superior performance. Therefore, it can be concluded that the proposed device can be useful for many analog and digital low power applications.

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Figures

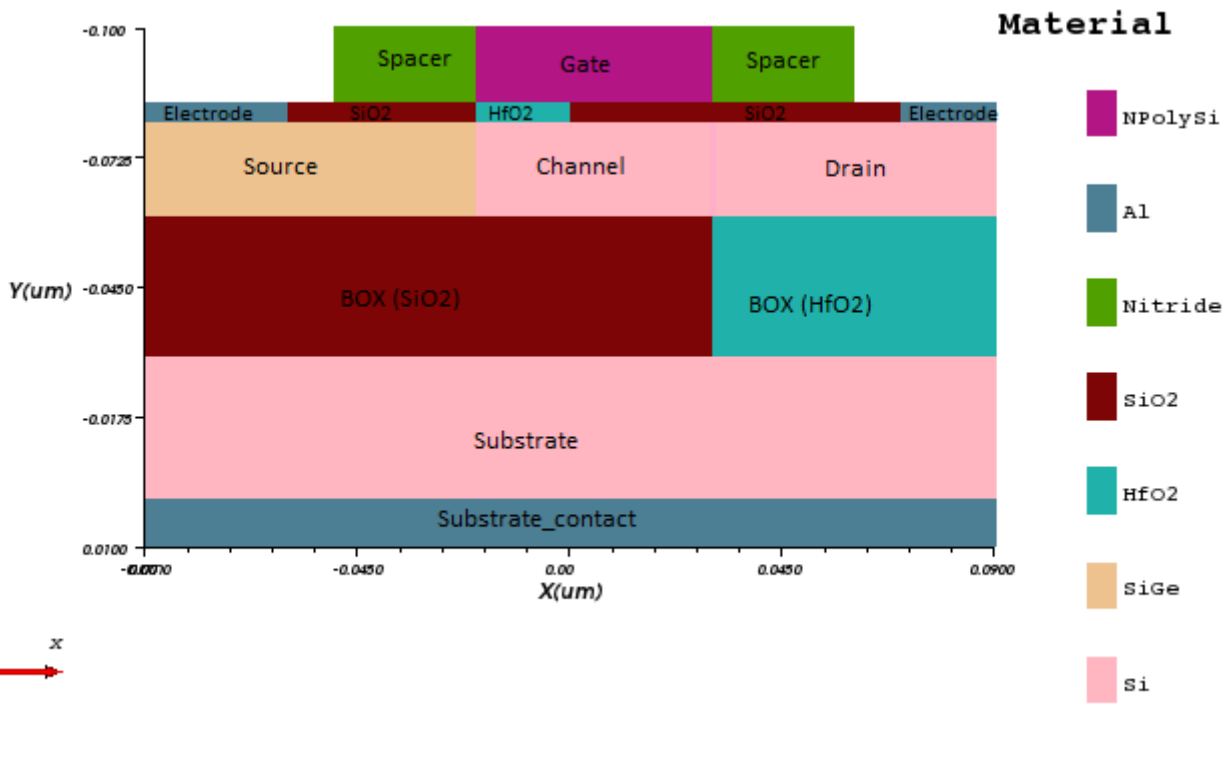

Figure 1

Proposed Device Structure

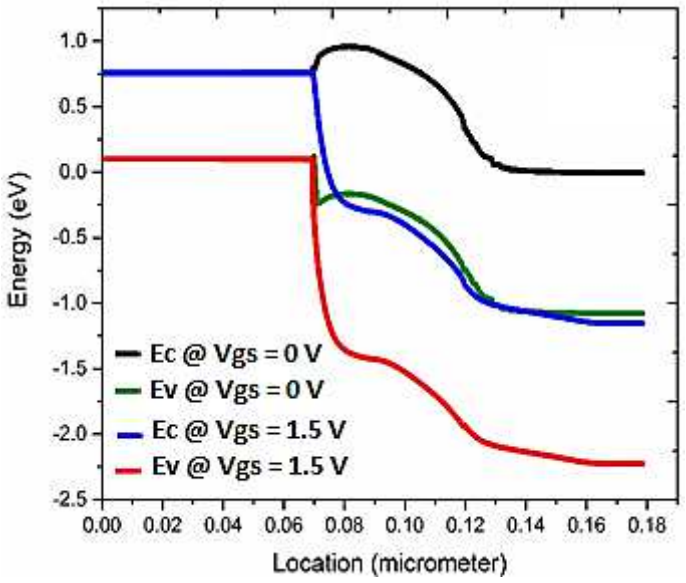

Figure 2

Energy Band Diagram for the proposed device

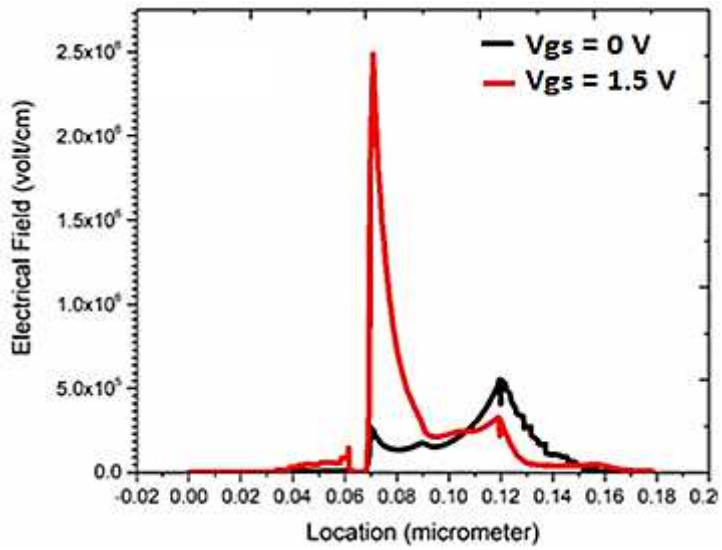

Figure 3

Electric Filed Variations at the source

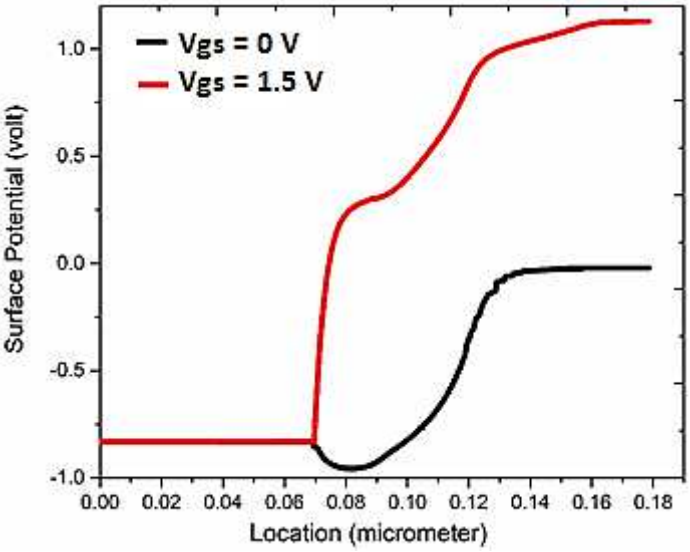

Figure 4

Surface Potential of a device

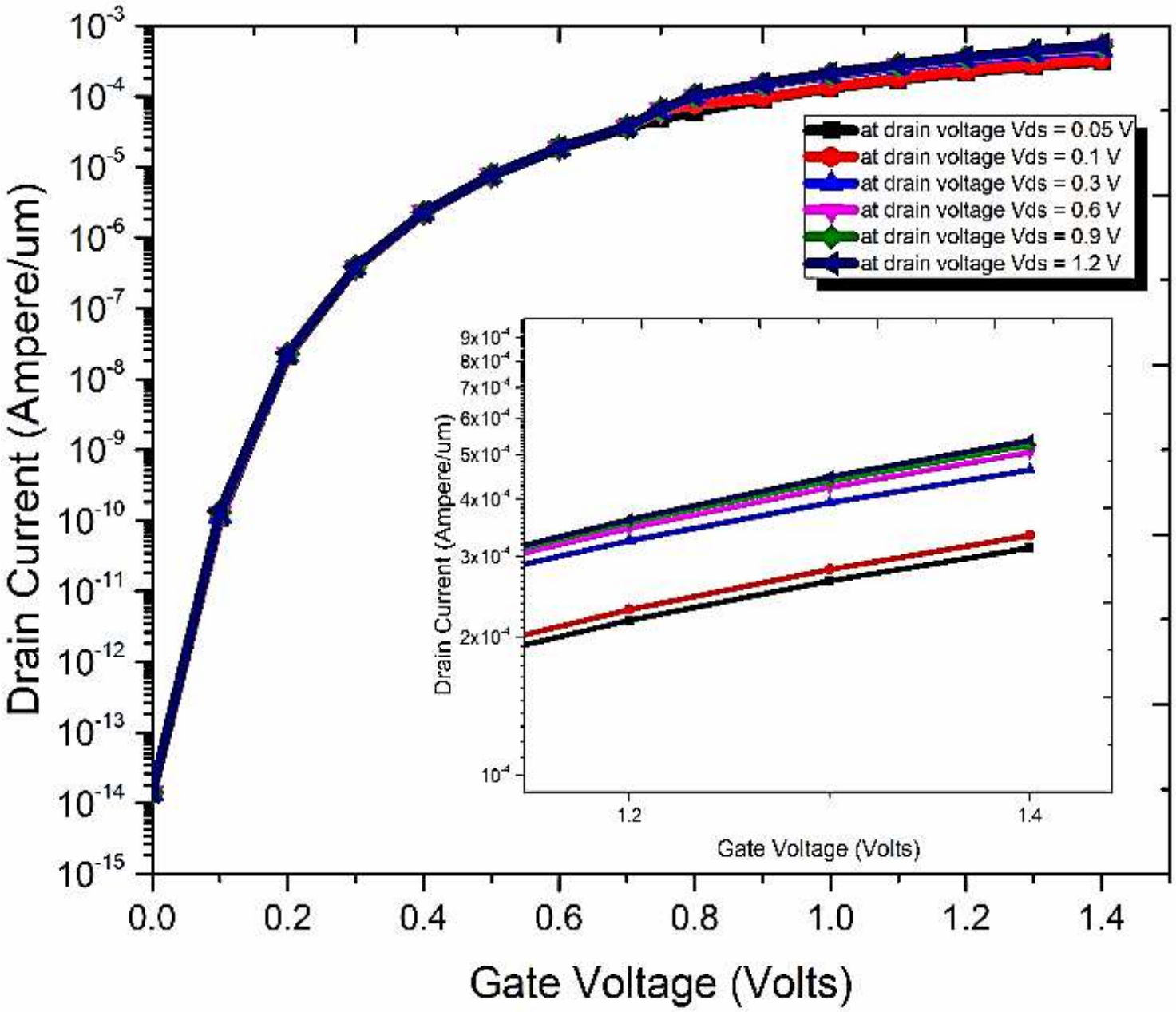

Figure 5

ID-VGS Transfer characteristics curve

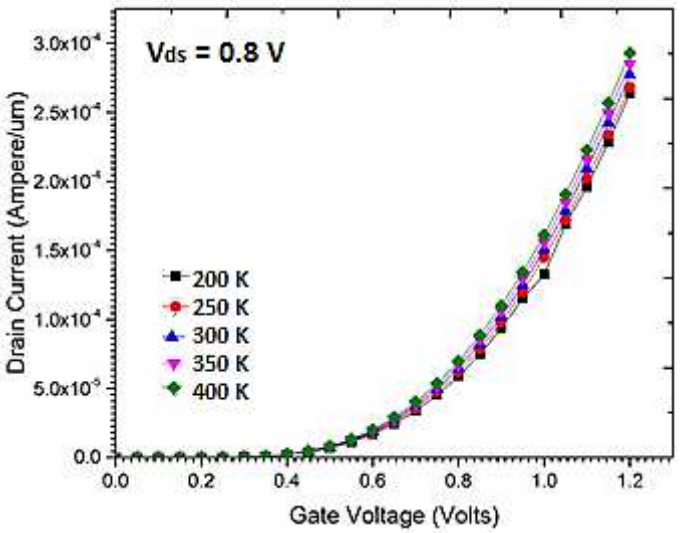

Figure 6

Temperature variations in ID-VGS Transfer characteristics curve

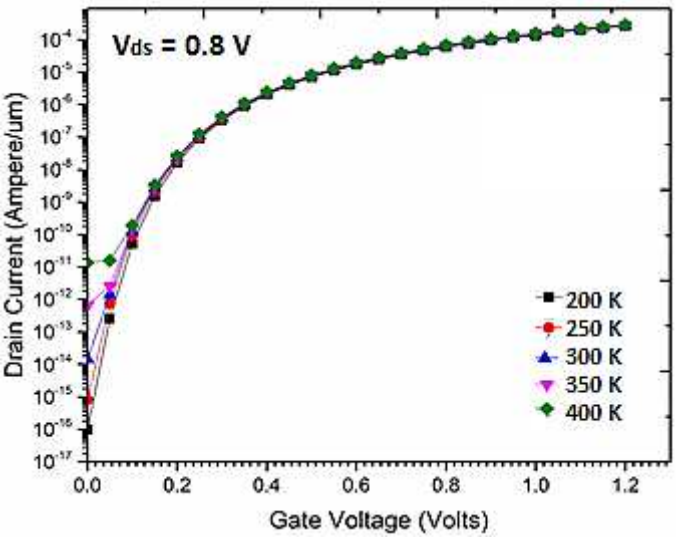

Figure 7

Temperature variations in logID-VGS Transfer characteristics curve

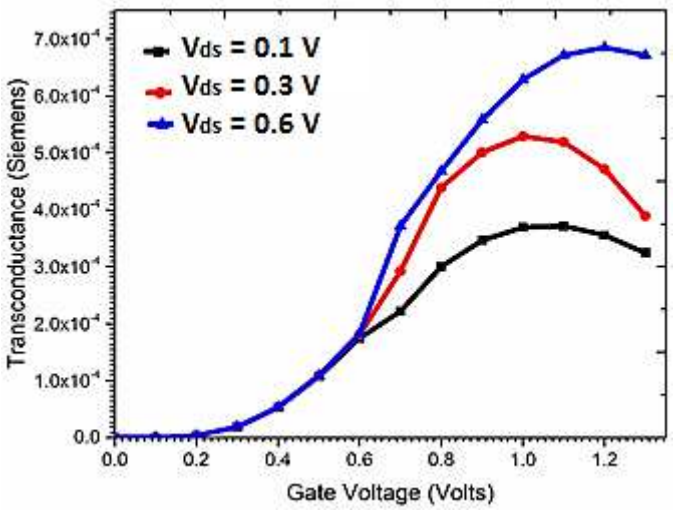

Figure 8

Transconductance vs Gate voltage curve

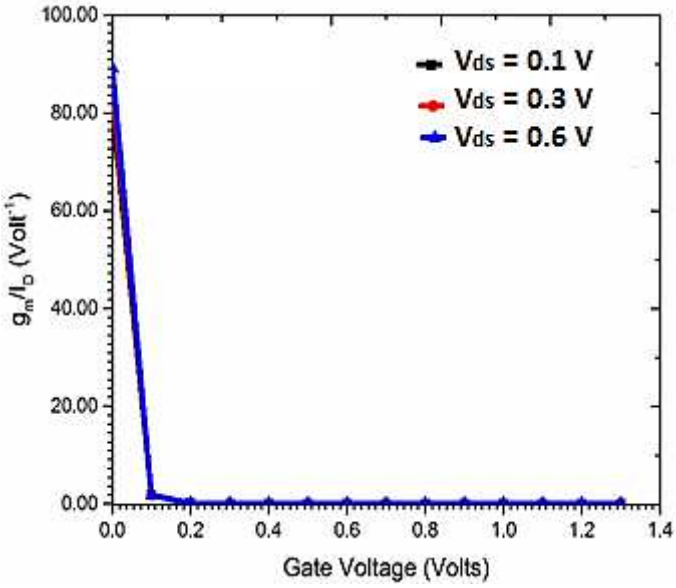

Figure 9

Device efficiency (gm/IDS) vs Gate Voltage curve

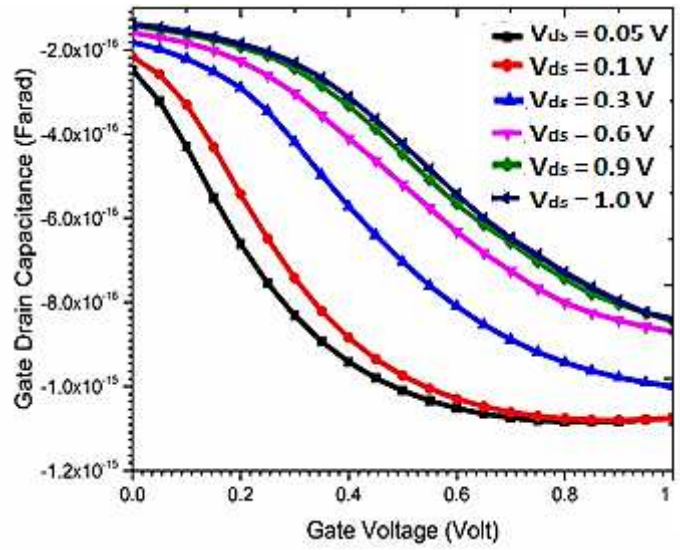

Figure 10

Gate-Drain capacitance curve

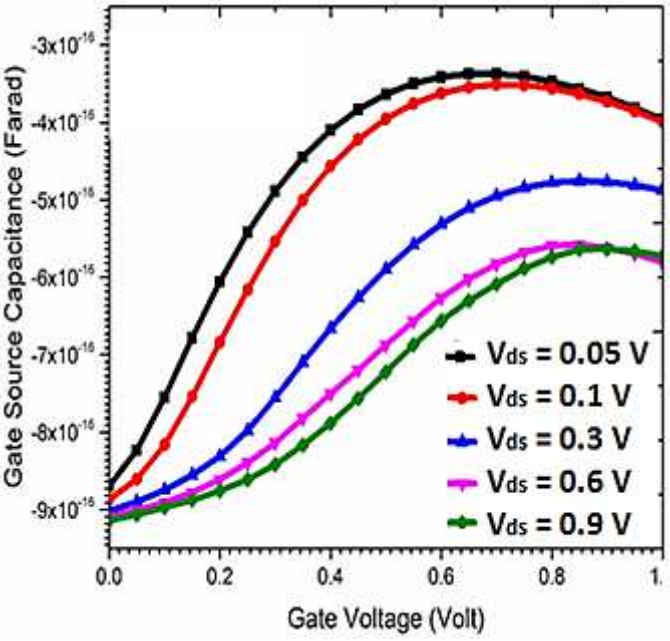

Figure 11

Gate-Source capacitance curve

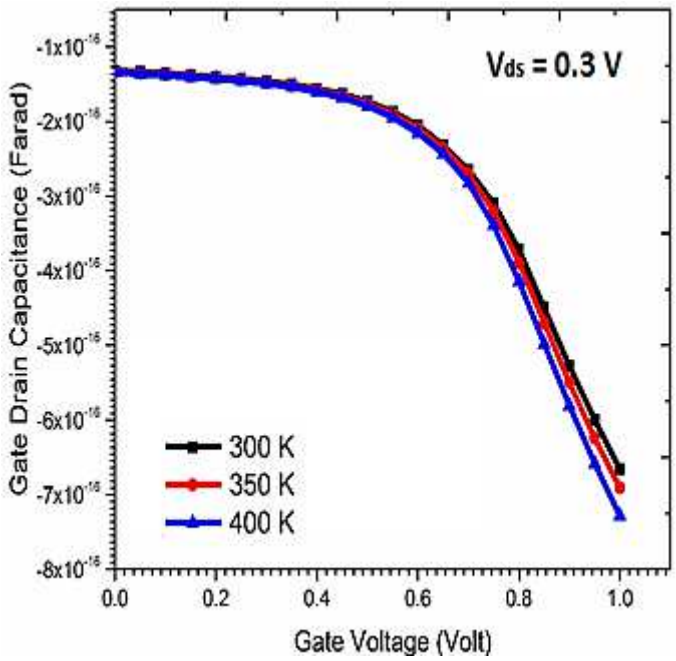

Figure 12

Temperature variations in Gate-Drain capacitance curve

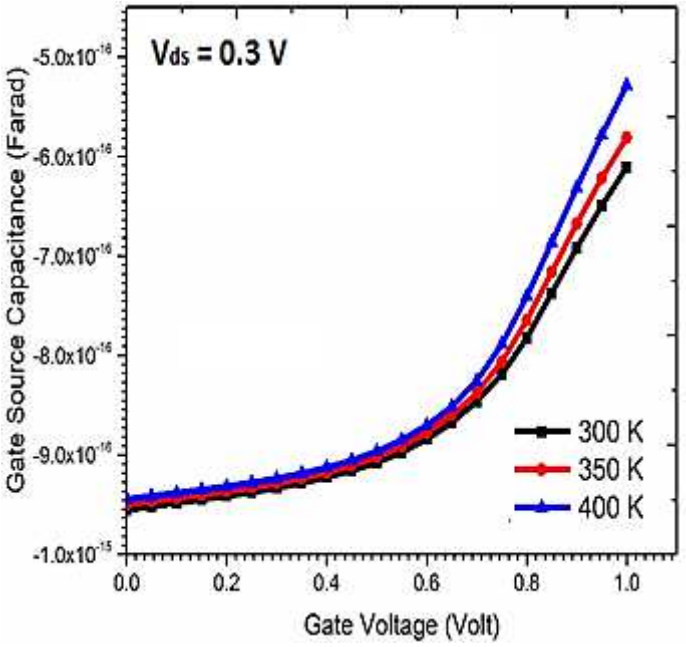

Figure 13

Temperature variations in Gate-Source capacitance curve

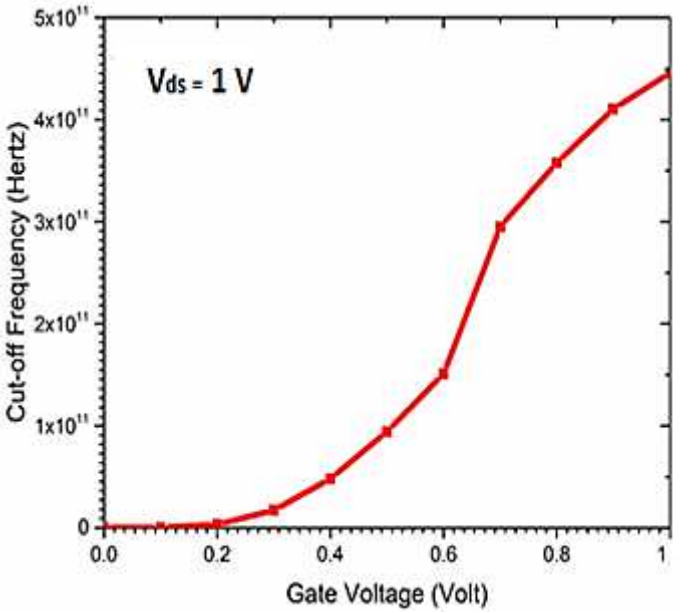

Figure 14

Cut-off frequency curve

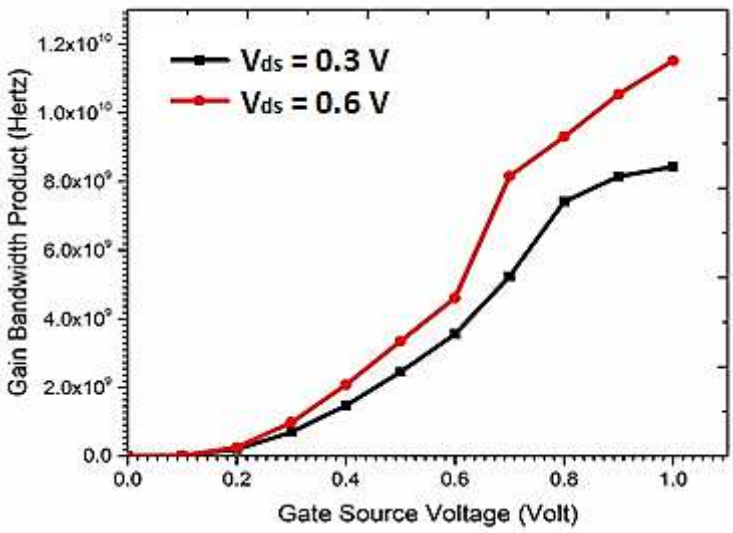

Figure 15

Gain Bandwidth Product Plot