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Research Article

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Ag Nanoparticles capped TiO₂ Nanowires Array based Capacitive Memory

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Abstract

Glancing angle deposition technique was used to fabricate Ag nanoparticles (NPs) capped TiO₂ Nanowire (NW) array structure for capacitive memory application. Electron microscopes confirmed the sandwiched structure of Ag NPs between TiO₂ thin-film (TF) and NW. The average length of the vertical TiO₂ NW and diameter of Ag NPs (with density $\sim 10^{12}$ cm²) were found to be ~ 350 nm ± 5 nm and ~ 3.2 nm ± 0.4 nm, respectively. An enhanced photoluminescence was observed in case of Ag NPs capped TiO₂ NWs due to the presence of high carriers as compared to bare TiO₂ NW. The capacitance (C) - voltage (V) hysteresis was measured for both Ag NPs capped TiO₂ NW and bare TiO₂ NW at different sweeping voltage (± 3 V to ± 10 V) at 1 MHz frequency. A high capacitive memory window of 7.12 V was obtained for Ag NP capped TiO₂ NW at ± 10 V with an excellent endurance upto 1000 cycle. Significantly lesser charge loss of 23% was obtained after a span of 10^4 s with a hole and electron loss of 10.6% and 17.8% respectively. The program and erase process in the device was explained with the help of a band diagram.

Keywords

TiO₂, nanoparticles (NPs), capacitive memory, memory window

Background

Recently metal nanoparticle (NP) (Ag, Au etc.) based non-volatile memory (NVM) have drawn much attention because of their ability of showing high non-volatile characteristics in terms of higher retention, endurance and scalability^[1]. Among the novel metal, Ag is suitable material for NP decoration due to its control growth, high thermal stability and cost-effectiveness^[2]. Interestingly, Ag with metal oxide can enhance the charge storage capability by creating Schottky contact with metal oxide i.e. TiO₂, ZnO etc.^{[1][2]}. L. Tang et. al.,

reported that Ag NP with carbon nano tube (CNT) enhanced the capacitance with better cycle stability [3]. However Ag nanoparticles easily form oxide as compared to Au which may further lead to enhancement in Schottky barrier potential (0.3 eV) between Ag and metal oxide as reported by T. Tachikawa et.al., [4]. Among the metal oxide semiconductors, TiO₂ is known as a High-K dielectric (~80) material, which allows higher scaling down of the effective oxide thickness (EOT) while increasing the performance of the device [5]. Also, high-K dielectric materials are used as a blocking oxide layer which improve capacitance with lower EOT and lower programming/erase voltage [6]. However, the leakage current has to be controlled as demonstrated by Dhar et. al., [7] on using glancing angle deposition (GLAD) technique to synthesize TiO₂ nanowire (NW) based superior MOS capacitor with a very low leakage current by increasing the offset values. Moreover, TiO₂ also shows great stability [8][9] and high performance as NVM application in comparison to other reported metal oxide NVM devices [10]. I. Salaoru et. al., have demonstrated capacitive memory using TiO₂, but significant improvement is required in terms of good retention and better memory window [11]. It is also reported that Ag NP based capacitive memory with the NPs density ranges between $\sim 10^{11}$ to 10^{12} cm⁻² can efficiently increase the charge storage capability [12], but to control its deposition is not an easy task. A. Ganguly et. al., have already demonstrated the controlled growth of Ag NP decoration over TiO₂ using GLAD technique [13]. Mondal et. al., also reported that Ag decorated TiO₂ TF enhanced the capacitive memory as compare to bare TiO₂ TF [14]. Similarly, enhanced memory window using metal NPs decorated high-k dielectric based capacitive memory was also reported [15][16] but all of the above memory needs a significant improvement.

In this paper, the authors have demonstrated how a simple modification at the tip of TiO₂ NW by depositing Ag NPs can significantly improve its charge retention capability. The Ag NPs were deposited over the TiO₂ NWs using a simple, well-controlled and cost effective technique called GLAD. The Ag NPs capped TiO₂ NW showed a very high memory window with good retention of over 10⁴ s and excellent endurance characteristics. However, no reports are so far available on the demonstration of charge trapping structure for capacitive memory applications using TiO₂/Ag NPs decorated over the tip of TiO₂ NW which can further enhance the NVM performance. This novel structure with Ag NP sandwiched in between TiO₂ NW and TF can significantly introduce intermediate states in between TiO₂ creating charge trapping centers and inject higher charges which can improve the NVM characteristics.

Methods

GLAD technique was incorporated inside the e-beam chamber (BC-300, HHV INDIA) to fabricate Ag NPs capped TiO₂ NWs over p-type Si substrate. A pictorial representation of the different fabrication process steps along with the GLAD technique are depicted in figure 1. The Si substrates were RCA cleaned, dried, and placed inside the e-beam chamber prior to the start of the deposition process. At first, TiO₂ thin-film (TF) of thickness 80 nm was deposited over Si substrate. The deposition was carried out by evaporating high purity TiO₂ source materials (99.999% pure, MTI, USA). The substrates were placed at a distance of 24 cm away from the source material. Then, TiO₂ NW of length 350 nm and diameter of 70 nm was fabricated over TiO₂ TF for which the substrate was kept at an oblique angle of 85° with respect to the source. TiO₂ NW diameter of 70 nm was chosen in order to grow Ag NPs with size (3 nm) over its tip with case having density in the range 10¹¹ to 10¹² cm⁻². The substrate was also azimuthally rotated at a constant speed of 20 rpm (The GLAD technique is shown in figure 1 (c)).

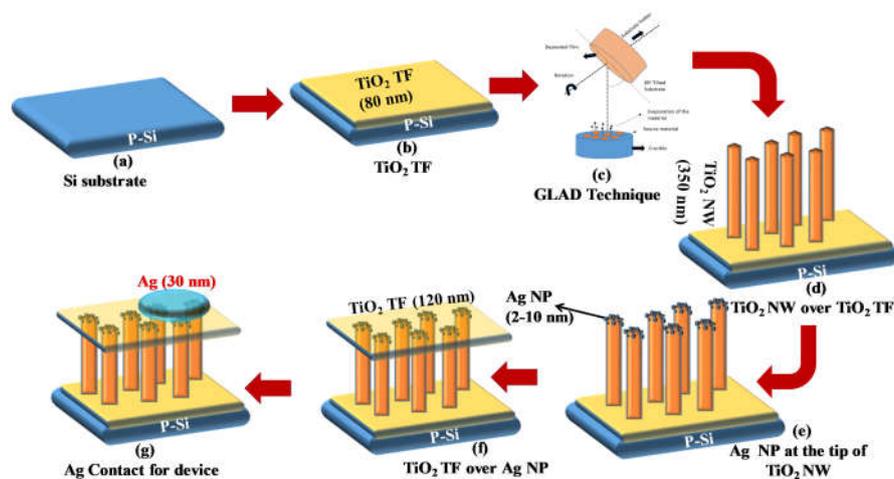


Figure 1 Fabrication process steps for Ag NPs capped TiO₂ NWs based memory device.

Thereafter, Ag NPs (~ 3 nm) were deposited over the tip of TiO₂ NWs using the same GLAD configuration i.e., the same substrate rotation and orientation as used for TiO₂ NWs. Afterwards, at the top of Ag NPs, TiO₂ TF of thickness ~ 120 nm was also deposited to form TiO₂ TF/Ag-NP/TiO₂ NW sandwiched structure. All the above depositions were carried out at a base pressure of 5×10^{-6} mbar with a constant growth rate of 0.12 nm/sec which was monitored by a quartz crystal installed inside the chamber. Later, Ag electrode of thickness 30 nm (area 1.13×10^{-6} m²) was evaporated over the TiO₂ TF to fabricate memory device. The device schematic is shown in figure 1. Another memory device without Ag NPs was also

prepared in order to compare the impact of Ag NPs over the TiO₂ NWs.

Characterization

The morphology and structure of the Ag NPs capped TiO₂ NW was studied using the field emission scanning electron microscope (FE-SEM) (Zeiss/Ultra 55) and transmission electron microscopy (TEM) (JEM 2100, JEOL) analysis. The optical characteristics were recorded using ultraviolet–visible spectroscopy (UV–Vis) (HITACHI UH4150) and photoluminescence spectroscopy (PL) (HITACHI, F-7000FL) by measuring the C-V characteristics (Keithley 4200-SCS).

Results and discussion

Figure 2 (a) shows the cross-sectional FE-SEM image of the TiO₂ TF/Ag NPs capped TiO₂ NWs/Si structure where each layers are marked accordingly. It can be seen that the TiO₂ TF of thickness ~ 80 nm is grown over the Si substrate on top of which the TiO₂ NWs are deposited. These TiO₂ NWs are perpendicularly oriented with average length of ~ 350 nm ± 5 nm. Ag NPs were then fabricated above the TiO₂ NWs, which are not visible in the FE-SEM image. As these Ag NPs decorated over the tip of TiO₂ NWs were very small in dimensions (~ 3 nm), they were completely enveloped by the TiO₂ TF (thickness ~ 120 nm) fabricated over the top of Ag NPs. Some under grown TiO₂ NWs are also visible in the FE-SEM image (marked as white dotted circles), which can be attributed to the competitive growth mode process that prevails in the fabrication (GLAD) technique [17]. The EDS spectrum (figure 2(b)) shows the emission from silicon (Si) K shell, titanium (Ti) K shell, oxygen (O₂) K shell and silver (Ag) K shell which designates the presence of Ti, O, Si and Ag elements in the fabricated sample. Figure 2 (b) inset also shows the chemical mapping of the fabricated sample.

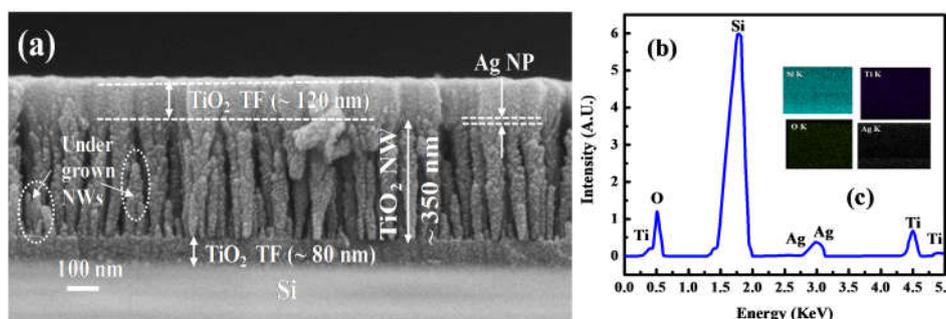


Figure 2 (a) Cross sectional FE-SEM image, and (b) EDS spectrum of Ag NPs capped TiO₂ NW with chemical mapping (inset).

Figure 3 (a) shows the TEM image that was examined on the Ag NPs capped TiO₂ single NW in order to determine the dimension of the NPs and the morphology of the grown NWs. The direction of the arrow shows the growth direction of the NW and also the length of the NW is calculated to be ~ 490 nm. The diameter of the NW is found to be 70 nm at the top and 40 nm at the bottom. The selected area electron diffraction (SAED) pattern of the NW shows that the grown NW is amorphous in nature (figure. 3 (a)). The maximized image (figure 3(a)) of the tip of the TiO₂ NWs depicts that the size of the sprinkled Ag NPs were non-uniform in nature, which may be due to the shadowing effect by GLAD technique. The average diameter of the Ag NP was measured to be ~3.2 nm ± 0.4 nm. The TEM also verifies that the NPs didn't cover the entire portion of the NWs except the tip, which was due to the shadowing effect of the GLAD technique. The pictorial representation of the shadowing mechanism is shown in figure 3(b). The incoming vapor fluxes create a shadow (dark zone in figure 3 (b)) where the fluxes cannot arrive due to the placement of oblique angle of the substrate (85°) with respect to the source. Therefore, the incoming Ag fluxes from the source could not get deposited around entire surface of the TiO₂ NW. The NP density in each NW is calculated to be 10¹² cm⁻².

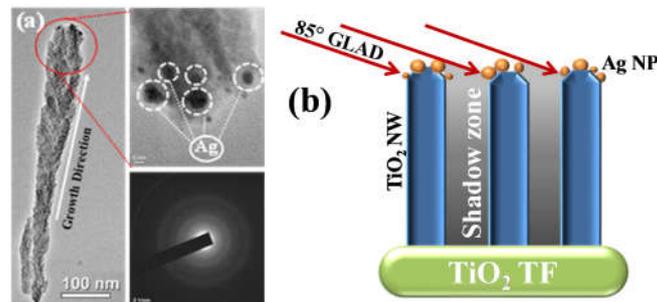


Figure 3 (a) TEM image of a single Ag NPs capped TiO₂ NW along with maximized image of the tip (with decorated Ag NPs) and SAED analysis of the TiO₂ NW (b) schematic representation of Ag NP decoration at the tip of TiO₂ NW at 85° GLAD.

Figure 4 (a) show the PL spectrum of both the Ag NPs capped TiO₂ NWs and bare TiO₂ NWs sample. The data were recorded at room temperature using a xenon lamp with an excitation wavelength of 250 nm. A higher intense PL peak was observed in the case of Ag NPs capped TiO₂ NW as compared to bare TiO₂ NW. Ag NPs capped TiO₂ NWs sample exhibit PL peak at 360 nm (3.44 eV) and 466 nm (2.67 eV). Whereas, PL emission peak for bare TiO₂ NW were found at 344 nm (3.6 eV) and 466 nm (2.67 eV). The primary PL emission peak was found at 3.6 eV for bare TiO₂ NW. This may be attributed to the direct bandgap of TiO₂ [18]. In case of Ag NPs capped TiO₂ NW the high energy PL emission peak

was found at 3.44 eV, which was slightly lower than the main band emission of TiO₂. This may be due to the presence of localized states in TiO₂ after the incorporation of Ag NPs. Moreover, PL emission peak at 466 nm was found for both the samples due to the radiative recombination on TiO₂ localized state^[19] with higher intensity for Ag capped sample due to the additional electron-hole pair generation after incorporation of Ag NP.

In order to understand this shifting of primary PL peak, tauc plot was done from the absorption measurement analysis. Figure 4 (b) shows the $(\alpha h\nu)^2$ versus $h\nu$ curve of Ag NPs capped TiO₂ NWs and bare TiO₂ NWs samples. Where α is defined as an absorption coefficient and $h\nu$ is photon energy. The extrapolation of the linear path of the curve to the $h\nu$ axis yields the band gap of the sample. The bandgap of the Ag NPs capped TiO₂ NWs and bare TiO₂ NWs samples were found to be 3.4 eV and 3.6 eV respectively. The obtained band gap of TiO₂ is in good agreement to the previously reported literature^[18]. Interestingly, Ag NPs capped TiO₂ NW sample showed a small red shift of 0.2 eV compared with the bare TiO₂ NW sample. Ag NPs can introduce some localized energy states in the band gap of TiO₂ which may give rise to absorption at lower energy and as such may reduce the band gap^[20]. Therefore, the excited photo-carriers recombine radiatively to these mid energy states and as a result a shift in PL was observed. Moreover, the higher carriers supplied from the Ag level to the TiO₂ conduction level significantly increased the PL intensity.

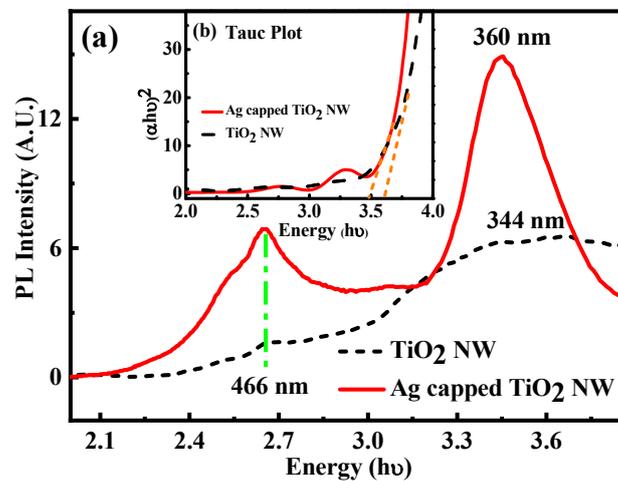


Figure 4 (a) PL emission and (b) $(\alpha h\nu)^2$ versus $(h\nu)$ curves of Ag capped TiO₂ NWs and bare TiO₂ NWs samples.

Figure 5 (a) show the C-V characteristics of Ag capped TiO₂ NW and bare TiO₂ NW device. The experimental study was carried out at room temperature at varying frequency of 10 K, 50 K, 100 K, 500 K and 1 M with applied sweeping voltage range from -10 V to +10 V. In figure 5(a), the capacitance for both the devices increases significantly with decrease in

frequency under ± 10 V applied bias. Similar characteristics of increase in capacitance with decreasing frequency were also observed by the authors [21]. Several parameters together including the series resistance, the inhomogeneous layer of semiconductor- dielectric (p-Si/TiO₂) interface defect states [22] etc. play a significant role in such observed characteristics. The accumulation capacitance was found to be 18 pF and 13 pF for Ag NPs capped TiO₂ NWs and bare TiO₂ NWs respectively at 1 MHz frequency. Ag NPs capped TiO₂ NW (figure 5(a)) shows high accumulation capacitance as compared to bare TiO₂ NW (figure 5(a) inset) device due to multi-layer charge trapping structure. The interface between TiO₂-Ag-TiO₂ acts as charge trapping layers due to incorporation of intermediate states and also the higher carriers injected after the incorporation of Ag contributes to the higher capacitance. Figure 5(b) shows the conductance versus voltage characteristics of Ag NPs capped TiO₂ NW and bare TiO₂ NW device (inset) at different voltage frequency. Ag NPs capped TiO₂ NW device shows lesser conductance value of 1.39×10^{-4} Ω^{-1} compare with the 2.34×10^{-4} Ω^{-1} for bare TiO₂ NW device under 1 MHz voltage (± 10 V) frequency. This may be attributed due to the high resistive carrier movement as a consequence of the charge trapping at the TiO₂-Ag-TiO₂ interface [14].

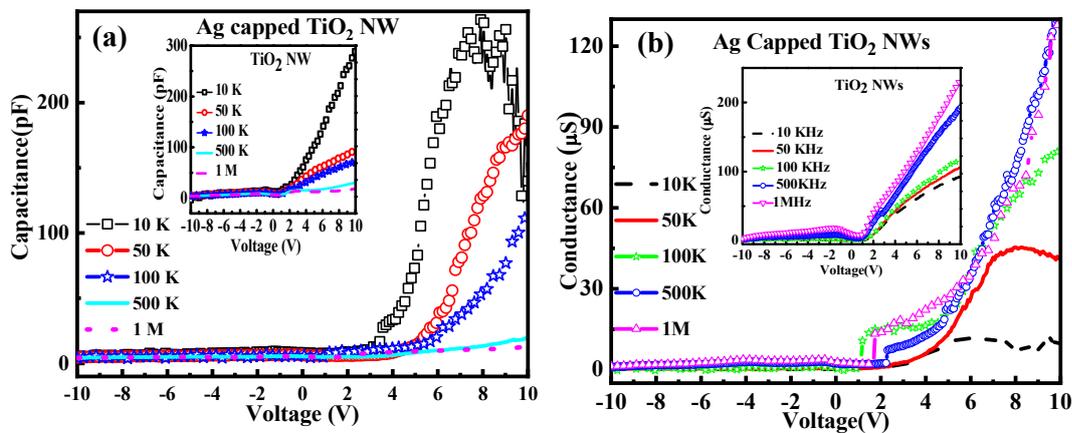


Figure 5 (a) Capacitance versus voltage characteristics and (b) conductance versus voltage characteristics at different frequency of Ag capped TiO₂ NW and bare TiO₂ NW (inset).

Figure 6(a) and (b) show the high frequency (1 MHz) C-V characteristics of the Ag NPs capped TiO₂ NW and bare TiO₂ NW based memory device respectively. The C-V hysteresis characteristics was measured by double sweeping the voltage from negative to positive and then from positive to negative. The C-V curve for Ag NPs capped TiO₂ NWs (figure 6(a)) display a significant counter clock-wise hysteresis with increase in the sweep voltage (from ± 3 V to ± 10 V), indicating the strong charge storage capability of the device. The nature of the

graph as obtained in our case is similar to other memory devices reported for TiO₂ [22]. Uncapped TiO₂ NW (figure 6(b)) shows almost a constant counter clock-wise hysteresis with increase in sweep voltage, which signifies that the charge storage/trapping capability is lacking in this case. Moreover, double hysteresis was observed for both the devices which may be due to the higher interface traps between TiO₂ and Si [23]. The flat band voltage shift (ΔV) was measured for both the positive and negative sweep for both the devices. The positive flat band voltage shift (ΔV electron) and negative flat band voltage shift (ΔV hole) for the Ag NPs capped TiO₂ NW device were calculated to be 0.81 V and 5.06 V respectively between the sweeping voltage of ± 10 V and ± 6 V. Whereas, for the same sweeping voltage, the (ΔV) electron and the (ΔV) hole for the bare TiO₂ NW device are calculated to be 0.12 V and -0.05 V respectively. This indicates that higher numbers of holes are trapped with ease in case of Ag NPs capped TiO₂ NWs device. The higher valance band offset between TiO₂ and Si (2.7 eV) as compared to the conduction band offset (0.65 eV) might be a possible reason that electrons can tunnel efficiently. The electron/hole trapping density was calculated for Ag NPs capped TiO₂ NW for the sweeping voltage shift from ± 6 V to ± 10 V using the equation (1) [24] given below.

$$N = \frac{\Delta V C_{OX}}{qA} \quad (1)$$

Where, q = electron charge, ΔV = difference of flat-band voltages, C_{OX} = oxide capacitance, and A = device area ($1.13 \times 10^{-6} \text{ m}^2$). The electron and hole trapping density was found to be $0.82 \times 10^{14} \text{ m}^{-2}$ and $5 \times 10^{14} \text{ m}^{-2}$ respectively.

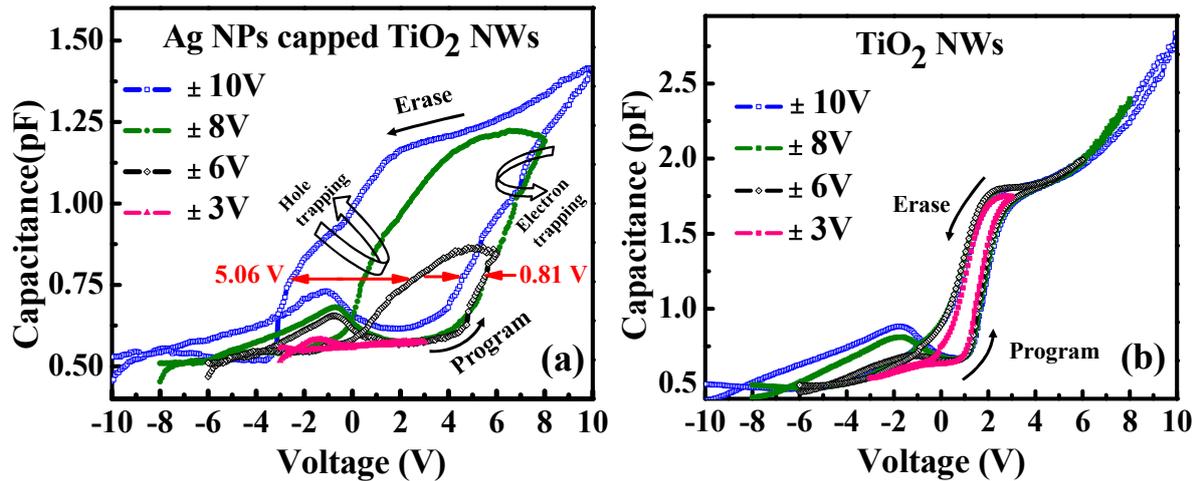


Figure 6 C-V hysteresis curve of (a) Ag NPs capped TiO₂ NWs device and (b) bare TiO₂ NW based memory device at 1 MHz frequency

The memory window versus the sweeping voltage is plotted in figure 7 (a) which clearly shows that the Ag NPs capped TiO₂ NWs had better window as compared to the bared TiO₂ NW. On increasing the sweeping voltage from ± 3 V to ± 10 V the memory window increases from 1.5 V to 2 V for TiO₂ NW and 2.5 V to 7.12 V for Ag NPs capped TiO₂ NWs. A maximum window of 7.12 V was observed for Ag NPs capped TiO₂ NW for ± 10 V sweep voltage which was higher than other high-k dielectric memory devices^[16] and also better than In doped TiO₂^[22] based memory devices. Moreover, TiO₂ NW is able to obtain a memory window of 2 V at ± 8 V, whereas the same memory window of 2 V is achieved in case of Ag NPs capped TiO₂ NW at a very low sweeping voltage of ± 3.64 V. The higher window in case of Ag NPs capped TiO₂ NWs may be ascribed to the presence of higher number of charges mainly in the Ag NPs and TiO₂/Ag/TiO₂ interface, which can act as a charge trapping multilayer interface. The band diagram for the Ag NPs capped TiO₂ NW memory device is given in figure 7 (b) (inset) showing the charge trapping phenomenon inside the device. For positive voltage sweeping (indicated by the arrow in figure 6 (a)), the electrons were injected easily from the substrate and trapped between the Ag and TiO₂ interface which acted as a trapping layer. Moreover, the TiO₂ grown using the GLAD method has already been reported to have higher oxygen vacancies^[25] that can act as shallow trap levels introducing higher energy levels within the band gap of TiO₂. Therefore, with the increase in positive voltage, there was a rise in electron trapping in Ag NPs, which were leaked through these trap levels (trap-assisted tunnelling) and collected at the electrode during the programming process. For negative sweeping, the holes stored in the Ag NPs cannot be flushed out with ease due to the higher valence band offset between the TiO₂ and Si (figure 7(b)). Therefore, with the increase in voltage, higher numbers of holes were trapped and as such higher voltage was required to perform the erasing process. This increases the negative voltage shift and as such the memory increases. Moreover, the higher Ag NPs density can increase the local electric field and also the Coulomb blockade effect for small size NPs^[15] which results in such enormous enhancement in memory window. The total charge storage density of both the Ag NPs capped TiO₂ NW and TiO₂ NW device were calculated as $7 \times 10^{14} \text{ m}^{-2}$ and $1.4 \times 10^{14} \text{ m}^{-2}$ respectively using equation (1) which indicates an obvious higher charge storage in case of Ag NPs capped TiO₂ NW device. Table 1 gives a comparison of the memory window of some recently reported metal oxide memory with our reported result.

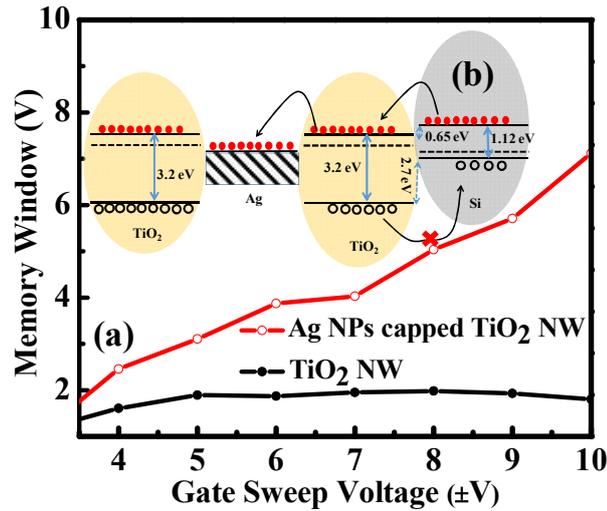


Figure 7 (a) Memory window at different sweeping voltage (b) Band diagram of Ag NP capped TiO₂ NW memory device.

Table 1: comparative table of metal oxide memory window

S. N.	Device	Memory Window	Sweeping Voltage	Reference
1.	HfO ₂ / TiO ₂ / SiO ₂	~1 V	±6 V	[26]
2.	Al/PMMA/NrGO/SiO ₂ /p-Si/Au	~3.3 V	±7 V	[27]
3.	Al ₂ O ₃ /HfO ₂ /Al ₂ O ₃	~5.4 V	±10 V	[28]
4.	Al ₂ O ₃ /SiO ₂ /Si	~1.91 V	±10 V	[29]
5.	Au/In doped TiO ₂ TF/ n-Si	~4.74 V	±8 V	[22]
6.	Ag NP/TiO ₂	~4.5 V	±10 V	[14]
7.	TiO ₂ TF/TiO ₂ NW/Ag NPs/TiO ₂ TF	~7.12 V	±10 V	(This device)

Further, the Ag NPs capped TiO₂ NW device was also tested for endurance and retention performance at room temperature. Figure 8(a) shows the retention characteristics of the Ag NPs capped TiO₂ NW device. After almost 10⁴ sec (~ 2.8 hrs.) a small loss of 23 % in memory window is observed which was calculated by using the equation reported in [30]. The hole loss of 10.6 % is lower than the electron loss of 17.8 % which can be attributed to the defects which allows for electron tunnelling. Moreover, a 40.8 % loss is predicted after a span

of 10 years, which is much lesser than other report literature ^[12]. Figure 8(b) shows the endurance characteristics of the Ag NPs capped TiO₂ NW upto 1000 program/erase cycles with respect to the flat band voltage shift. The program and erase voltages were +10 V and -10 V respectively. The Ag NPs capped TiO₂ NW device showed an excellent stable endurance characteristic upto 1000 cycles. Therefore, our device showed characteristics which can pave way for designing superior Ag/ TiO₂ TF/ Ag NP/ TiO₂ NW/ Si charge trapping structure for NVM application. Further analysis on the impact of size of Ag metal NPs is necessary to understand the exact impact of the size of metal NPs.

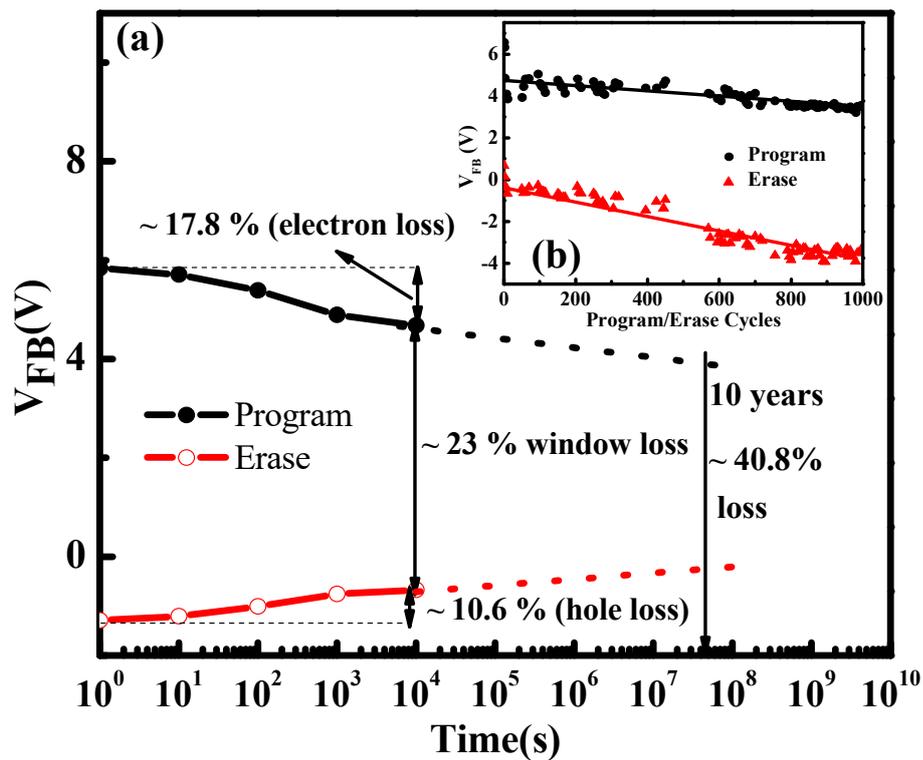


Figure 8 (a) Retention and (b) endurance (inset) of Ag NPs capped TiO₂ NWs NVM device.

Conclusions

Ag NPs was successfully deposited over the tip of the TiO₂ NWs using a controlled and cost-effective GLAD technique. The shadowing effect that prevails in GLAD prevented the Ag NPs to decorate the TiO₂ NWs entirely which was verified using TEM analysis. The Ag NPs introduced some localized energy states in the band gap of TiO₂, which might have increased both its absorption and PL intensity at lower energy level and also indicating injection of higher number of carriers. A lesser conductance value for Ag NPs capped TiO₂

NW device indicated that charge trapping was occurring at the interface between the Ag and TiO₂ (TiO₂-Ag-TiO₂ sandwiched structure). As a result of the trapping of charge carriers, a significant enhancement in C-V hysteresis was observed for Ag NPs capped TiO₂ NWs as compared to the bare TiO₂ NW NVM device. The excellent endurance and retention characteristic makes the device structure a suitable candidate for capacitive memory applications.

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Figures

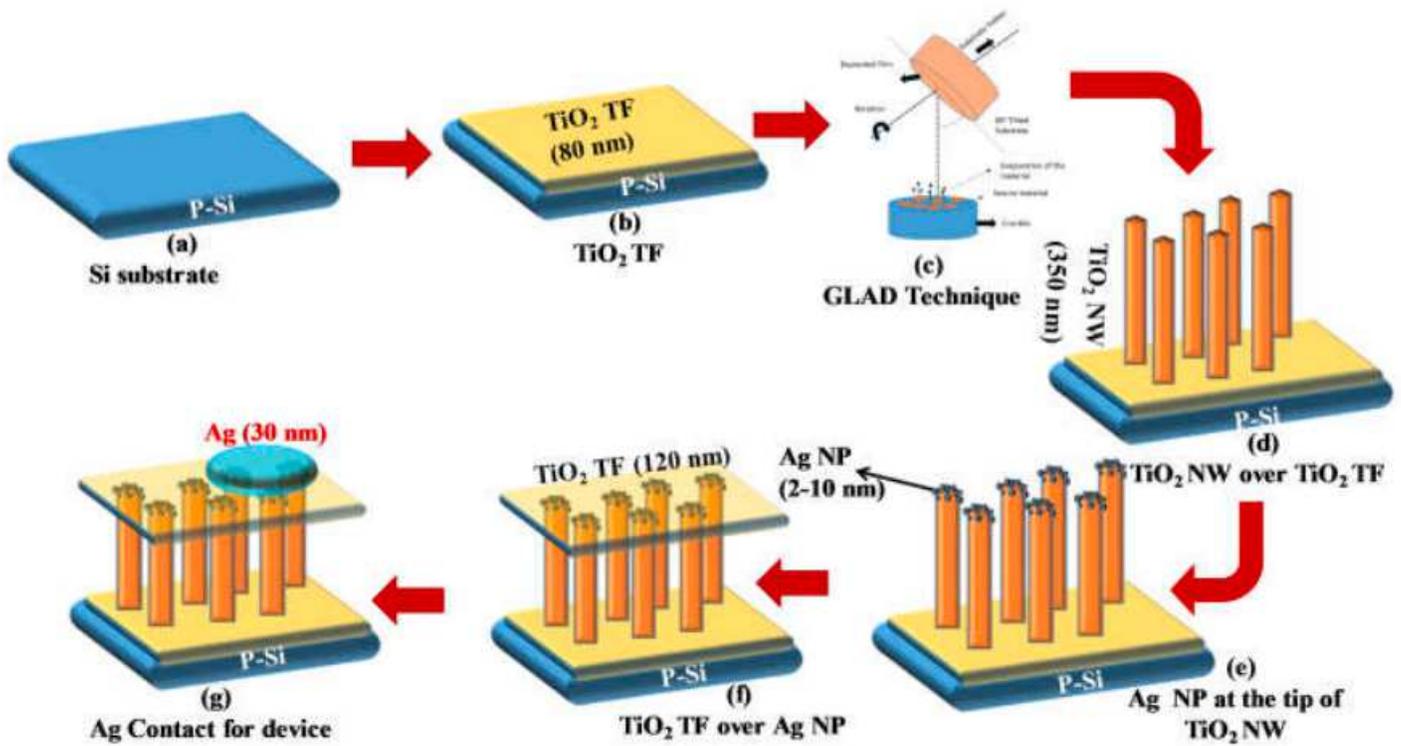


Figure 1

Fabrication process steps for Ag NPs capped TiO₂ NWs based memory device.

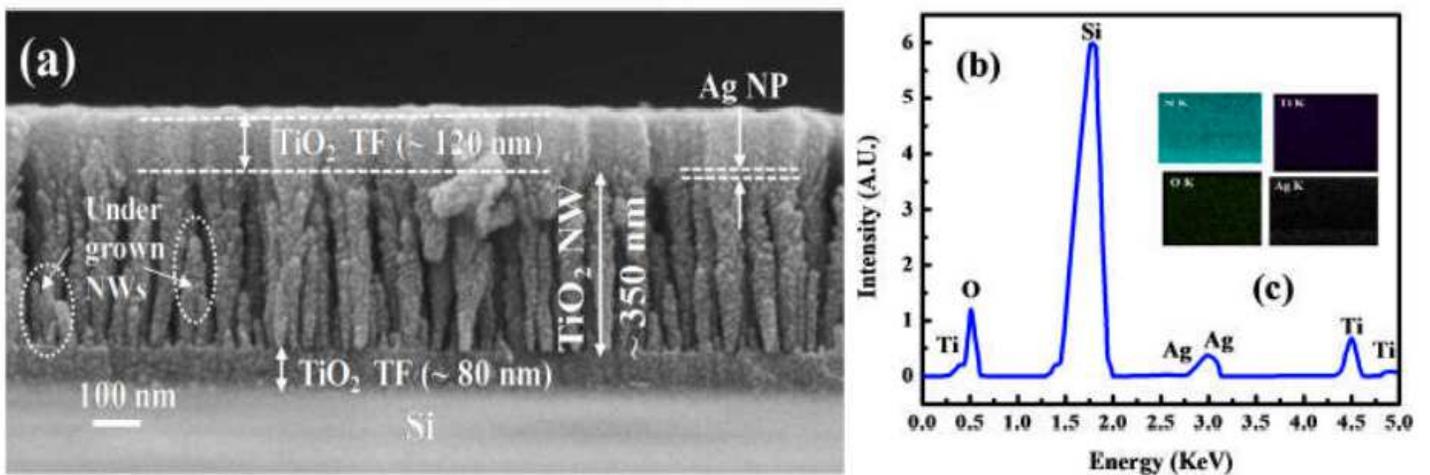


Figure 2

(a) Cross sectional FE-SEM image, and (b) EDS spectrum of Ag NPs capped TiO₂ NW with chemical mapping (inset).

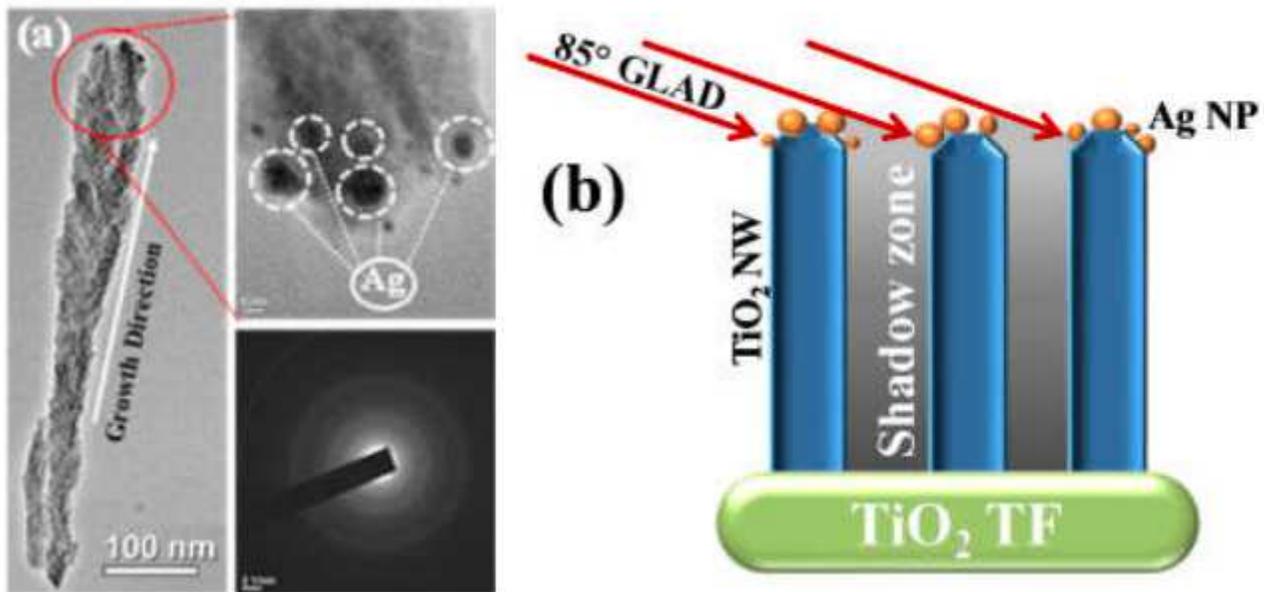


Figure 3

(a) TEM image of a single Ag NPs capped TiO₂ NW along with maximized image of the tip (with decorated Ag NPs) and SAED analysis of the TiO₂ NW (b) schematic representation of Ag NP decoration at the tip of TiO₂ NW at 85° GLAD

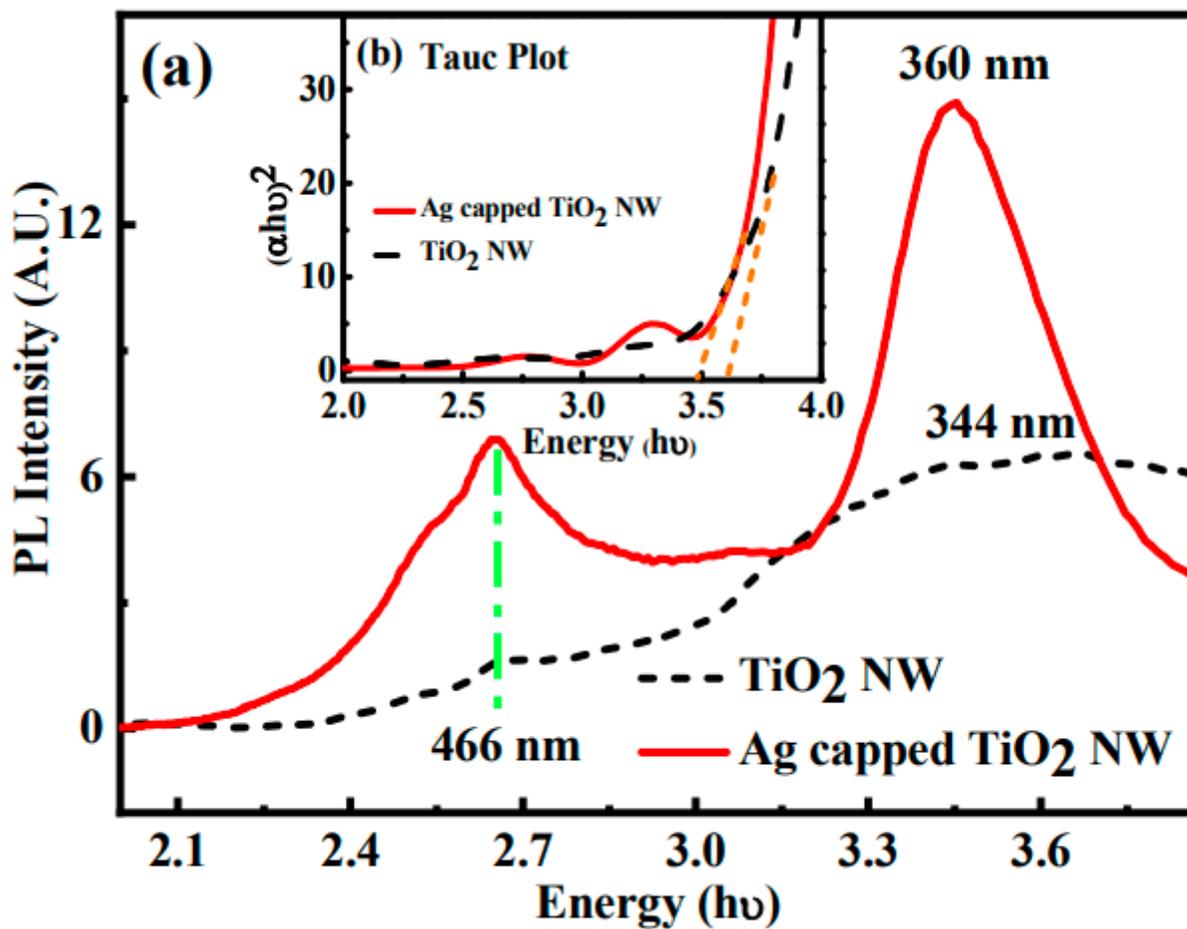


Figure 4

(a) PL emission and (b) $(ah\nu)^2$ versus $(h\nu)$ curves of Ag capped TiO₂ NWs and bare TiO₂ NWs samples

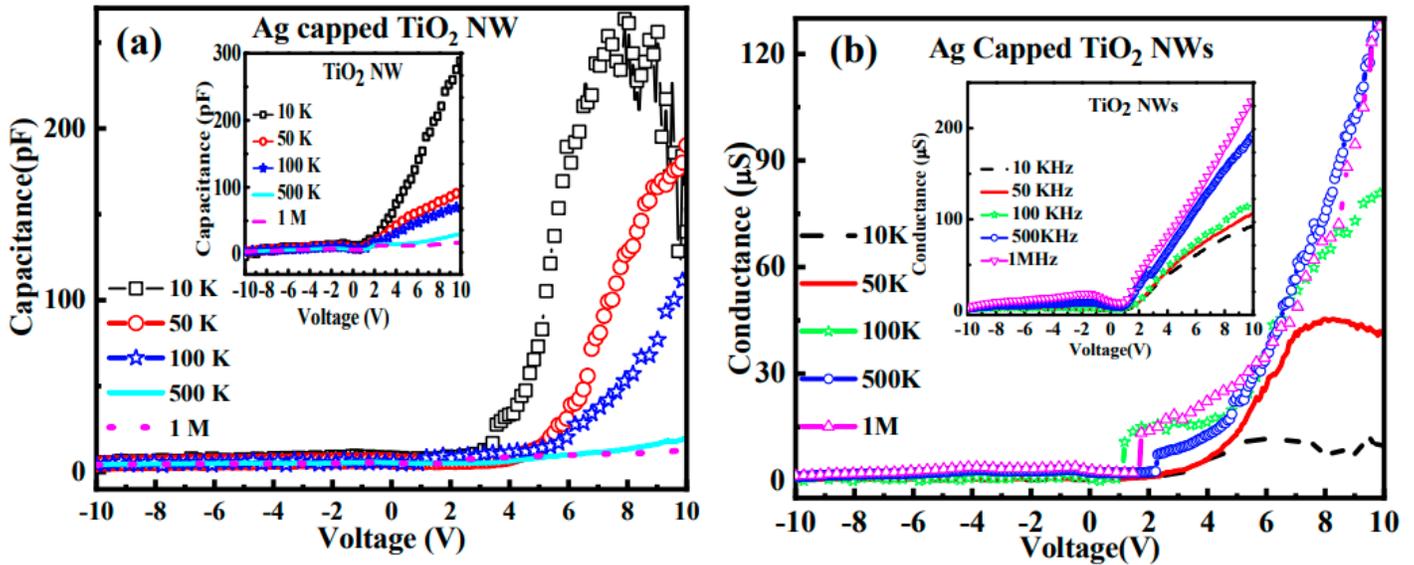


Figure 5

(a) Capacitance versus voltage characteristics and (b) conductance versus voltage characteristics at different frequency of Ag capped TiO₂ NW and bare TiO₂ NW (inset).

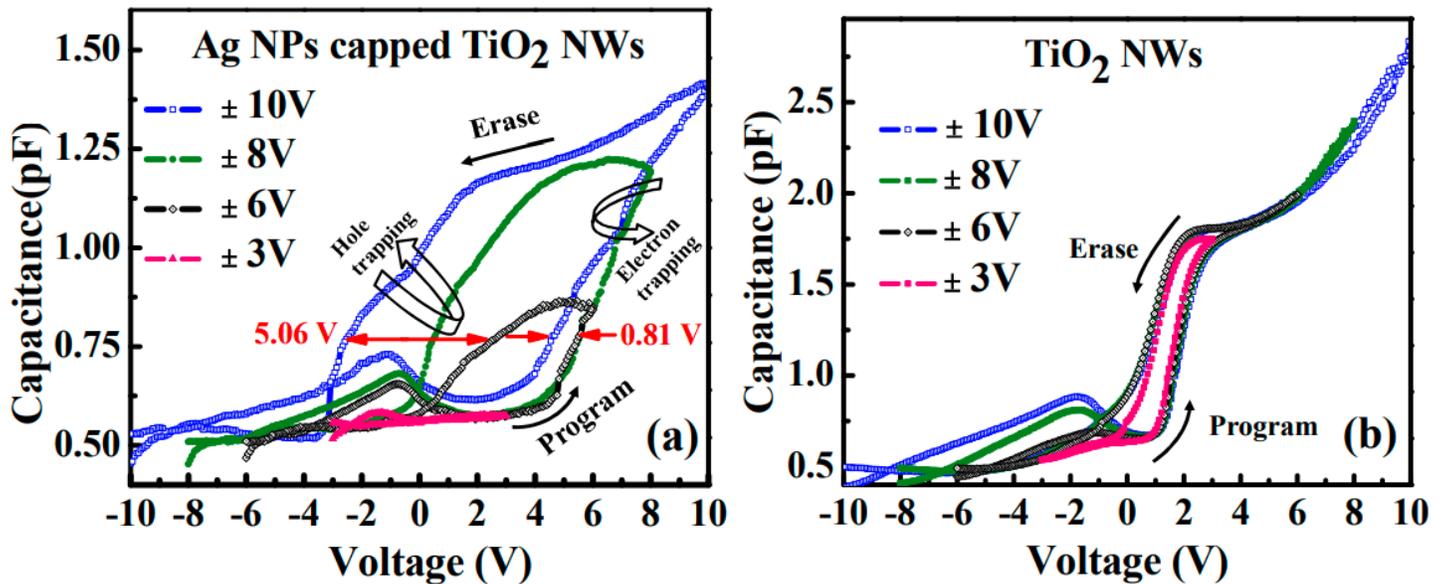


Figure 6

C-V hysteresis curve of (a) Ag NPs capped TiO₂ NWs device and (b) bare TiO₂ NW based memory device at 1 MHz frequency

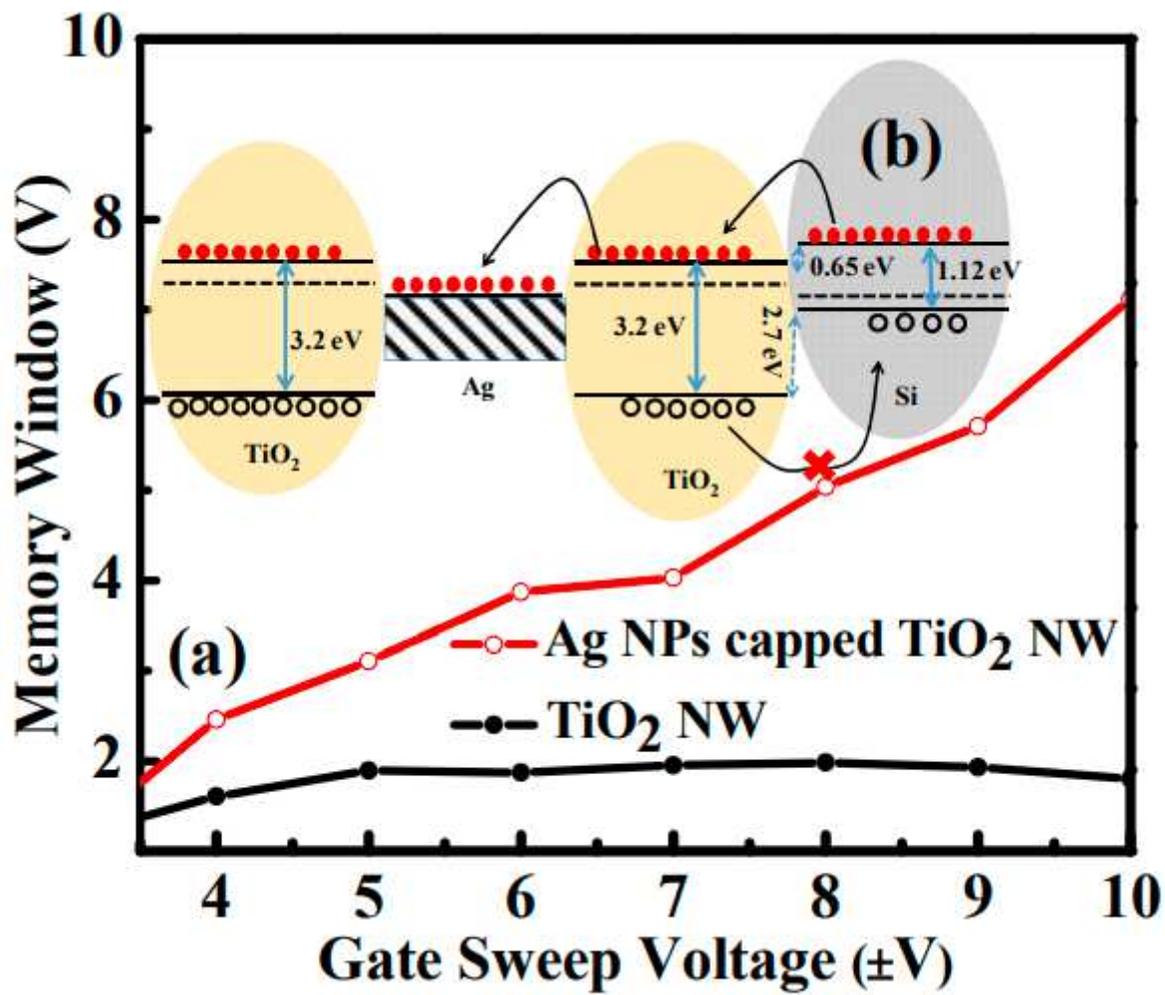


Figure 7

(a) Memory window at different sweeping voltage (b) Band diagram of Ag NP capped TiO₂ NW memory device.

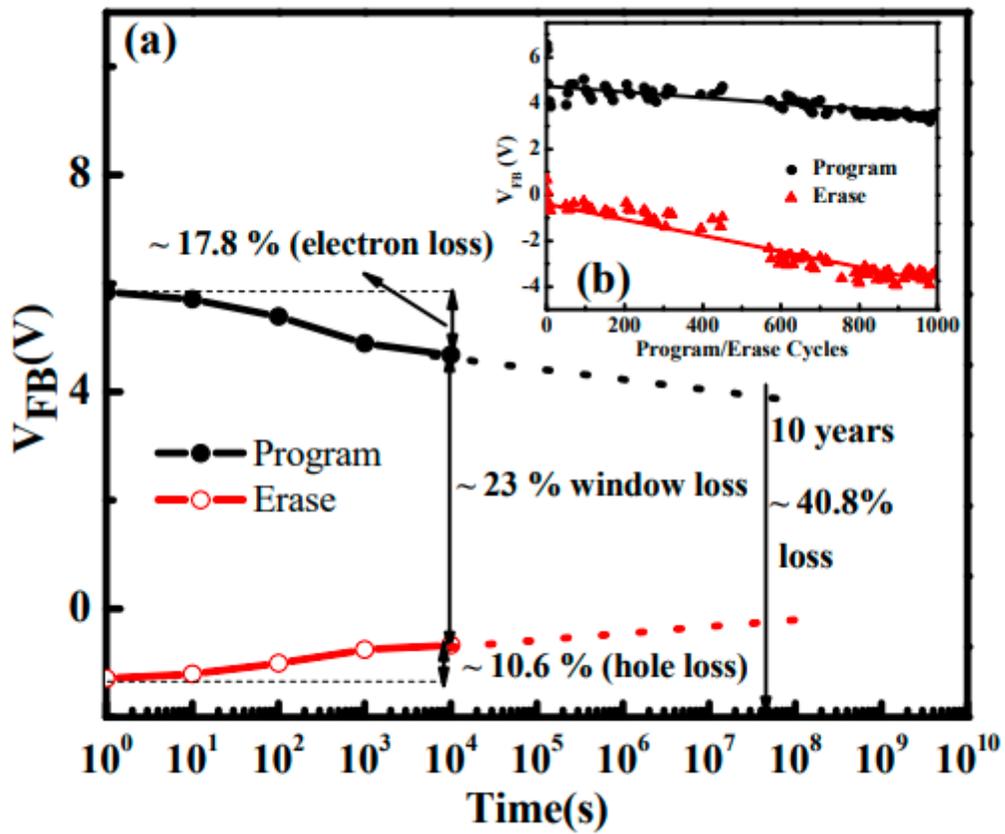


Figure 8

(a) Retention and (b) endurance (inset) of Ag NPs capped TiO₂ NWs NVM device.