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Suppressed Distortion Performance Metrics of 20nm GAA-GaN/Al_2O_3 Nanowire MOSFET: Based on Quantum Numerical Simulation

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***Abstract*—This work investigates the suppressed distortion performance metrics of gate all around (GAA) Gallium Nitride (GaN)/Al_2O_3 Nanowire (NW) n-channel MOSFET (GaNNW/Al_2O_3 MOSFET) based on quantum numerical simulations at room temperature (300 K). The simulation results show high switching ratio (≈10^9) with low subthreshold swing (67mV/decade), high QF value (4.1μS-decade/mV) of GaNNW/Al_2O_3-MOSFET in comparison to GaNNW/SiO_2 and SiNW MOSFET for V_{ds}=0.4V due to the lower permittivity of GaN and more effective mass of the electron. Furthermore, linearity and distortion performance is also examined by numerically calculating transconductance and its higher derivatives (g_{m2} and g_{m3}); voltage and current intercept point (VIP2, VIP3 and IIP3); 1-dB compression point; Harmonics distortions (HD2 and HD3) and IMD3. All these parameters show high linearity and low distortion at zero crossover point (where g_{m3}=0) in GaNNW/Al_2O_3 MOSFET. Thus, GaNNW MOSFET can be considered as a promising candidate for low power high-performance applications. In addition, effect of ambient temperature (250K-450K) on the performance of GaNNW/Al_2O_3 is studied and discussed in terms of the above mentioned metrics. It is very well exhibited that SS, I_{on}, V_{th}, and QF improved when the temperature is lowered which makes it suitable for low-temperature environments. But, linearity degrades as the temperature lowers down.**

***Index Terms*— Analog, GaNNW, Linearity, Distortions, Temperature, SiNW.**

INTRODUCTION

From the past 20 years, silicon-based MOSFETs dominate in the IC industry and are commonly used in microprocessor chips etc., due to its superior performance. But the major challenge was fabrication of such transistors successfully to accommodate on small chips. Though researchers were trying to miniaturize the device dimensions in such a way that it will not compromise device performance but the growing innovative device structures such as dual gate, recessed channel, FinFETs, omega gate have been proposed in recent years to improve electrostatic control of channel [1-3]. In addition, novel approaches have also been investigated by containing the use of different materials such as SiC [4], III-V semiconductors [5], CNT, Nanowires [6], etc for different applications. Among them, Gallium Nitride based transistors are appropriate for electronic devices due to its high cut-off frequency reaching 500 GHz, high mobility, the electric field of about 3MV/cm and high electron velocity [7, 8]. In addition,

because of its direct and wide bandgap (3.4 eV) it is widely used in optical communication since it is maintained up to high temperatures in comparison to silicon [9, 10]. Moreover, nanowire transistor is the most promising one owing to its integration with nano-devices and also due to ease in fabrication feasibility in comparison to planar silicon. It is also suitable in gate-all-around design which boosts device performance [11].

From device and circuit performance of NW transistors, it has proved that they have gained significant consideration due to its high performance and good scalability to few nm in circuits [12]. Existing methods in nano-scale fabrication techniques have shown that semiconductor nanowires may turn into a candidate for next-generation technologies. In general, GaN-based nanowire FETs are thus attractive for high-end applications such as high-power, high-speed, and high-temperature due to high surface to volume ratio [13, 14]. It has been reported in the literature that Al_2O_3 as a gate oxide is best suited for GaNNW MOSFET owing to no hysteresis (i.e., forward and backward sweep V_{th} shift of ~0.2V) in comparison to conventional SiO_2 which shows large hysteresis [8, 15]. Also, in terms of fabrication GaNNW/Al_2O_3 MOSFETs were believed to provide more stable process than SiNW/SiO_2 FETs in terms of interface traps [16, 17]. Therefore, in this paper, for the first time, analog and linearity/distortions performance of GaNNW/Al_2O_3 MOSFET is explored to find potential applications of GaNNW for ULSI technology.

Moreover, it is required to understand the temperature-dependent behaviour of MOSFET to predict accurately the circuit behaviour as ICs usually operate at high temperatures [18]. Therefore, it is looked-for a bias point that can show either zero or very less variation in drain current with temperature. This point of inflection is known as Zero temperature coefficient (ZTC) or temperature compensation point (TCP) [19, 20]. It is experimentally identified by Jeon and co-workers for SOI MOSFETs [21]. It is an important issue to address when IC operates at high temperatures especially for analog and digital applications. Therefore, temperature investigation is done to find the reliability of GaNNW/Al2O3-MOSFET for analog and linearity applications [22].

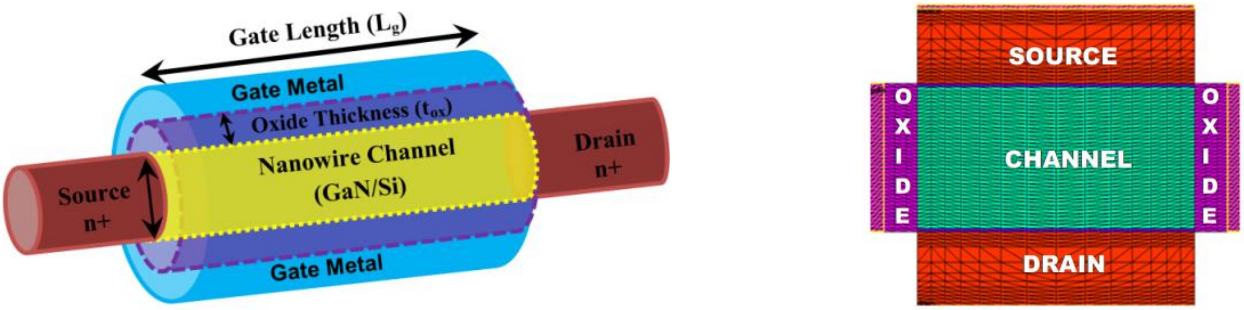
II. Device Structure and Simulation Methodology

Fig. 1 illustrates the schematic view 3D structure of cylindrical gate GaN/Si NW MOSFET and Fig. 1(b) shows the meshed structure of 2D GaNNW MOSFET. It shows that meshed lines are very fine in the channel region (area under study) and less fine in source and drain regions. Table-I shows all the key parameters of the device structure. In this work, effective oxide thickness is taken as 1.2nm for SiO_2 dielectric and 2.8nm for Al_2O_3 dielectric. The simulations of GaNNW and SiNW MOSFETs executed during this study are based on the Bohm Quantum Potential (BQP) which deals with quantum confinement inside the nanowire. Due to its better convergence and better calibration to Schrodinger-Poisson model, BQP model is chosen over the density gradient model. This model introduces a position-dependent quantum potential, QP, which is added to the Potential

Energy (V) of a given carrier type. Q_P is derived by considering the Bohm interpretation of quantum mechanics and is defined below:

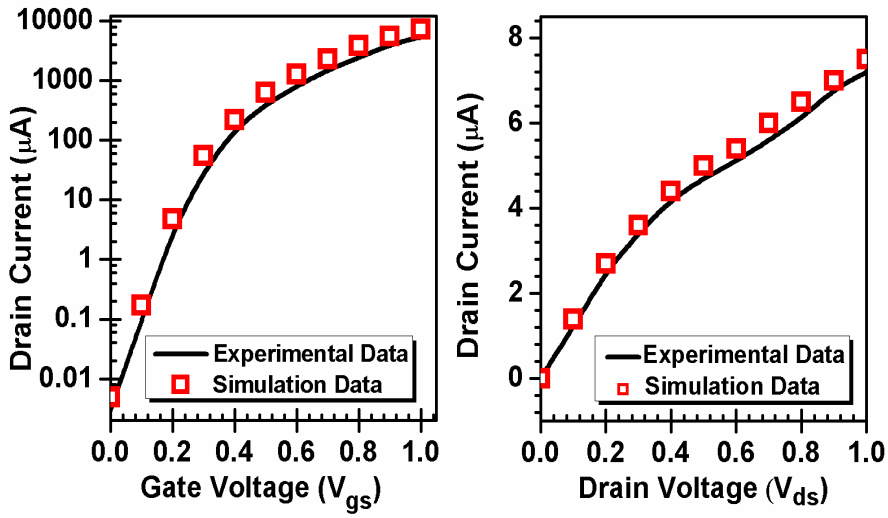
$$Q_P = \frac{-\eta^2}{2}\beta\nabla\frac{[m^{-1}\nabla(n^{\alpha})]}{n^{\alpha}} \quad ....(1)$$

where α and β are two adjustable parameters with alpha=0.5 and beta=1.2, m^{-1} is the inverse effective mass, n is the electron density and $\hbar$ is a Planck's constant. In addition, at the sub-nm range, non-local carrier heating effects become important therefore, energy balance model (EBM) is invoked along with BQP model. Physical models such as the lateral electric field-dependent mobility model, Shockley–Read–Hall recombination/generation with doping-dependent carrier lifetime are also used in this simulation.



1(a) 1(b)

Fig. 1: (a) Schematic view of simulated GAA GaN/SiNW MOSFET and (b) 2-D simulated structure of GaNNW MOSFET showing mesh lines.



2(a) 2(b)

Fig. 2 (a-b): Calibration of simulation models with experimental data.

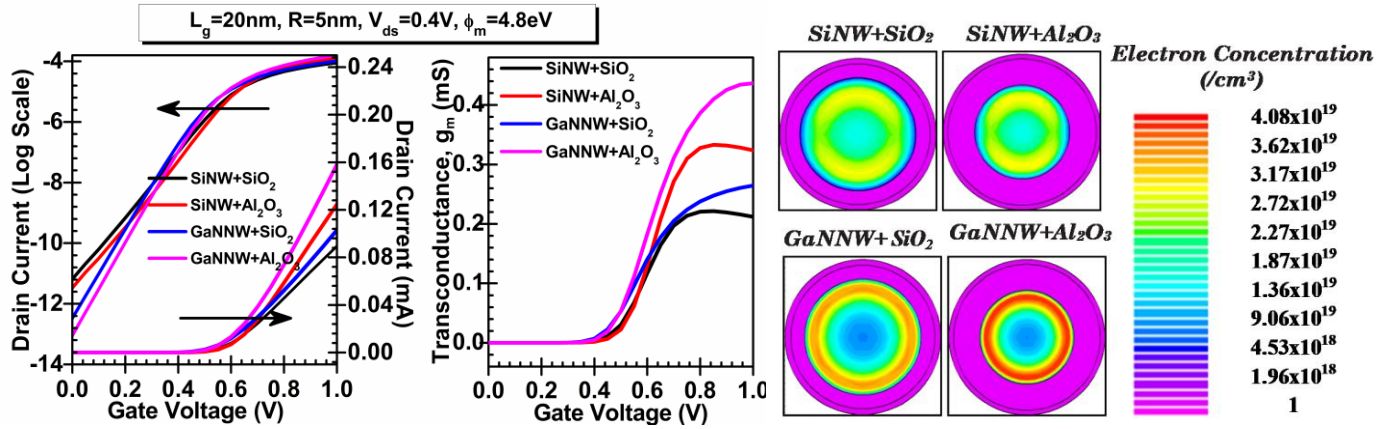
Table-I: Device Parameters

Parameter	Value
Gate Length (L_g)	20nm
Radius (R)	5nm
t_{SiO2} /t_{Al2O3}	1.2nm/2.8nm
Source/Drain Doping	1e20cm^{-3}
Channel Doping	1e16cm^{-3}
Gate Metal Workfunction	4.8eV

Fig. 2(a-b) depicts the calibrated I-V and transfer characteristics of the device. Result obtained using physical models invoked during simulations are compared with experimental data and illustrates good agreement with the experimental result thus validate the transport and physical models used during simulation

III. Results and Discussion

In this section, the performance of GaNNW/Al_2O_3 MOSFET is studied in terms of analog FOMs for low power, applications and the results are simultaneously compared with SiNW MOSFET with silicon oxide (SiO_2) and Aluminium oxide (Al_2O_3) as gate oxide material. It is evident from Fig. 3(a) that GaNNW/Al_2O_3 exhibits higher drain current in comparison to SiNW MOSFET due to the fact that GaN has optimum effective mass and relative permittivity in comparison to Si [13]. GaNNW MOSFET has large electron concentration as clearly shown in Fig. 3(c) in comparison to SiNW and concentration further enhances with Al_2O_3. Also, the integration of Al_2O_3 as a gate oxide also reduces the leakage current as reflected in Fig. 3(a) as it increases the physical gate oxide thickness and contains a lower density of interface traps in comparison to SiO_2.



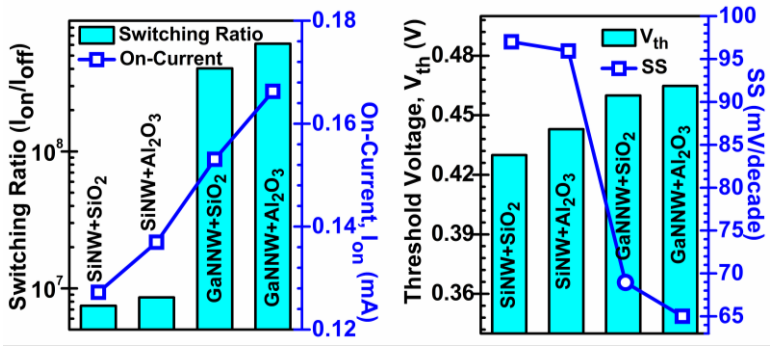
3(a) 3(b) 3(c)

Fig. 3 (a-c): (a) Variation of Drain Current with respect to gate voltage both in linear and log scale, (b) Transconductance as a function of gate voltage for four different device structures at V_{ds}=0.4V and (c) Contour plot of four different device structures at V_{ds}=0.4V, V_{gs}=1.0V showing electron concentration in the channel for Lg=20nm, t_{ox}=1.2nm, V_{ds}=0.4V and gate metal workfunction (ϕ_m) =4.8eV.

Moreover, transconductance (g_m) which is a key parameter for high-performance applications is considerably increased in

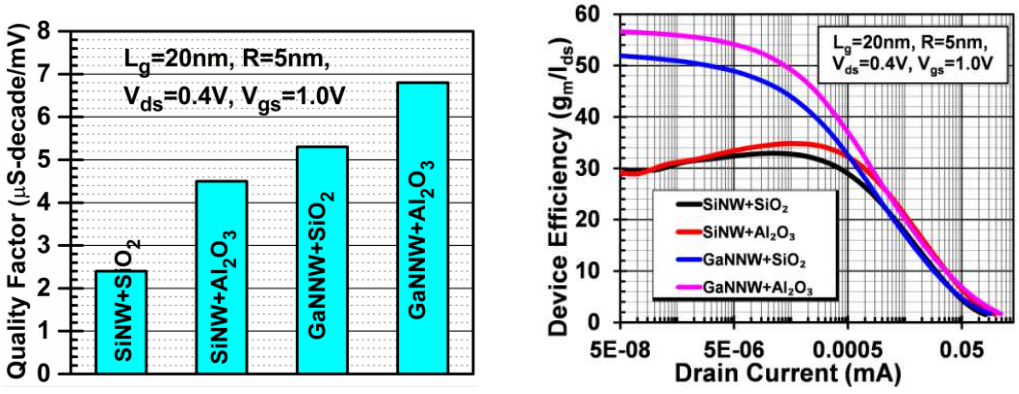
GaNNW/Al_2O_3 as in comparison to other device structures as shown in Fig. 3(b). This is due to high current driving capability as evident from Fig. 3(a). On the other hand, the switching ratio (I_{on}/I_{off}) of GaNNW is ≈10^9 in comparison to SiNW (≈1x10^7) due to high on current and low off current as reflected from Fig. 4(a). It is further enhanced by incorporating high–k oxide i.e. Al_2O_3 (k=9) which reduces the off-current considerably in comparison to SiO_2 since Al_2O_3 has a higher conduction band offset which reduces leakage current. On the other hand, the threshold voltage (V_{th}) is slightly higher in the case of GaNNW/Al_2O_3 MOSFET which is 0.46V in contrast to 0.44V for SiNW MOSFET as shown in Fig. 4(b). It is also evident from the figure that GaNNW has very steep subthreshold swing (SS) i.e., 68mV/decade because of its higher effective mass of the electron ($0.37m_0$) which reduces S/D leakage [13, 23]. With Al_2O_3 as a gate dielectric, SS further decreases to 65mV/dec which is close to ideal SS as evidently shown in Fig. 4(b).

In addition, an important parameter that determines device performance in terms of I_{on} and I_{off} is Quality Factor (QF) is depicted in Fig. 7. It is mathematically given by QF=g_m/SS [24]. QF is 2 μS-dec/mV for SiNW and 3.8 μS-dec/mV for GaNNW which is significantly improved as shown in Fig. 5(a) because of improved transconductance and reduced off current.



4(a) 4(b)

Fig. 4 (a-b): (a) Switching Ratio and on-current and (b) Threshold Voltage and Subthreshold swing for four different devices at V_{gs}=1.0V and V_{ds}=0.4V.



5(a) 5(b)

Fig. 5 (a-b): (a) Quality Factor and (b) Device Efficiency four different devices at V_{gs}=1.0V and V_{ds}=0.4V for L_g=20nm.

It further increases by 1.8 times with Al_2O_3 as gate oxide due to reduced leakage current. Device efficiency (reflected in Fig. 5(b)) which is a function of transconductance (g_m) and drain current (I_{ds}) is also higher in the case of GaNNW/Al_2O_3 MOSFET and its value is 58 V^{-1} in the subthreshold region due to lower off current which dominates over g_m unlike in linear region where g_m dominates over I_{ds}. Further, to investigate the device performance, the electric field is evaluated and presented using contour plot for SiNW with SiO_2, SiNW with Al_2O_3, GaNNW with SiO_2, and GaNNW with Al_2O_3 as reflected in Fig. 6(a-d).

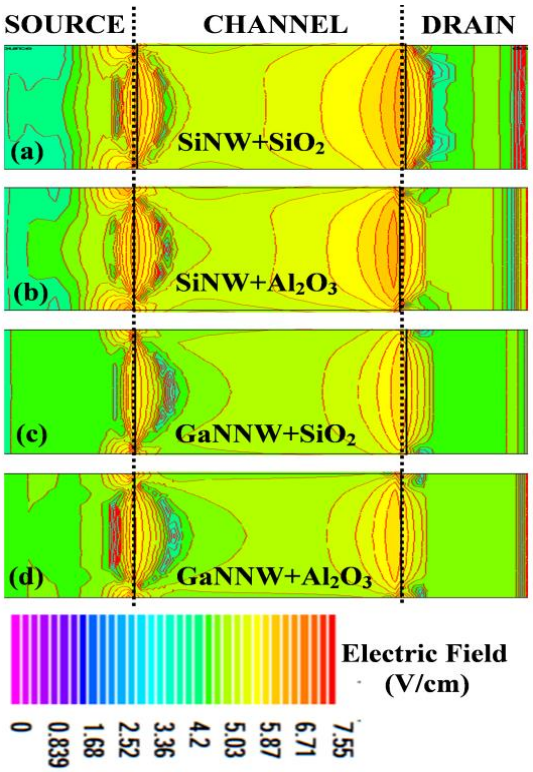


Fig. 6: Contour plot of Electric field for (a) SiNW with SiO_2 (b) SiNW with Al_2O_3 (c) GaNNW with SiO_2 and (d) GaNNW with Al_2O_3 at V_{gs}=1.0V and V_{ds}=0.4V for L_g=20nm.

From the contour plot, it is observed that the electric field is higher at the source side and lower at drain side in GaNNW device as compared to the SiNW device. The higher electric field at source side and lower electric field at the drain side leads to reduction in HCEs which also leads to low leakage current and thus improves the device performance in comparison to SiNW MOSFET.

A. Linearity Figure of Merits (FOMs)

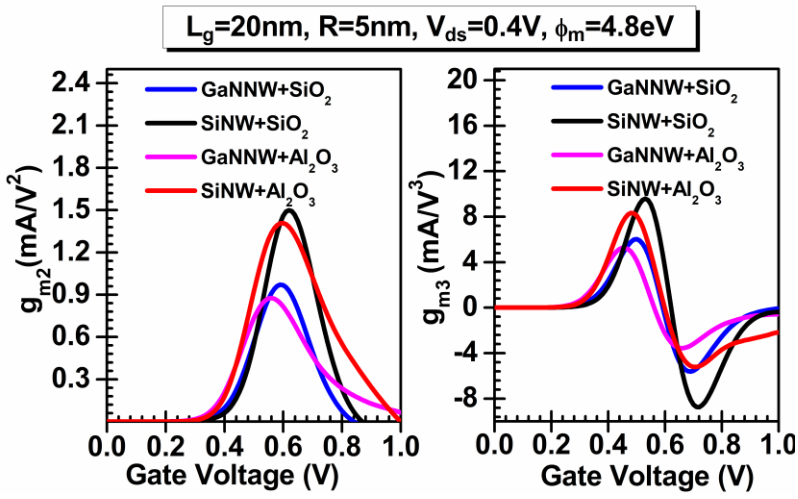
For RF amplifiers, linearity is an important constraint that must fulfill with low intermodulation distortions and high-order harmonics. The non-linearity exhibited by higher-order derivatives of transconductance (generally g_{m2} and g_{m3}), defines a lower limit on the distortion and therefore the amplitude of g_{m2} and g_{m3} should be as low as possible for enhanced linear performance

and lesser distortion. This segment evaluates the linearity and harmonic distortions of all four devices at 300K to examine the effectiveness of GaNNW/Al_2O_3 as a linear amplifier for low power IoT. High order transconductance (g_{m2} and g_{m3}) given by Eq. 2 is illustrated in Fig. 7(a-b) as a function of gate voltage

$$g_{m2} = \frac{\partial^2 I_{ds}}{\partial V_{gs}^{\ 2}} \quad ; \quad g_{m3} = \frac{\partial^3 I_{ds}}{\partial V_{gs}^{\ 3}} \qquad \ldots. (2)$$

It is found that amplitudes of both g_{m2} and g_{m3} are lower in the case of GaNNW in comparison to SiNW which shows lower distortion and high linearity. The value of gate voltage at which the g_{m3} becomes zero is known as zero crossover point (ZCP) [25], indicates at which DC bias point device can operate high linearity with low distortions. And by setting DC bias point close to V_{th}, higher gain can be realized. It is found that ZCP is 0.56V and 0.62V for GaNNW and SiNW respectively as shown in Fig. 7(b).

The metrics used to determine linearity are VIP2 and VIP3 which signify extrapolated input gate voltage at which 2nd and 3rd order harmonics of drain current respectively become equal to 1st order harmonics of drain current. It is given by Eq. 3 and 4 [26]. Fig.8 (a) shows the variation of VIP2 as a function of gate voltage and it is evident from the graph that VIP2 increases with an increase in gate voltage and attains maximum value for GaNNW/Al_2O_3 MOSFET in comparison to SiNW due to the higher value of transconductance (g_m) and comparatively lower value of g_{m2} according to Eq. 3.



7(a) 7(b)

Fig. 7(a-b): High order transconductance g_{m2} and g_{m3} as a function of gate voltage at V_{ds}=0.4V

$$VIP2 = \frac{4 \times g_{m1}}{g_{m2}} \qquad \ldots (3)$$

$$VIP3 = \sqrt{\frac{24 \times g_{m1}}{g_{m3}}} \quad \ldots (4)$$

The peak value of VIP3 reveals the cancellation of the third-order nonlinearity coefficient by device internal feedback around second-order nonlinearity. Thus, the higher the VIP3 value more linear the device and given by Eq. (4). Fig.8 (b) shows that there are two peaks observed in VIP3 one at g_{m3}=0 (lower bias point) and the other at saturation voltage. Here, linearity is examined at g_{m3}=0 (moderate inversion region) instead of high voltage at which power dissipation is more which is desired for analog applications in ULSI. It is found that the peak value of VIP3 is increasing from 0.7 to 1.7 dBm from SiNW to GaNNW MOSFET respectively. This increase is due to the higher effective mass of GaN ($0.37m_0$) in comparison to silicon which therefore improves the transconductance and thus linearity in the inversion region.

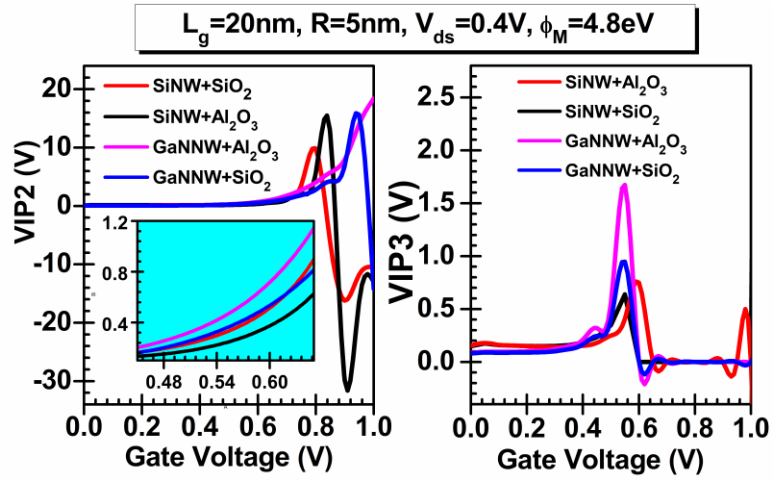
Further, IIP3 and 1-dB compression are two significant FOMs that govern the amplifier's efficiency and linearity in ICs [25]. IIP3 is defined as the intercept point at which the third-order harmonics output signal amplitudes equal the input power. Mathematically, it is given by Eq. 5. Again for better device linearity, it is required that IIP3 should be large. It is evidently shown in Fig. 9(a) that the peak value of IIP3 is higher in case of GaNNW/Al_2O_3 in comparison to SiNW/SiO_2 and SiNW/Al_2O_3. This is due to the higher value of transconductance as compared to g_{m3} [see Fig. 7(b)].

$$IIP3 = \frac{2 \times g_{m1}}{3 \times g_{m3} \times R_s} \quad \ldots (5)$$

$$1-\text{dB Compression Point} = 0.22 \times \sqrt{\left(\frac{g_{m1}}{g_{m3}}\right)} \quad \ldots (6)$$

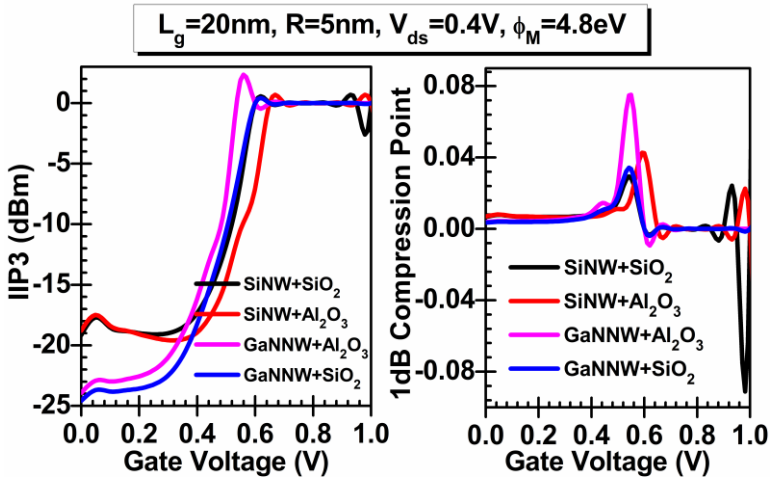
Where R_s=50ohm.

Moreover, an input power that causes the gain to fall 1dB from the normal gain is defined by 1dB Compression Point and given by Eq. (6). It is that point at which if input level restricts then distortions can be minimized and if input power exceeds the compression point then gain starts decreasing due to distortions.



8(a) 8(b)

Fig.8 (a-b): Second order (VIP2) and third order (VIP3) Voltage Intercept Point of of SiNW and GaNNW MOSFET at V_{ds}=0.4V for L_g=20nm.



9(a) 9(b)

Fig. 9 (a-b): IIP3 and 1 dB compression point of SiNW and GaNNW MOSFET at V_{ds}=0.4V for L_g=20nm.

Therefore, it is required that its value should be as high as possible for highly linear applications. It is very well depicted in Fig. 9(b) that the peak value of IIP3 at g_{m3}=0 is 0.073dB which is higher in comparison to SiNW (0.039dB) due to reduced high order harmonics (g_{m2} and g_{m3}).

B. Distortion Figure of Merits (FOMs)

For a linear amplifier, it is required that the device should possess low distortion at the output. In analog and RF applications, distortions are an important issue arises owing to the nonlinear performance of the device as they generate components whose frequency different from the input frequency. These unwanted components interfere with the desired band of frequencies and

thus degrades the signal strength. As done in our previous works [27], contrary to Fourier based methods, distortion has been evaluated using an integral function method (IFM) as this considers DC measurements instead of AC characterization. The following evaluated analytical expressions are listed as Eq. (7-9):

$$IMD3 = \left(0.45 \times \left(VIP3\right)^2 \times g_{m3}\right)^2 \times R_S \quad \text{.... (7)}$$

$$HD2 = 0.5V_a \frac{\left(\frac{dg_m}{dV_{gs}}\right)}{2g_m} \quad \text{.... (8)}$$

$$HD3 = 0.25V_a^2 \frac{\left(\frac{d^2 g_m}{dV^2_{gs}}\right)}{6g_m} \quad \text{.... (9)}$$

Where R_s=50ohm, and V_a=0.05V

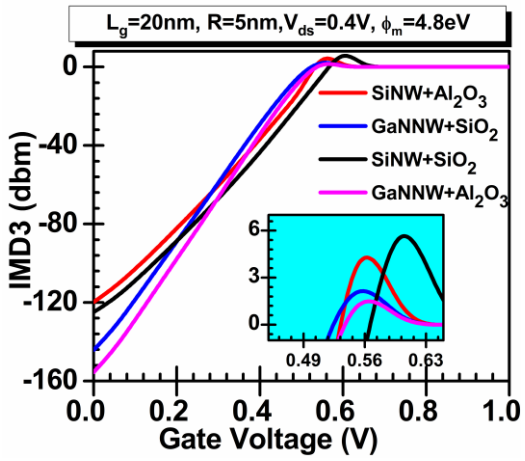
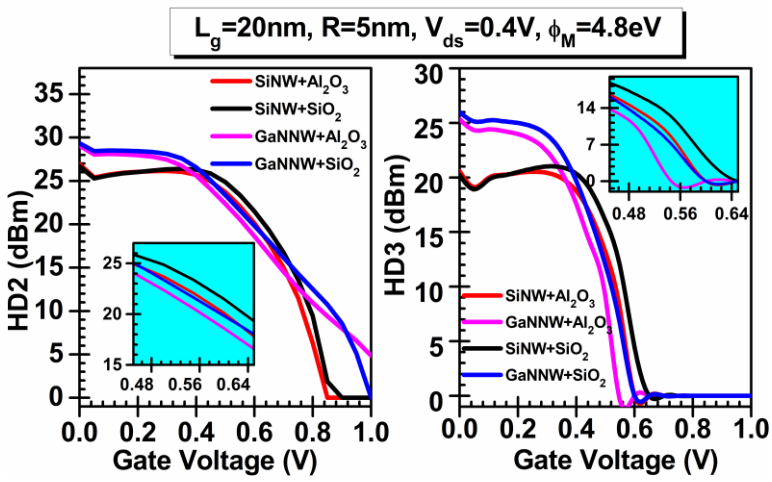


Fig. 10: IMD3 of SiNW and GaNNW MOSFET at V_{ds}=0.4V for L_g=20nm.



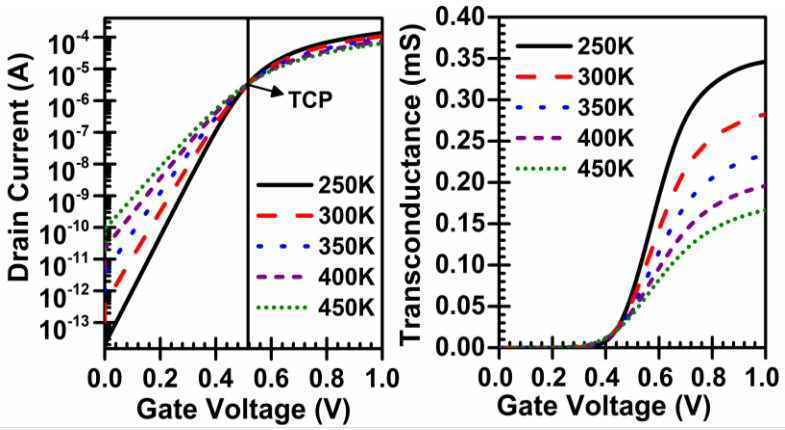
11(a) 11(b)

Fig. 11 (a-b): HD2 and HD3 of Si and GaNNW MOSFET at Vds=0.4V for Lg=20nm

IMD3 as a function of gate voltage is shown in Fig.10. It is the third-order intermodulation distortion in terms of current at which the first and third-order harmonic currents are equal. Its value must be small for keeping lower distortions. It is found from the inset graph of Fig. 10 that the peak value of IMD3 is comparatively lesser in GaNNW in comparison to SiNW. This decrement is further with Al_2O_3 as reflected in Fig. 10. This is due to the high value of VIP3, which dominates over g_{m3}. Thus, it will affect the RF transceivers by enhancing the system overall performance and reducing distortions. In addition, HD2 and HD3 the second and third-order harmonic distortions respectively are also analyzed and found that their value reduces with an increase in gate voltage as perceived from Fig. 11(a-b). This is due to improved transconductance and reduced higher-order transconductance for GaNNW/Al_2O_3 in comparison to SiNW as reflected in Fig. 7(a-b). Thus, signifying that GaNNW/Al_2O_3 is more linear with fewer distortions than SiNW and GaNNW/SiO_2.

C. Impact of Temperature

In order to investigate the issue of device reliability, GaNNW/Al_2O_3 is examined under different ambient temperatures (250K-450K) in terms of analog and linearity FOMs. It is found that off current is reduces with decrease in temperature or in other words, drain current is increases with rise in temperature till ~0.5V. After this point, current starts decreases with rise in temperature as illustrated in Fig. 12(a). This inflection point is called Temperature Compensation Point (TCP) and useful for high-temperature applications. A similar kind of trend is also shown in [27]. Fig. 12(b) shows the transconductance as a function of gate voltage and it depicts that its value increases as the temperature lowers down in the linear region.



12(a) 12(b)

Fig. 12 (a-b): Variation of Temperature on (a) Drain Current and (b) Transconductance of GaNNW MOSFET at V_{ds}=0.4V for L_g=20nm.

SS, V_{th} and QF as a function of temperature is shown in Fig. 13 and it is clearly observed that SS decreases with a decrease in temperature and goes below the ideal limit of MOSFET (60mV/decade) at 250K which results in high switching ratio and this is clearly visualized as QF is high for 250K in comparison to other temperatures. Since, as temperature increases, it causes lattice vibration and phonon scattering which increases leakage current and thus degrades QF which is a measure of switching performance. V_{th} value also increases with an increase in temperature due to the shift in bandgap and Fermi level as depicted in Fig. 13.

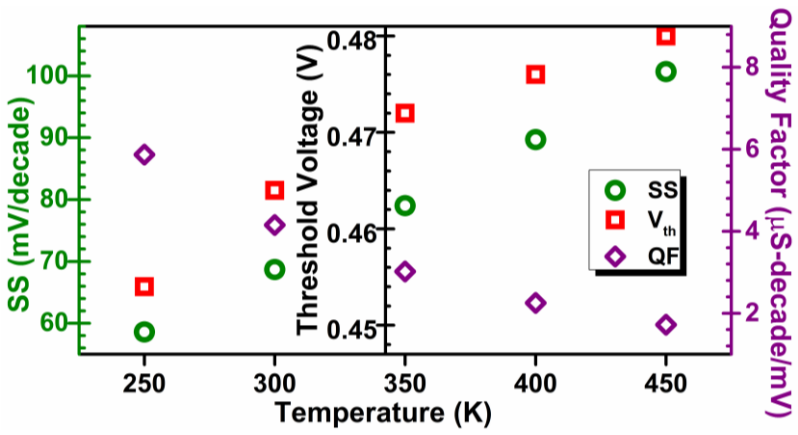


Fig. 13: Sub-threshold Swing, Threshold Voltage and Quality Factor as a function of temperature of GaNNW MOSFET at V_{gs}=1.2V and V_{ds}=0.4V.

Furthermore, the impact of temperature has also been investigated on linearity and distortion FOMs. All the linearity and distortion FOMs are evaluated as per eq. 2-9 and plotted as a function of gate voltage. Fig. 14(a-b) represents the high-order harmonics i.e. g_{m2} and g_{m3} whose amplitude decides the distortions and thus linearity of a device. It is observed that with rise in temperature, both g_{m2} and g_{m3} decrease which indicates lower harmonics or distortions owing to reduce leakage current. Linearity

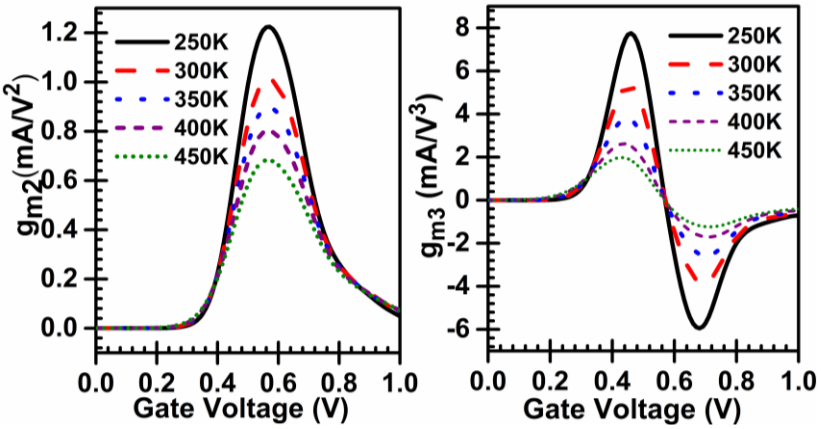
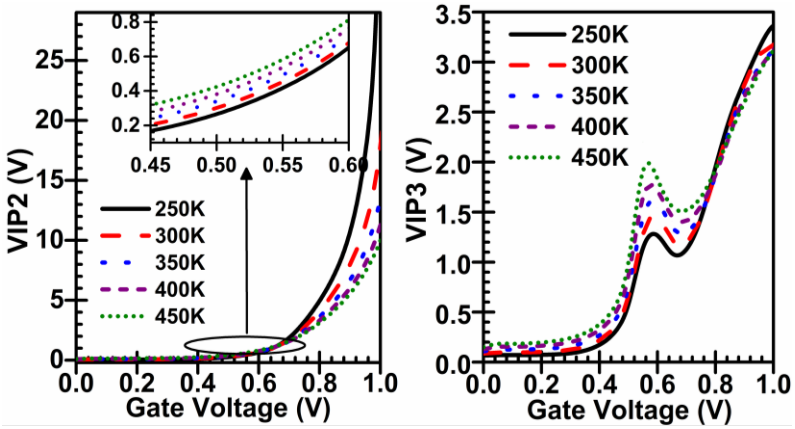
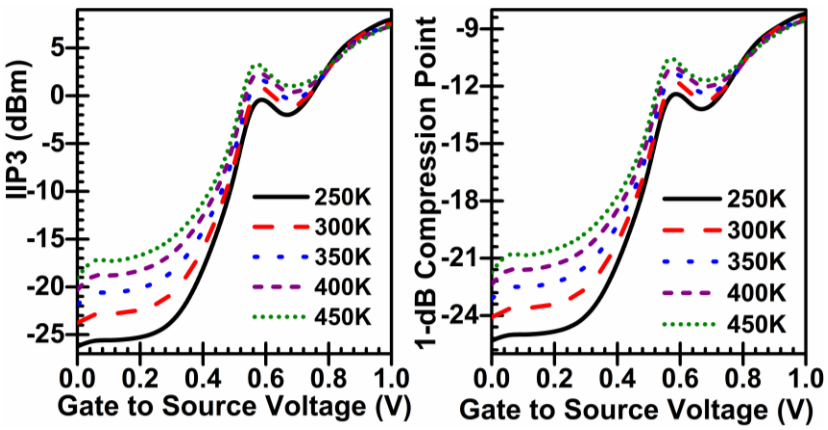


Fig. 14: High-order Transconductance (g_{m3}) of GaNNW MOSFET for different temperatures at V_{ds}=0.4V for L_g=20nm.



15(a) 15(b)



15(c) 15(d)

Fig. 15: (a) IIP3 and (b) 1-dB Compression for GaNNW MOSFET for different temperatures at V_{ds}=0.4V for L_g=20nm.

parameters such as VIP2 and VIP3 has been evaluated for different temperature and it is observed that both voltage intercept points improve as the temperature is increased from 250 K to 450K as reflected in Fig. 15(a) and (b) respectively. This

enhancement is due to more flatness in g_m at a high temperature which reduces g_{m2} and g_{m3} and thus improves linearity metrics. A similar kind of trend is also shown in [28]. Other parameters such as IIP3 and 1-dB Compression Point (CP) are also examined and from Fig. 15(c) and 15(d), it is clear that at high temperatures both IIP3 and 1-dB CP improves. This improvement is observed at lower gate voltage at which the self-heating is nor prominent unlike at high voltage which degrades the drain current and transconductance [see Fig, 12(a-b)]. Thus, the linearity of GaNNW/Al_2O_3 improves as temperature rises.

Moreover, IMD3 which determines distortion is shown in Fig. 17 and demonstrates that as temperature increases IMD3 reduces due to lower the value of g_{m3} which dominates over VIP3, Thus, signifies that GaNNW/Al_2O_3 exhibits high linearity with low distortions at high temperature and will be useful in microwave RF applications.

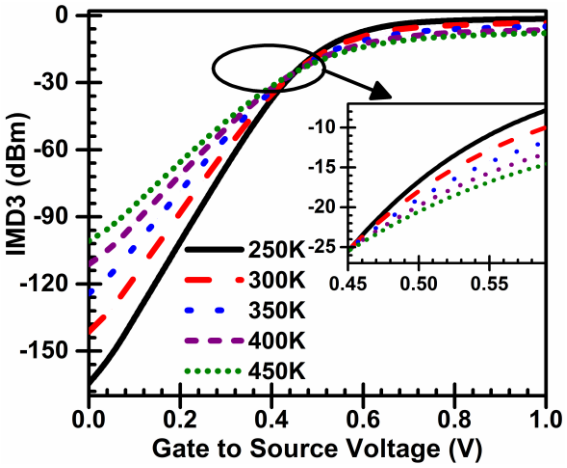


Fig. 17: IMD3 for GaNNW MOSFET for different temperatures at V_{ds}=0.4V for L_g=20nm.

IV. Conclusion

In this work, performance investigation of GaNNW MOSFET is done in terms of analog, linearity and intermodulation distortions and found that with Al_2O_3 as a gate oxide, its performance improves significantly in comparison to SiO_2 gate due to lower density of interface states and high CB offset which reduces leakage current. Performance metrics also improves in comparison to SiNW MOSFET due to low effective mass of GaN which improves current driving capability and thus improves linearity at low gate voltage in comparison to other devices. Thus, GaNNW/Al_2O_3 is suitable for low power applications where high linearity is concerned. Further, the impact of temperature has also been investigated on linearity FOMs to study the reliability issues of GaNNW/Al2O3 and found that the device exhibit TCP at 0.52V beyond which drain current and transconductance degrades with an increase in temperature. However, linearity performance improves due to a reduction in g_{m3} and g_{m2} at lower gate voltage which indicates low power dissipation.

ACKNOWLEDGMENTS

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CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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Figures

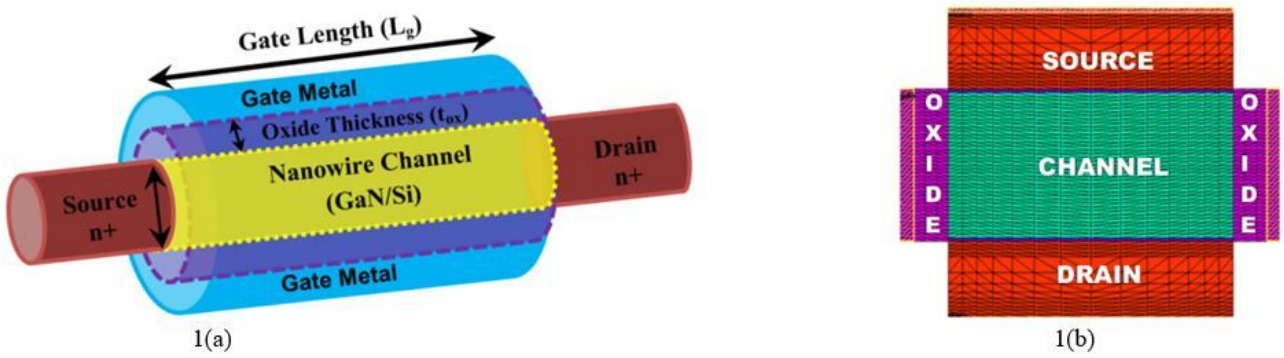


Figure 1

(a) Schematic view of simulated GAA GaN/SiNW MOSFET and (b) 2-D simulated structure of GaNNW MOSFET showing mesh lines.

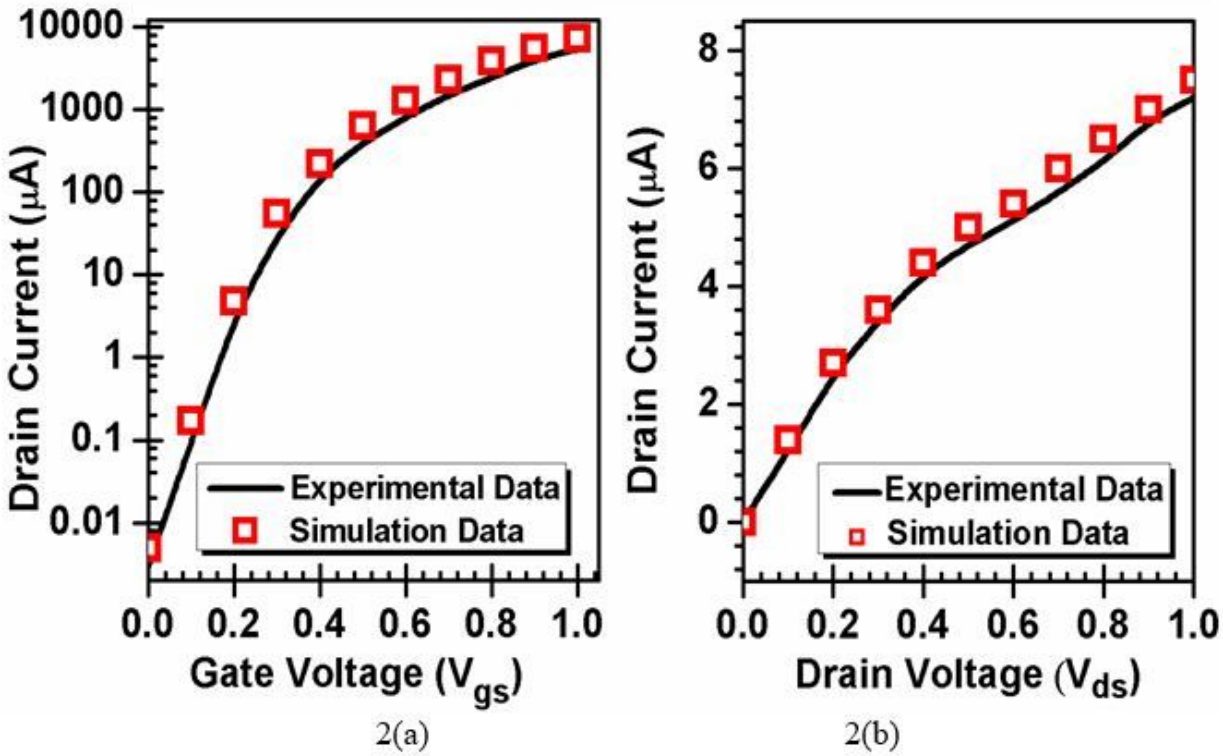


Figure 2

(a-b): Calibration of simulation models with experimental data.

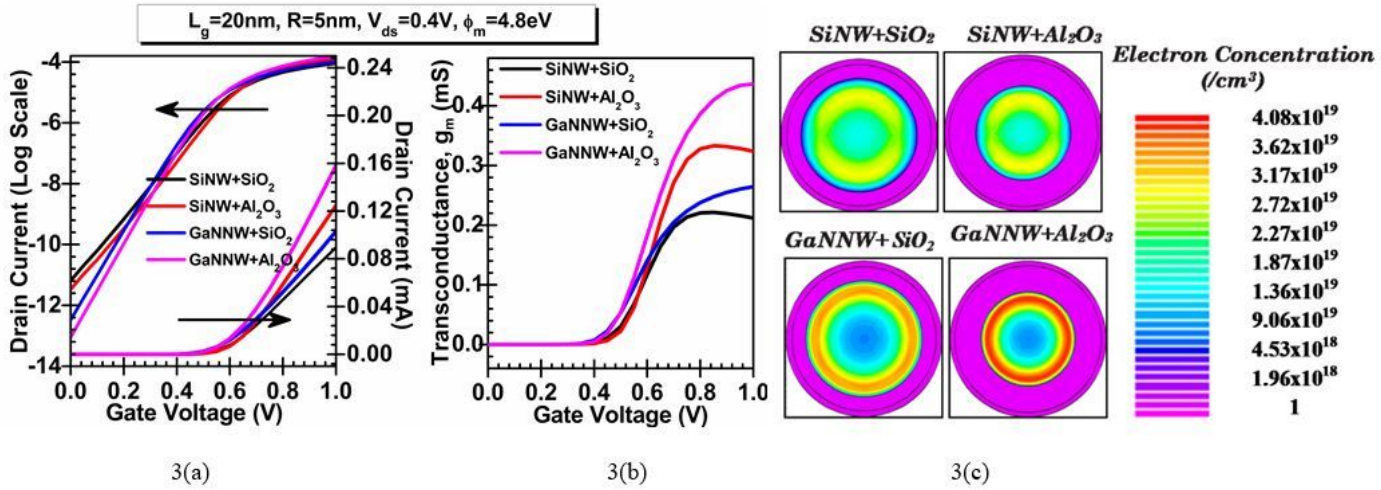


Figure 3

(a-c): (a) Variation of Drain Current with respect to gate voltage both in linear and log scale, (b) Transconductance as a function of gate voltage for four different device structures at Vds=0.4V and (c) Contour plot of four different device structures at Vds=0.4V, Vgs=1.0V showing electron concentration in the channel for Lg=20nm, tox=1.2nm, Vds=0.4V and gate metal workfunction (ϕm) =4.8eV.

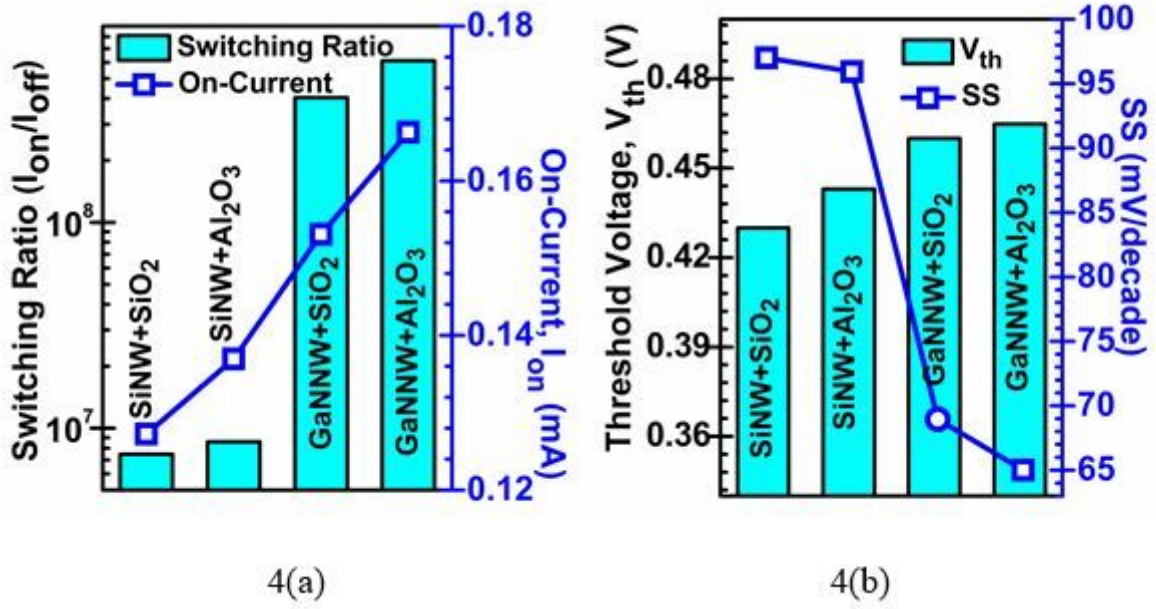
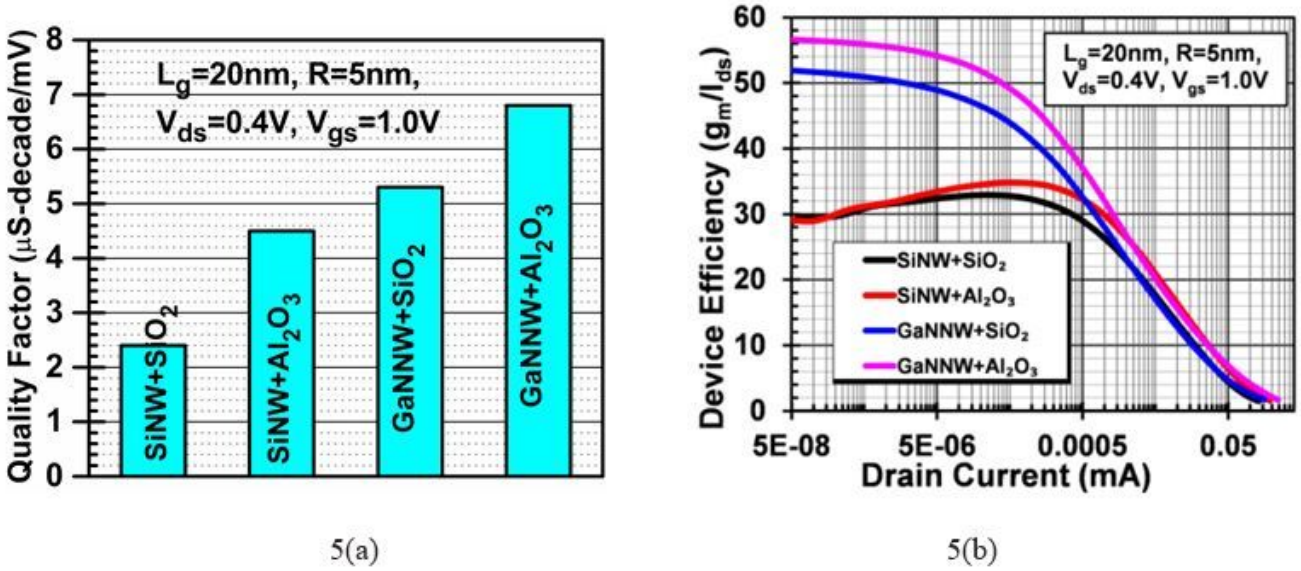


Figure 4

(a-b): (a) Switching Ratio and on-current and (b) Threshold Voltage and Subthreshold swing for four different devices at Vgs=1.0V and Vds=0.4V.



5(a) 5(b)

Figure 5

(a-b): (a) Quality Factor and (b) Device Efficiency four different devices at Vgs=1.0V and Vds=0.4V for Lg=20nm.

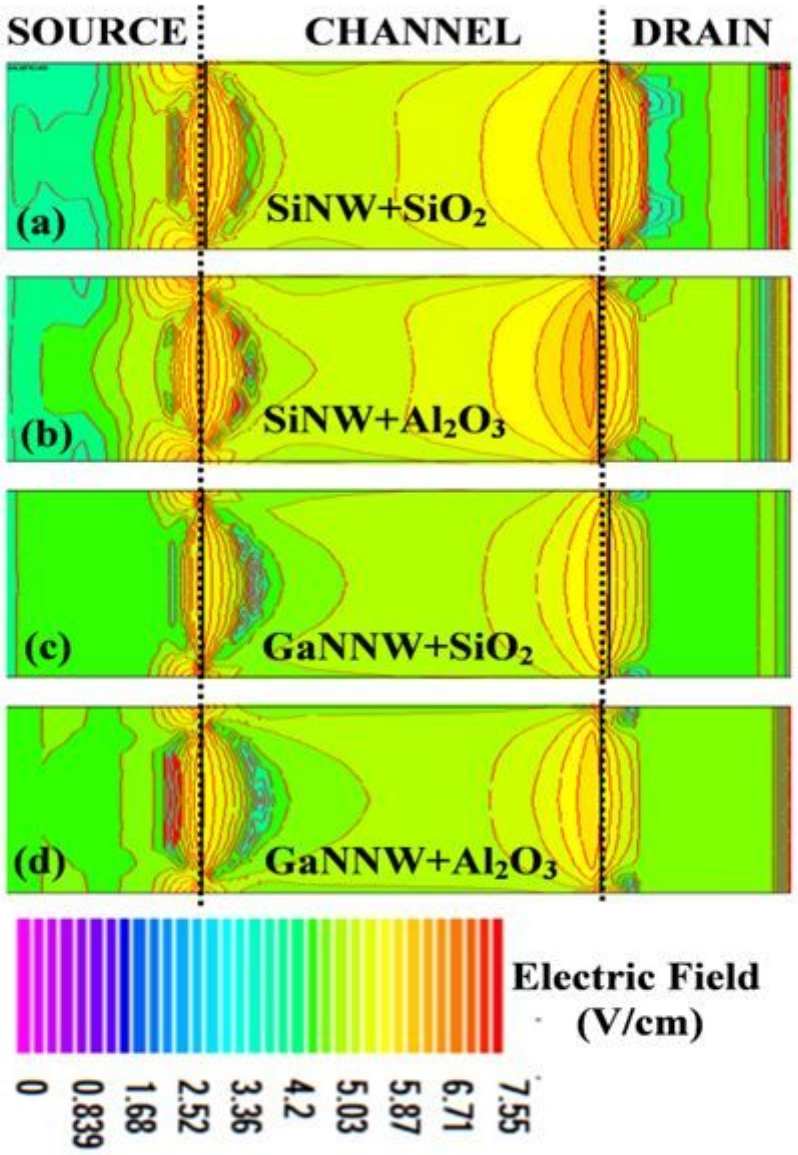


Figure 6

Contour plot of Electric field for (a) SiNW with SiO2 (b) SiNW with Al2O3 (c) GaNNW with SiO2 and (d) GaNNW with Al2O3 at Vgs=1.0V and Vds=0.4V for Lg=20nm.

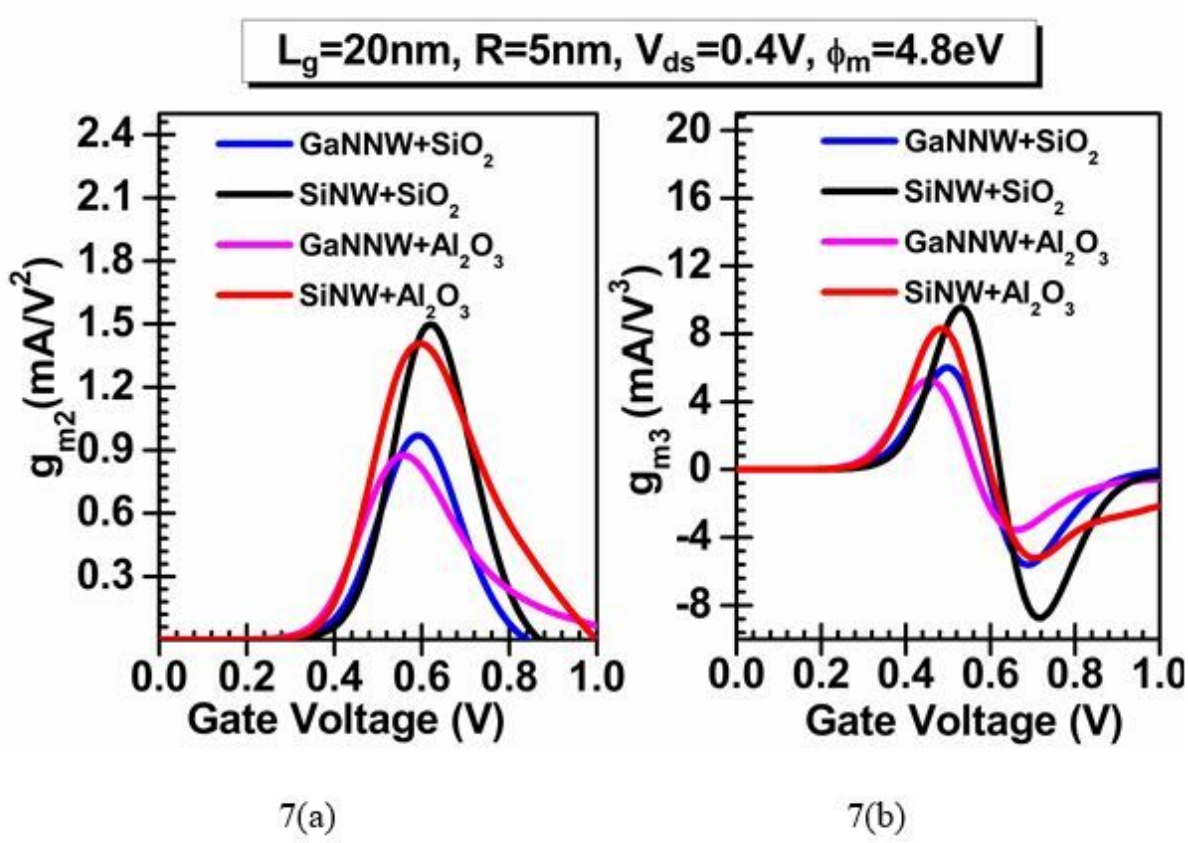


Figure 7

(a-b): High order transconductance gm2 and gm3 as a function of gate voltage at Vds=0.4V

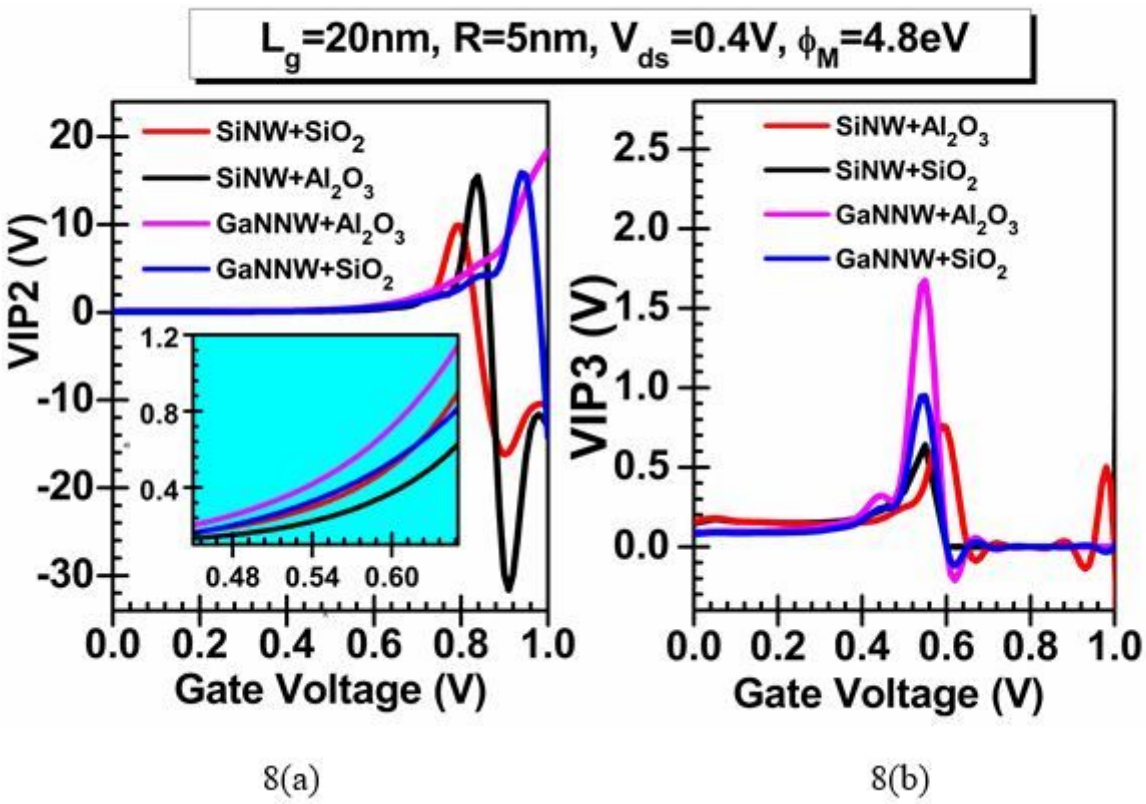
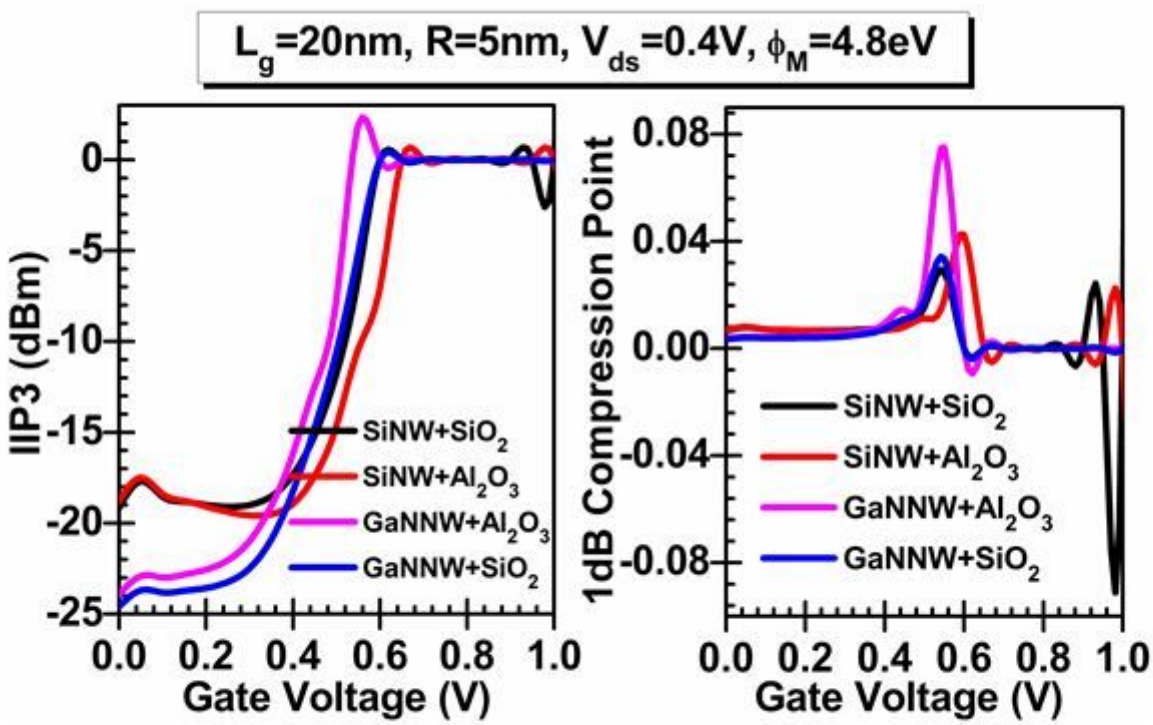


Figure 8

(a-b): Second order (VIP2) and third order (VIP3) Voltage Intercept Point of of SiNW and GaNNW MOSFET at Vds=0.4V for Lg=20nm.



9(a) 9(b)

Figure 9

(a-b): IIP3 and 1 dB compression point of SiNW and GaNNW MOSFET at Vds=0.4V for Lg=20nm.

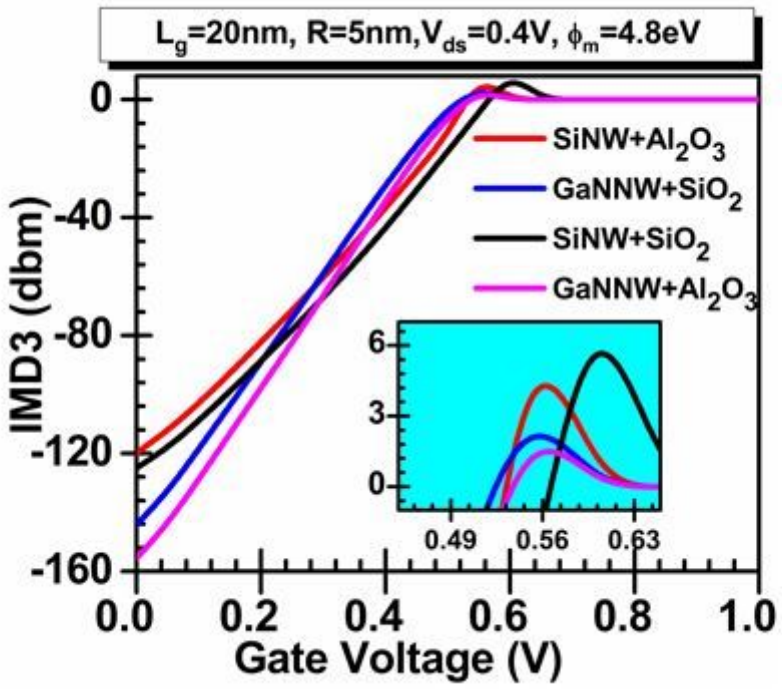


Figure 10

IMD3 of SiNW and GaNNW MOSFET at Vds=0.4V for Lg=20nm.

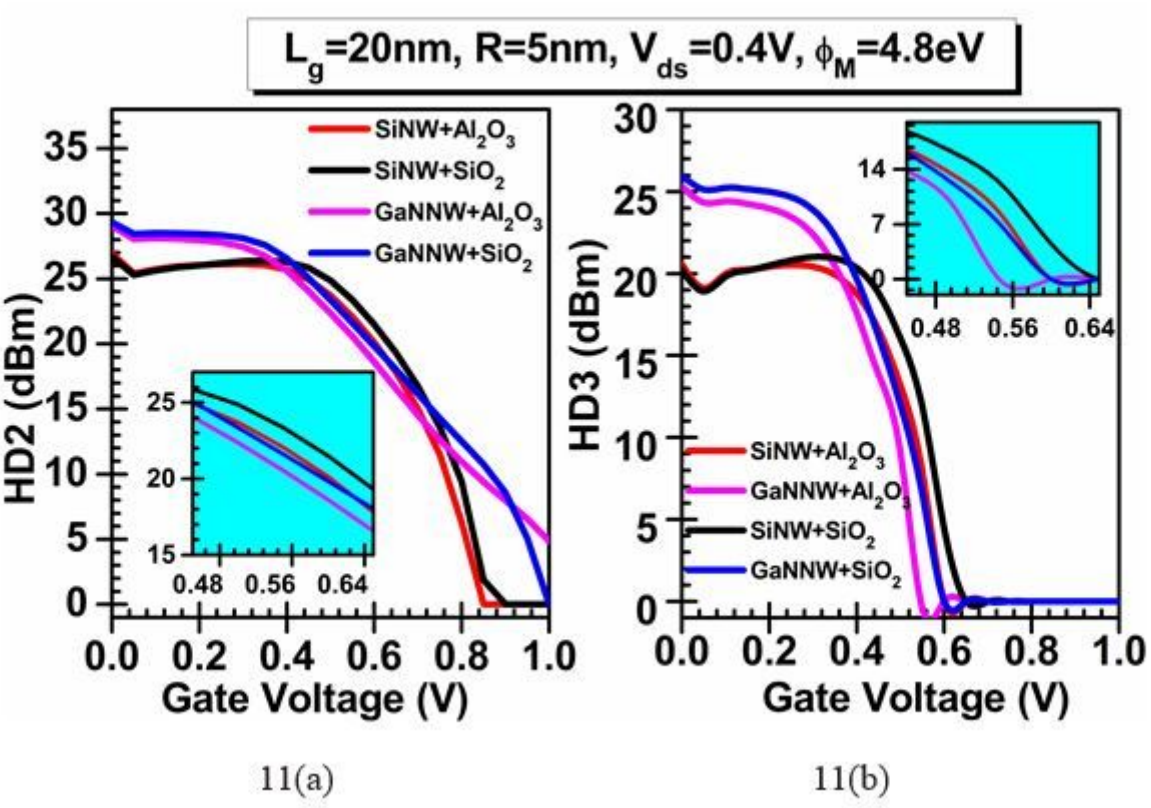
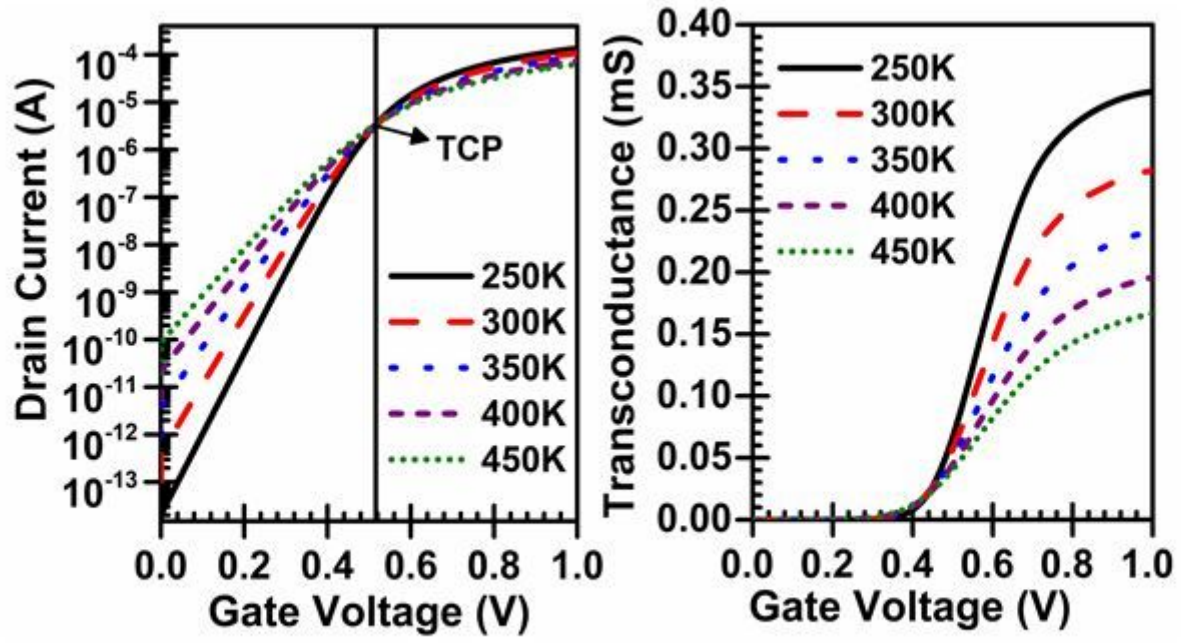


Figure 11

(a-b): HD2 and HD3 of Si and GaNNW MOSFET at Vds=0.4V for Lg=20nm



12(a) 12(b)

Figure 12

(a-b): Variation of Temperature on (a) Drain Current and (b) Transconductance of GaNNW MOSFET at Vds=0.4V for Lg=20nm.

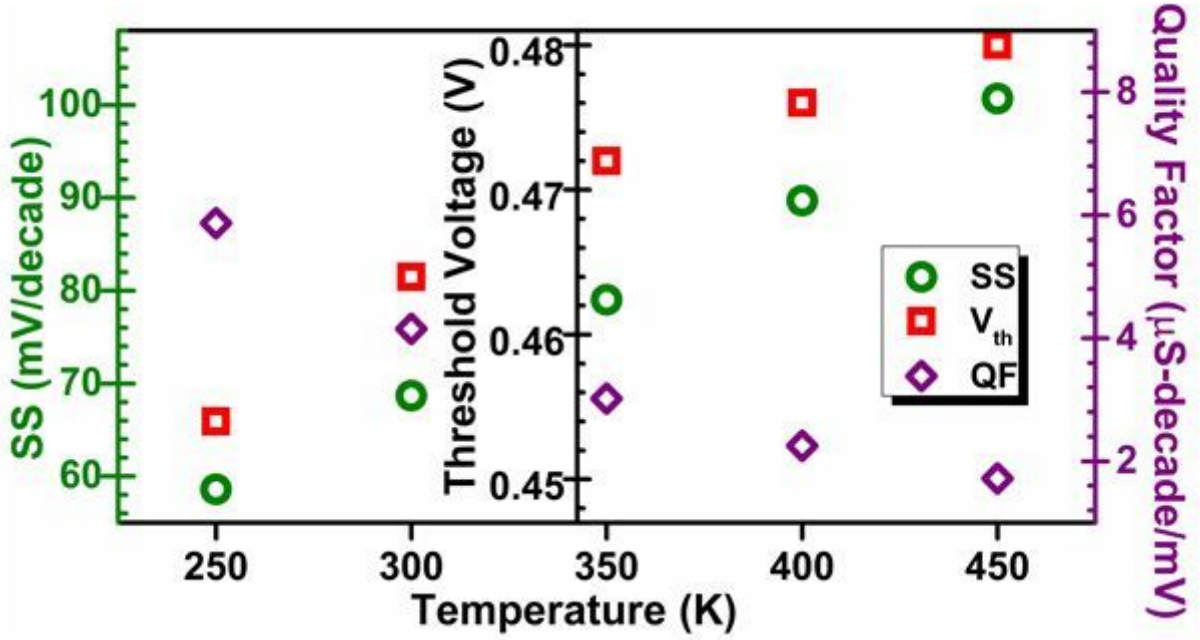


Figure 13

Sub-threshold Swing, Threshold Voltage and Quality Factor as a function of temperature of GaNNW MOSFET at Vgs=1.2V and Vds=0.4V.

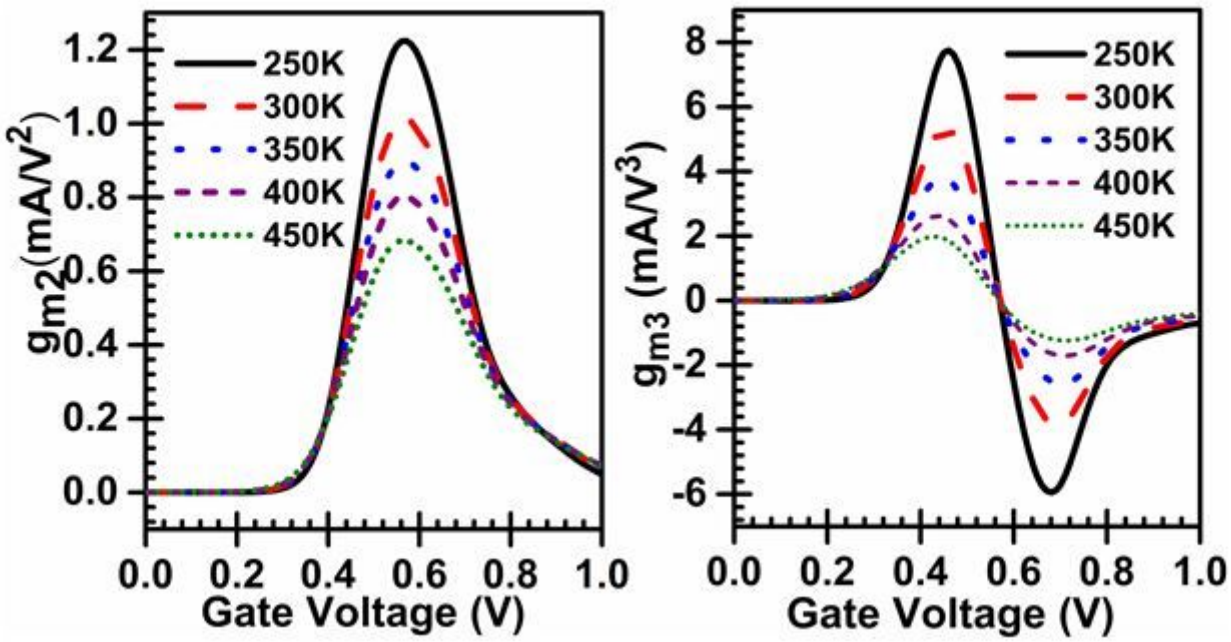
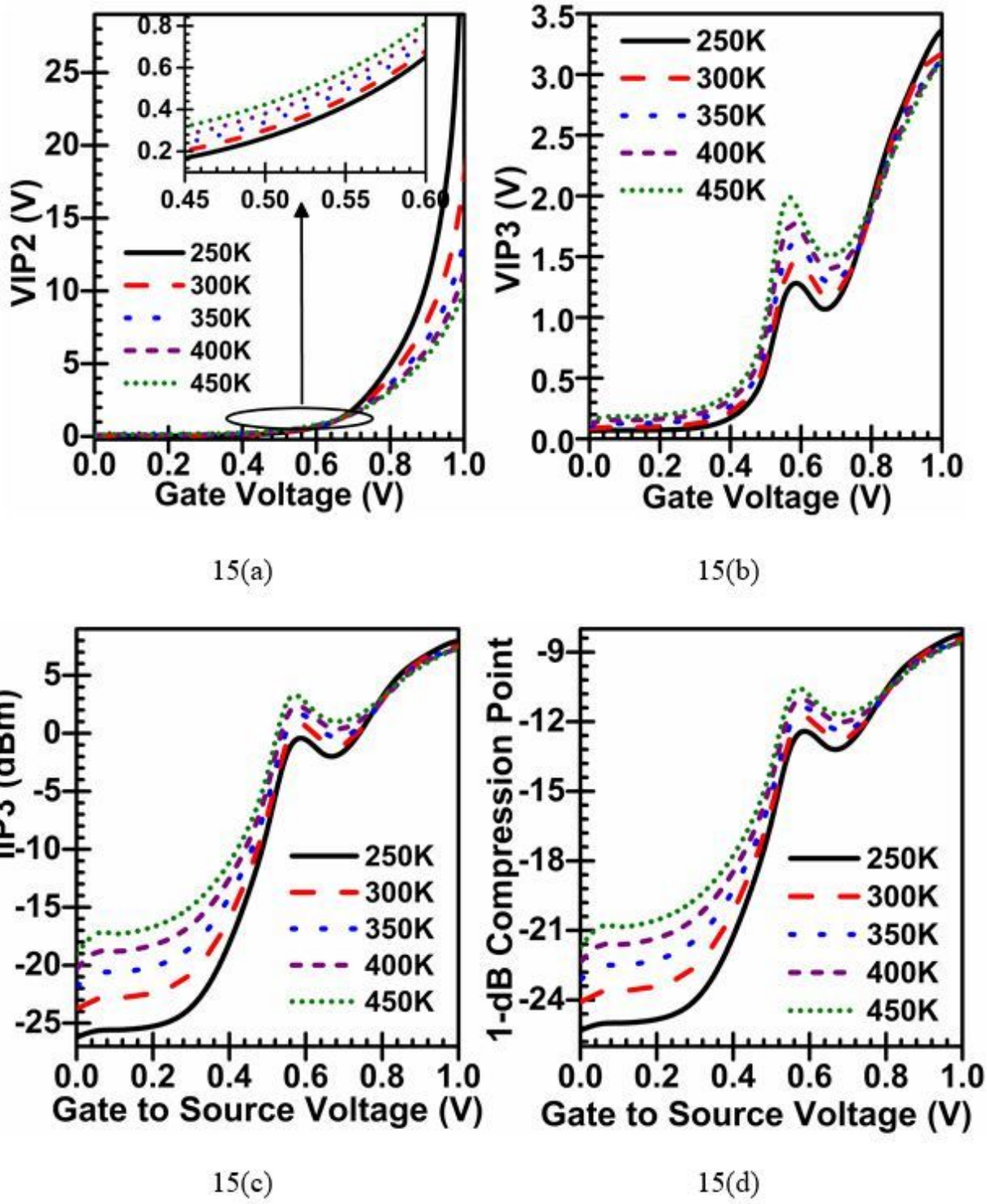


Figure 14

High-order Transconductance (gm3) of GaNNW MOSFET for different temperatures at Vds=0.4V for Lg=20nm.



15(a) 15(b)

15(c) 15(d)

Figure 15

(a) IIP3 and (b) 1-dB Compression for GaNNW MOSFET for different temperatures at Vds=0.4V for Lg=20nm.

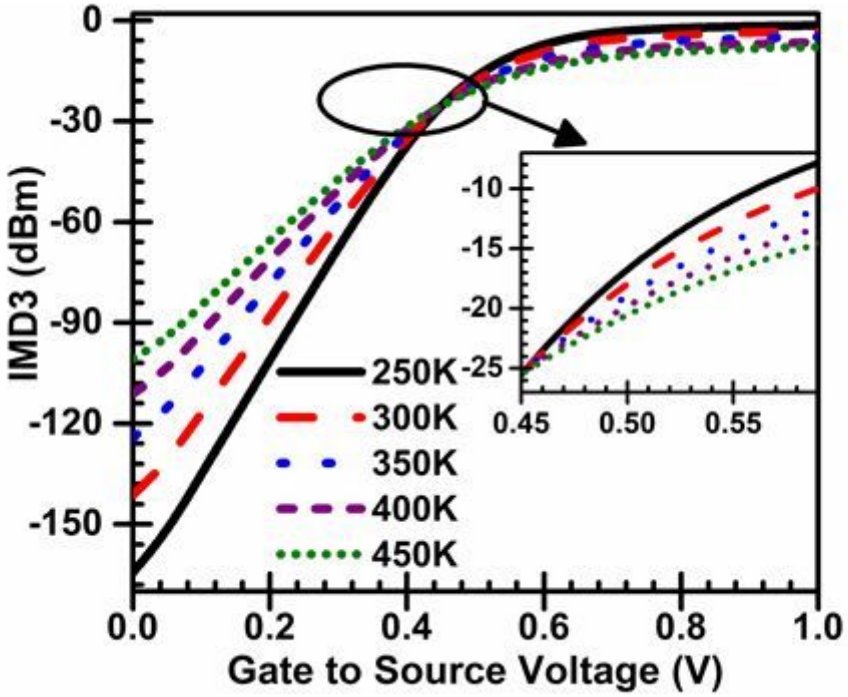


Figure 16

IMD3 for GaNNW MOSFET for different temperatures at Vds=0.4V for Lg=20nm.