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Research Article

Keywords: all-optical logic gates, metal-insulator-metal waveguide, Y-combiner, linear interference, plasmonic, FDTD

Posted Date: March 22nd, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-327354/v1>

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Version of Record: A version of this preprint was published at Journal of Computational Electronics on August 6th, 2021. See the published version at <https://doi.org/10.1007/s10825-021-01748-x>.

Design, analysis, and simulation of all-optical optimized AND gate using Y-shaped plasmonic waveguide for high-speed computing devices

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Abstract

All-optical logic gates have proven their significance in the digital world using which all high-speed computations are calculated. In this paper, we have proposed a novel structure for all-optical AND using the concept of power combiner using Y-shaped metal-insulator-metal waveguide under the footprints of $4\ \mu\text{m} \times 7\ \mu\text{m}$. This design works under the principle of linear interference. The insertion loss and extinction ratio of the design are given by 0.165 dB and 14.11 dB, respectively. The analysis of the design is carried out by finite-difference-time-domain (FDTD) method and verified using MATLAB. This minimized structure can be used to design any complex logic circuits to achieve better performance in future.

Keywords: all-optical logic gates, metal-insulator-metal waveguide, Y-combiner, linear interference, plasmonic, FDTD

Introduction

The role of communication in the day-to-day life of humans can never be replaced by any other alternative. As technology is advancing, the need for faster communication is also advancing at the same pace. Along with the speed of communication, there are several other factors to be considered while designing a device, like the cost of the individual circuit, size of the device, power handling capacity, heat dissipation issues, and interconnect delays [1]. The first generation of electronics is based on semiconductor technology which makes use of vacuum tube-based transistors for logical operations but is less preferred due to its high heat dissipation and interconnects delay [2]. These limitations are somewhat mitigated by the next technology called photonics [3-4]. In this field, instead of electrons, photons are used to exchange information [5]. But the optical devices suffer diffraction limit when the size of the device is closer to the operation wavelength [6]. Also, the size of optical components is nearly 1000 times greater than the electronic devices which adds another drawback to it [7]. The next generation of technology came with a new proposal called surface plasmons, where the optical signal interacts with the metallic structures at a nano-scale giving a new branch called plasmonic [8-9]. It is the combined effect of a miniaturized version of electronics and the capacity of photonics [10]. When light of a certain wavelength is incident on the metal surface, the free electrons are excited by absorbing the energy

from light and are bonded at the interface of metal and dielectric [11]. These surface plasmon polaritons (SPPs) are capable of eliminating the diffraction limit in photonics [7, 11-14]. These SPPs can able to confine and control the light beyond the diffraction limit and the losses inside the SPs can be overcome by using different waveguides like metal-insulator-metal (MIM) [15-16], insulator-metal-insulator (IMI), dielectric-loaded surface plasmon polariton waveguide (DLSPPW) [14, 17-24]. Among these, the MIM waveguide is best suited because of its capacity to confine light to deep sub-wavelength [2, 16]. Logic gates are the basic building blocks of all digital circuits. Several optical devices like directional coupler (DC), Mach-Zehnder-Interferometer (MZI), power combiners, power splitters are used to realize the several logic gates like AND, OR, NOT, XOR, XNOR, and the universal gates like NAND and NOR [25-32, 45]. These all-optical logic gates hence are used to design all the combinational circuits like multiplexers, demultiplexers, code converters, adders and subtractors, parity generators [33-41]. In this paper, a minimized design of all-optical AND gate based on power combiner using Y-shaped waveguide is proposed and verified using FDTD method [42]. Section 2 will describe the design of Y-combiner followed by design of AND gate. The simulation results are provided in Section 3. Section 4 includes a result analysis where the present work is compared with previously reported works and Section 5 gives the conclusion of the proposed design.

2. Design of AND gate using Y-Combiner

In this paper, the proposed design of AND gate using Y-combiner works on the principle of linear interference [43]. The inputs applied to the arms of the power combiner are controlled by an external phase shifter to obtain the desired output of the logical AND gate. The Y-combiner is designed using the S-bend sine waveguide whose equation is defined as

$$y(t) = \frac{D-2*W}{4} + \frac{D}{4} \cos\left(\frac{\pi t}{L}\right) \quad (1)$$

where D is the input separation gap between two arms of a combiner, W is the width of the waveguide and L is the length of the S-Bend-shaped waveguide. The waveguide is structured using Eq. 1, as shown in Fig. 1.

Fig. 1: Structure of S-bend sine waveguide

Another waveguide of S-bend shape is arranged symmetrically along the X-axis to obtain the actual Y-combiner. In this paper, the all-optical AND gate has been designed using the concept of power combiner with the help of a Y-shaped waveguide. The design of the Y-combiner is achieved by combining the two symmetrical S-bend structures joined at one end to form a Y-shape structure as shown in Fig. 2.

Fig. 2: Schematic of symmetric Y-combiner

The above structure is designed using the plasmonic waveguide by keeping refractive index as 2.1. The final minimized structure is obtained as a result of altering the parameters of the Y-combiner like S-bend length, Input separation gap, and the length of the linear waveguide.

Table. 1: Extinction ratio values for various S-bend lengths of Y-combiner

Sl. No.	S bend length (μm)	P_{ON}	P_{OFF}	Extinction Ratio (dB)
1	4.3	1.9668	0.0916	13.31
2	4.2	1.9516	0.0903	13.34
3	4.1	1.9462	0.0889	13.40
4	4	1.9156	0.0878	13.38
5	3.9	1.9300	0.0869	13.47
6	3.8	1.9267	0.0871	13.44
7	3.7	1.9250	0.0879	13.40
8	3.6	1.9099	0.0879	13.37

By keeping the input separation gap at $3\mu\text{m}$, various parameters like peak output power at ON state, peak output power at OFF state, Y-angle, and the ER are calculated by varying the S-bend length and are tabulated. From Table. 1, it is found that the ER is the maximum at S-bend length of $3.9\mu\text{m}$ and its value is 13.47 dB. A plot of S-bend length versus ER is shown in Fig. 3.

Fig. 3: Plot of S-bend length versus extinction ratio at $D = 3\mu\text{m}$

Similarly, the mentioned parameters are calculated by varying the input separation gap by keeping the S-bend length constant at $L = 3.9 \mu\text{m}$ and the values are mentioned in Table 2.

Table. 2: Extinction ratio values for various Input separation gaps at $L = 3.9 \mu\text{m}$

S. No.	D	P _{ON}	P _{OFF}	Extinction ratio (dB)
1	3.2	1.9109	0.0884	13.34
2	3.1	1.9425	0.0888	13.39
3	3.0	1.9300	0.0869	13.46
4	2.9	1.9401	0.0851	13.57
5	2.8	1.9905	0.0873	13.58
6	2.7	2.0181	0.0883	13.59
7	2.6	2.0307	0.0883	13.62
8	2.5	2.0585	0.0895	13.61

From Table. 2, at the value of $D = 2.6 \mu\text{m}$, the ER is found to be greater than the previously noted value and it is 13.62 dB. A graphical representation of input separation gap versus ER is shown in Fig. 4.

Fig. 4: Plot of input separation gap versus extinction ratio at $L = 3.9 \mu\text{m}$

The S-bend length and the input separation gap are kept constant at $3.9 \mu\text{m}$ and $2.6 \mu\text{m}$, respectively and the length of the linear waveguide is modified to attain the maximum extinction ratio. The ER at various lengths of linear waveguide is shown in Table. 3.

Table. 3: Extinction ratio values for various lengths of linear waveguide

S. No.	Linear	P _{ON}	P _{OFF}	Extinction ratio (dB)
1	3.1	2.0307	0.0883	13.62
2	3	2.0526	0.0807	14.05
3	2.9	2.0775	0.0806	14.11
4	2.8	2.0781	0.0813	14.07
5	2.7	2.0845	0.0815	14.07
6	2.6	2.0865	0.0815	14.08

7	2.5	2.0941	0.0928	13.53
8	2.4	2.0956	0.0938	13.49

The ER is found to be larger at the linear waveguide length of 2.9 μm which is 14.11 dB, significantly greater than already obtained values. A plot of linear waveguide length versus ER is shown in Fig. 5.

Fig. 5: Plot of linear waveguide length versus extinction ratio at $L = 3.9 \mu\text{m}$ and $D = 2.6 \mu\text{m}$

The final dimensions of the Y-combiner at which the maximum ER is obtained are depicted in Table. 4.

Table. 4: Design parameters of AND gate using Y-combiner

S. No	Parameter	Value
1	S-bend length (L)	3.9 μm
2	Input separation (D)	2.6 μm
3	Linear length	2.9 μm
4	Refractive index of waveguide	2.1
5	Width of the waveguide	0.25 μm

3. Simulation results of AND gate using FDTD

The minimized design of logical AND gate has been verified using MATLAB and FDTD. The analysis of the structure is carried out with the help of FDTD method. A continuous wave of 1550 nm is applied at both the input terminals of Y-combiner. The input optical signals with the power of $1e^9 \text{ W/m}$ and $3e^9 \text{ W/m}$ are considered as the low and high optical intensity signals. The entire simulation is carried out in the Transverse Electric (TE) mode of the plasmonic waveguide, excited by the source with Gaussian wave for both inputs. The simulation parameters of the proposed design are given in Table. 5.

Table. 5: Simulation parameters of the AND gate using Y-combiner

Parameter	Value
Type of polarization	TE

Wavelength	1.55 μ m
Mesh size X (μ m)	0.0114
Mesh size Z (μ m)	0.0114
No. of mesh cells X	349
No. of mesh cells Z	603
Input field transverse	Gaussian
Low-intensity signal power	1e ⁹ W/m
High-intensity signal power	3e ⁹ W/m

As shown in the truth table of AND gate in Table. 6, the output of the AND gate is high when both of the inputs are high, otherwise, it is low. The timing diagram of AND gate is shown in Fig. 6, is verified using MATLAB; where the two input signals A and B are represented by first and second row and the last row represents the output of logical AND gate.

Fig. 6: The timing diagram of AND gate using MATLAB

Case 1: when A = 0 and B = 0

In this case, two inputs of the Y-combiner are given a low-intensity signal of power 1e⁹ W/m. According to the truth table of AND gate, the output power is low. A phase difference of 180° is created between the two input signals. Since two input signals are having the same amplitude and are out of phase, destructive interference will occur and the output of AND gate is low (Y = 0)

Case 2: when A = 0 and B = 1

In this case, the upper arm of combiner is provided with the low-intensity signal (1e⁹W/m) and the lower arm of the combiner is given the high-intensity signal (3e⁹ W/m). A phase shift of 180° is introduced between the two input signals. Similarly, in case of A = 0 and B = 0, destructive interference will occur which in turn reduces the intensity of output signal. Hence the output of the AND gate is low (Y = 0). The optical field propagation for logic '0 & 1' is shown in Fig. 7(a).

Fig. 7: Light propagation through proposed AND gate for all combinations of input signals using FDTD method

Case 3: when A = 1 and B = 0

Unlike the previous case, here the upper arm of the combiner is provided with the high-intensity signal ($3e^9$ W/m) and the lower arm is supplied with the low-intensity signal ($1e^9$ W/m). Thereby due to the similar amplitudes of the input signals and out of phase (180°), again the destructive interference will make the output of AND gate to low ($Y = 0$). The optical field propagation for logic '1 & 0' is shown in Fig. 7(b).

Case 4: when A = 1 and B = 1

In this case, both the input ports of the power combiner are supplied with a high-intensity signal ($3e^9$ W/m). Here the phase difference between the signals is made to 0° . According to the principle of Constructive interference, when two signals are having the same amplitude and same phase difference, then the intensity of output signal will be twice the input signal intensity ($Y = 1$). The optical field propagation for logic '1 and 1' is shown in Fig. 7(c).

All the input combinations along with phase values are shown in Table. 6.

Table. 6: Truth table for AND gate along with phase and transmission efficiency

Inputs					Output	
A	B	Input phase A	Input phase B	Phase Difference	Transmission efficiency	(A.B)
0	1	180°	0°	180°	19.67%	0
1	0	180°	0°	180°	21.64%	0
1	1	0°	0°	0°	152.6%	1

4. Result analysis

In this paper, the suggested device is in the footprints of $7\ \mu\text{m} \times 4\ \mu\text{m}$. The performance parameters like insertion loss and extinction ratio are calculated using the output results. The Insertion Loss is given by

$$\text{Insertion Loss (IL)} = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right),$$

where P_{out} is the peak output power, P_{in} is the peak input power.

The Extinction Ratio is defined as

$$\text{Extinction Ratio (ER)} = 10\log_{10}\left(\frac{P_{out}|ON}{P_{out}|OFF}\right),$$

where $P_{out}|ON$ is output optical power in ON state, $P_{out}|OFF$ is output optical power in OFF state.

The IL and ER of our work are found to be 0.165 dB and 14.11 dB respectively. For better performance of logic gates, the insertion loss should be low and the Extinction ratio should be high as possible [44]. This paper work is compared with the previously published works in following parameters as shown in the Table. 7.

Table. 7: Comparison of a proposed device with existing one

Sr. No.	Material used	Extinction ratio	Wavelength	Design footprints	Refractive index	Low-intensity	High-intensity	Structure	Ref.
1	Plasmonic MIM waveguide	-	1550 nm	-	-	$4.45\text{e}^8\text{W/m}$	$4.45\text{e}^9\text{W/m}$	3 MZIs and 2 Splitters	[2]
2	2-D photonic crystals	8.47 dB	1550 nm	-	3.4	-	-	21×21 array of Si rods	[25]
3	Surface plasmon polaritons	-	800 nm	$10\ \mu\text{m} \times 20\ \mu\text{m}$	1.52	-	-	Two crossed linear waveguides	[26]
4	2-D photonic crystals	-	1550 nm	$10\ \mu\text{m} \times 10\ \mu\text{m}$	3.4	-	-	16×17 array of Si rods	[32]
5	Nanoring IMI plasmonic waveguides	-	1550 nm	$400\ \text{nm} \times 400\ \text{nm}$	1.357	-	-	3 Straight stripes and 2 nano-ring resonators	[38]
6	Plasmonic MIM waveguide	-	900 nm & 1330 nm	-	1.357	-	-	3 slot and 4 nano-rings	[45]
7	Plasmonic MIM waveguide	14.11 dB	1550 nm	$7\ \mu\text{m} \times 4\ \mu\text{m}$	2.1	$2\text{e}^8\text{W/m}$	$3\text{e}^9\text{W/m}$	One Y-combiner	This Work

5. Conclusion

In this work, an all-optical AND logic gate is designed with the help of a Y-shaped plasmonic MIM waveguide. The design is in the area of $4 \times 7 \mu\text{m}^2$ which is smaller when compared to the previous works. The key parameters like insertion loss and extinction ratio are calculated. The IL and ER of our work are found to be 0.165 dB and 14.11 dB respectively. The design parameters like S-bend length, input separation gap, and linear waveguide are optimized to obtain the maximum extinction ratio and to minimize the losses inside the waveguide. Due to simple structure and controllability, the Y-combiner based AND gate can provide a new method to implement logic functions in digital electronics. This design has a minimized structure and is also used in future works to design ultra-compact devices for fast optical computing.

Acknowledgment

This work was supported by the Science and Engineering Research Board, India [grant number: TAR/2018/000051].

Disclosure

The authors declare that there are no conflicts of interest related to this article.

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Figures

Figure 1
Structure of S-bend sine waveguide

Figure 2

Figure 3

Plot of S-bend length versus extinction ratio at $D = 3 \mu\text{m}$

Figure 4

Plot of input separation gap versus extinction ratio at $L = 3.9 \mu\text{m}$

Figure 5

Plot of linear waveguide length versus extinction ratio at $L = 3.9 \mu\text{m}$ and $D = 2.6 \mu\text{m}$

Figure 6

The timing diagram of AND gate using MATLAB

Figure 7

Light propagation through proposed AND gate for all combinations of input signals using FDTD method