Design and Parametric Variation Assessment of Dopingless Nanotube Field-Effect Transistor (DL-NT-FET) for High Performance

Jeetendra Singh (jeetendras15.phd@nitj.ac.in)
NIT Sikkim: National Institute of Technology Sikkim
Debapriya Chakraborty
NIT Sikkim: National Institute of Technology Sikkim
Naveen Kumar
NIT Jalandhar: Dr BR Ambedkar National Institute of Technology

Research Article

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Abstract

In this paper, a dopingless nanotube field-effect transistor (DL-NT-FET) has been proposed and its performance analysis is done using a technology computer-aided design (TCAD) tool, ATLAS provided by Silvaco. The elimination of doping is brought in by the application of the charge-plasma (CP) technique. A comparative examination of transfer characteristics (I D -V GS), transconductance (g m), gate capacitances (C gs and C gd), output characteristics (I D -V DS), output conductance (g ds), average subthreshold slope (AVSS), the threshold voltage (V t), the ratio of on-current to off-current (I ON /I OFF) and on-current has been made by varying the channel length (Lg), radius (R), gate work function (Φ), and temperature. Results revealed that increasing the channel length improves subthreshold slope with greater I ON /I OFF and less threshold voltage. It has been also noticed that increase in the radius of the nanotube or an increase in temperature results in just the opposite effect of that observed in the case of increasing channel length. The I OFF value increases significantly on increasing the temperature while the small degradation in the I ON has been noticed as a result of mobility degradation and velocity saturation. The I ON degrades 15% by increasing the temperature from 200K to 400K. The output conductance g ds also degrades on increasing the temperature. A proliferation of 39% is observed in the C gs at the V GS of 0.45V on increasing the channel length from 20 nm to 35 m whereas no significant changes are observed in the C gd for the same increment in the channel length.

Introduction

The complementary metal-oxide-semiconductor (CMOS) technology has advanced through the decades to dominate the semiconductor industry with excellent features of low power and cost, dense packaging, and high-speed devices that are continuously scaled down in size [1-3]. When it comes to designing RF/analog circuits in the nanometer regime, several challenges have been encountered due to strict process requirements to maintain sharp source/drain region and short channel effects (SCEs) [4-7]. The junctionless field-effect transistor (JLFET) solves many of the issues related to SCEs but still, it suffers from poor carrier mobility due to high channel doping, which leads to transconductance/gain degradation and hence low ON current [8, 9]. Dopingless nanotube FET (DL-NT-FET) can provide a solution by making use of the charge-plasma (CP) technique in which abrupt doped source and drain regions are formed in the intrinsic substrate with the help of suitable work function metal electrode or poly-Si electrode at the high temperature [10-12]. The gate-all-around (GAA) and shell-gated nanotube provide strong gate control over the channel carrier which results in enhanced surface inversion and hence superior drain current [13, 14]. Hence, the proposed device exploits both the advantages of GAA structure (i.e. allowing better electrostatics and reduced SCEs) and dopingless configuration (like reduced random dopant fluctuations(RDFs), less mobility degradation, better gm) [15, 16]. Besides the collective merit of GAA and dopingless nanotube, the impact of temperature on the performance parameters of the proposed DL-NT-FET is the first time investigated along with other design parameters.

In this article, a dopingless nanotube field-effect transistor (DL-NT-FET) is designed and its various performance parameters; transfer characteristics (ID-VGS), transconductance (gm), gate capacitances

(Cgs and Cgd), output characteristics (ID-VDS), output conductance (gds), average subthreshold slope (AVSS), the threshold voltage (Vt), the ratio of on-current to off-current (ION/IOFF) are investigated. The impact of nanotube radius (R), channel length (Lg), and gate work function variations on the performance parameters are examined to achieve high performance. The various performance parameters are also evaluated at a different temperature to study the temperature-dependent variability.

Device Structure

The 2-D structure of the proposed device is shown in Fig. 1(a) whereas the 3-D structure of the same is depicted in Fig. 1(b). The source, channel, and drain regions have been formed on an intrinsic Si body with the radius being 10nm and the silicon thickness being 7nm leaving the inner oxide thickness. CP technique is used to establish the source and drain regions of this dopingless device [17]. The gate oxide is made of SiO2 and is 2nm in thickness. Both drain and source lengths are 30nm while the channel length is 20nm. P-type polysilicon (workfunction= 3.9eV) is used in forming the source and drain core-electrodes. The gate contact is also made of polysilicon (workfunction=4.6eV). The poly-Silicon core-electrodes help to induce N+ regions at the source and drain sides. A SiO2 layer surrounds these electrodes followed by an intrinsic Silicon layer in the core. Poly-silicon electrodes are also attached at the bottom and top of this layer. The second layer of SiO2 is muffled on all sides of the Si layer. A shell consisting of polysilicon (work function=4.6 eV) has been wrapped over the oxide layer to form a contact for the gate. Aluminum is generally preferred for gate material of MOSFET but here the polysilicon is mainly utilized because polysilicon composition matches with the channel bulk-silicon and therefore offers low threshold voltage as compared to that of metal gate material [18]. The proposed device is simulated utilizing Silvaco TCAD to analyze the various results. To account for accurate mobility evaluation in the channel, the Lombardi mobility model along with concentration and field-dependent mobility models are considered. Shockley–Read–Hall (SRH) and Auger generation-recombination models are contemplated to acknowledge the lifetime of constant minority carriers and large current density. The simulation temperature was initially 300K for the proposed device and then observations were also taken at different temperatures to compare the effect on different device parameters.

The variation of the electron-hole concentration and the energy band diagram of the proposed DL-NT-FET is illustrated in Fig. 2 for OFF-state conditions (VGS=0V and VDS=1V) and ON-state conditions (VGS=1V and VDS=1V) respectively. As it can be noticed from Fig. 2(a) that the concentration of the electrons in the channel region goes high from the low and the holes concentration goes low from high when the device comes into the ON-state condition from OFF-state condition due to the formation of the inversion layer of the electrons and depletion of the holes from the channel [19]. The energy levels of the conduction band and valance band are high in the OFF-state condition as compared to the energy levels of the conduction band and valance band in the ON-state condition Fig. 2(b). The bands bend downwards in ON-state because when a positive gate voltage is applied in the polysilicon gate, the Fermi potential (potential between Fermi level and intrinsic Fermi level) decreases due to an increase in the surface potential, and this result in large electron carriers in the intrinsic (initially) channel region [20]. The introduction of these high electrons shifts the conduction band down towards the Fermi level.

Simultaneously the holes are also de-voided from the channel due to positive potential on the gate therefore the valance band also shifts downwards away from the Fermi level.

Fig. 3 depicts the variation of electric field and potential in the OFF-state and ON-state conditions. It can be seen from Fig. 3(a) that the electric field uplifts in the interface of source-channel and suppressed at the interface of channel-drain when the device comes in the ON-state condition from the OFF-state, this is due to the application of the positive gate voltage along with the drain voltage [21]. The low electric field at the channel-drain interface indicates less control of the drain to the channel and hence the DL-NT-FET implies low short channel effects. On the other hand, the surface potential goes high in the ON-state as intended due to more bending in the energy bands, at this stage the surface becomes doubled that of Fermi potential.

Fig. 4 shows the variation of the electron mobility and electron-hole pair recombination rate of the DL-NT-FET in OFF-state and On-state conditions. The electron mobility goes lower at the source-channel interface and becomes higher at the channel-drain interface Fig. 4(a). It is because the electric field is higher at the source-channel interface and lower at the channel-drain interface as is seen in Fig. 3(a). It can be observed from Fig. 4(b) that the recombination rate of the electron-hole pairs is zero in the channel region ON-state condition of the device channel region.

The drain current variation with channel length is plotted in Fig. 5(a) and its extracted performance parameters are listed in Table 1, it is noted that on increasing the channel length the ION/IOFF ratio enhances while the threshold voltage and Average sub-threshold slope (AVSS) of the DL-NT-FET reduce. An augmentation of 2 orders in the ION/IOFF ratio and a reduction of 22% and 13% in the threshold voltage and AVSS respectively have been recorded on increasing the channel length from 15 nm to 35 nm. The impact of the gate work function variation on the transfer characteristics of the DL-NT-FET is shown in Fig. 5(b) and various device properties that are extracted from its transfer characteristics are mentioned in Table 2. It can be observed that the OFF-current (IOFF) reduces significantly as compare to the ON-current (ION) and therefore the ION/IOFF ratio enhances on increasing the gate work function. The threshold voltage also decreases on augmenting the gate work function whereas the AVSS initially decreases up to a work function of 4.5eV but then starts increasing. Six orders increment in the ION/IOFF ratio and an 81% reduction in the threshold voltage has been observed when the gate work function is augmented from 4.3eV to 4.7eV. Fig. 5(c) exhibits the variation of ID-VGS characteristics with temperature and the various performance parameters at different temperatures are summarized in Table 3. The IOFF value increases significantly on increasing the temperature while the small degradation in the ION has been noticed as a result of mobility degradation and velocity saturation. And therefore 6 orders diminution in the ION/IOFF ratio is noticed when the temperature is increased from 200 K to 450 K. threshold voltage and the AVSS both are rose with the temperature. The threshold voltage rises 92% while the AVSS rises 114% on increasing the temperature from 200K to 450K. The effect of nanotube radius on the transfer characteristics and hence on various performance parameters are depicted in Fig. 5(d) and Table 4 respectively. On enhancing the radius of the nanotube of the DL-NT-FET, the ION and IOFF both are increasing but the IOFF increases more rapidly as compare to the ION and therefore the ION/IOFF

ratio reduces. The ION/IOFF ratio is degraded by 3 orders on augmenting the radius from 8 nm to 16 nm. The threshold voltage and AVSS are increased by increasing the radius of the nanotube; there is an increment of 47% in threshold voltage whereas an increment of 19% in the AVSS has been observed while increasing the radius of the nanotube from 8 nm to 16 nm.

Table 1

Effect of gate work-functions on various device performance parameters of DL-NT-FET

Gate-work function (eV)	AVSS (mV/decade)	Threshold voltage(V)	I_{ON} (A/m)	I_{OFF} (μA/m)	I_{ON}/I_{OFF}
4.3	70.7	0.494785	41.29	930287	44.3891
4.4	68.7	0.394785	38.03	52766.2	720.727
4.5	68.3	0.294785	34.53	1935.24	17845.3
4.6	68.8	0.194785	30.93	64.15	482264
4.7	71	0.0947849	27.21	2.04	13316400

Table 2

Various device performance parameters at the different channel length of nanotube of DL-NT-FET

Channel length (nm)	AVSS (mV/decade)	Threshold voltage(V)	I_{ON} (A/m)	I_{OFF} (μA/m)	I_{ON}/I_{OFF}
15	74.58	0.219144	31.15	367.3	84711.9
20	68.8	0.194785	30.93	64.15	482264
25	67.7	0.18286	30.81	21.95	1403350
30	66.0	0.176297	30.70	11.26	2725660
35	64.57	0.170009	30.57	7.38	4141140

Table 3

Variation in the device performance parameters at various temperature conditions

Temperature (K)	AVSS (mV/decade)	The threshold voltage(V)	I_{ON} (A/m)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}
200	48	0.14432	31.9	0.024	1287990000
250	58.6	0.168484	31.44	2.68	11714000
300	68.8	0.194785	30.93	64.15	482264
350	80.7	0.222111	30.40	637.585	47691.7
400	89.2	0.249834	29.83	3624.34	8232.48
450	103.3	0.277697	29.22	14074.1	2076.18

Table 4

Various device performance parameters at the different radius of nanotube of DL-NT-FET

Radius(nm)	AVSS (mV/decade)	The threshold voltage(V)	I_{ON} (A/m)	I_{OFF} (μA/m)	I_{ON}/I_{OFF}
8	67.5	0.178221	24.17	13.05	1852290
10	68.8	0.194785	30.93	64.15	482264
12	72.2	0.212351	37.72	298.04	126582
14	78.1	0.231078	44.63	1308.17	34118
16	80.3	0.250602	51.70	5366.02	9635.24

Fig. 6 (a) shows the variation of transconductance with VGS at different channel lengths which is a specific figure of merit of a FET and it measures the precision in the conversance of gate voltage into the current. It is noticed from Fig. 6(a) that the transconductance increases with the increasing channel length (up to 25 nm) then it remains constant. The transconductance increases with the channel length because of higher change in drain current is obtained at the large channel length with a small change in gate voltage. At the 25 nm channel length, the obtained value of the gm is 5.2x10-5 S/μm at the gate voltage of 0.45 V. Fig. 6(b) depicts the changes in the gate to source capacitance (Cgs) and drain to source capacitance (Cgd) with the gate voltage. A proliferation of 39% is observed in the Cgs at the VGS of 0.45V on increasing the channel length from 20 nm to 35 m whereas no significant changes are observed in the Cgd for the same increment in the channel length.

The behavior of drain current concerning VDS for different values of VGS at the channel length of 20 nm and 35nm has been shown in Fig. 7(a), where it is again found that ID is more for channel length 20nm than that of for channel length 35nm. Moreover, it is also noticed that at smaller VGS, the saturation in

the drain current occurs earlier as compare to the large VGS; this is because of limited space-charge inversion in the channel which implies greater gate control over the channel. Fig. 7(b) shows how the output conductance (gds) varies with VDS where VGS is fixed at 1V and readings for 20nm and 35nm channels are taken. It is well known that gds is a crucial parameter in determining the intrinsic gain of a device and for better gain, it should be low. It can be seen from Fig. 7(b) that its value does not change with the channel length and the obtained value of the gds for the designed DL-NT-FET is 3.4x10-5 (S/μm).

The output characteristics (ID-VDS) at the various temperatures are plotted in Fig. 8(a) and it is observed that the drain current decreases with an increase in the temperature. The ID decreases with the temperature because scattering phenomena increase with the temperature and this results in low carrier mobility in the channel and hence low drain current at the higher temperature [22]. The ID degrades 15% on increasing the temperature from 200K to 400 K. Fig. 8(b) shows the variation of the output conductance (gds) with the VDS at different temperature and it is found that gds also degrades on increasing the temperature and it is due to the reduction of ID at the higher temperature.

The impact of the nanotube radius in the output characteristics and output transconductance is plotted in Fig. 9(a) and Fig. 9(b) respectively and it is found that both the parameters are increasing with augmenting the radius. The ID enhances the increasing radius because a large radius renders large space charges in the inversion condition and the large drain current implies the higher output transconductance. An increment of 100% in the drain current and 137% in the output transconductance has been noted when the radius of the nanotube increases from 8 nm to 16 nm.

Conclusion

This manuscript covers a proposed dopingless nanotube FET structure. Different characteristics of the device have been examined by TCAD simulated results. The obtained AVSS for 20nm channel length, the radius of 10nm simulated at 300K is 68.80mV/decade which has much scope of improvement by optimization of the device. A comparative analysis of transfer characteristics (ID-VGS), transconductance (gm), gate capacitances (Cgs and Cgd), output characteristics (ID-VDS), and output conductance (gds), has been made by varying the channel length (Lg), radius (R), gate work function (Φ) and temperature. An increment of 100% in the drain current and 137% in the output transconductance has been noted when the radius of the nanotube increases from 8 nm to 16 nm. The gate capacitances Cgs and Cgd are higher for the longer channel. On increasing the temperature from 300k to 400K, the output conductance is found to decrease as well as the drain current gets saturated to a lower value whereas, by decreasing temperature to 200K, the opposite happens. An augmentation of six orders in the ION/IOFF ratio and 81% reduction in the threshold voltage has been observed when the gate work function is enhanced from 4.3eV to 4.7eV. The ION/IOFF decreases with a temperature rise, there are 6 orders diminution in the ION/IOFF ratio is noticed when the temperature is increased from 200 K to 450 K. The threshold voltage and the AVSS both are rose with the temperature. The threshold voltage rises 92% while the AVSS rises

114% on increasing the temperature from 200K to 450K. The transconductance curve has the highest peak value for the longest channel. It can thus be concluded that, after a thorough investigation of the behavior of the proposed dopingless nanotube FET parameters under several variations, it can be well understood that there are a good number of challenges to get the optimized results.

Declarations

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Conflict of Interest:

The authors declare that they have no conflict of interest.

Author contributions:

All authors have equally participated in the preparing of the manuscript during implementation of ideas, findings results, and writing of the manuscript.

Availability of data and material:

current submission does not contain the pool data of the manuscript but the data used in the manuscript will be provided on request.

Compliance with ethical standards:

The Authors accepted principles of ethical standard and they have no conflict of interest.

Consent to participate:

Informed consent.

Consent for Publication:

Consent is granted.

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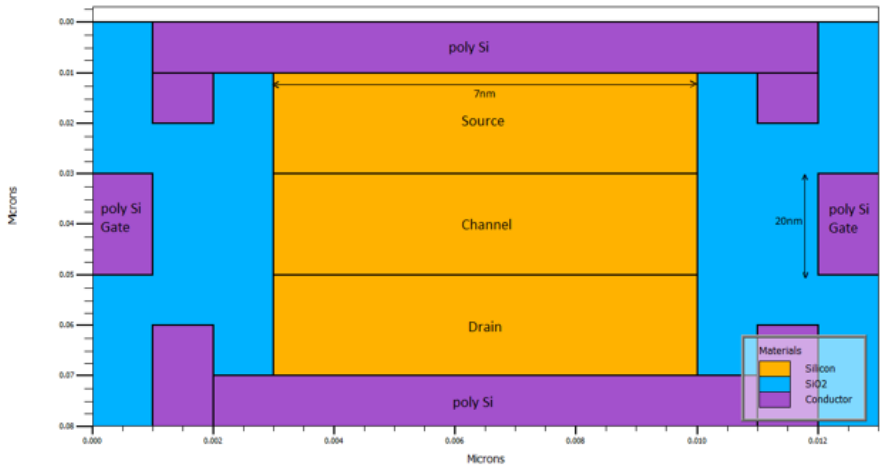
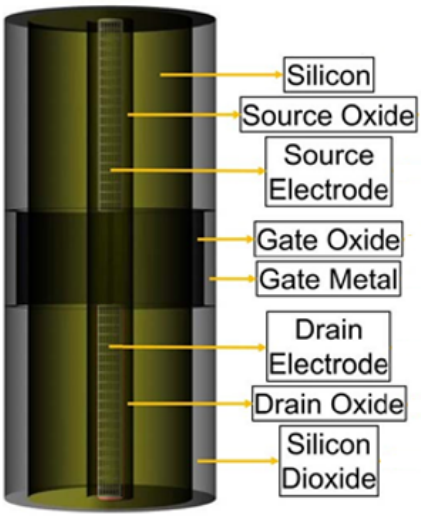
Figures



(a)



(b)

Figure 1

(a) 2-D cross-sectional view of the proposed device (b) 3-D view of the proposed device

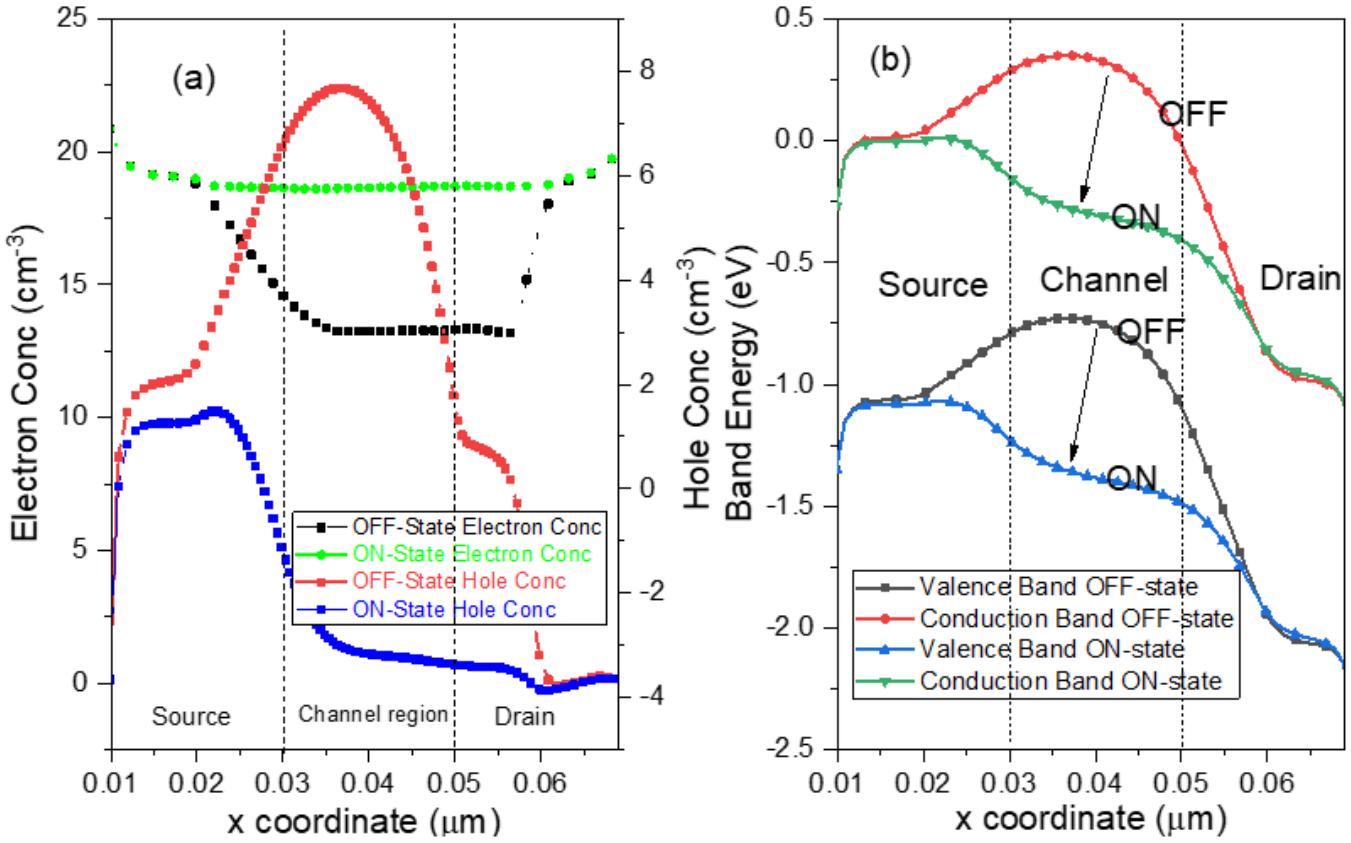


Figure 2

Variation of (a) Electrons and holes carrier concentration and (b) the energy band diagram of DL-NT-FET in OFF condition (VGS=0V and VDS=1V) and in ON condition (VGS=1V and VDS=1V), x coordinate shows the distance from the source to drain along the channel

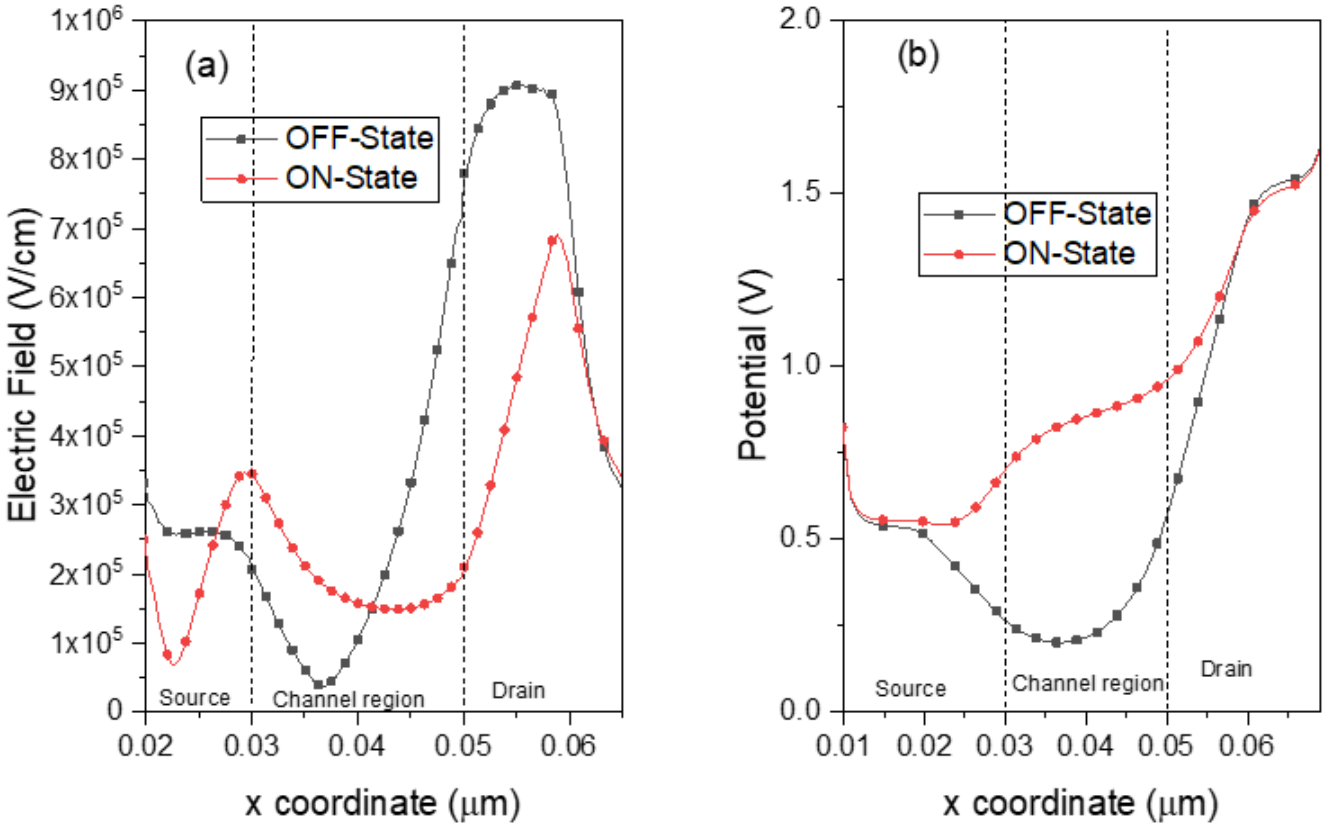


Figure 3

Variation of (a) Electric Field and (b) Potential of DL-NT-FET in OFF condition (VGS=0V and VDS=1V) and in ON condition (VGS=1V and VDS=1V), x coordinate shows the distance from the source to drain along the channel

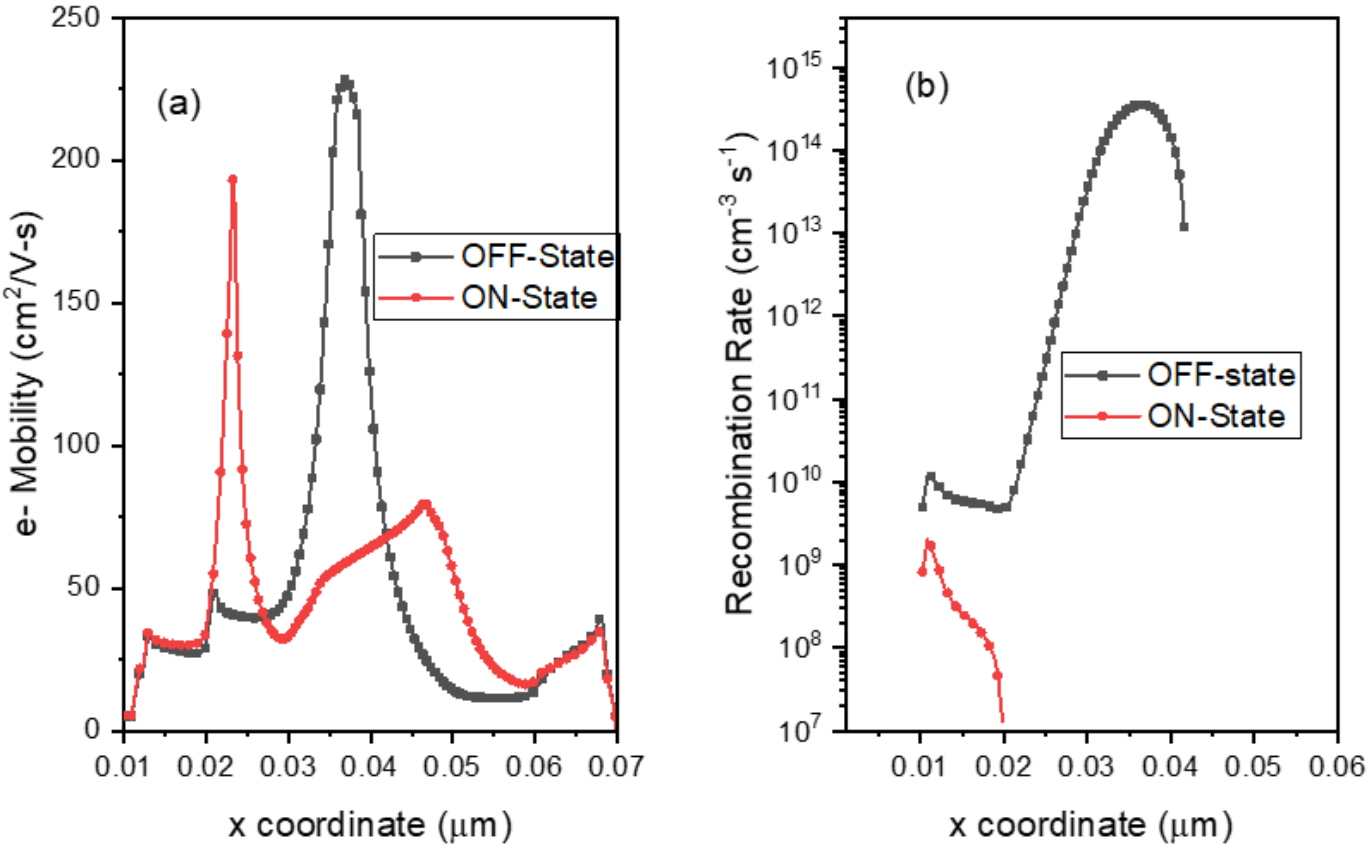


Figure 4

Variation of (a) Electron Mobility and (b) Electro-hole recombination rate of DL-NT-FET in OFF condition (VGS=0V and VDS=1V) and in ON condition (VGS=1V and VDS=1V), x coordinate shows the distance from the source to drain along the channel

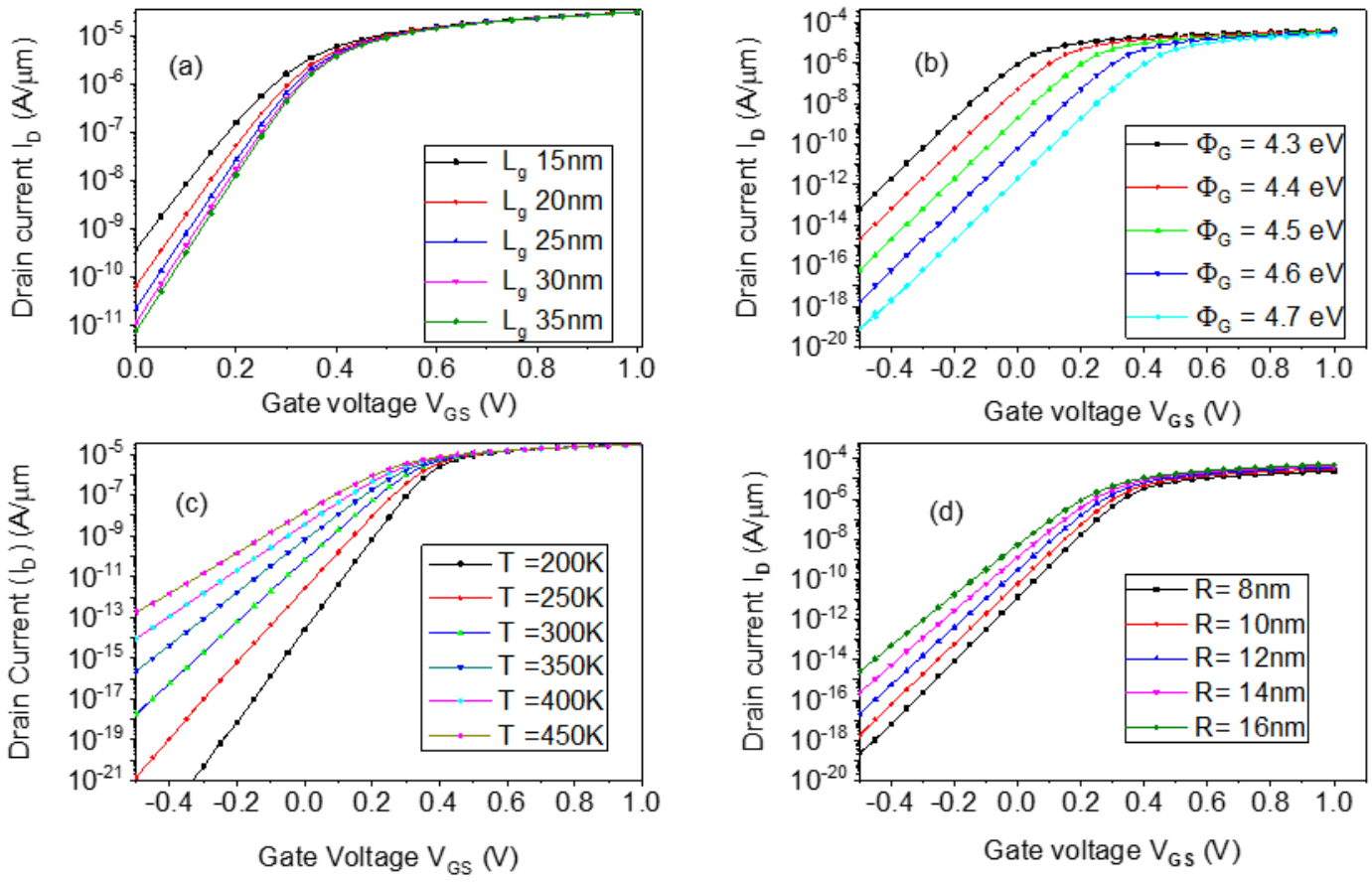


Figure 5

Variation of (ID-VGS) characteristics of the DL-NT-FET at VDS=1V for (a) the varying the channel length (Lg) (b) the varying the gate electrode work function (ΦG) (c) at various temperature (T), and (d) the varying the radius (R) of the DL-NT-FET.

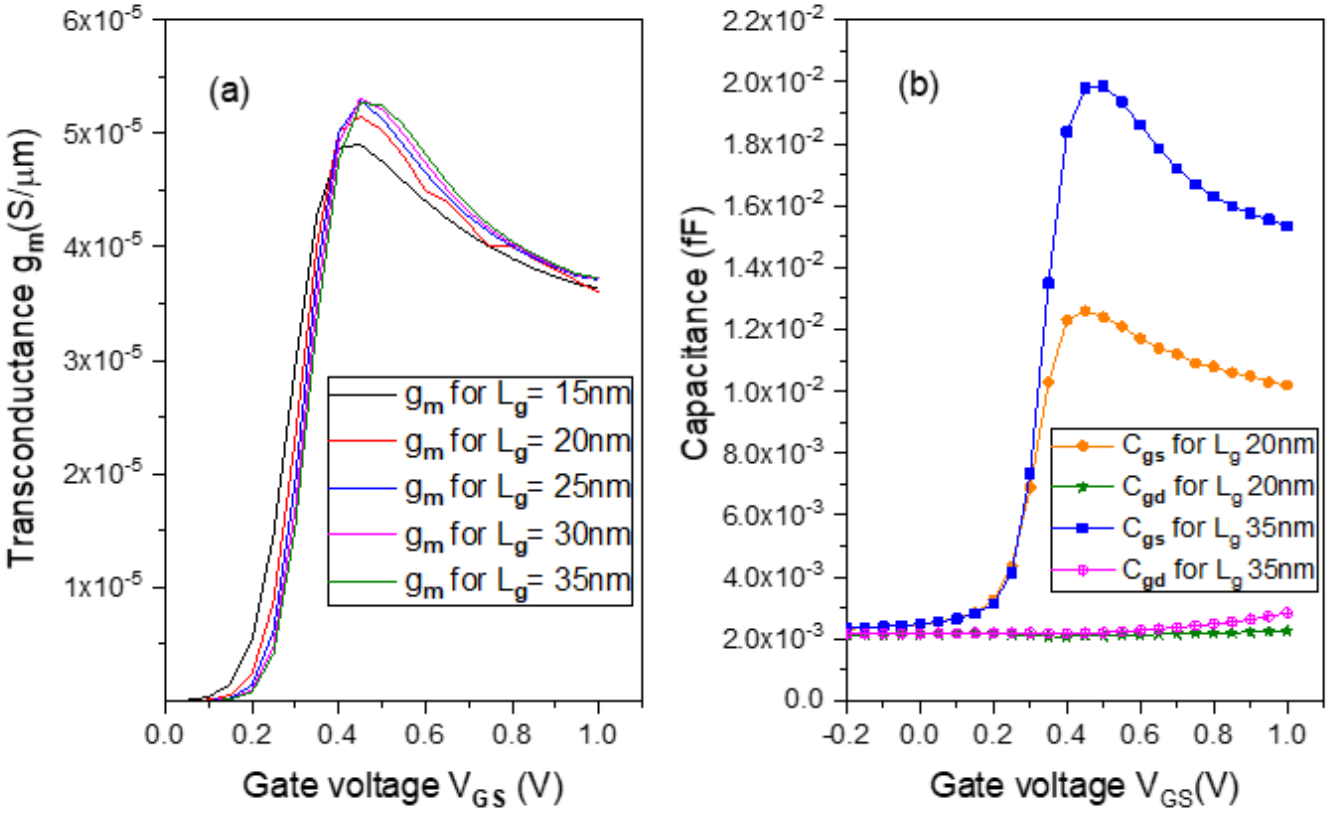


Figure 6

Variation of (a) transconductance (gm) and (b) gate to source capacitance (Cgs) and gate to drain capacitance (Cgd) with gate voltage at various channel length and VDS=1V

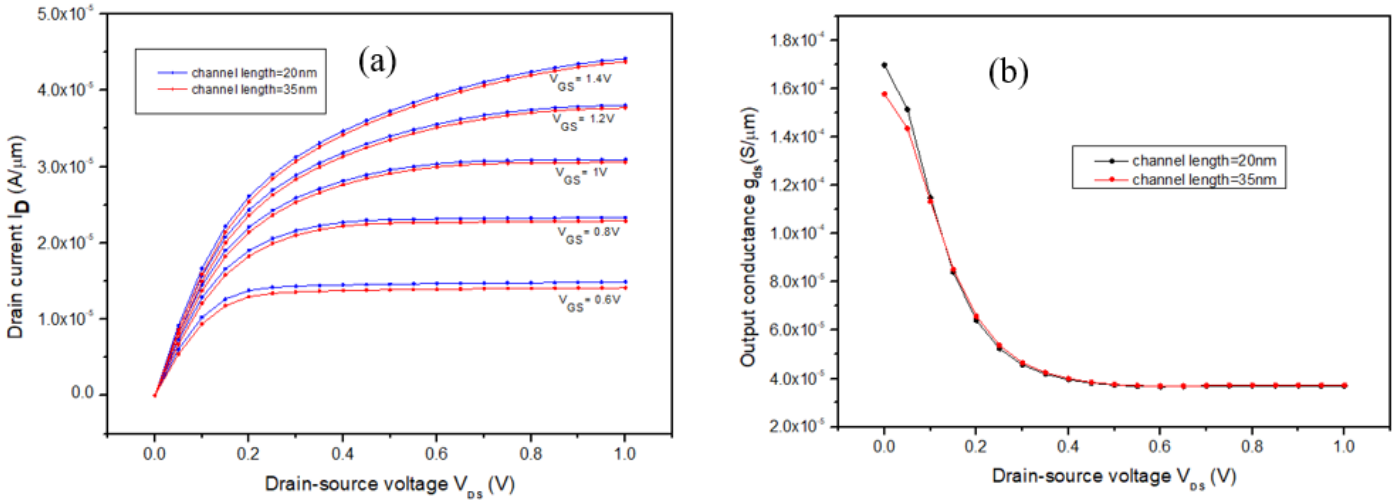


Figure 7

(a) Output characteristics for channel lengths 20nm and 35nm at different VGS. (b) Output conductance vs VDS for channel lengths 20nm and 35nm at VGS=1V.

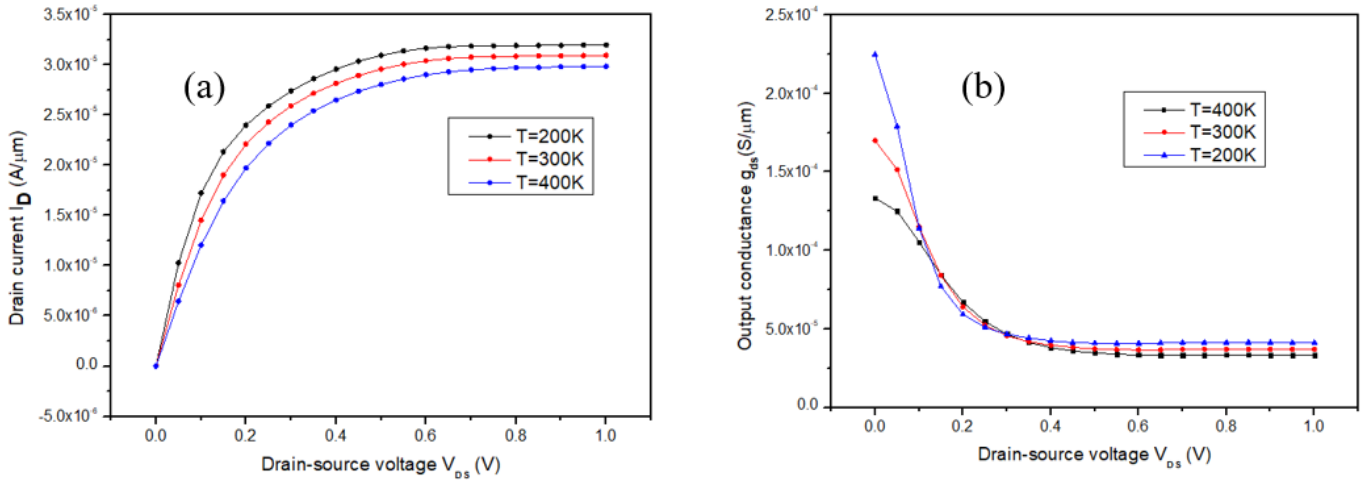


Figure 8

Variation of (a) output characteristics (IDS-VDS) at different temperatures and (b) output conductance for different temperatures (both at VGS=1V)

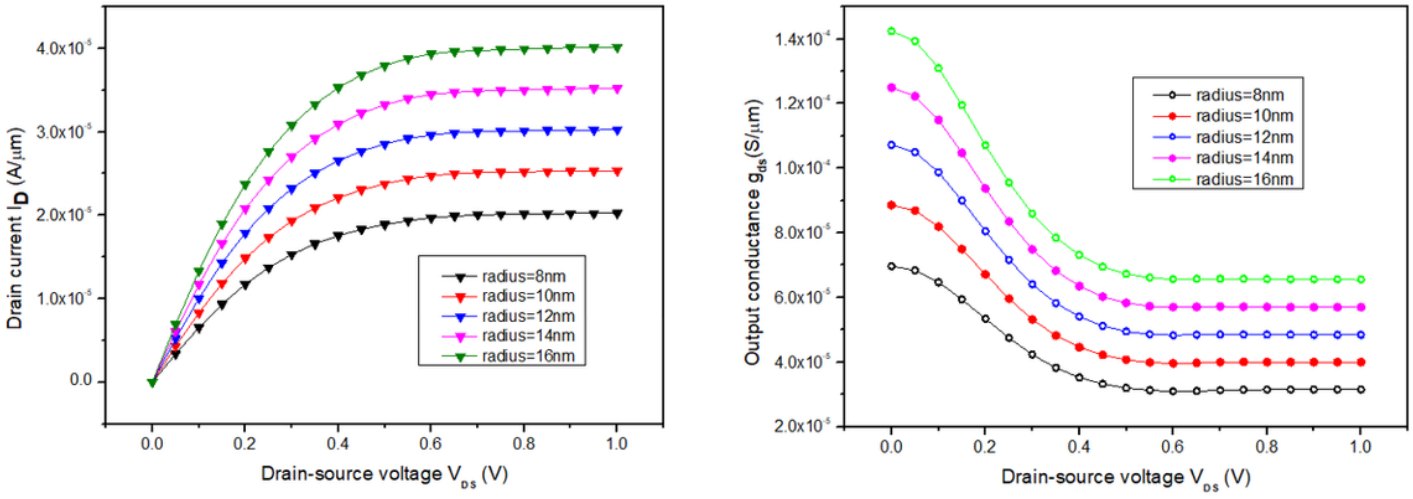


Figure 9

(a) Output characteristics for different radius (b) Output conductance Vs. VDS for the different radius (both at VGS=1V)