Impactful Study of F-shaped Tunnel FET

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Research Article

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Impactful Study of F-shaped Tunnel FET

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Abstract In this proposed work, a novel single gate F-shaped channel tunnel field effect transistor (SG-FC-TFET) is proposed and investigated. The impact of thickness of the source region and lateral tunneling length between the gate oxide and edge of the source region on analog and radio frequency parameters are investigated with appropriate source and drain lateral length through the 2D-TCAD tool. The slender shape of the source enhanced the electric field crowding effect at the corners of the source region which reflect in term of high On-current (I_{on}). The I_{on} of proposed device is increased up to $10^{-4} A/\mu m$ with reduced sub-threshold swing (SS) is 7.3 mV/decade and minimum turn-ON voltage ($V_{on} = 0.28 V$). The analog/RF parameters of SG-FC-TFET are optimized.

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1 Introduction

The steeper subthreshold slope devices are necessary to alter next generation low power device application in

Fig. 1 2D cross sectional schematic of SG-FC-TFET (Proposed device): $L_{drain} = 38nm$, $t_{drain} = 5nm$, $L_{gate} = 20nm$, $t_{gate} = (2t_{c-u} + T_{source}) = 35nm$, $t_{oxide} = 1nm$, $L_{c-u} = 71nm$, $L_{c-b} = 65nm$, $t_{c-b} = (t_{oxide} + t_{drain}) = 6nm$, $L_{source} = 40nm$, $t_{source} = 3nm$, $L_{tunnel} = 4nm$, $t_{c-u} = 16nm$, $T_{total} = 40nm$ and $L_{total} = 103nm$ with SiO_2 as gate oxide.

Fig. 2 Schematic corresponds to fig.1, Electric field strength analysis for different horizontal (AA', BB', and CC') and vertical cut lines (VV')

the field of electronics. The TFET is one of the most extensively investigated novel devices and their methodologies that can potentially surpass the 60 mV/decade MOSFET threshold at room temperature [1]. The TFET working operation is based on B2BT mechanisms and

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Fig. 3 (a) Transfer characteristics ($I_{ds} - V_{gs}$) (b) Transconductance (g_m) (c) Output Transconductance (g_{ds}) (d) Intrinsic gain

Fig. 4 (a) Gate to drain capacitance (C_{gd}) (b) Gate to source capacitance (C_{gs}) (c) Cut-off frequency (f_t) (d) Gain bandwidth product (GBP)

it is capable to attain a smaller SS value. However, the ambipolar behavior (high ambipolar current ($I_{amb} \approx 10^{-7}$ A/ μ m)) and low I_{on} ($\approx 10^{-6}$ A/ μ m) for which TFET can be realized by a small tunneling junction with limiting SCi region. To get the better of these leading limitations of TFET, many researchers investigated different structures and materials by using antithetic concepts and techniques [2–5]. In this simulation based work, a novel SG-FC-TFET has been investigated and optimized to obtain high I_{on} , suppressed I_{amb} , and minimum V_{on} with the steeper sub threshold slope of $I_d - V_{gs}$ curve. Along with this, the analog and radio frequency performance parameters were analyzed through the 2D-TCAD tool, to optimize the device performance for high frequency applications with low power consumption.

2 Designed device specifications

The 2D cross-sectional view of the device structure under study is illustrated in fig.1 and it resembles a finger-like ultra-thin N-type source region (dark green color) which is completely enclosed by a lightly doped P-type channel region. Because of complete insertion of source in channel region the tunneling area is increased and at the corner of source region, electric field crowding

effect came into existence. A metal gate ($WF_{gate} = 4.6$ eV) with a SiO_2 as gate oxide is used to improve the controllability over channel region. Along with different colors displayed in fig.1 defining various regions of simulated device like oxide, source, gate, channel, drain electrodes and their region, etc. The simulated device is silicon-based with drain doping $N_{DN} = 1 \times 10^{18} cm^{-3}$ (N+ type), source doping $N_{SP} = 1 \times 10^{20} cm^{-3}$ (P+ type), channel doping $N_{CP} = 1 \times 10^{15} cm^{-3}$ (P-type) and SiO_2 ($k = 3.9$) as gate oxide material.

From a fabrication point of view, self-align process would be used to fabricate the proposed device. The key steps for self align process flow are as follows: (1) Epitaxial layer grown for P+ type silicon layer, active region patterning, and SiO_2 hard-mask deposition (2) Mesa patterning is followed by SiO_2 buffer layer deposition (3) dummy gate deposition and etch-back process with drain region formation with the help of ion implantation and annealing process (4) for exposure of dummy gate, chemical mechanical polishing can be used (5) after that, for lateral tunneling region epitaxial layer is grown and at the last (6) oxide/metal gate formed by atomic layer deposition [6].

Fig. 5 (a) Gain frequency product (GFP) (b) Transconductance frequency product (TFP) (c) Transconductance generation factor (TGF) (d) Transit time

3 Results and Observations

The SG-FC-TFET is simulated in a 2D-TCAD simulator using nonlocal B2BT, SRH, FLDMOB, auger, FERMI, and CONMOB models. Along with, quantum tunneling region (qt region) for accurate lateral tunneling of electrons and holes at both interfaces (SCi and DCi).

The electric field (ELF) variation of proposed device along with different cut lines is illustrated in fig.2. The band bending of energy bands is sharper when the device is in ON-state which indicates the higher tunneling probability at SCi. The ELF plays an important role in the proposed device operations, hence it can be analyzed in different regions by imposing cut lines. AA' (Black circle) and BB' (Red upward triangle) horizontal cut lines are used to compare ELF at the corners of source region where ELF crowding takes place [7, 8]. Along with, CC' (Green square) cut line is used to analyze the ELF for complete device length including DCi. Here, we can see that ELF at DCi junction in range of 1.5×10^5 V/cm (lower peak of green graph) and 4.5×10^5 V/cm (Upper peak of green graph) throughout the channel region. For analysis of ELF crowding effect at corner and flat region of source, VV' cut line used (Blue downward triangle), from which we can observe that at the corner of source region ELF is very high ($E_{corner} = 4 \times 10^5$ V/cm) compare to flat region ($E_{flat} = 2.3 \times 10^5$ V/cm). As we depict, the high ELF at source corners (fig.2), causes higher drain current due to improved tunneling probability at SCi. From fig.3a, we can observe that the drain current (I_{ds}) increased rapidly w.r.t., V_{gs} at fixed $V_{ds} = 0.7$ V.

The slope of $I_{ds} - V_{gs}$ curve defines the amplification ability of the device, which is also known as g_m . The g_m of a device also depends on the I_{ds} [9, 10]. Hence, higher I_{ds} reflect in terms of higher g_m in the range of $830 \mu S$ (fig.3b). On the other hand, g_{ds} of the device is required low for better device performance because output resistance (R_{out}) of device inversely proportional to

g_{ds} . For better amplification property, we need a device with high R_{out} [11]. For the proposed device, the g_{ds} is obtained $23 \mu S$, as displayed in fig.3c. The ratio of g_m to g_{ds} is known as intrinsic gain, it should be high for better amplification property of a device [12]. From fig.3d, the intrinsic gain of the proposed device is increasing with V_{gs} (up to 0.9 V) and attain the peak value 68 obtained as an ratio. Furthermore, it starts decreasing due to mobility saturation of charge carriers a significant reduction been observed in g_m .

The radio frequency (RF) parameters play a very crucial role in the circuit level analysis of the device. Regarding this, the parasitic capacitances (C_{gd} and C_{gs}) are analyzed and depicted by fig.4a and 4b. The C_{gd} is a critical parameter that affects many other RF parameters (f_t , GBP, etc.) [11]. The lower value of capacitances are observed in this proposed device because of less accumulation of charge carriers at SCi and collected by drain region. The reduced value of C_{gd} helps to improve the gate controllability over the channel region with enhanced f_t and GBP values of proposed device [12], as illustrated in fig.4c, 4d. The f_t and GBP increased to achieve their apex, then with higher C_{gd} it starts decreasing.

To explain the trade-off between intrinsic gain and cut-off frequency, another parameter is introduced named GFP. It is increasing with V_{gs} due to an increment in intrinsic gain and f_t (fig.5a). Its curves start decreasing due to mobility saturation of the charge carriers which are responsible for existence of parasitic capacitances. Along with, TFP and TGF are also examining to check the device efficiency and consumption of power. TFP defines the relation between power and bandwidth [12]. Therefore, a higher value of TFP = 0.31 GHz (fig.5b) indicates that the proposed device is suitable for low-power applications. On the other hand, TGF defines the device efficiency in terms of circuit operation. The higher value of TGF reflect in terms of high device efficiency [12]. From fig.5c, we can observe that TGF of

$8 \times 10^4 \text{ V}^{-1}$ is achieved for the proposed device (SG-FC-TFET).

The transit time (τ) is inversely propositional to f_t . For higher f_t , transit time is less [6]. In other words, τ represents the delay of a device, so the speed of SG-FC-TFET is improved with a reduced value of τ . From fig.5d, we can analyze that τ is in the range of $210.5 \mu\text{s}$, which indicates that the proposed device can be used in digital circuits with the advancement of high speed as well as low power consumption [13]. According to the above impactful studies carried out, the proposed device (SG-FC-TFET) is best suited for low power high speed with enhanced RF performance.

4 Conclusion

In this study, we have inspected the solitary characteristics of SG-FC-TFET. It is worth pointing of the effect of a finger-like shape of the source region on analog/RF parameters is investigated using a 2D-TCAD simulator in this analysis. The proposed device achieved $I_{on} = 4.35 \times 10^{-4} \text{ A}/\mu\text{m}$, $I_{ambi} = 6.35 \times 10^{-18} \text{ A}/\mu\text{m}$, $I_{on}/I_{off} = 6.85 \times 10^{13}$, $V_{on} = 0.28 \text{ V}$ and SS of 7.3 mV/decade . Along with these results, some important parameters were also examined to study the RF performance of the SG-FC-TFET device like g_m ($830 \mu\text{S}$), g_{ds} of ($23 \mu\text{S}$), C_{gd} of 0.23 fF , C_{gs} of 0.28 fF , $f_t = 370 \text{ GHz}$, GBP = 176 GHz , and GFP of 24 THz . To achieve high performance, some additional parameters related to the speed and power of the device are also investigated that as TFP (0.31 GHz), TGF ($8 \times 10^4 \text{ V}^{-1}$), and transit time ($210.5 \mu\text{s}$). The promising results obtained for the proposed design demonstrate its applicability in both analog and digital technologies.

Declarations

The manuscript follows all the ethical standards, including plagiarism.

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 - Prabhat Singh: Conceptualization, data curation, formal analysis, methodology, investigation, writing – original draft.
 - Dharmendra Singh Yadav: Supervision, validation, visualization, writing – review & editing
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References

1. Villalon, Anthony and Le Carval, Gilles and Martinie, Sebastien and Le Royer, Cyrille and Jaud, Marie-Anne and Cristoloveanu, Sorin, "Further insights in TFET operation," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2893–2898, Aug. 2014. DOI: 10.1109/TED.2014.2325600
2. Bagga, Navjeet and Kumar, Anil and Dasgupta, Sudeb, "Demonstration of a novel two source region tunnel FET," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 5256–5262, Dec. 2017. DOI: 10.1109/TED.2017.2759898
3. V. Nagavarapu, R. Jhaveri and J. C. S. Woo, "The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor," *IEEE Transactions on Electron Devices*, vol. 55, no. 4, pp. 1013–1019, April 2008. DOI: 10.1109/TED.2008.916711
4. Sang Wan Kim, Jang Hyun Kim, Tsu-Jae King Liu, Woo Young Choi, Byung-Gook Park, "Demonstration of L-shaped tunnel field-effect transistors," *IEEE transactions on electron devices*, vol. 63, no. 4, pp. 1774–1778, April 2016. DOI: 10.1109/TED.2015.2472496
5. Zhaonian Yang, "Tunnel field-effect transistor with an L-shaped gate," *IEEE electron device letters*, vol. 37, no. 7, pp. 839–842, July 2016. DOI: 10.1109/LED.2016.2574821
6. Seunghyun Yun, Jeongmin Oh, Seokjung Kang, Yoon Kim, Jang Hyun Kim, Garam Kim, Sangwan Kim, "F-Shaped Tunnel Field-Effect Transistor (TFET) for the Low-Power Application," *Micromachines*, vol. 10, no. 11, pp. 760–761, November 2019. DOI: 10.3390/mi10110760
7. Yukinori Morita, Takahiro Mori, Shinji Migita, Wataru Mizubayashi, Akihito Tanabe, Koichi Fukuda, Takashi Matsukawa, "Performance enhancement of tunnel field-effect transistors by synthetic electric field effect," *IEEE electron device letters*, vol. 35, no. 7, pp. 792–794, July 2014. DOI: 10.1109/LED.2014.2323337
8. Yeqing Lu, Guangle Zhou, Rui Li, Qingmin Liu, Qin Zhang, Timothy Vasen, Soo Doo Chae, Thomas Kosel, Mark Wistey, "Performance of AlGaSb/InAs TFETs with gate electric field and tunneling direction aligned," *IEEE Electron Device Letters*, vol. 33, no. 5, pp. 655–657, May 2012. DOI: 10.1109/LED.2012.2186554
9. Shivendra Yadav, Rahul Madhukar, Dheeraj Sharma, Mohd. Aslam, Deepak Soni, Neeraj Sharma, "A new structure of electrically doped TFET for improving electronic characteristics," *Applied Physics A*, vol. 124, no. 7, pp. 1–9, July 2018. DOI: 10.1007/s00339-018-1930-9
10. Alan C. Seabaugh, Qin Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010. DOI: 10.1109/JPROC.2010.2070470
11. Dharmendra Singh Yadav, Dheeraj Sharma, Bhagwan Ram Raad, Varun Bajaj, "Impactful study of dual work

- function, underlap and hetero gate dielectric on TFET with different drain doping profile for high frequency performance estimation and optimization,” *Superlattices and Microstructures*, vol. 96, pp. 36–46, August 2016. DOI: 10.1016/j.spmi.2016.04.027
12. Dharmendra Singh Yadav, Bhagwan Ram Raad, Dheeraj Sharma, “A novel gate and drain engineered charge plasma tunnel field-effect transistor for low sub-threshold swing and ambipolar nature,” *Superlattices and Microstructures*, vol. 100, pp. 266–273, December 2016. DOI: 10.1016/j.spmi.2016.09.029
 13. Behnam Sedighi, Xiaobo Sharon Hu, Huichu Liu; Joseph J. Nahas, Michael Niemier, “Analog circuit design using tunnel-FETs,” *IEEE transactions on circuits and systems I: regular papers*, vol. 62, no. 1, pp. 39–48, Jan. 2015. DOI: 10.1109/TCSI.2014.2342371

Figures

Figure 1

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Figure 2

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Figure 3

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Figure 4

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Figure 5

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