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Posted Date: April 5th, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-336166/v1>

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An Innovative Step-up DC-DC Converter for Fuel Cell-based Power Source to Decrease Current Ripple and Increase Voltage Gain with Low Stress and Switch Counts

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Abstract: As for the insufficient nature of the fossil fuel resources, the renewable energies as alternative fuels are much needed and highly heeded. To deliver the required electric power to the industrial and domestic consumers from DC renewable energy sources like Fuel Cell (FC), the power converter operates as an adjustable interface device. This paper suggests a new boost structure to provide the required voltage with wide range gain for FC power source. The proposed structure based on the boost converter and the quazi network, so-called SBQN, can effectively enhance the FC functionality against its high operational sensitivity to experience low current ripple, and also propagate voltage and current with low stress across its semiconductors. Furthermore, the switching power losses have been decreased to make this structure more durable. Full operational analysis of the proposed SBQN and its advantages over the conventional and famous structures has been compared and explained. To more evaluate the high-step up voltage capability of the proposed SBQN and validate the simulations results, a prototype of the single-phase converter has been constructed and tested in the laboratory.

Keywords: FC; SBQN; DC-based RESs; current ripple; voltage stress; high-step up voltage

1. Introduction

Renewable based-power systems have been widely used to indicate the environmental challenges and concerns resulting from fossil fuel exhaustion, energy cost growth and greenhouse gas emissions [1-3]. Among the wide variety of renewable energy sources (RESs), wind, solar, geothermal, biomass, fuel cell, and hydrogen energy are more common and widespread than other kinds [4, 5]. Due to the intermittent characteristic and wide operating range of these resources, an electric power converter-based network interface is required to adjust the output power [6, 7]. Since the conventional voltage and prevalent converters have a limited operating range, utilization of dc-dc converters as interface components is not cost-effective and efficient. The ZSC gives a single-stage voltage buck-boost conversion with low switching power losses that is found to be cut-price for DC-based RESs [8, 9].

FC source is such the DC-based RESs which provides a low voltage and high current from the direct combination of fuel and oxidizer without environmental pollution, noise emission and health hazard [10]. Direct production of the electricity without the thermodynamic limitations of the Carnot cycle is to convert the chemical energy of fuel into heat and mechanical energy, and accordingly electricity which reduces energy loss and achieves high electrical energy efficiency [11]. As a result of the development of the material technology in recent years, the power of FC source can meet the requirement of low voltage domestic components [12]. Since the voltage output of FC source is not sufficient to supply the inverter and consequently the output load, ZSC is used to provide the required voltage with wide voltage range [13, 14].

A number of studies have been performed to augment the DC voltage gain, and then lead to suggestion of dozens of the cascaded structures and transformers [15-17]. A mutual connection of three-winding with inductor-based LZSC is proposed as an upgraded dc-dc converter for hybrid output applications [18]. An advanced quasi-ZSC coupled with a single-phase three-level inverter is presented in [19] to increase the output voltage, whereas, it is modulated using an alternative phase opposition disposition pulse width modulation strategy to boost the dc-link voltage and balance the two series capacitor voltages via controlling the shoot-through state. A five-level neutral-point-clamped dual quasi-ZSC with a complementary inductor-capacitor is presented in [20] to impede the initial current of ZSC's inductor and appropriately boost the dc-link voltage. A quasi-ZSC with an additional switch and diode is suggested to enhance the boost factor which can be more suitable for the photovoltaic-based power system [21]. Since an almost complicated control strategy must be used for modular multilevel converters to balance the voltages of several modules, a disposition sinusoidal pulse width modulation is applied to operate as voltage modulator [22]. A Fuzzy-based DC-DC converter integrated with ZSC which is controlled by a modified switching strategy is proposed to create and boost the desired output voltage [23].

The deep and major drawbacks of such these converters are their large size inductor, high peak inverse voltage on switches, high total cost, low electrical energy efficiency and unqualified output voltage. Due to low voltage of DC-based RESs [20-24], their voltage must be increased to the required value without ignoring the essential voltage quality. That is to say, some DC-based RESs are connected in series to each other to obtain a high-level voltage, if so, it is inevitable to meet the high cost-price and complicated control circuits.

This paper suggests a novel SBQN topology to provide the high qualified voltage with wide range gain and low sensitivity to obviate the aforementioned drawbacks. Based on the configuration of the suggested SBQN topology, the rate of components along with the pinch off voltage of semiconductors is decreased, therefore, it will be more cost-effective than other topologies. Among the DC-based RESs, FC

source is appropriate choice to test the high-step up voltage capability of suggested SBQN, because of low output voltage and high sensitivity to the current ripples [25, 26].

Due to imperfect and non-ideal characteristic of semiconductors, when the switch changes from on state to off state and vice-versa with high frequency, the switching power losses takes place [27-29]. Beyond that, the switch has to withstand severe voltage and current stress as the charged energy of capacitors and inductors increase [30]. The voltage and current stress on the switch also heighten the switching power losses, undermines the switch longevity and degrades the converter efficiency [31]. To make the switch more durable and better performance of SBQN, the switching power losses must be decreased. The important benefit of this switching control strategy is for its low switching frequency, which will lead to mitigation of switching power losses.

At long last, full operational analysis of the proposed SBQN and its advantages over the conventional and famous structures has been compared and explained. The structure of proposed SBQN has been modeled using MATLAB/SIMULINK software. The high-step up voltage capability of the proposed SBQN along with its DC voltage quality has been evaluated under different scenarios. To more validate the simulations results, a prototype of the single-phase converter has been constructed and tested in the laboratory.

2. Fuel Cell Features and Functions

FC source actually operates as a battery albeit oxygen and hydrogen or methane are used as its fuels, indeed, some important kinds are: Proton Exchange Membrane Fuel Cell (PEMFC), Solid Oxide Fuel Cell (SOFC) [32]. The fuels have been electrolytically attained using a single system which operates in either electrolyzer state or fuel cell state [33]. Given the low operating temperature, high energy density and quick starting feature, the PEMFC has found significant attraction among different FC types [34]. Likewise, it has been being successfully advanced as a reliable and portable power source to meet the power demands of various domestic applications. Analogous response of anode and cathode in the Membrane Electrode Assembly (MEA) for can be expressed as follows [35]:

The anode response: $\text{H}_2 \rightarrow 2\text{H}^+ + 2\text{e}^-$

The cathode response: $1/2\text{O}_2 + 2\text{H}^+ + 2\text{e}^- \rightarrow \text{H}_2\text{O}$

MEA can be seen in the single PEMFC schematic presented in Fig. 1. MEA is commonly put into two metal platters which are mutually correlated to provide a bipolar platter when cells are stacked for higher voltages.

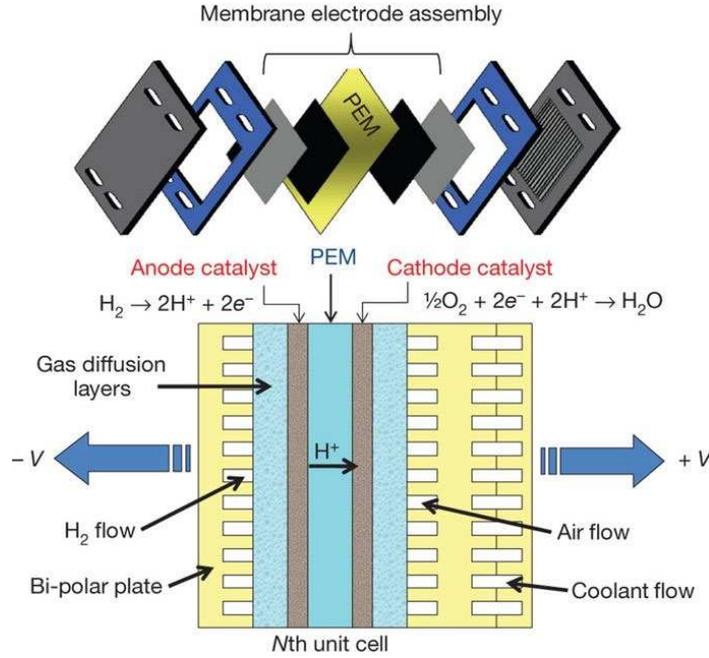


Fig. 1. Schematic of a single conventional PEMFC

The FC performance has been practically distinguished according to the polarization curve, which depicts the FC output voltage in terms of the load current. Based on the Tafel equation [36], the stack voltage can be presented as follows:

$$V_{stack} = V_{open} - V_{ohmic} - V_{activation} - V_{concentration} \quad (1)$$

Where,

$$V_{open} = N_0 \cdot (E^0 + E^1) = N_0 \cdot \left(-\frac{\Delta \bar{g}_f^0}{2F} + \frac{RT}{2F} \ln \left(\frac{p_{H_2} \cdot \sqrt{p_{O_2}}}{p_{H_2O}} \right) \right) \quad (2)$$

$$V_{ohmic} = R_{FC} \cdot (i + i_n) = R_{FC} \cdot I_{dc} \quad (3)$$

$$V_{activation} = N_0 \cdot \frac{RT}{2\alpha F} \ln \left(\frac{I_{dc}}{I_0} \right) \quad (4)$$

$$V_{concentration} = -c \ln \left(1 - \frac{I_{dc}}{I_{lim}} \right) \quad (5)$$

Where, N_0 indicates the number of cells, V_0 indicates the open cell voltage, R is the ideal gas constant, T is the stack temperature, F is the Faraday constant, P_{H_2O} , P_{H_2} and P_{O_2} respectively are the water, hydrogen and oxygen partial pressures, P_0 indicates the reference pressure, α indicates the charge transfer constant, I_{dc} represents the stack current, I_{lim} represents the limited stack current, I_0 represents the stack total current density and c is the experimental constant for concentrate voltage. The steady-state voltage considering one cell along with the power in terms of current density according to Eq. 1 can be attained as presented in Fig. 2.

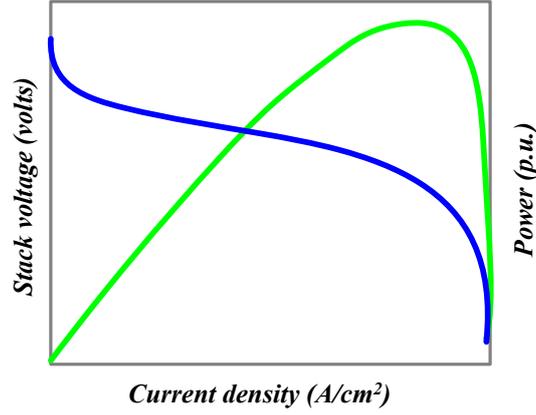


Fig. 2. Stack voltage along with power in terms of current density

3. Principle and Analysis of Proposed Converters

3.1. Structure of SBQN

Fig. 3 presents the overall structure of the suggested step up dc–dc converter. As can be seen, it contains a switched-quasi-Z-source network (L_1 , L_2 , C_1 , C_2 , and Q_2), power switch Q_1 , and high voltage side energy storage along with the capacitor filter C_3 . This converter has operated in the step-up state which enables the power unidirectionally flows from the low voltage side to the high voltage side.

To more simplification and comprehension, the following terms are assumed.

1) The power electronic components are considered to be ideal, i.e., the conducting or on-state resistance $R_{DS(on)}$ for the power electronic switches are neglected, and also the series resistance of the inductors and capacitors.

2) The ripples of the inductors' currents and the capacitors' voltages have linearly increased and decreased.

3) The capacitors' voltages are fixed.

Two basic operating modes *Mode I* and *Mode II* related to the proposed converter have been illustrated as follows:

During the operation of the SBQN in the step-up mode, the power has flowed from the low voltage side to the high voltage side. T_1 has here operated as a prime power switch, while D_1 and D_2 are the synchronous rectifiers. K is considered as the duty cycle of the gate signal T_1 :

$$K = \frac{t_0}{T} = t_0 \cdot f_s \quad (6)$$

Where, t_0 , T and f_s are respectively the conducting time, switching time and switching frequency.

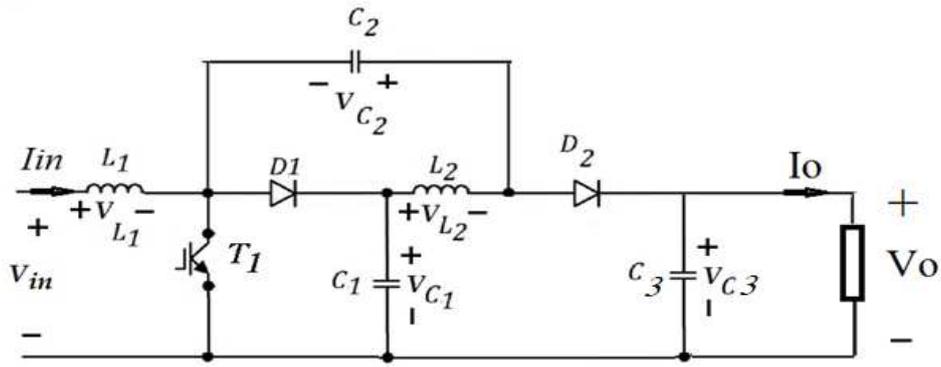
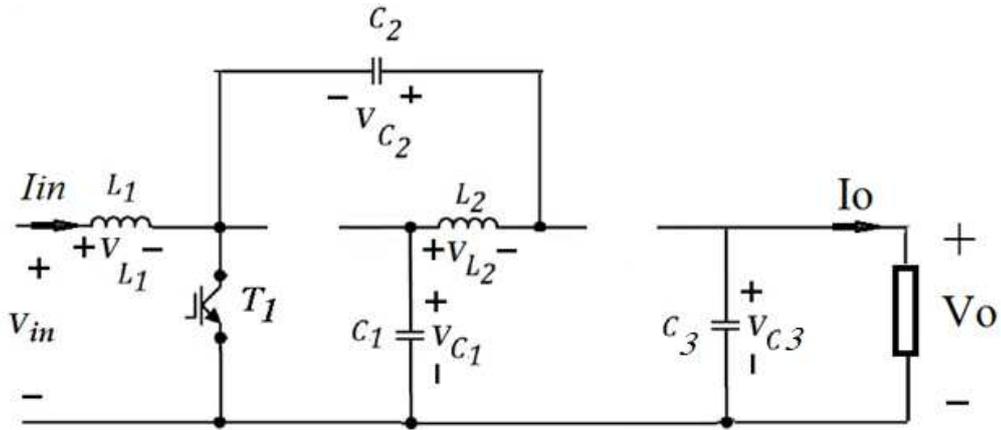
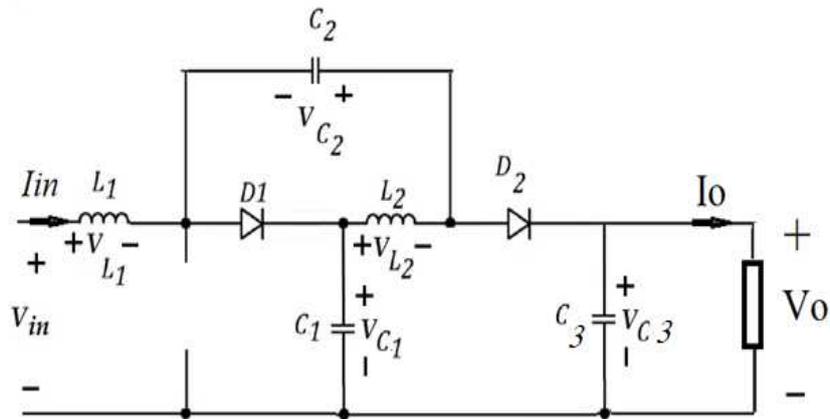


Fig. 3. Structure of proposed step-up SBQN

The current-flow paths operated in both states can be seen in Fig. 4(a) and (b).



(a)



(b)

Fig. 4. Current-flow paths of the proposed converter (a) State 1. (b) State 2.

State 1): During the conduction of T_1 , and D_2 and D_3 are switched off. Fig. 3(a) presents the current flow paths. In this condition, V_{in} has energized the inductor L_1 via T_1 , while the charge of capacitor C_1 is

depleted, and then the capacitor C_2 and the inductor L_2 via T_1 receive the required energy. The charge of capacitor C_3 provides the energy of the load R_{load} Boost. As for Fig. 3(a), the following equations can be derived in state 1:

$$\begin{cases} V_{L1} = V_{in} \\ V_{L2} = V_{C1} - V_{C2} \\ V_O = V_{C3} \end{cases} \quad (7)$$

State 2): In off-state of Q_1 , D_1 and D_2 have been conducting in reverse, while, Fig. 4(b) shows the current flow paths. The capacitor C_1 has been energized during this interval by means of the input voltage V_{in} and the inductor L_1 charge. The capacitor C_2 and inductor L_2 are connected to each other in parallel, and then connected with V_{in} and L_1 in series to energize the capacitor C_3 to transfer its energy to the load. Hence, the output voltage V_O becomes higher than the input voltage V_{in} . As for Fig. 4(b), the voltage of inductors and capacitors in state 2 can be presented as follows:

$$\begin{cases} V_{L1} = V_{in} - V_{C1} \\ V_{L2} = V_{C1} - V_{C3} = -V_{C2} \\ V_{C3} = V_{C2} + V_{C1} \\ V_O = V_{C3} \end{cases} \quad (8)$$

Based on the principle of inductor volt-second balance in average steady-state operation, the voltage gain has been extracted in terms of the duty cycle K in CCM state.

$$\overline{V_{L1}} = 0 = KV_{in} + (1 - K)(V_{in} - V_{C1}) \Rightarrow V_{C1} = \frac{V_{in}}{(1 - K)} \quad (9)$$

$$\overline{V_{L2}} = 0 = K(V_{C1} - V_{C2}) + (1 - K)(-V_{C2}) \Rightarrow V_{C2} = KV_{C1} \quad (10)$$

$$V_O = V_{C1} + V_{C2} \Rightarrow V_O = \frac{(1 + K)}{(1 - K)} V_{in} \quad (11)$$

3.2. Voltage stresses of the capacitors

In accordance with the (8) and (9), the capacitors' voltage stresses can be presented as follows:

$$\begin{cases} V_{C1} = \frac{V_{in}}{1-K} = \frac{V_O}{1+K} \\ V_{C2} = \frac{KV_{in}}{1-K} = \frac{KV_O}{1+K} \end{cases} \quad (12)$$

3.3. Average currents of inductor

In accordance with Fig. 4(a) and 4(b), the average currents of inductor for states 1 and 2 can be presented as follows.

State 1:

$$\begin{cases} I_{C1} = -I_{L2} \\ I_{C2} = I_{L2} \\ I_{C3} = -I_O \end{cases} \quad (13)$$

State 2:

$$\begin{cases} I_{C1} = I_{L1} + I_{C2} - I_{L2} \\ I_{C3} = I_{L2} - I_{C2} - I_O \end{cases} \quad (14)$$

Ignoring the losses, the inductor current can be calculated by:

$$I_{L1} = \frac{1+K}{1-K} I_O \quad (15)$$

Based on the principle of capacitor ampere-second balance in average steady-state operation, the average capacitor currents I_{C1} and I_{C2} has been extracted in terms of the duty cycle K in CCM:

$$\overline{I_{C1}} = 0 = -KI_{L2} + (1-K)(I_{L1} + I_{C2} - I_{L2}) \quad (16)$$

$$\overline{I_{C3}} = 0 = -KI_O + (1-K)(I_{L2} - I_{C2} - I_O) \quad (17)$$

Substituting the equations (15) and (16) into the (14) in (17)

$$(-K - 1 + K + 1 - K)I_{L2} + (1-K)I_{L1} - I_O = 0 \quad (18)$$

$$(-K)I_{L2} + (1-K)\frac{1+K}{1-K}I_O - I_O = 0 \Rightarrow I_{L2} = I_O \quad (19)$$

3.4. Voltage Stress of the semiconductors

Regardless of the voltage drop on the power switches, the voltage stress of semiconductors can be calculated by:

$$\begin{cases} VS_{T1} = VS_{D1} = V_{C1} = \frac{V_{in}}{1-K} = \frac{V_O}{1+K} \\ VS_{D2} = V_O - V_{C2} = V_O - \frac{KV_O}{1+K} = \frac{V_O}{1+K} \end{cases} \quad (20)$$

3.5. Current Stress of the semiconductors

In the same way, the current stress of semiconductors can be also calculated by:

$$\begin{cases} I_{T1} = \frac{2}{1-K} I_O \\ I_{D2} = I_{D3} = \frac{1}{1-K} I_O \end{cases} \quad (21)$$

3.6. Current ripple of inductors

According to the voltage drop of inductors in mode 1, their currents ripples can be calculated by:

$$V_{L1} = V_{in} = \frac{\Delta I_{L1}}{\Delta t} L_1 = \frac{\Delta I_{L1} \cdot f_s}{K} L_1 \Rightarrow \Delta I_{L1} = \frac{K}{f_s \cdot L_1} V_{in} \quad (22)$$

$$V_L = V_{C1} - V_{C2} = (1-K)V_{C1} = V_{in} = \frac{\Delta I_{L2}}{\Delta t} L_2 \Rightarrow \Delta I_{L2} = \frac{K}{f_s L_2} V_{in} \quad (23)$$

Where, the ripple of input current is equal to the ripple of inductor (L_1) current.

3.7. Voltage ripple of capacitors

During mode 1, inductor L_2 transfers its energy into the capacitors C_1 and C_2 . Thus, the voltage ripple of the capacitors can be calculated by:

$$\Delta V_{C1} = \frac{K}{f_s \cdot C_1} I_{L2} \quad (24)$$

$$\Delta V_{C2} = \frac{K}{f_s \cdot C_2} I_{L2} \quad (25)$$

The voltage ripple of the capacitor C_3 can be also calculated by:

$$\Delta V_{C3} = \frac{K}{f_s \cdot C_3} I_O \quad (26)$$

The general waveforms of the suggested SBQN in CCM are depicted in Fig. 2(a).

4. Power Semiconductor Switch Losses

The power electronic converter losses can be aggregated with power losses experienced by all semiconductor switches. As a rule, this problem has been characterized by three kinds of losses: blocking (OFF) state, conducting (ON) state and switching (transition between ON and OFF) state. Due to trivial value of leakage currents during blocking state [37], it is ignored. Thus, the conducting and the switching losses have been calculated as power switch losses.

4.1. Conduction Losses

The instantaneous conduction losses for transistor and diode can be generally presented as follows [38, 39]:

$$p_{c,T}(t) = (V_T + R_T i^\alpha(t)). i(t) \quad (27)$$

$$p_{c,D}(t) = (V_D + R_D i(t)). i(t) \quad (28)$$

Where, $p_{c,T}(t)$ and $p_{c,D}(t)$ respectively indicate the instantaneous conduction losses related to transistor and diode. V_T and V_D respectively indicate the conducting voltage drops related to transistor and diode. R_T and R_D respectively indicate the equivalent conducting resistances related to transistor and diode. Also, α indicates the transistor constant.

Let $N_T(t)$ and $N_D(t)$ be the numbers of transistors and diodes which conduct the current at instant t . based on Eq. 47 and Eq. 48, the average conduction losses is attained:

$$p_{c,avg}(t) = \frac{1}{\pi} \int_0^\pi ([N_T(t)V_T + N_D(t)V_D]. i_L(t) + [N_T(t)R_T i_L^{\alpha+1}(t) + [N_D(t)R_D i_L^2(t)]] d(\omega t) \quad (29)$$

4.2.Switching Losses

To extract the switching losses, the energy losses during the transition between ON and OFF states must be calculated. According to the Fig. 8, the voltage and current variations in this state are almost linear. The energy loss during the turn-on state is given as follows:

$$E_{on,j} = \int_0^{t_{on}} v(t)i(t) dt = \int_0^{t_{on}} \left\{ \left[V_{o,j} \frac{t}{t_{on}} \right] \left[-\frac{I}{t_{on}} (t - t_{on}) \right] \right\} dt = \frac{1}{6} V_{o,j} I t_{on} \quad (30)$$

Where, $E_{on,j}$ is the turn-on loss associated with the j th switch; t_{on} is the turn-on time; I is the current through the switch before turning off; $V_{o,j}$ is off-state voltage on the j th switch.

In the same way, the energy loss during the turn-off state can be presented as follows:

$$E_{off,j} = \int_0^{t_{off}} v(t)i(t) dt = \int_0^{t_{off}} \left\{ \left[V_{o,j} \frac{t}{t_{off}} \right] \left[-\frac{I'}{t_{off}} (t - t_{off}) \right] \right\} dt = \frac{1}{6} V_{o,j} I' t_{off} \quad (31)$$

Where, t_{off} indicates the turn-off time. I' indicates the current through the switch after turning on.

The switching loss is attained by summing the energy losses during transition state. Let's consider $I=I'$, then, the total switching losses can be presented as follows:

$$p_s = \sum_{j=1}^{N_{sw}} \left(\frac{1}{6} V_{o,j} I (t_{on} + t_{off}) f_j \right) \quad (32)$$

Where, f_j indicates the switching frequency

Finally, the total switching losses can be presented as follows:

$$p_{losses} = p_{c,avg} + p_s \quad (33)$$

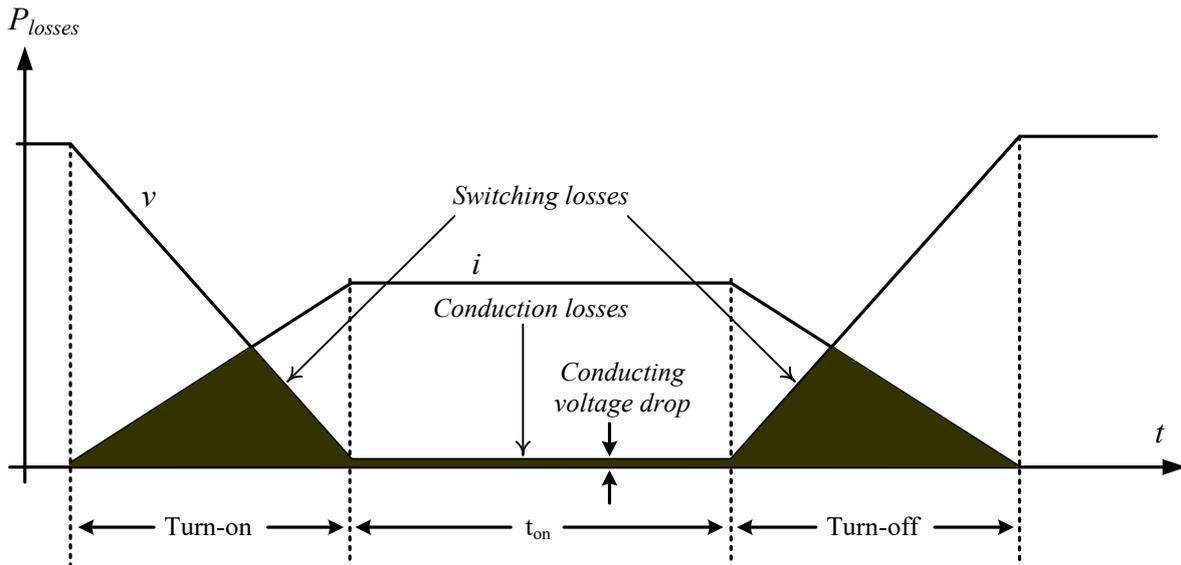


Fig. 5. Switching waveforms of transistor

5. Simulation, Experimental and Comparison Results and Discussion

5.1. Simulation verification

To verify the operation of the proposed converter, a case study has been structured which is presented in Fig. 6. Providing the required power via FC source for DC load is the main target of the case study. Its relevant parameters are tabulated in Table 1.

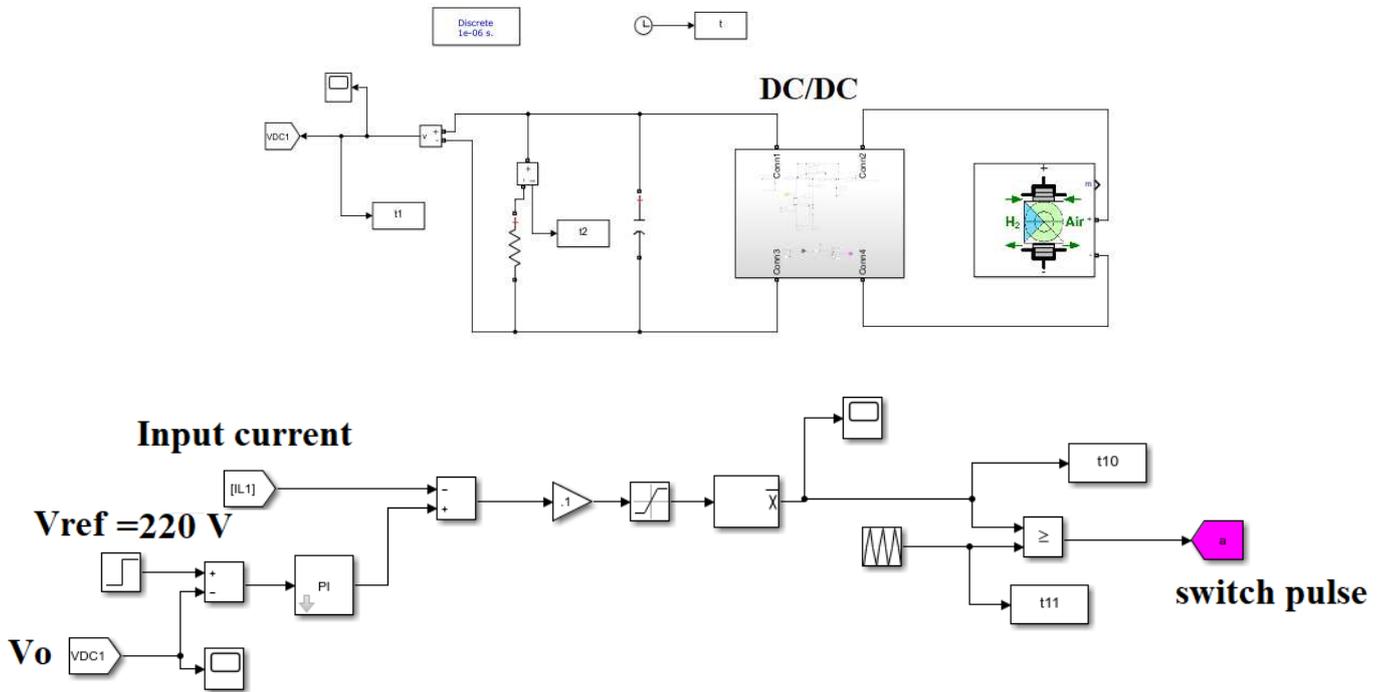


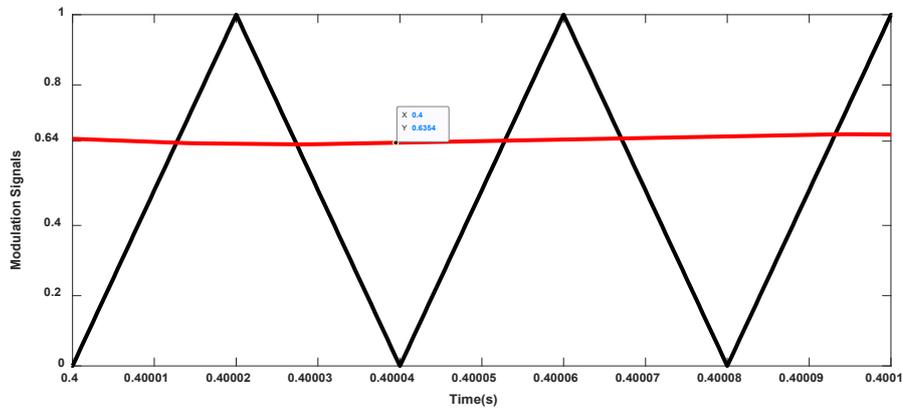
Fig. 6. The case study system with presence of SBQN.

Table 1: Case study parameters.

DC bus(V_o)	220 V
Input Voltage	48 V
L_1, L_2	500 and 1000 μ H
C_1, C_2 and C_3	470 μ F
Switching frequency	25000 Hz
Load	220 W

Such these simulation results have well demonstrated the performance of the proposed structure. As the FC's voltage becomes lower than DC bus, the SBQN will boost it. According to the Fig. 7, the dc/dc converter boosts the input voltage by changing duty cycle. Let duty cycle be 0.64, then FC's voltage becomes 48. Fig. 8 depicts both the output voltage and current:

$$V_o = 220V = \frac{(1 + 0.64) * 48}{(1 - 0.64)} V \quad (27)$$

**Fig. 7.** Modulation Signals.

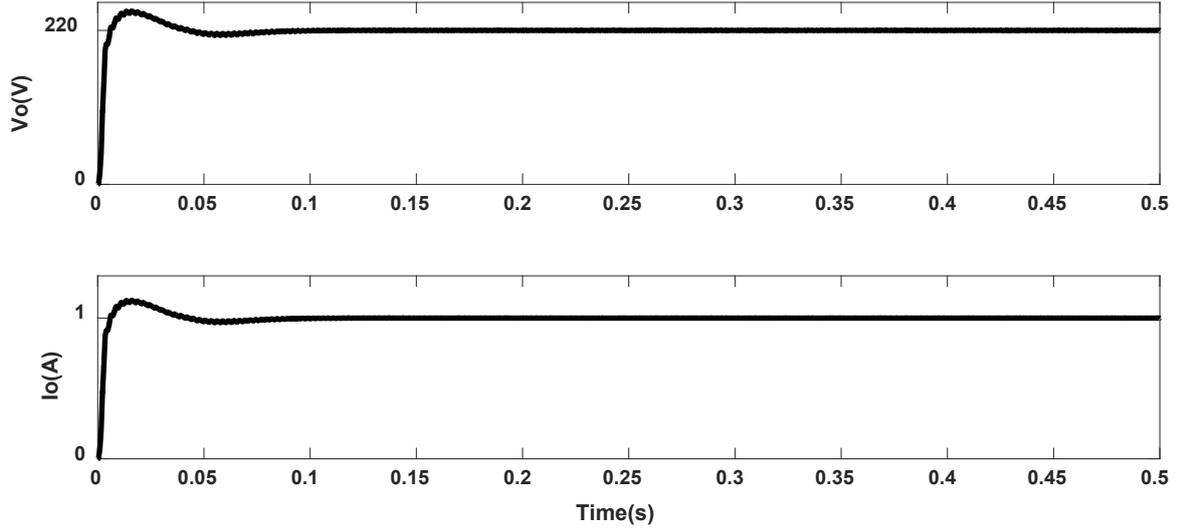


Fig. 8. Output voltage and current

Good thing, the SBQN needs switches and diodes with low standing voltage. According to Eq. 20, their voltages can be attained which are depicted in Fig. 9:

$$V_{T1} = V_{D1} = V_{D2} = \frac{220}{(1 + 0.64)} = 134.146V \quad (28)$$

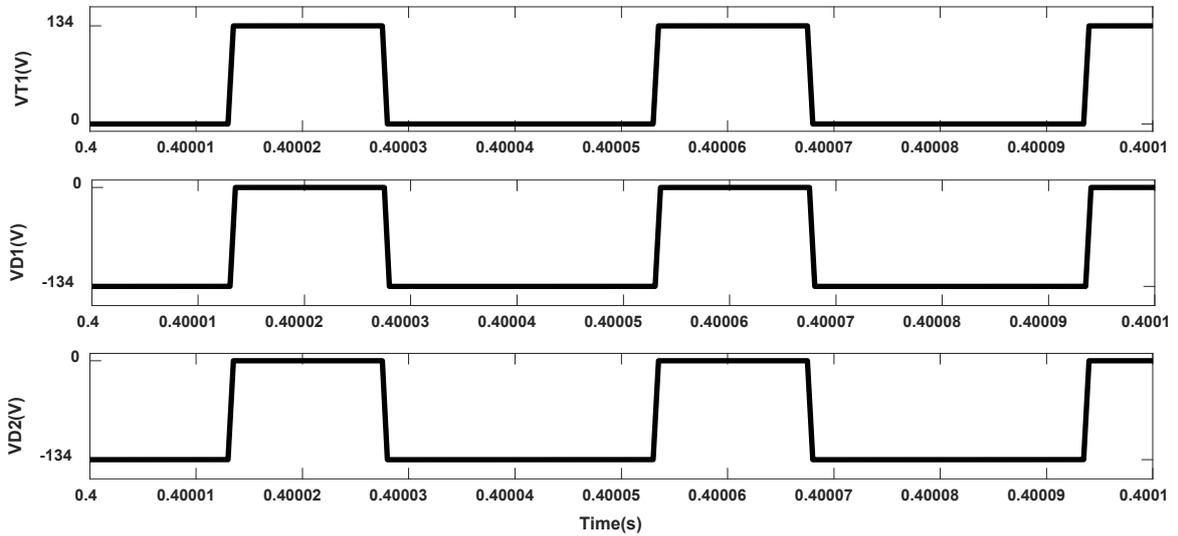


Fig. 9. Voltage of semiconductor.

Meanwhile, Fig. 10 shows the current of inductors and the voltage of capacitors which respectively satisfy the charge and discharge of inductors and capacitors. According to Eq. 22, the ripple of input current can be attained which is 2.4. Fig. 10 validates the accuracy of proposed structure:

$$\Delta I_{L1} = \frac{0.64}{25000 * 0.5 * 10^{-3}} * 48 = 2.45 \quad (28)$$

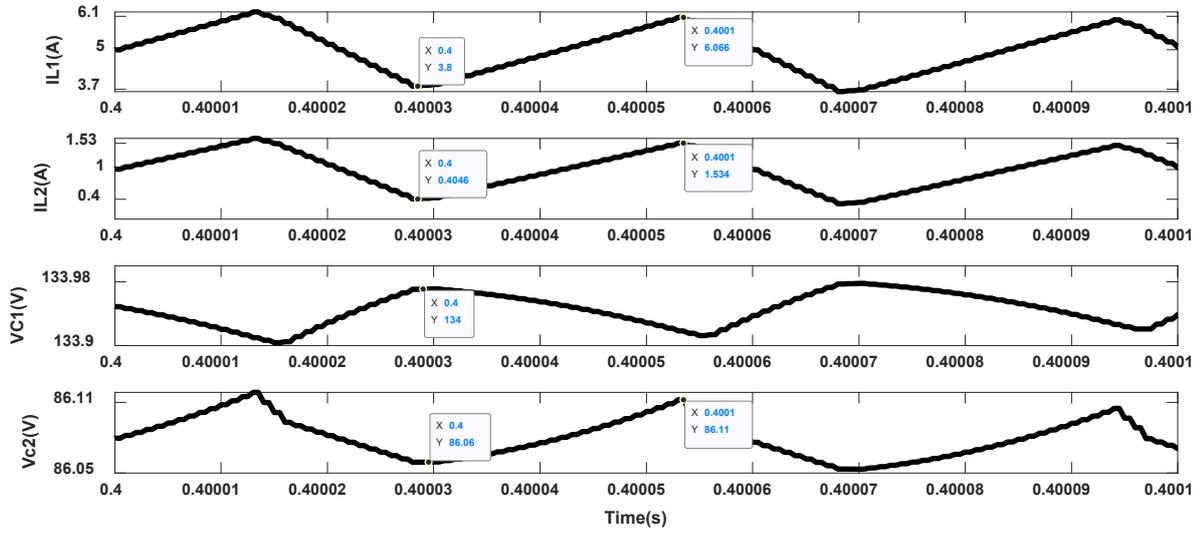


Fig. 10. Current of inductors and voltage of capacitors

5.2. Experimental verification

To verify the performance of the presented dc/dc converter, a prototype circuit is essentially provided in the laboratory. A developed 220 W prototype is shown in Fig. 11, and its relevant values are presented in Table 1. A Texas Instruments microcontroller TMS320F28335 is taken into account for the voltage loop controller. The SBQN includes two inductors, one IXFT36N50P switch, two RURG8060 diodes, and two capacitors. Fig. 12 presents the voltage stress waveforms of T_1 , D_1 and D_2 during the operation of the proposed converter in the step-up mode at the rated condition. As can be seen, the voltage stress on T_1 , D_1 and D_2 is 134 V which almost equals half of the high-side voltage. It is worth mentioning that, Channel 1 shows the voltage of switch and Channel 2 and 3 shows the voltage of diodes, whereas T_1 and D_1 or T_1 and D_2 must not be simultaneously turned on. At the same condition, the current waveforms of L_1 and L_2 are presented in Fig. 13. The current ripple rate of L_1 and L_2 are respectively about 2.45 A and 1.2 A which satisfy the inductor design due to its low average current value. As can be seen, the input current i.e. L_1 is continuous wave with low ripple. Likewise, Fig. 14 shows the output voltage which keeps at 220 V, while

the input voltage is 48 V. At the same condition, the voltage of capacitors V_{C1} and V_{C2} are shown in Fig. 14. Voltage of C_1 and C_2 are respectively about 85 V and 134 V, which satisfy the capacitor design.

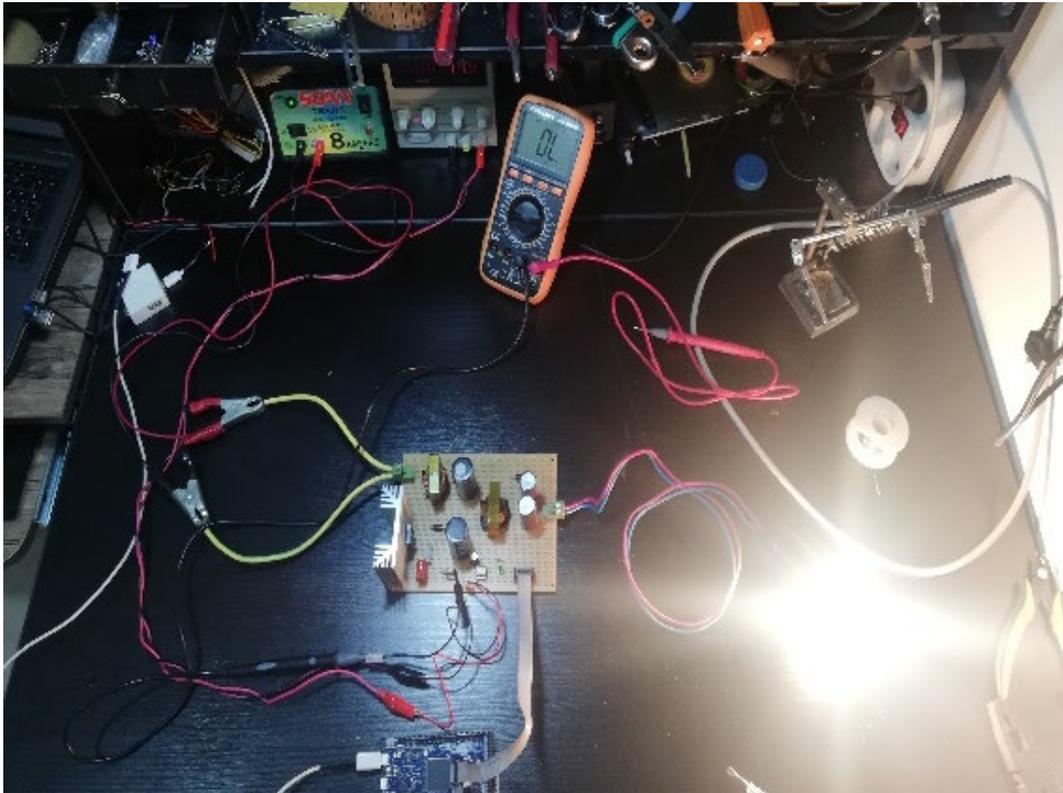


Fig. 11. Prototype model of proposed converter

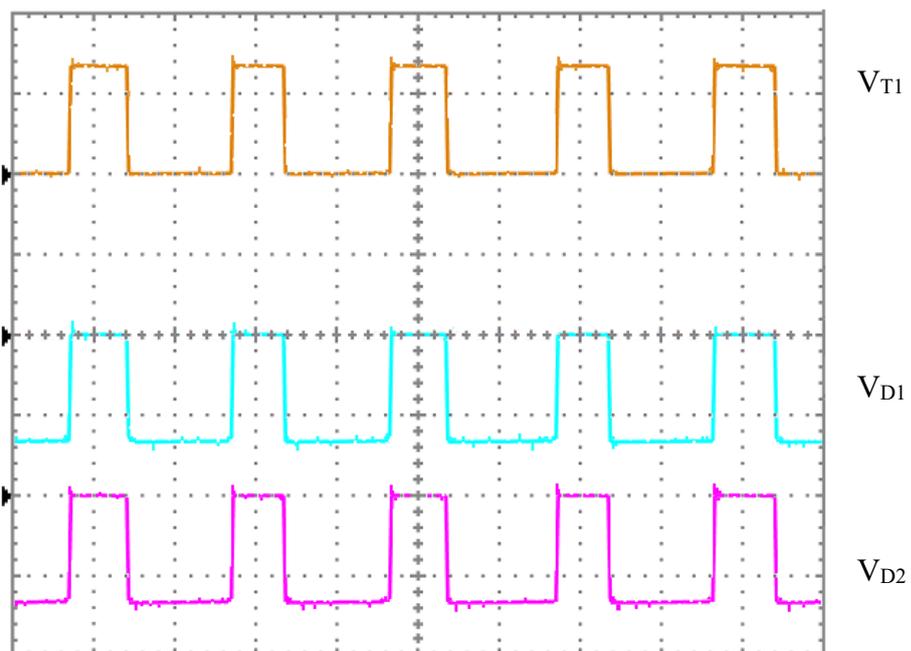


Fig. 12. Voltage of semiconductors (Time/div=2.5 μ s, Volt/div=100 V)

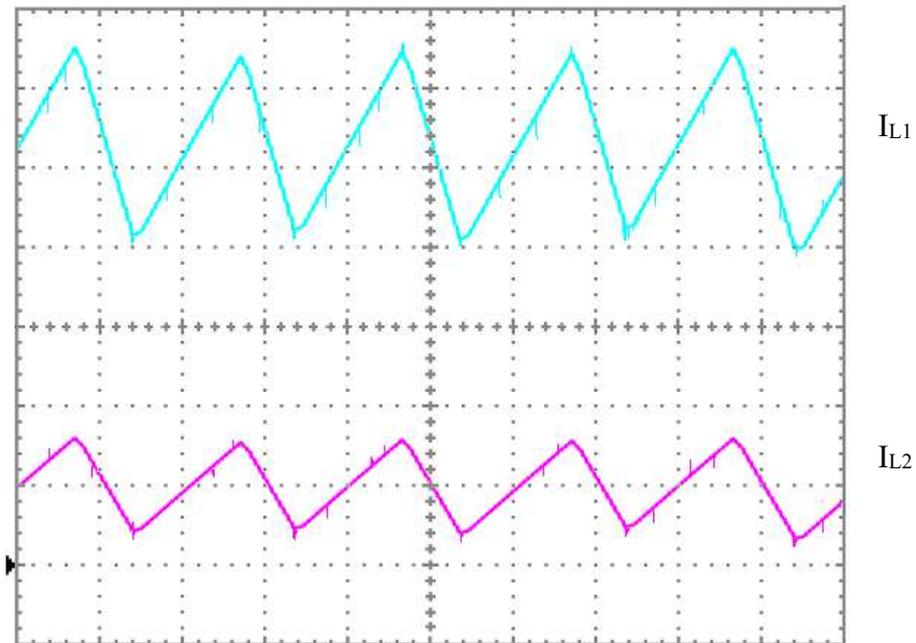


Fig. 13. Inductor currents (Time/div=2.5 μ s, Volt/div=1V)

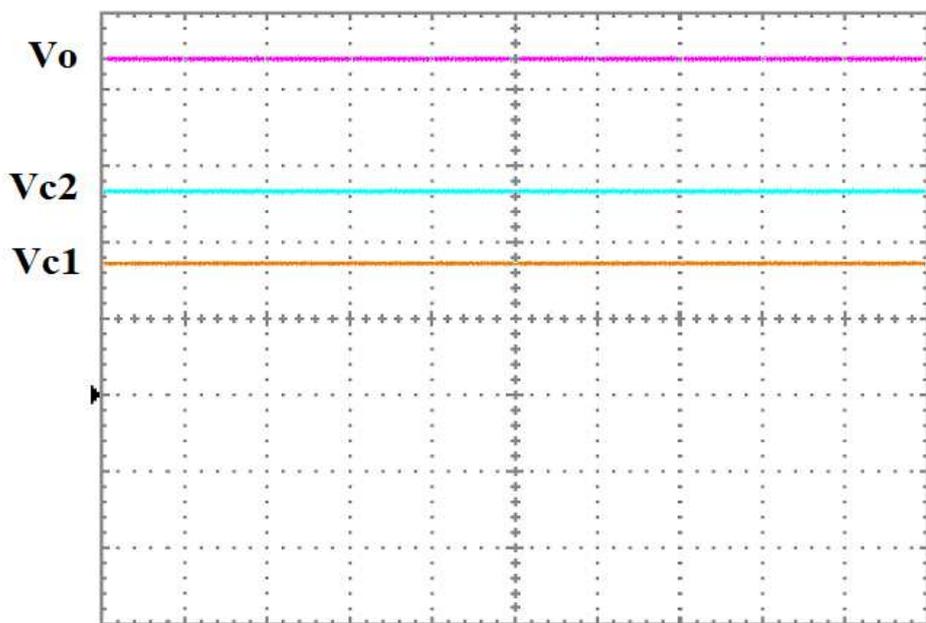


Fig. 14. Output voltage and voltage of capacitors (Time/div=20ms, Volt/div=50 V)

5.3. Comparison verification

To validate the high-step up voltage capability of the SBQN, a comparison is done with the conventional boost converter which is shown in Fig. 15. It is obvious that, the gain of the SBQN is higher than the conventional boost converter as for the factor of $(1 + D)$.

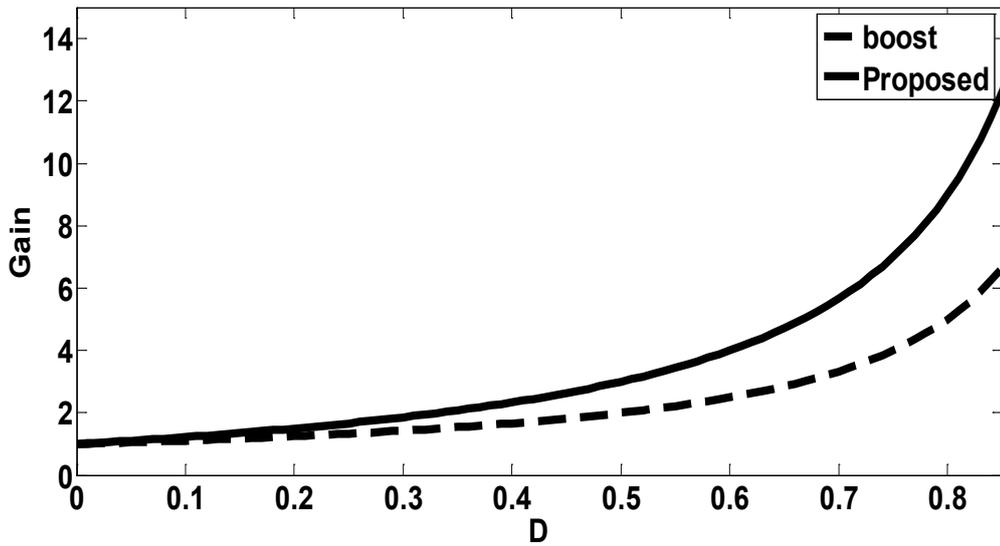


Fig. 15. Comparison between the gain of the proposed and classic boost converters.

Assuming the same duty cycle, the proposed topology has been compared with the classical quasi-Z-source, the switched inductor boost converter and the presented dc–dc converter in [40] and [41]. Table 2 presents a comprehensive comparison between the proposed and other converters with respect to the component counts, voltage gain, semiconductor voltage stress and maximum duty cycle. As can be seen, the proposed converter contains low number of components as compared with QZS and presented converter in [40], [41] and [42]. Table 2 compares the voltage stresses in the converter switches. It is clear that the voltage are increased for the converters presented in [41], [42], [43] and QZS, but the voltage stresses on their semiconductors are increased which are equal to their output voltages. In contrast to all understudy structures, it can be seen that the proposed transducer withstands less voltage stress than them.

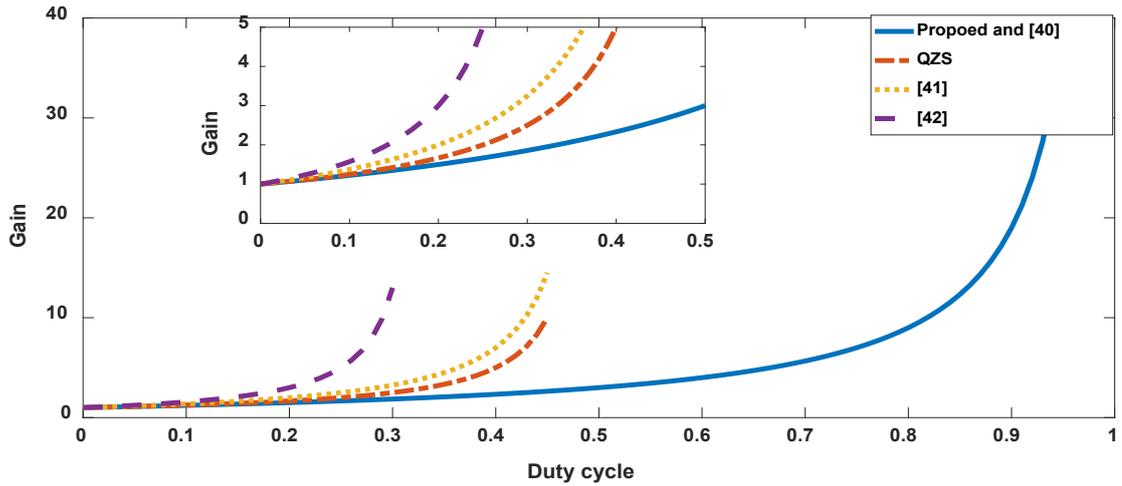


Fig. 16. Voltage gain comparison between the proposed and other dc/dc converters.

6. Conclusion

This paper aims to propose an innovative boost structure to provide an essential voltage with wide range gain for FC power source. The functionality of FC power source against its high operational sensitivity is realized using so-called SBQN to experience low current ripple, and also propagates voltage and current with low stress across its semiconductors. Meanwhile, the durability of the proposed converter has been increased due to reduction of the switching power losses, and also the switch counts are reduced which make it will be more cost-effective than other topologies. To validate its high-step up voltage capability, low voltage stress and switch counts, it has been compared with the some famous and recently introduced structures. Both the results and comparisons associated with the simulation and prototype structures have been well validated the aforementioned advantages of the proposed converter.

Acknowledgements

Not applicable

Authors' contributions

All authors listed have significantly contributed to the development and the writing of this article.

Funding

This work did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors.

Availability of data and materials

All data generated or analysed during this study are available upon request.

Competing interests

The authors declare they have no competing interests.

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Figures

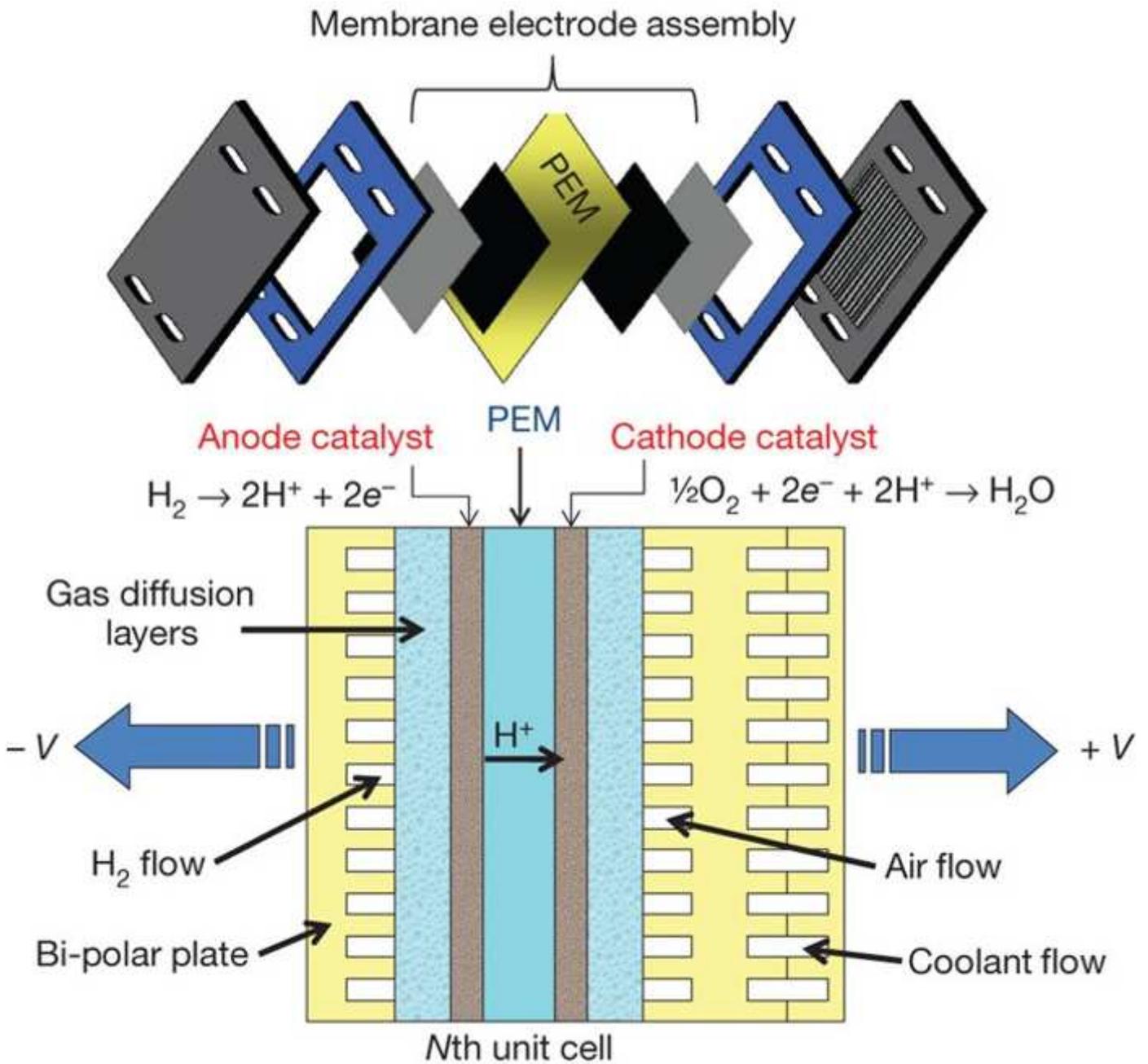


Figure 1

Schematic of a single conventional PEMFC

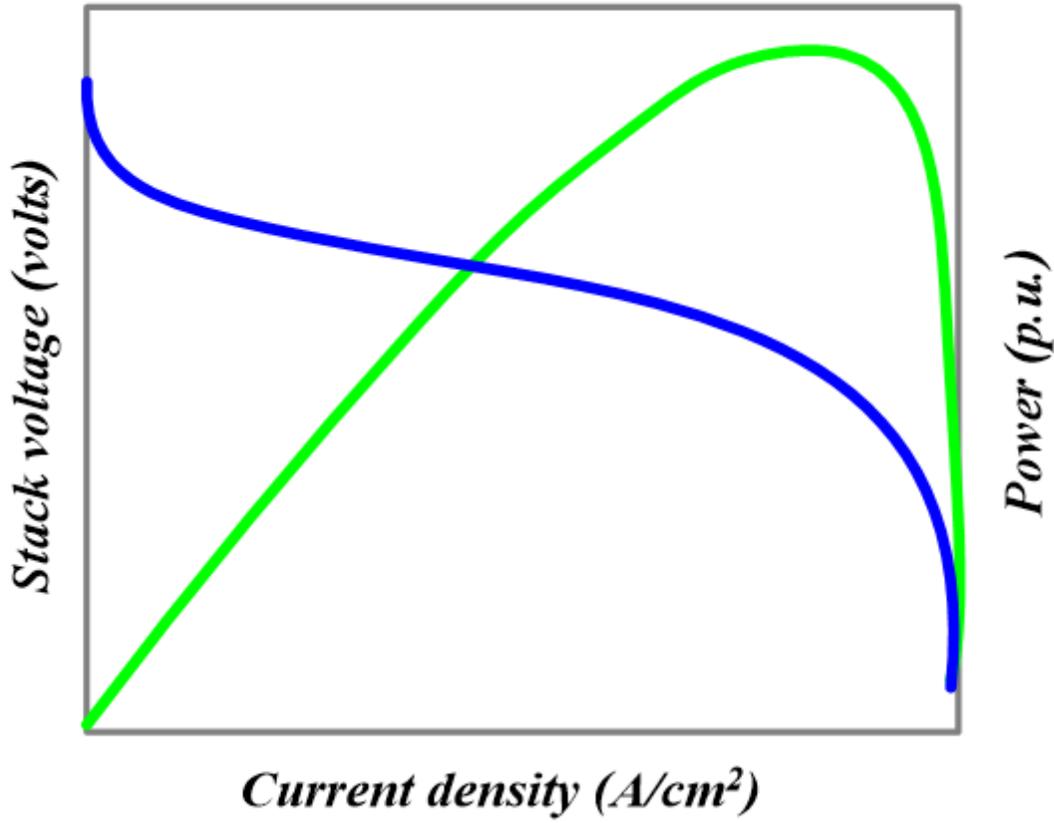


Figure 2

Stack voltage along with power in terms of current density

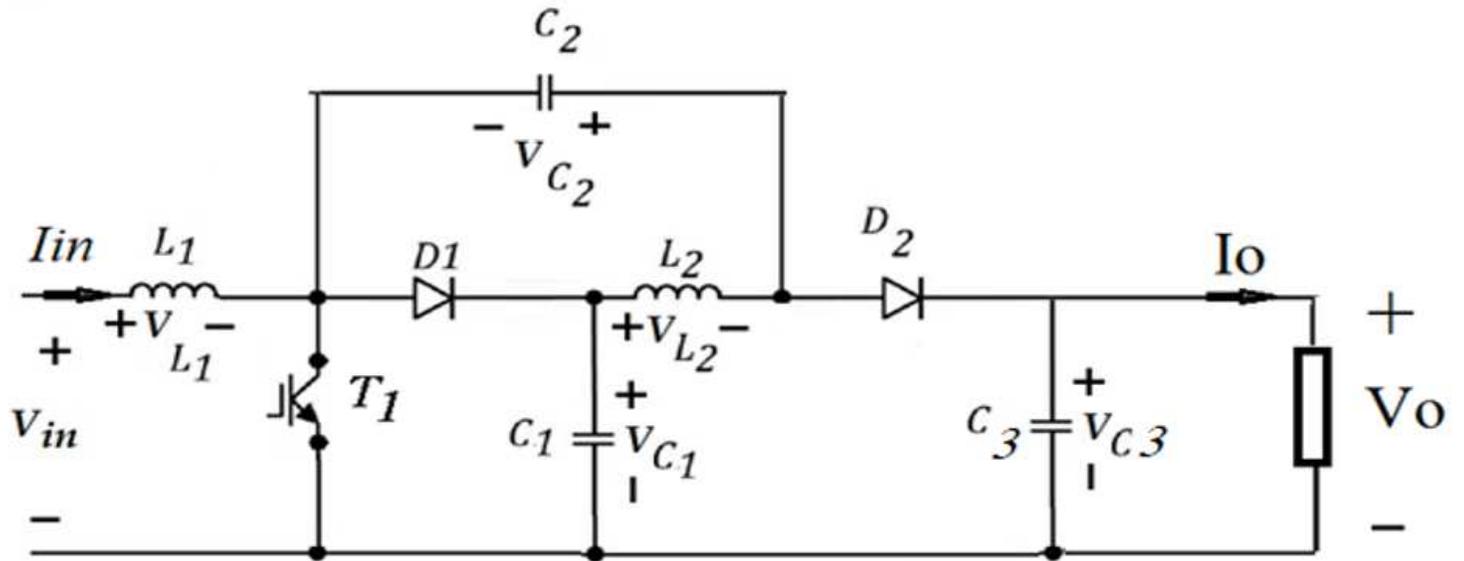
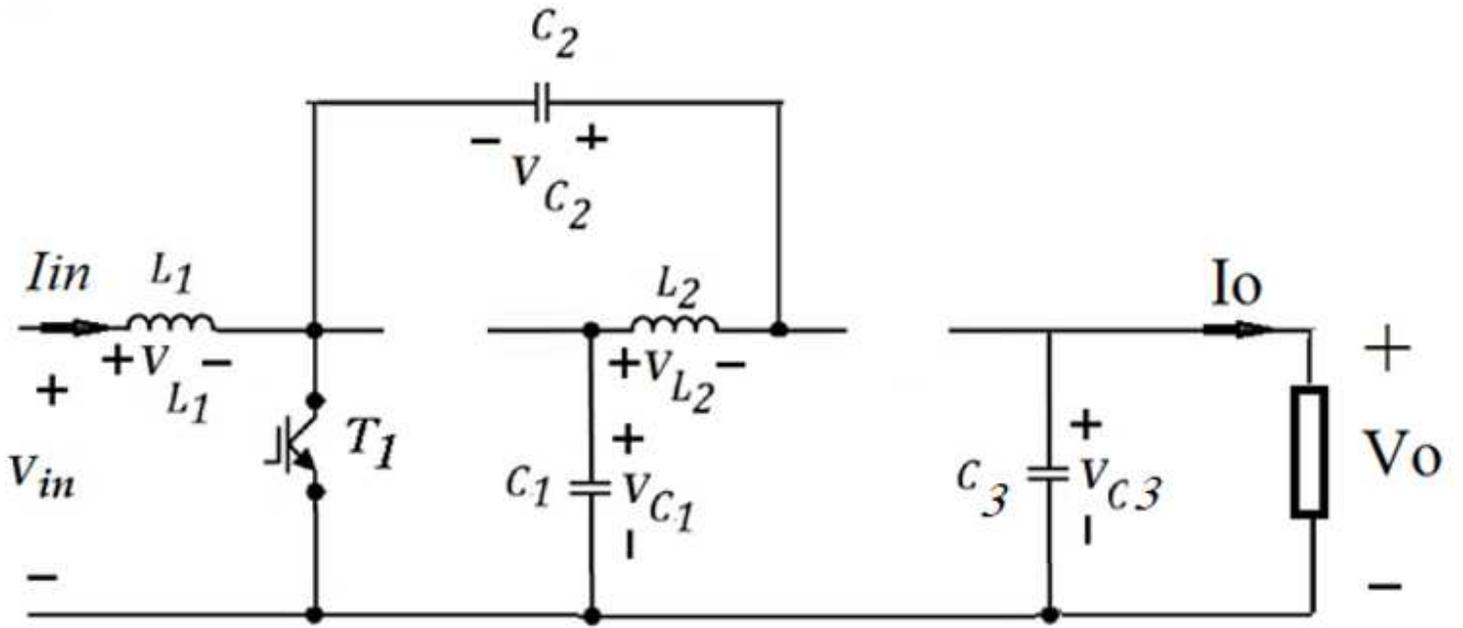
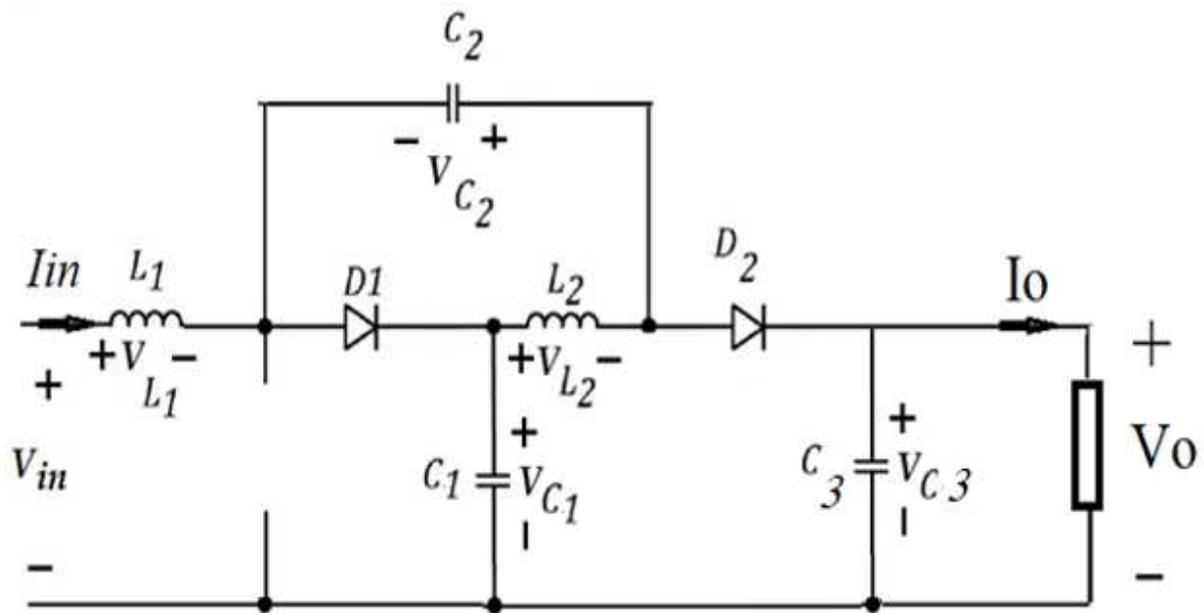


Figure 3

Structure of proposed step-up SBQN



(a)



(b)

Figure 4

Current-flow paths of the proposed converter (a) State 1. (b) State 2.

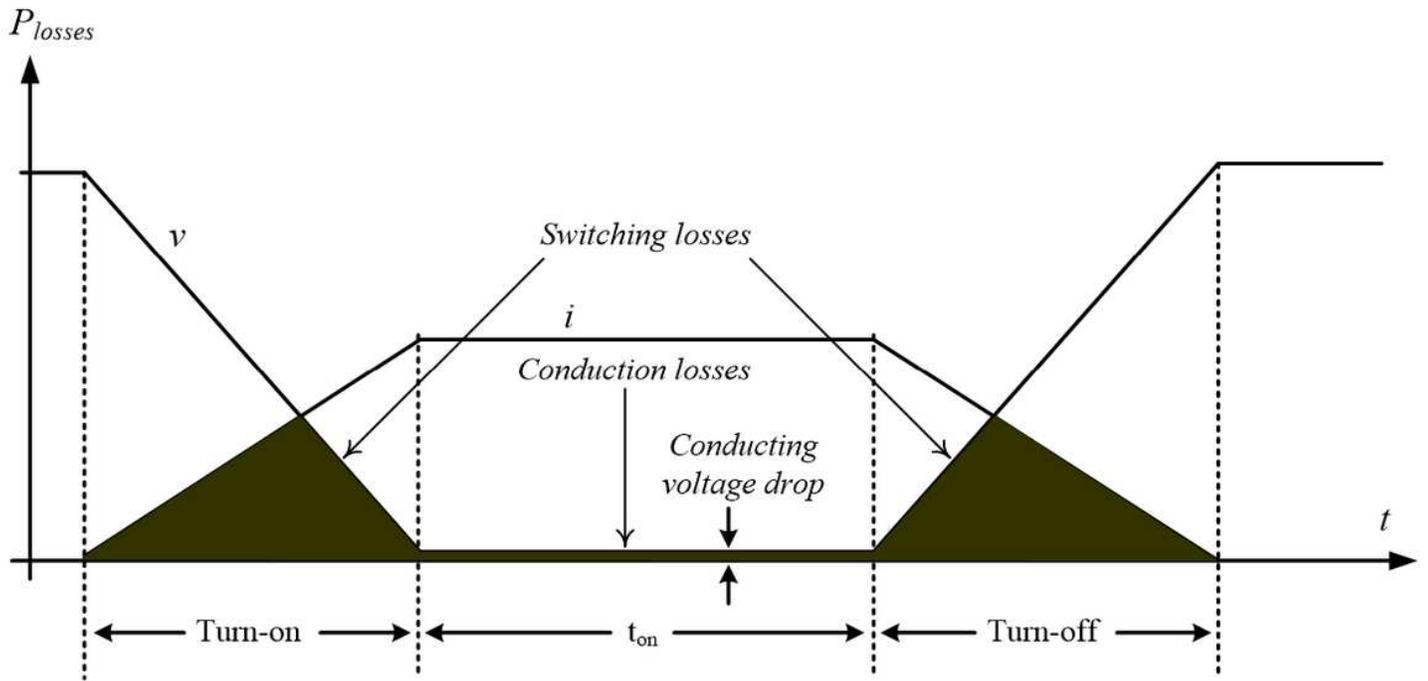


Figure 5

Switching waveforms of transistor

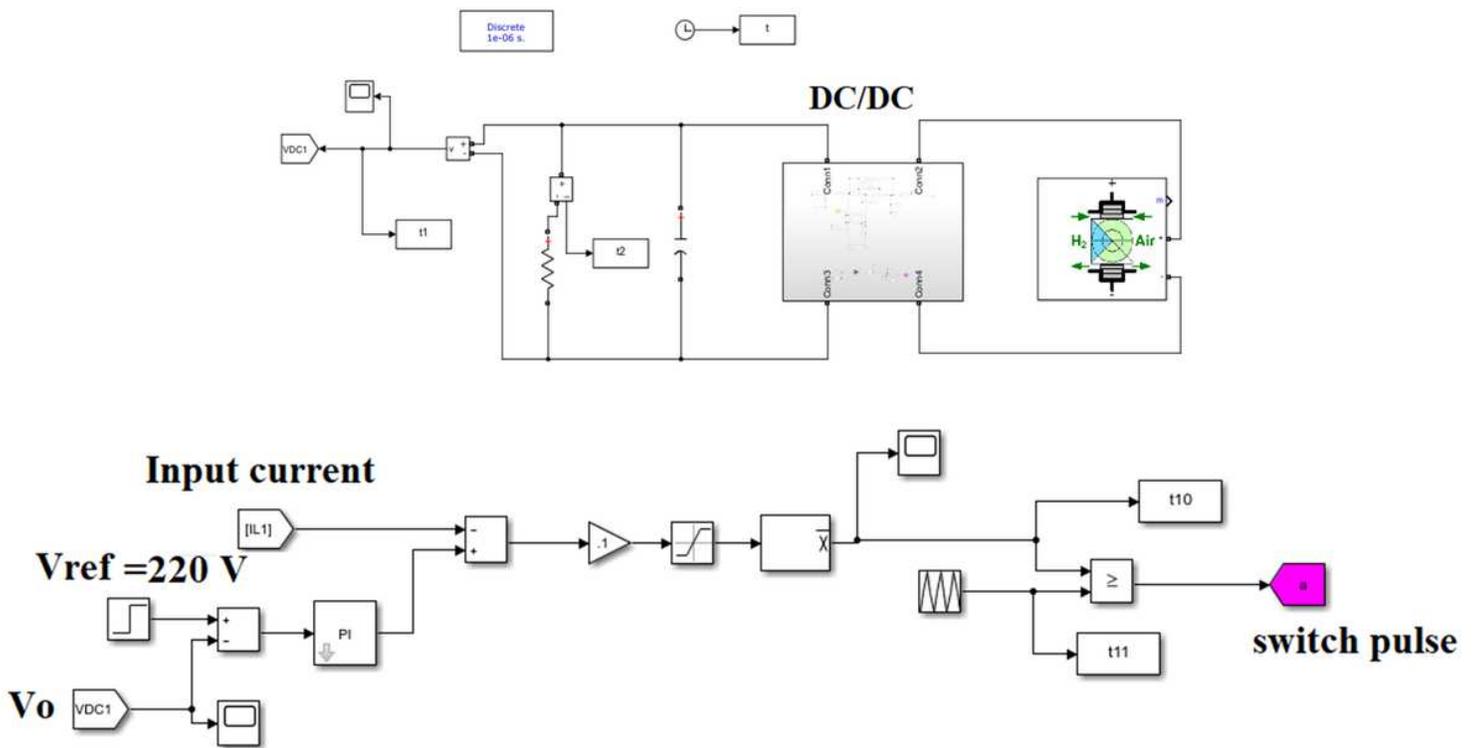


Figure 6

The case study system with presence of SBQN.

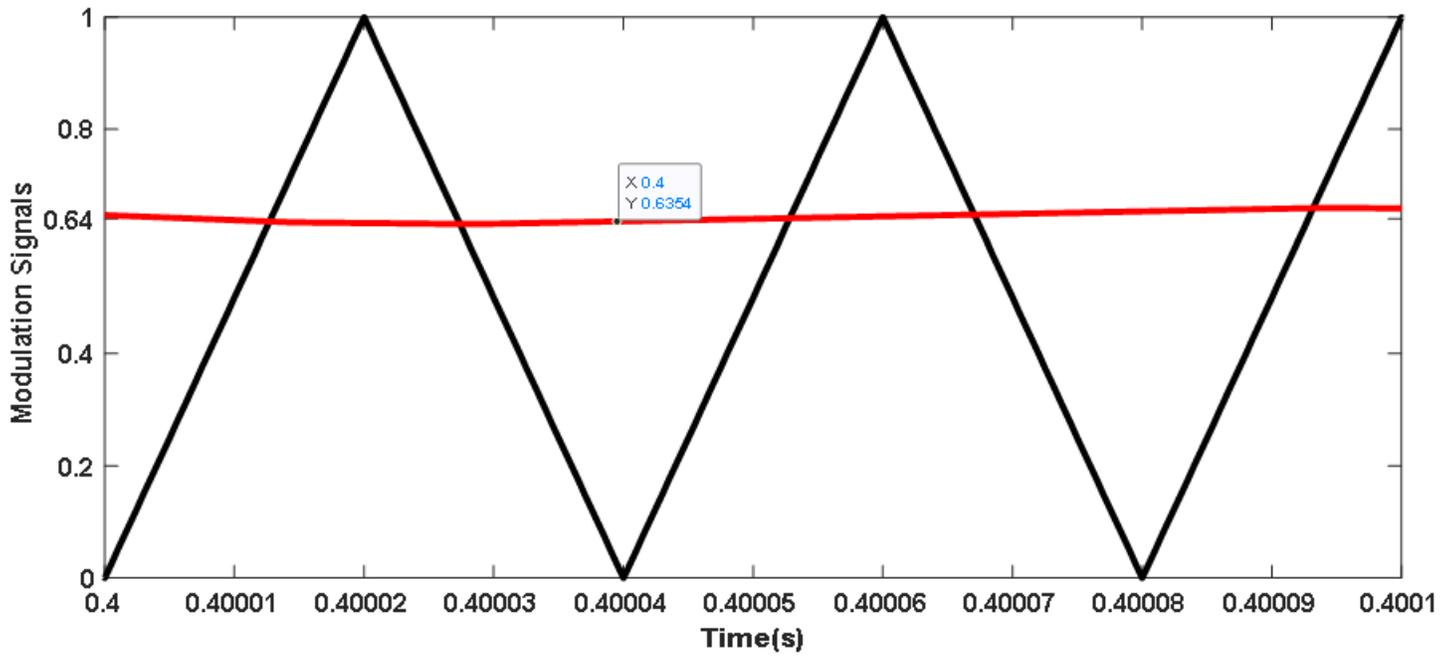


Figure 7

Modulation Signals.

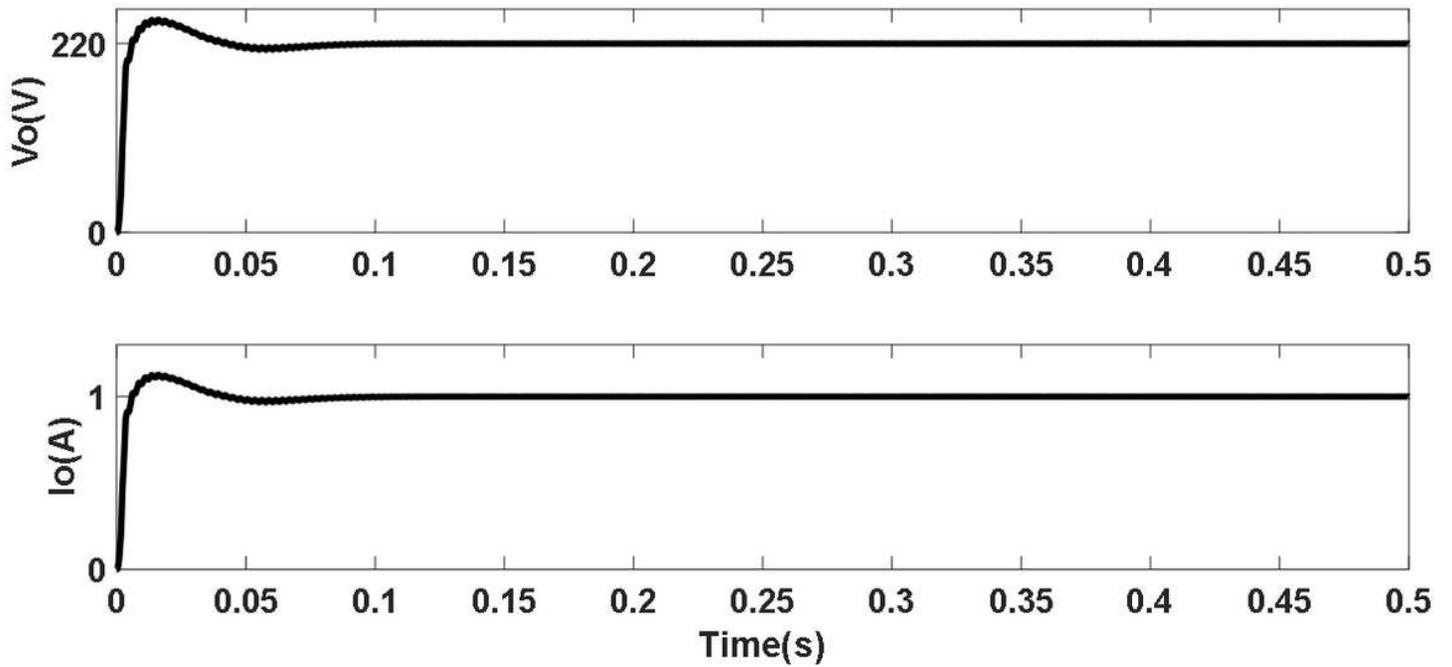


Figure 8

Output voltage and current

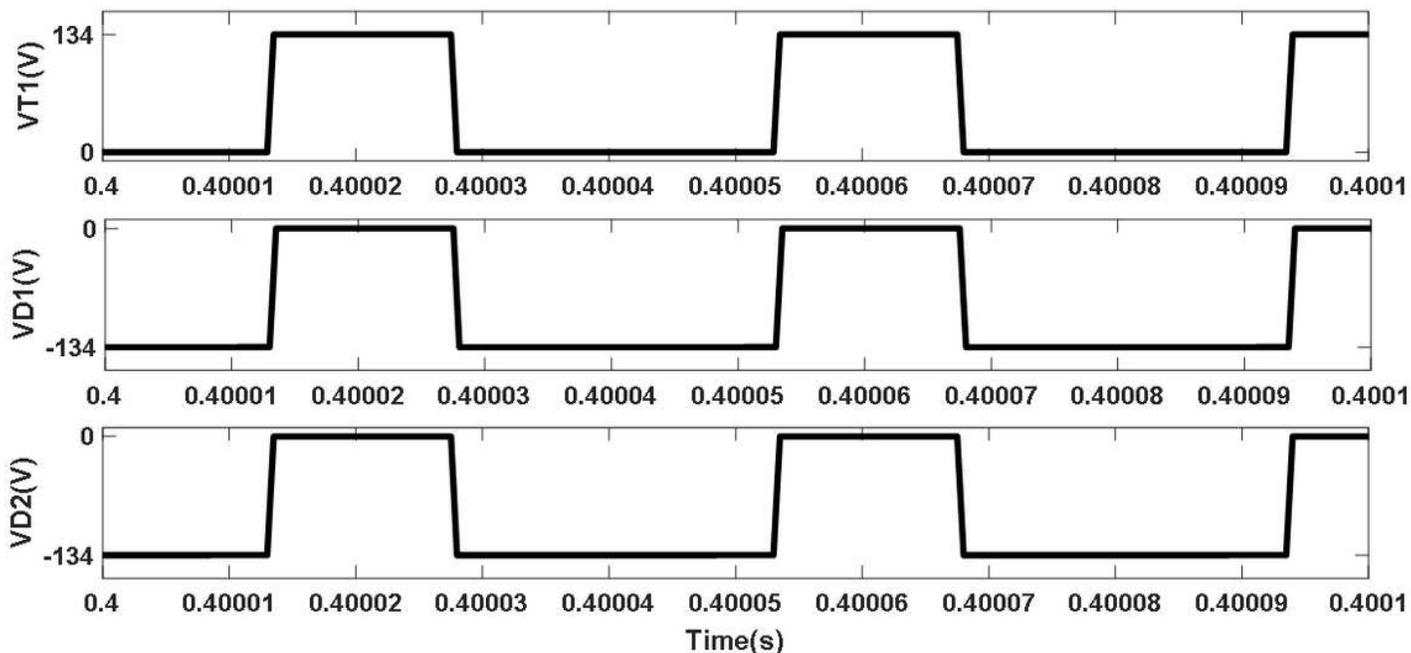


Figure 9

Voltage of semiconductor.

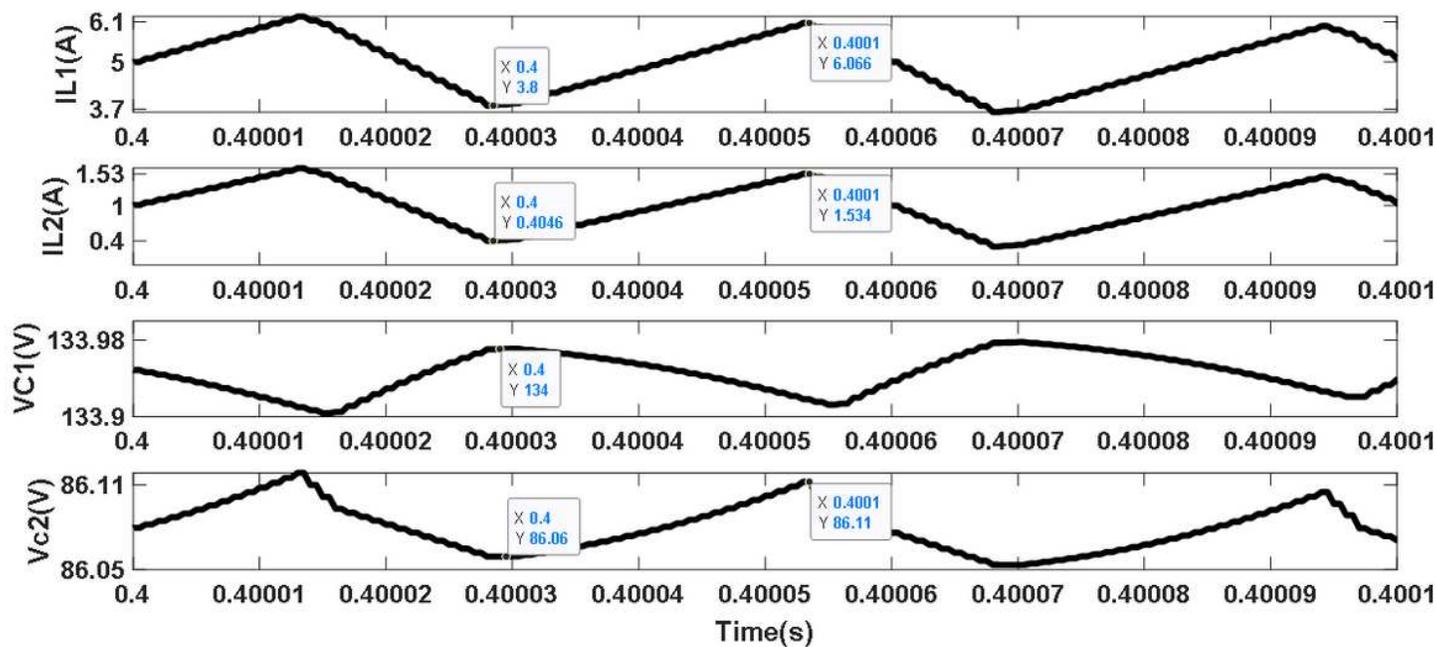


Figure 10

Current of inductors and voltage of capacitors

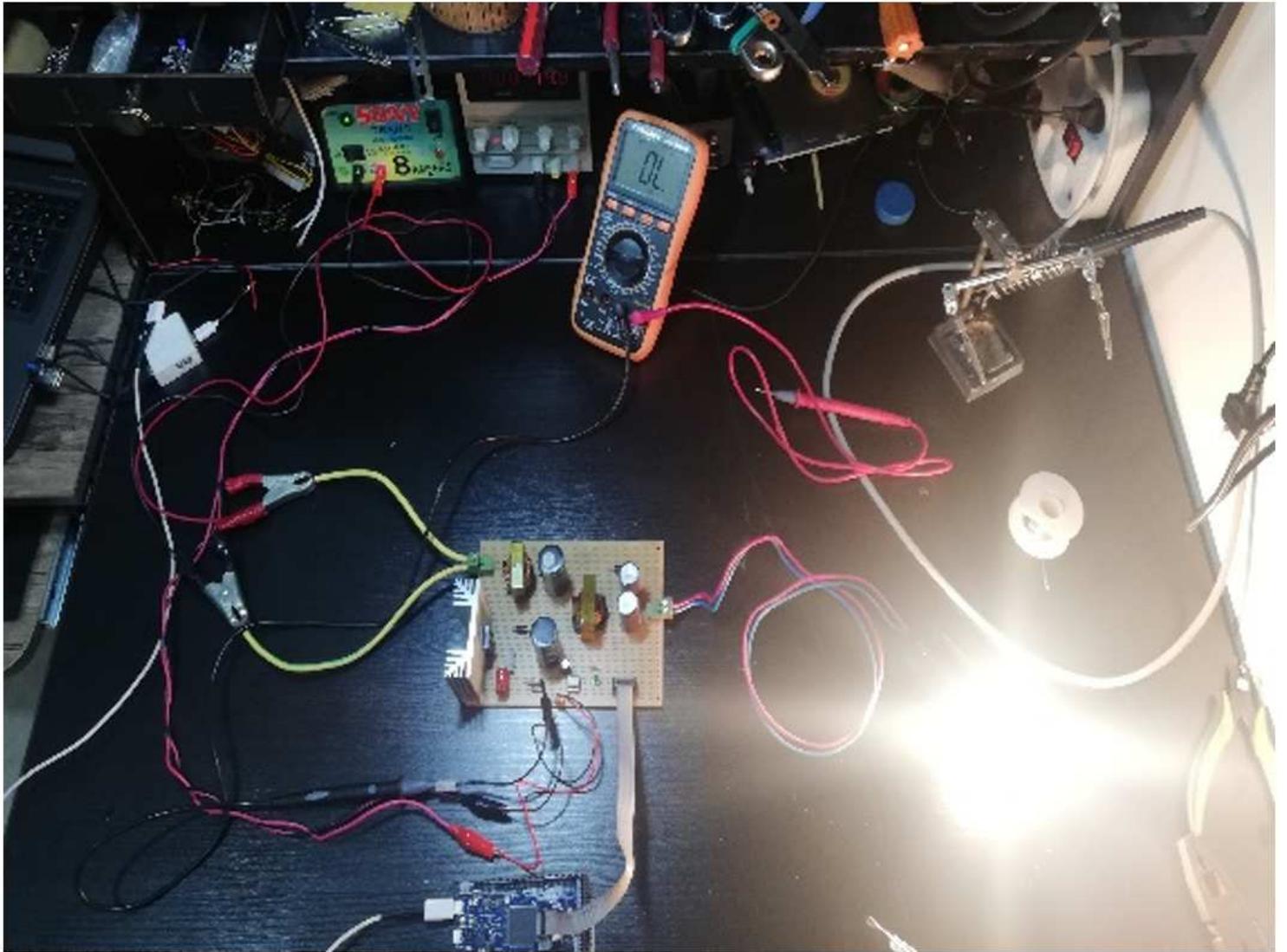


Figure 11

Prototype model of proposed converter

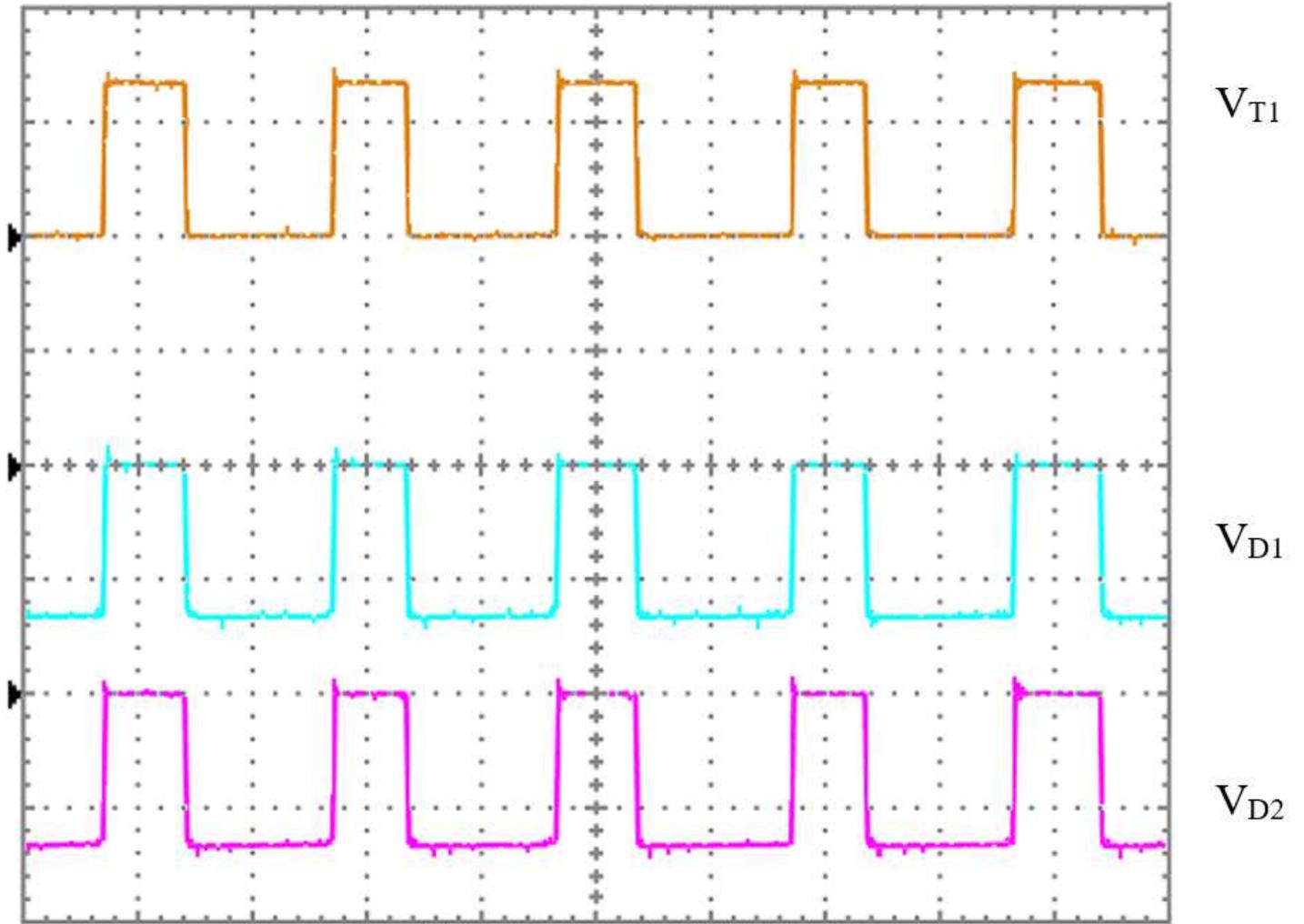


Figure 12

Voltage of semiconductors (Time/div=2.5 μ s, Volt/div=100 V)

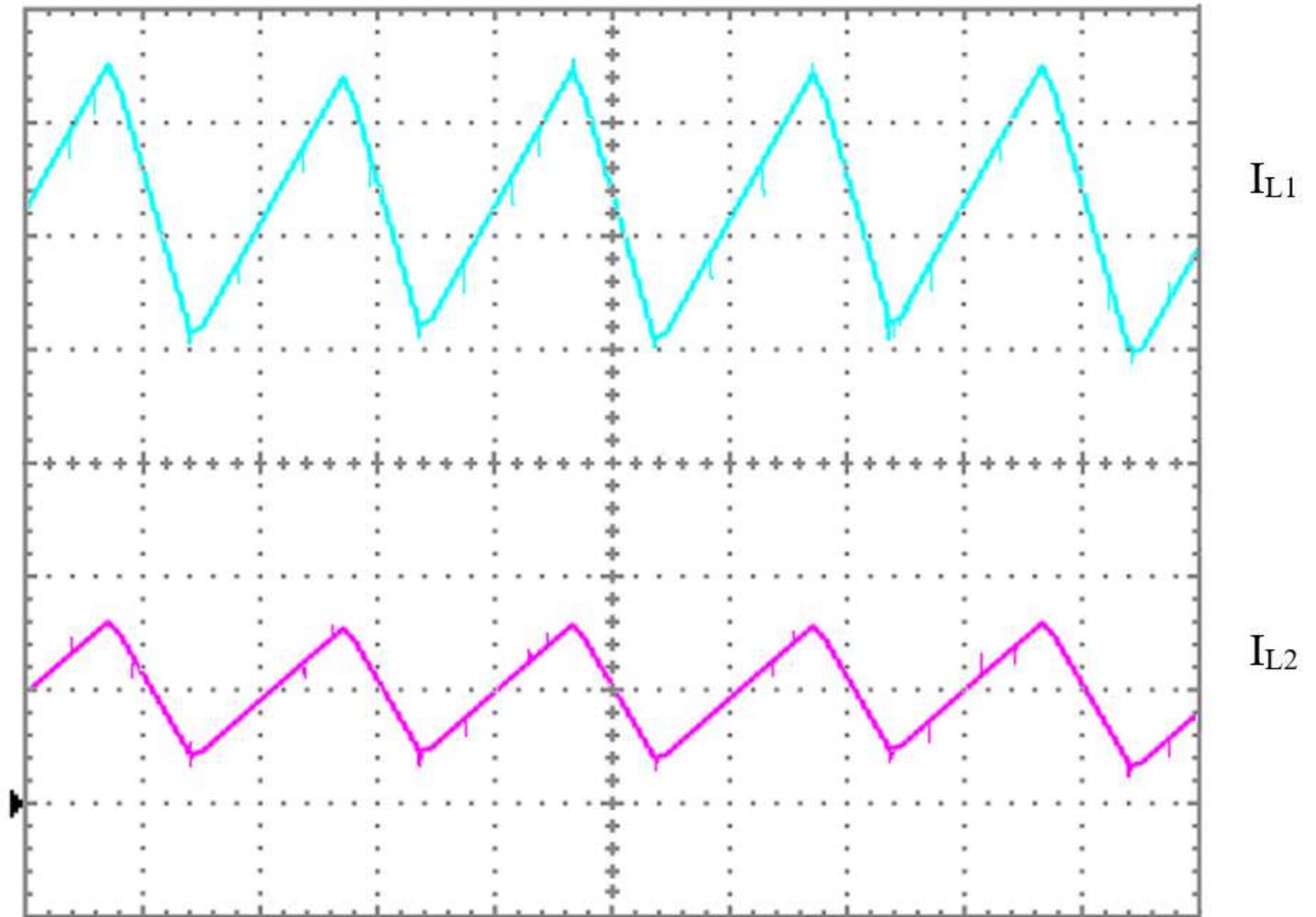


Figure 13

Inductor currents (Time/div=2.5 μ s, Volt/div=1V)

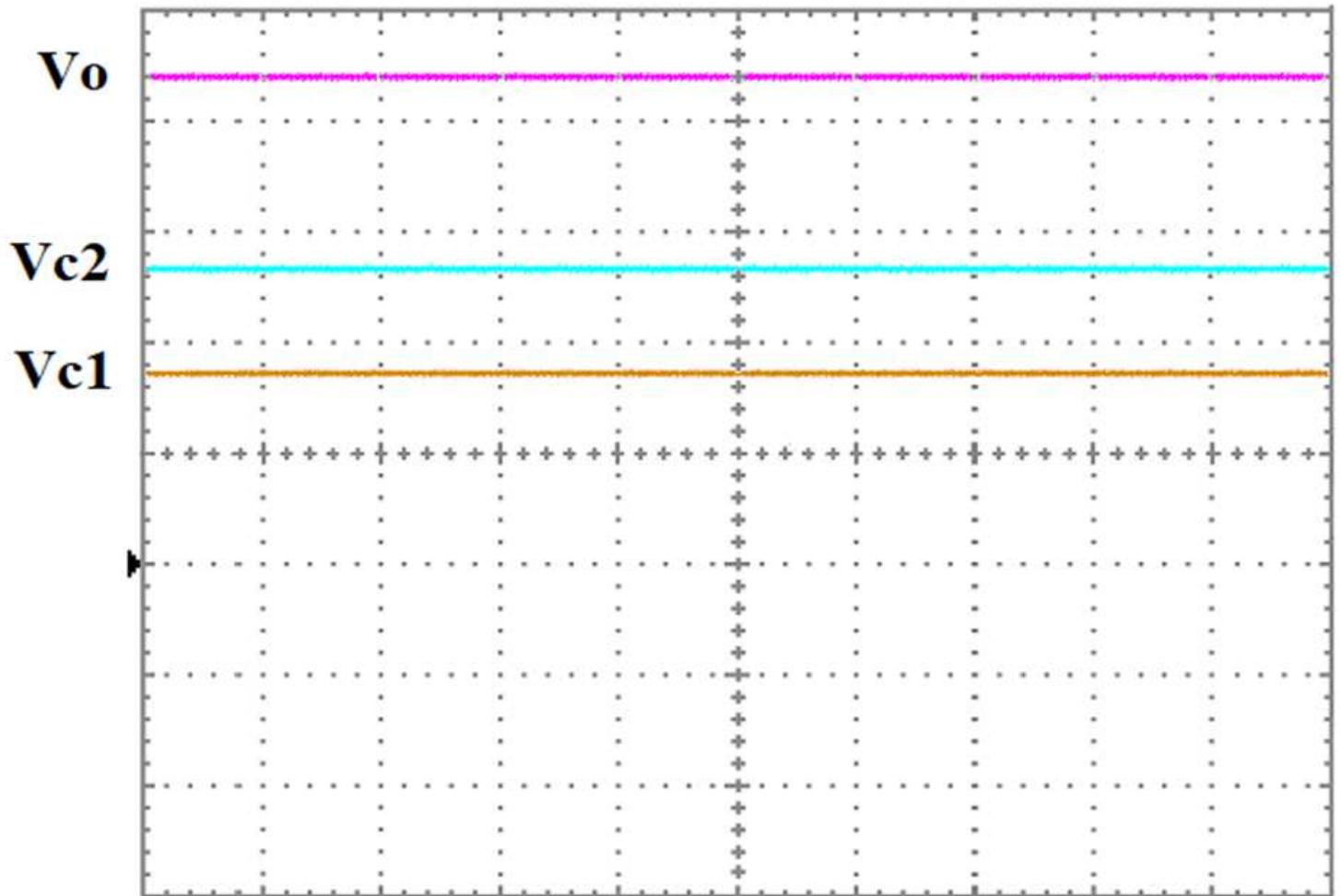


Figure 14

Output voltage and voltage of capacitors (Time/div=20ms, Volt/div=50 V)

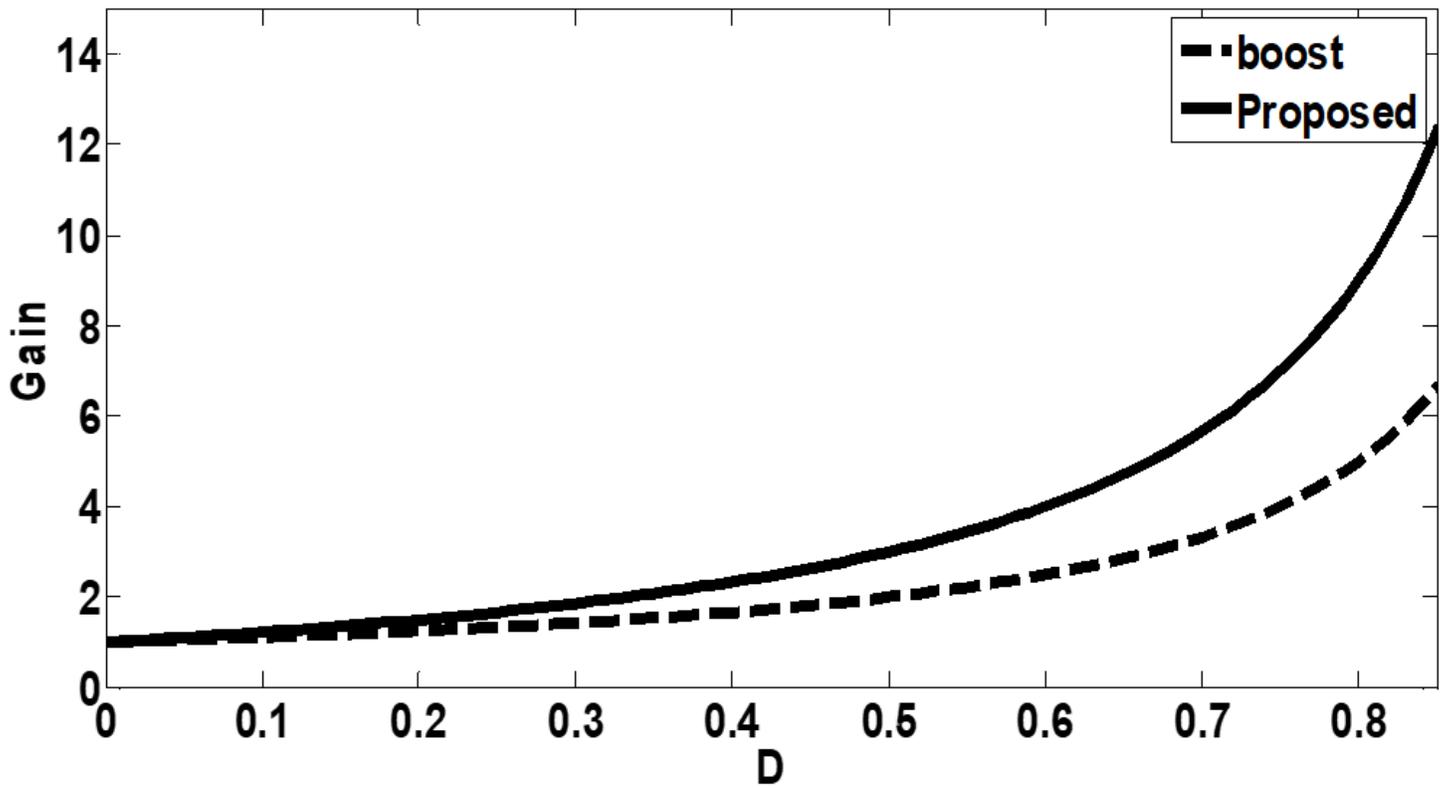


Figure 15

Comparison between the gain of the proposed and classic boost converters.

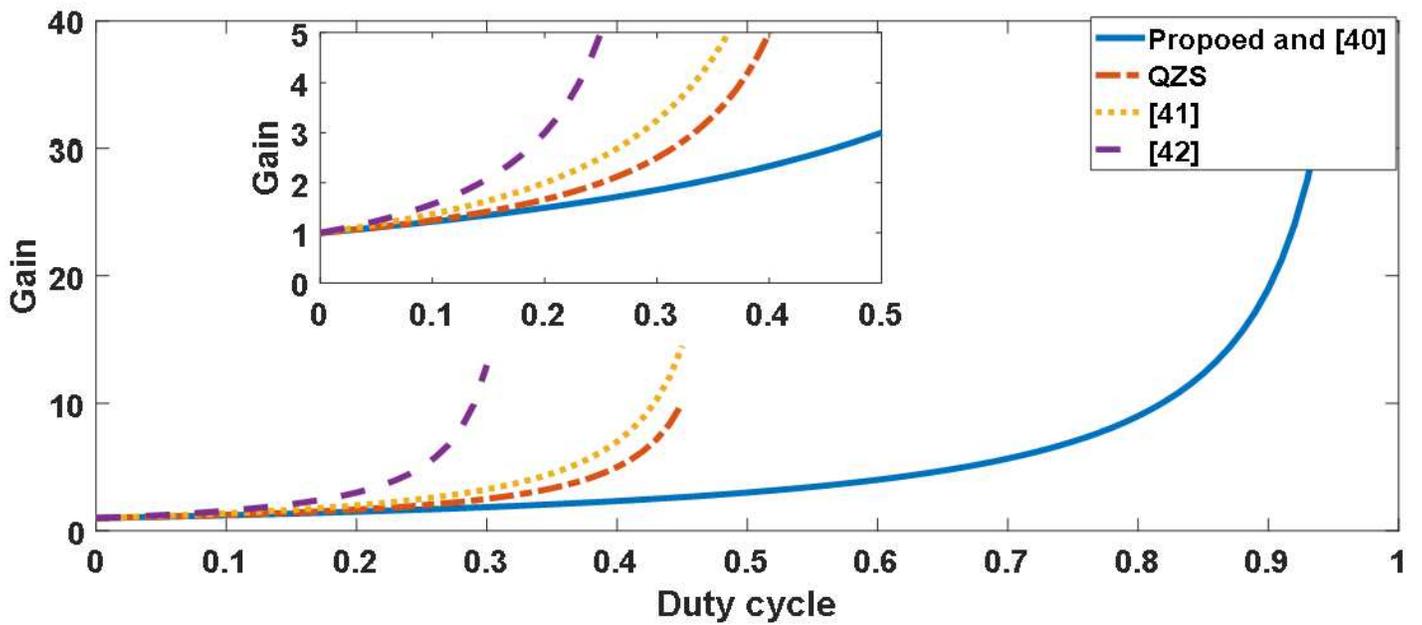


Figure 16

Voltage gain comparison between the proposed and other dc/dc converters.