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RESEARCH

Ge N-Channel MOSFETs with ZrO₂ Dielectric Achieving the Improved Mobility

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Abstract

High mobility Ge nMOSFETs with ZrO₂ gate dielectric are demonstrated and compared against transistors with Al₂O₃/ZrO₂, ZrO₂, and O₃/ZrO₂ gate dielectrics. The Al₂O₃/ZrO₂ provides for dramatically enhanced-effective electron mobility (μ_{eff}), boosting transistor drive current. Ge nMOSFETs with the Al₂O₃/ZrO₂ gate insulator achieve a 50% μ_{eff} improvement as compared to the Si universal mobility at an inversion charge density (Q_{inv}) of $5 \times 10^{12} \text{ cm}^{-2}$. An Al₂O₃ interfacial layer leads to a boost in μ_{eff} but increases capacitance equivalent thickness (CET). Utilizing O₃ oxidation of Ge surface, Al₂O₃-free Ge nMOSFETs having a CET of 1.1 nm obtains a peak μ_{eff} of 682 cm²/Vs, which is higher than that of the Si universal mobility at the similar Q_{inv} .

Keywords: Germanium, ZrO₂, MOSFET, CMOS, Mobility

Background

GERMANIUM (Ge) has exhibited the advantages of higher carrier mobility and lower processing temperature compared with the Si devices. These make Ge to be an alternative for the applications of ultrascaled CMOS logic devices and thin-film transistors (TFTs) as top-layer in three-dimensional integrated circuits[1-3]. In the past few years, great efforts focused on surface passivation, gate dielectric, and channel engineering for Ge p-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) have contributed to the significant improvement of electrical performance for the devices.

But for Ge n-channel MOSFETs, the low effective carrier mobility (μ_{eff}) strongly limits the performance of the transistors. Various surface passivation techniques including Si passivation [1], plasma post oxidation [4], and InAlP passivation [5], and several high- κ dielectrics including HfO₂, ZrO₂ [6-8], Y₂O₃ [9], and La₂O₃ [10] have been explored in Ge nMOSFETs to boost the electron μ_{eff} . It was demonstrated that ZrO₂ dielectric integrated with Ge channel can provide a robust interface due to that a GeO₂ interfacial layer can react and intermix with the ZrO₂ layer [7]. A decent hole μ_{eff} has been reported in Ge p-channel transistors [6-8], while there is still a lot of room for improvement in electron μ_{eff} for their counterparts.

In this work, Ge nMOSFETs with ZrO₂ gate dielectric are fabricated to achieve the improved μ_{eff} over Si in the entire range of the inversion charge density (Q_{inv}). Ge transistors obtain a 50% improvement in electron μ_{eff} compared to the Si universal mobility at a medium Q_{inv} of $5.0 \times 10^{12} \text{ cm}^{-2}$.

Methods

The key process steps for fabricating Ge nMOSFETs on 4-inch p-Ge(001) wafers with a resistivity of 0.136 ~ 0.182 $\Omega \cdot \text{cm}$ are shown in Fig. 1(a). The source/drain (S/D) regions were implanted with the phosphorous ion at a dose of $1 \times 10^{15} \text{ cm}^{-2}$ and an energy of 30 keV followed by the dopant activation at 600°C. After the pre-gate cleaning, Ge wafers were loaded into an atomic layer deposition chamber for the formation of the gate dielectric layer(s): Al₂O₃/O₃ oxidation/ZrO₂, ZrO₂, or O₃ oxidation/ZrO₂ for wafers A, B, or C, respectively. For wafer A, 0.9 nm Al₂O₃ was used to protect the channel surface during O₃ oxidation. O₃ oxidation was carried out at 300 °C for 15 minutes for both wafer A and C. For all the wafers, the thickness of ZrO₂ was ~ 3.3 nm. Subsequently TiN(100nm) gate metal was deposited via physical reactive sputtering, and lithography patterning and reactive ion etching were used to form the gate electrode. After that, a 25-nm thick Ni layer was deposited in S/D regions. Finally, the post metallization annealing (PMA) at 350 °C was carried out to form the Ni germanidation and improve the interface quality. Schematic and microscope image of the fabricated transistor are shown in Figs. 1(b) and (c), respectively.

Figs. 2(a) and (b) show the high-resolution

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transmission electron microscope (HRTEM) images of the gate stacks on wafer A and B, respectively. The unified thickness of the $\text{Al}_2\text{O}_3/\text{GeO}_x$ interfacial layer (IL) for wafer A is ~ 1.2 nm indicating the 0.2~0.3 nm GeO_x . For the device on wafer B, an ultrathin GeO_x IL was experimentally demonstrated [7].

Results and Discussion

The measured capacitance (C) and the leakage current (J) characteristics for Ge MOS capacitors on wafer A, B, and C are measured and shown in Fig. 3(a) and (b), respectively. The capacitance equivalent thickness (CET) of the devices on wafer A, B, and C are extracted to be 2.1, 0.9, and 1.1 nm, respectively. Assuming the GeO_x IL provides an extra equivalent oxide thickness (EOT) of ~ 0.2 nm for wafer A and C by comparing wafer B and C, the 3.3 nm ZrO_2 contributes an EOT of ~ 0.9 nm with κ value of ~ 14.3 .

The $\text{GeO}_x/\text{Al}_2\text{O}_3$ IL for wafer A and GeO_x IL for wafer C produce the EOT of 1.2 and 0.3 nm, respectively. The CET of the devices can be further reduced by decreasing the IL thickness or improving the interface quality, and enhancing the permittivity of ZrO_2 with some surface passivation, e.g. NH_3/H_2 plasma treatment [6]. Fig. 3(c) compares J vs. CET characteristics for the Ge nMOSFETs in this work against values for other reported Ge devices [5,11-15].

Fig. 4(a) shows measured drain current (I_D) and source current (I_S) vs. gate voltage (V_G) curves of Ge nMOSFETs from wafer A, B, and C. All transistors have a gate length L_G of 4 μm and a gate width W of 100 μm . The point subthreshold swing (SS), defined as $dV_G/d(\log I_D)$, as a function of I_D curves for the transistors in Fig. 4(a) are calculated and shown in Fig. 4(b). It is clarified that the transistor on wafer A exhibits the degraded I_D leakage floor and SS compared to the devices on wafer B and C. This should be attributed to the fact that the device with the Al_2O_3 inserted layer has a higher density of interface traps (D_{it}) within the bandgap of the Ge channel in comparison with the wafer B and C.

Fig. 4(c) shows the measured output characteristics *i.e.* I_D - V_D curves for various values of gate overdrive $|V_G - V_{TH}|$ of the devices demonstrating that the Ge transistor on wafer A achieves significantly improved drive current compared to the devices on wafer B and C. Here, V_{TH} is defined as V_{GS} corresponding to an I_D of 10^{-7} A/ μm . The boosted I_{DS} for transistors on wafer A is attributed to the higher μ_{eff} . The Al_2O_3 layer has not led to the degradation of D_{it} performance near the conduction band of the Ge

channel.

Fig. 5(a) shows the total resistance R_{tot} as a function of L_G for the Ge nMOSFETs with ZrO_2 dielectric with an L_G ranging from 2 μm to 10 μm . The values of R_{tot} are extracted at a gate overdrive of 0.6 V and a V_D of 0.05 V. The S/D resistance R_{SD} of the transistors is extracted to be ~ 13.5 k $\Omega \cdot \mu\text{m}$, utilizing the fitted lines intersecting at the y -axis. The channel resistance R_{CH} values of the devices are obtained by the slope of the fitted lines, *i.e.* $\Delta R_{tot}/\Delta L_G$, which can be used for calculating the μ_{eff} characteristics of Ge nMOSFETs. Fig. 5(b) shows the inversion gate capacitance C_{inv} as a function of V_G curves for the Ge nMOSFETs. The device on wafer B achieves the highest C_{inv} due to its smaller physical thickness. To evaluate the interface quality, interface-trap densities D_{it} were extracted utilizing Hill's method [16]. where q is the electronic charge, A is the area of the capacitor, $G_{m,max}$ is the maximum value of measured conductance, with its corresponding capacitance C_m , ω is the angular frequency, and C_{ox} is gate oxide capacitance. The D_{it} values are calculated to be 3.7, 3.2, and 2.3×10^{12} eV $^{-1} \cdot \text{cm}^{-2}$ for the devices on wafer A, B, and C, respectively.

It is known that the calculated values correspond to the midgap D_{it} . The device with Al_2O_3 IL on wafer A has a higher midgap D_{it} compared to the devices on wafer B and C. This is consistent with the results in Fig. 3(a) and Fig. 4(a), and the higher midgap D_{it} gives rise to a larger depletion capacitance dispersion in wafer A causing a higher leakage current of I_{DS} in comparison with the other two wafers. Note the wafer A should have the lower D_{it} near the conduction bandgap due to its higher μ_{eff} over wafer B and C.

It is well known that μ_{eff} is the bottleneck for high drive current and transconductance in Ge nMOSFETs. Here, μ_{eff} can be calculated by $\mu_{eff} = 1/[WQ_{inv}(\Delta R_{tot}/\Delta L_G)]$, where $\Delta R_{tot}/\Delta L_G$ is the slope of the R_{tot} vs. L_G as shown in Fig. 5(a). Q_{inv} can be obtained by integrating the measured C_{inv} - V_G curves. In Fig. 6, we compare the μ_{eff} vs. Q_{inv} of the Ge nMOSFETs on wafer A, B, and C with those reported previously in [17-21]. The extracted peak μ_{eff} values of the transistors on wafer A and C are 795 and 682 $\text{cm}^2/\text{V} \cdot \text{s}$, respectively, and that of Ge nMOSFETs on wafer B is 433 $\text{cm}^2/\text{V} \cdot \text{s}$. Ge nMOSFETs with Al_2O_3 IL achieve a significantly improved μ_{eff} in comparison with the transistors on wafer B or C, the devices in [17-21] in a high field, and Si universal mobility in the entire Q_{inv} range. At a Q_{inv} of 5×10^{12} cm^{-2} , a 50% μ_{eff} enhancement is achieved in devices on wafer A as compared to the Si universal mobility. This demonstrates that by protecting the channel surface using Al_2O_3 , a high-quality interface between gate insulator and Ge is realized to boost the mobility characteristics. μ_{eff} in transistors on wafer C is higher than the Si universal at a Q_{inv} of 2.5×10^{12} cm^{-2} , although it rapidly decays with the increase of Q_{inv} range. This indicates that the used O_3 oxidation before ZrO_2 deposition does not lead to enough flat channel

surface to effectively suppress the surface roughness scattering of the carrier at high Q_{inv} . Optimizing the O_3 oxidation process or reducing the Al_2O_3 IL thickness can make the Ge transistor achieve a reduced CET while maintaining a higher μ_{eff} at the high Q_{inv} .

Conclusions

The impacts of gate dielectric structure and morphology on Ge nMOSFET electrical characteristics are investigated. An Al_2O_3/ZrO_2 gate dielectric provides for significantly-improved μ_{eff} as compared to the Si universal mobility. μ_{eff} can be improved by inserting an Al_2O_3 layer between the ZrO_2 and Ge channel, which however inevitably leads to a larger CET. Al_2O_3 -free Ge nMOSFETs with O_3 oxidation of the Ge surface prior to ZrO_2 deposition achieve a peak μ_{eff} of $682 \text{ cm}^2/\text{V}\cdot\text{s}$ which is higher than that of Si at the similar Q_{inv} .

Abbreviations

Ge: Germanium; ZrO_2 : zirconium dioxide; Al_2O_3 : aluminum oxide; O_3 : Ozone; Si: silicon; PMA: post metal annealing; PDA: post deposition annealing; IL: Interfacial layer; TiN: Titanium nitride; MOSFETs: Metal-oxide-semiconductor field-effect transistors; ALD: Atomic layer deposition; HF: Hydrofluoric acid; μ_{eff} : effective carrier mobility; PPO: Plasma post oxidation; SS: Subthreshold swing; CET: capacitive equivalent thickness; EOT: equivalent oxide thickness; Q_{inv} : inversion charge density; HRTEM: High resolution transmission electron microscope; Ni: Nickel; GeO_x : Germanium oxide; I_{DS} : drain current; V_{GS} : gate voltage; V_{TH} : threshold voltage;

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Competing interests

The authors declare that they have no competing interests.

Author's contributions

LLC carried out the experiments and drafted the manuscript. HL and YP provided the discussion on the results. GQH and YL supported the study and helped to revise the manuscript. YH provided constructive advice in the drafting. All the authors read and approved the final manuscript.

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Availability of Data and Materials

The datasets supporting the conclusions of this article are included in the article.

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Figure title and legend section:

Fig. 1 (a) Key process steps for fabricating Ge nMOSFETs. (b) Cross-sectional schematic and (c) microscope image of the fabricated devices.

Fig. 2 HRTEM images of (a) $\text{TiN}/\text{ZrO}_2/\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$, (b) $\text{TiN}/\text{ZrO}_2/\text{GeO}_x/\text{Ge}$ stacks for the devices on wafer A and B, respectively.

Fig. 3 (a) Measured C as a function of voltage V characteristics for Ge pMOS capacitors on wafer A, B, and C. (b) The J vs. V curves for the devices. (c) Benchmarking of J (extracted at $V_{FB} \pm 1$ V) of the Ge MOS capacitors in this work against data obtained for similar bias conditions from the literature.

Fig. 4 (a) Measured I_D and I_S vs. V_{GS} curves of Ge nMOSFETs on wafer A, B, and C. (b) Point SS as a function of I_D for the transistors. (c) I_D - V_D characteristics show that the Ge nMOSFET on wafer A has a higher drive current compared to the devices on wafer B and C.

Fig. 5 (a) R_{tot} vs. L_G curves for Ge nMOSFETs on wafer A, B, and C. The fitted line intersecting at the y-axis and the slope of linear fit lines are utilized to extract the R_{SD} and R_{CH} , respectively. (b) C_{inv} vs. V_G curves for Ge nMOSFETs measured at a frequency of 50 kHz.

Fig. 6 μ_{eff} for the Ge nMOSFETs in this work vs. previously published results for unstrained Ge transistors. The devices on wafer A show the improved μ_{eff} than the Si universal mobility in the entire range of Q_{inv} .

Figures

(a) Key Process Steps

- S/D Implantation and Activation
- Pregate Cleaning
- **Gate Dielectric Deposition**
 - Wafer A: Al_2O_3 (0.9 nm)/ O_3 / ZrO_2
 - Wafer B: ZrO_2
 - Wafer C: O_3 / ZrO_2
- Post Deposition Annealing
- TiN Deposition
- Gate Patterning and Etching
- Ni Deposition in S/D regions
- Rapid Thermal Anneal

Figure 1

(a) Key process steps for fabricating Ge nMOSFETs. (b) Cross-sectional schematic and (c) microscope image of the fabricated devices.

Figure 2

HRTEM images of (a) TiN//ZrO₂/Al₂O₃/GeO_x/Ge, (b) TiN/ ZrO₂/GeO_x/Ge stacks for the devices on wafer A and B, respectively.

Figure 3

(a) Measured C as a function of voltage V characteristics for Ge pMOS capacitors on wafer A, B, and C. (b) The J vs. V curves for the devices. (c) Benchmarking of J (extracted at $V_{\text{FB}} \pm 1$ V) of the Ge MOS capacitors in this work against data obtained for similar bias conditions from the literature.

Figure 4

(a) Measured I_D and I_S vs. V_{GS} curves of Ge nMOSFETs on wafer A, B, and C. (b) Point SS as a function of I_D for the transistors. (c) I_D - V_D characteristics show that the Ge nMOSFET on wafer A has a higher drive current compared to the devices on wafer B and C.

Figure 5

(a) R_{tot} vs. L_G curves for Ge nMOSFETs on wafer A, B, and C. The fitted line intersecting at the y-axis and the slope of linear fit lines are utilized to extract the RSD and RCH, respectively. (b) C_{inv} vs. V_G curves for Ge nMOSFETs measured at a frequency of 50 kHz.

Figure 6

μ_{eff} for the Ge nMOSFETs in this work vs. previously published results for unstrained Ge transistors. The devices on wafer A show the improved μ_{eff} than the Si universal mobility in the entire range of Q_{inv} .