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Kuleen Kumar
NIT Mizoram: National Institute of Technology Mizoram
Rudra Sankar Dhar (rdhar@uwaterloo.ca)
National Institute of Technology Mizoram https://orcid.org/0000-0002-6571-3808

Research Article

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Physics and Modelling of Tri-Layered Strained Channel for Development of Double Gate n-channel FET

Kuleen Kumar and Rudra Sankar Dhar*

Department of Electronics & Communication Engineering, National Institute of Technology Mizoram, Aizawl, Mizoram, India (796012)

*Corresponding author e-mail: rdhar@uwaterloo.ca

Abstract- The strain silicon technology with FET is a dominant technology providing enrichment in carrier velocity in nanoscaled device by change of band structure arrangement. Leakage reduction while enhancement in drain current is another major objective therefore, designing a nano-regime double gate FET with strained channel is perceived. So, design and implementation of a double gate strained heterostructure on insulator (DG-SHOI) FET with tri-layered channel (s-Si/s-SiGe/s-Si) is the core. Biaxial strain is created in channel by inculcating three layers with optimal thicknesses while narrow channel depletion regions are strongly controlled by equipotential gates. Consequently, maximum charge carriers accumulate in channel due to quantum carrier confinement instigating ballistic transport across the 22 nm channel length device leading to lessening of intervalley scattering. In comparison to existing 22 nm DGSOI FET, drain current augmentation of 56% and transconductance amplification of 87.6% is observed while DIBL is prudently reduced for this newly designed and implemented DG-SHOI FET, signifying advancement in microelectronic technology.

Keywords: Strain Silicon, quantum carrier confinement, ballistic transport, SOI, FET devices

1. INTRODUCTION

On scaling CMOS technology into nano regime the conventional metal oxide field effect transistor (MOSFET) faces major hindrance due to massive short-channel effects such as drain induced barrier lowering (DIBL) subthreshold leakage, velocity saturation, punchtrough, hot electron effect, gate induced drain leakage (GIDL) [1-4], and accordingly the expected output characteristics and performance of the device at nanoscale is tarnished [3-5]. Multiple methodologies are incorporated in conventional MOSFETs to improve the performance at nanoscale, which are namely reduction in gate oxide thickness, increased doping concentration, indulging high-k dielectrics, incorporation of dual material gate, pocket implantation, lateral channel engineering, silicon-on-insulator (SOI) technology, strained silicon (s-Si) technology [4-8]. But, as source and drain

doping concentrations are increased the mobility of charge carriers decreases, while the junction capacitances at gate-source (C_{gs}) and at gate-drain (C_{gd}) escalate significantly [3, 5-9]. With reduction in gate oxide thickness the carriers acquire enough energy due to applied gate voltage and become trapped into the gate oxide region at high electric field [10]. So, the overall performance degrades hence, induction of high-k dielectric substituted compensating the reduced oxide thickness by increasing the total gate capacitance for nano-regime device. On the other hand, introduction of high-k creates additional hitches in channel mobility leading to fermi level pinning at the MOS work function near the gate [11] resulting in tunnelling based leakage within the device, which is not desired. Pocket implantation technique is another dominating choice to enhance device performance but, this generates large drain induced threshold voltage shift and low output resistance, which is not suited for application in high performance analog circuits [12-14], thereby discarded at many instances.

Due to shortening of channel length, gate tends to lose its control over the channel and the device, so subthreshold leakage current engenders [3, 15, 16] prompting abnormality in device performance. Hence, developing vertical FETs in the form of double-gate/tri-gate structures and integrating them with unconventional technologies (SOI, high-k, etc.) are some of the alternatives that researchers are looking into since the last decade for augmentation of device performance at nanoscale [12, 14-16]. One of the promising device structure that surfaced in nano-regime having an additional gate on other side for better control over channel depletion region employing SOI technology is the double gate silicon-on-insulator (DGSOI) MOSFET, which avoids field penetration from source/drain to the substrate ensuing reduction in leakage enriching the output characteristics [17-19].

The DGSOI FET provide superior performance but for devices with L_g at sub-50 nm and beyond the performance worsens due to major short channel effects such as DIBL and punchthrough of carriers [17], which leads to stimulation of quantum tunnelling heaving in the nanostructure. Consequently, strain engineering phenomenon is designed in device physics. The concept of strain technology was first incepted in semiconductor physics in 1980s by growing strain silicon film over relaxed SiGe [20], but then the strain effect was largely overlooked. It was in 1990s that MIT, USA revived the concept of strain

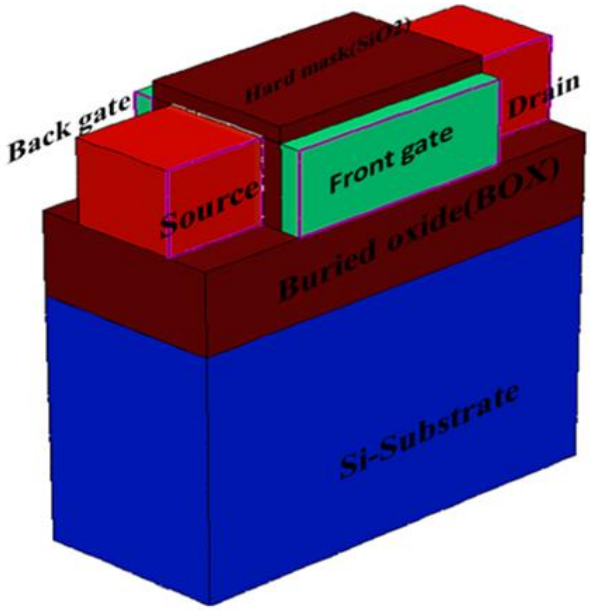
effect and the first n-channel MOSFET with strained silicon channel exhibiting 70% higher mobility was developed [21, 22]. Strain technology was later adopted by major semiconductor device companies like Intel, IBM and AMD at 90 nm node along with Silicon on Insulator (SOI) technology [23]. In 2008, Kumar et al. [24] already developed a dual channel based strain silicon technology device for improved performance at 100 nm channel length. For nano-devices below 100 nm mobility becomes field dependent due to increase in lateral and vertical electric fields. Thus, velocity saturation and negligible scattering of carriers near the surface, affects in elevating mobility and drive current of the device immensely as observed by Khiangte et al. [25]. Thereby, Khiangte et al. [25] developed a tri-layered (s-Si/s-SiGe/s-Si) channel heterostructure on insulator (HOI) planar MOSFET, where the concept of strain channel engineering was employed to modify the band structure, increasing mobility and drain current. The HOI MOSFET incubated ~49% drive current advancement for 40 nm channel length device [26]. On scaling down to L_g = 30 nm, the HOI MOSFET had to be deformed by Dhar et al. [26] for enriched performance with allowable short channel effects as per the International technology roadmap for semiconductor (ITRS) 2015 [27]; hence, further scaling the gate length is nearly impossible in planar MOSFETs. Henceforth, designing a novel device implementing the established HOI system in the vertical form may be a probable solution and is therefore the need of the hour.

Having the concept for inducing strain engineering in the channel region of FET to eliminate quasi-neutral floating body effect in SOI FETs to deepen drain current by quantum carrier confinement [23] and ballistic transport of carriers is the motivation, so employing HOI system in double gate (DG) structure to design and develop a novel DG-SHOI FET for the first time with the distinguished tri-layered channel system sandwiched between the two-gates is therefore, the focus of this paper. This SHOI structure based DG device is expected to induce quasi-ballistic transport leading to quantum carrier confinement in the well region of the channel and in turn achieve enhanced drain current when implemented. So, the novel nano-regime DG-SHOI FET anticipates to be capable of minimising short channel effects inculcating quantum tunnelling phenomenon for ballistic transport of carriers providing increased mobility at

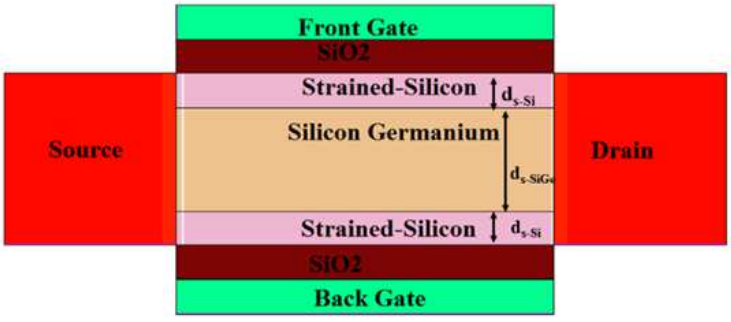
maximum electric field for minimal DIBL and high transconductance with boosted electron drift velocity.

2. THEORY AND DEVICE STRUCTURE

To design and develop the proposed Double Gate Strained Heterostructure on Insulator (DG-SHOI) n-channel transistor a detailed theory and understanding for the device is to be established, which is based on implementing strain engineering incorporated within the device channel. A schematic device structure in 3-dimensional (3D) is shown in Figure 1(a) while Figure 1(b) provides the cross-sectional view of the channel and Figure 1(c) details the channel lattice structure. The device structure is designed and developed using Sentaurus TCAD [28] employing the parameters and constraints as tabulated in Table 1. The drift diffusion and piezo-resistive coefficient models are combined along with the Shockley Read Hall (SRH) doping dependence parameters while modelling the device in Sentaurus TCAD [28].



(a)



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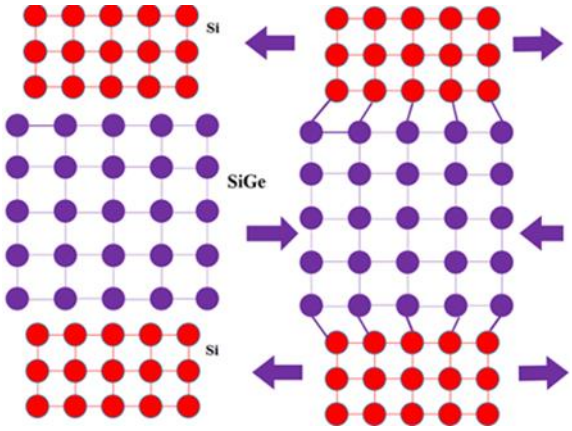


(c)

Figure 1 (a) A schematic structure of DG-SHOI FET on 22 nm channel length. (b) A cross sectional view of channel region along with source and drain in DG-SHOI FET. (c) Atomic structure layout for strained system within tri-layered channel.

The device surface considered for demonstrating is oriented along (100) direction while the channel is along (011) direction being oriented vertically on the structure. The buried oxide layer is incubated in the device to prevent the penetration path of the electric field from source/drain to substrate as is the case in SOI MOSFETs [29-31] thereby a DG-SHOI structure is designed and developed. The SiO_2 (gate oxide) layers are grown on either side over the s-Si layer as hard mask to avoid field penetration from the top eluding formation of additional defects in the structure, which may deform expected device performance. The strained heterostructure channel forms a tri-layered system comprising of s-Si/s-SiGe/s-Si with 2-6-2 nm thicknesses, is implemented and nurtured between front and back gates as depicted in Figure 1(b) while the strain amalgamation is shown in Figure 1(c). Both gates are symmetrically designed having same work function and are electrostatically coupled. So, strong electric potential is settled across the channel effectively controlling source and drain energy barriers for carrier transport with less scattering effect than in planer MOSFETs of L_g = 30 nm and beyond that installs variety of short channel effects [14-16, 25, 26, 32-34]. The electric field at drain edge is expected to reduce on employing the two gates due to hot carrier effect being condensed [4]. Hence, source/drain doping concentrations are made high to reduce the channel resistance, which eventually anticipates in increasing the drive current lessening the leakage current in the proposed device.

Table. 1 Double Gate SHOI FET with Tri-Layered channel parameters

Parameters	**Dimensions**
Channel length (L_g)	22 nm
Channel width (W_{ch})	100 nm
BOX thickness (d_{Box})	1μ m
Ge mole fraction (m_0)	0.4
s-Si layer thickness ($d_{s\text{-}Si}$)	2 nm
s-SiGe layer thickness ($d_{s\text{-}SiGe}$)	6 nm
Gate Oxide thickness (d_{ox})	2 nm
Si Source and Si Drain doping (N_D)	10^{18} cm^{-3}
Channel doping (N_A)	10^{16} cm^{-3}

Hence, stands the motivation for scheming of the vertical channel DG-SHOI FET, which is projected to be beneficial over the planer MOSFET ensuring admirable control on the channel providing greater device performance following minimal current leakage, though highly optimistic due to incorporation of strain engineering especially for the narrow width channel region [24-26]. The two Si layers generates a mismatch of 4.2% in the channel with sandwiched SiGe alloy inviting strain with the band structure of the layers [30-34], thus, biaxial strain is realized [25, 26]. Based on the design developed by Harrington et. al. [32] the total strain for the proposed DG-SHOI FET device is calculated and is given as:

$$\varepsilon_{strain} = \frac{d_{soi} - d_{ch}\ (\varepsilon_{ch-strain})}{d_{soi}} \qquad (1)$$

where $\varepsilon_{ch\text{-}strain}$ is the biaxial strain induced in the channel which is a function of d_{ch} the strained channel thickness that embraces three layers ($d_{s\text{-}Si}$ $d_{s\text{-}SiGe}$ $d_{s\text{-}Si}$) and each layer thicknesses are as specified in Table 1. Total device strain is calculated considering the mismatch strain along with the SOI substrate. $\varepsilon_{ch\text{-}strain}$ is designed as summation of the total strain among the layers in the channel and as s-SiGe is 6 nm thick it serves equally (3 nm each) as the base for both the s-Si layers of the device and is calculated as:

$$\varepsilon_{ch-strain} = \sum \frac{d_{s-SiGe} - d_{s-Si}}{d_{s-SiGe}} \qquad (2)$$

So in total the channel strain ($\varepsilon_{ch\text{-}strain}$) is given by:

$$\varepsilon_{ch-strain} = 2\left(\frac{d_{s-SiGe} - d_{s-Si}}{d_{s-SiGe}}\right) \qquad (3)$$

On substituting $\varepsilon_{ch\text{-}strain}$, the total device strain, ε_{strain}, is achieved for the tri-layered system to be:

$$\varepsilon_{strain} = \frac{d_{soi}\, d_{s-SiGe} - 2(d_{s-SiGe} - d_{s-Si})}{d_{s-SiGe} d_{soi}} \qquad (4)$$

where d_{s-Si} and d_{s-SiGe} are different lattice thicknesses in channel as shown in Figure 1(b) and (c) and d_{soi} is the substrate thickness. On incorporation of this biaxial strain at high electric field negligible amount of degradation of electron and hole mobility is observed due to reduction in effective mass of the material [23, 28-31]. The strain in the channel is applied in (010) and (001) directions as the channel is oriented in (011) direction. As the effective mass lies parallel to strain axes, strain valleys are created perpendicularly as shown in Figure 2, consequently lowers the effective mass of electrons and in turn increases the electron mobility in the system [25, 31, 33]. This biaxial strain in device is actuated on applying strain throughout the channel, which reduces effective mass by shifting the degeneracy levels at the conduction and valance band edges. Shifting of energy bands enact in splitting the energy levels, which occurs due to the fact that no two electrons can reside in the same energy level as per Pauli's exclusion principle. The energy level splitting relates to band splitting directly instigating that conduction band splits into two fold valleys ($\Delta 2$) and four fold valleys ($\Delta 4$) as illustrated in Figure 2. This result of band splitting and lowering of effective mass due to strain is in line with the atomistic calculation carried out using Density Functional Theory (DFT) [34, 35] and its effect was later developed and studied for strained channel MOS transistors [36-37].

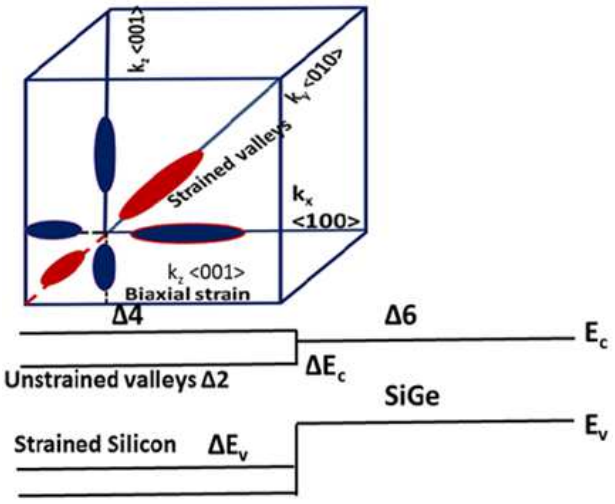


Figure 2. Schematic illustration of band structure deformation with biaxial strain.

The valance and conduction band energy level splitting along the thickness of the channel alters the band structure and affect the carrier transport phenomenon as atomic lattice spacing in the region becomes loosely packed in the s-Si layers enhancing electron mobility leading to ballistic transport at nano-dimensions; an oblivious occurrence with less scattering events [24, 25, 36]. This is supplemented with the device having nanometer scale channel length and width that endorses in increasing mobility. Thereby, with incorporation of biaxial strain along with the cohort of additional control over the nano-channel DG-SHOI FET, enhanced carrier mobility is expected leading to influence device performance by enriching the drive current.

3. RESULTS AND DISCUSSION

The novel DG-SHOI FET structure is designed and developed for the first time solving the carrier continuity and Poisson's equations simultaneously in both the dielectric interfaces while implementing the solved biaxial strained lattice calculation for the hetero-tri-layered (s-Si/s-SiGe/s-Si) interface along with the 1D Schrodinger's equation. The design accuracy is based on the exactness of calculating the threshold voltage of the device. The threshold voltage for unstrained silicon DG FET is given by [38]:

$$V_{th} = V_{FB} + \varphi_{ms} + V_T ln\left(\frac{Q_{inv}}{n_a d_{ch}}\right) \qquad (5)$$

where the flat band voltage $V_{FB} = \frac{\varphi_m - \varphi_s}{q}$ φ_m and φ_s are metal and semiconductor work functions, q is electronic charge, φ_{ms} is gate work function with respect to

intrinsic silicon, n_a is the acceptor doping concentraion present in the channel, dch is the silicon channel thickness, V_T is thermal voltage and Q_{inv} is inversion charge density of the device. Now for the DG-SHOI device the induced biaxial strain developed in Eq (3) is substitued in Eq (5) along with the potential work function of the hetero-materials in the channel and finally the threshold voltage, V_{th} for DG-SHOI FET is calculated as:

$$V_{th} = V_{s-FB} + \varphi_{ms} + V_T ln\left(\frac{Q_{inv}}{2n_a\left(\frac{d_{s-SiGe} - d_{s-Si}}{d_{s-SiGe}}\right)}\right) \qquad (6)$$

where $V_{s-FB} = \frac{\varphi_m - (\varphi_{s-Si} + \varphi_{s-SiGe} + \varphi_{s-Si})}{q}$

Acquiring the threshold voltage (V_{th}) of the tri-layered strained channel device, the vigorous leakage drain induced barrier lowering (DIBL) is calculated for a minimum and maximum drain voltage (V_{DS}) of 0.05V and 1V respectively, applied on the DG-SHOI FET and is given as:

$$DIBL = \frac{V_{th=1v} - V_{th=0.05v}}{V_{DS=1v} - V_{DS=0.05v}} \qquad (7)$$

The calculated threshold voltage, V_{th}, and DIBL for DG-SHOI FET is plotted and compared with HOI MOSFET [25] and DGSOI FET [17] devices as shown in Figure 3. As evident the V_{th} for 22 nm DG SHOI FET is observed to be less with respect to DGSOI FET while an enormous reduction of 57.6% in DIBL is perceived, subsequently authorizing the benefit of implementing strained channel in the device. This reduction in DIBL can be substantiated due to unfolding of band bending effect on strain application in channel instigating quantum tunneling of carriers with minor scattering. Also the V_{th} and DIBL of HOI MOSFET and DG-SHOI FET are found to be analogous, which is highly advantageous as the leakage is maintained within limits, though device gate length is drastically scaled from 50 nm to 22 nm while forming the DG structure. Therefore, it can be ascertained as two gates of DG-SHOI FET equally and simultaneously controls the ultrathin strained channel the threshold voltage roll off dispute in planar HOI MOSFET is outshined due to occurrence of ballistic transport of carriers with less scattering events in the channel as is inherent from Figure 3. Therefore, these effects are expected to stimulate improvement in mobility in the DG-SHOI FET device.

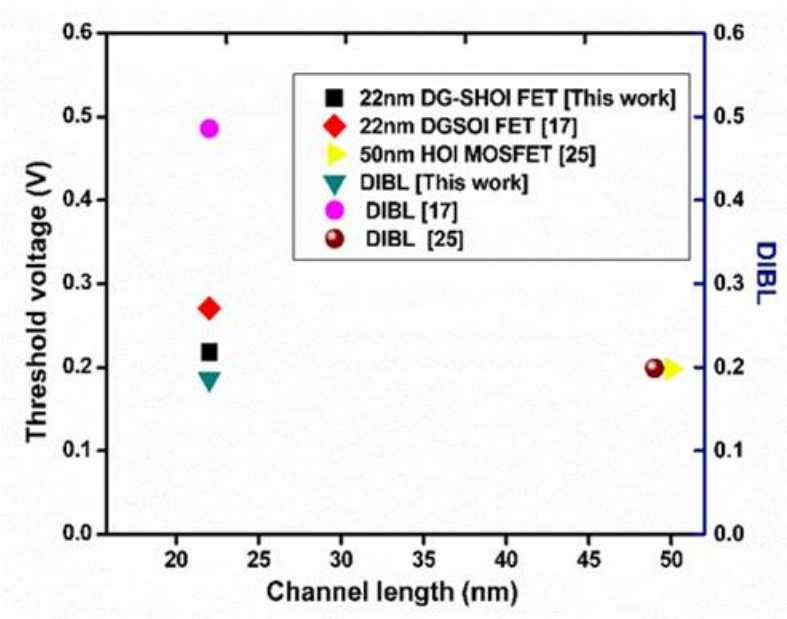


Figure 3. Threshold voltage and DIBL compared among DG-SHOI FET, DGSOI FET and HOI MOSFET devices.

The proposed expansion in mobility is mostly prompted due to strain induction in the channel on hole based structure as analysed using empirical pseudopotential (EPM) and k-p methods [39, 40]. With the mole fraction of Ge as 0.4 in $Si_{1-x}Ge_x$, electron affinity of silicon increases due to strain [39] influencing the band splitting effect and decreases the bandgap to a lower energy level at conduction band edge as observed in Figure 4 at V_{GS} = 0.28 V and V_{DS} = 1 V. Thereby, distorting the fermi level for the structure on induction of electric field in the channel system. This Si/SiGe/Si heterostructure appendages to the formation of Type-II band alignment in the channel with ultrathin layers forming quantum well barrier system capitulated between two gate dielectric (gate oxide-SiO_2) layers that forms infinite potential barriers. The energy gap between allowed energy level increases as a consequence of electron confinement in these nano layers, so, the mobility of charge carriers escalates leading to quasi-ballistic transport in the system. The density of states (DOS) of holes in valance band decreases as an effect of strain while the transverse effective mass increases perpendicular to stress and decreases parallel to stress. So, the conduction band energy level is increased leading to added carrier accumulation in the s-Si layer which infuse transport of electrons through the quantum well-barrier system in the channel. On having an extra gate and narrow channel width in comparison to the planer HOI MOSFET of Khiangte et al. [25], additional potential exists along

with quantum carrier confinement occurring in the ultrathin channel. Most of the charge carriers accumulate in top s-Si layer for either gate, so inversion layer is developed from bottom to top s-Si layer. The lattice spacing between s-Si and s-SiGe increases due to the induced strain, subsequently, mobility of charge carrier is amplified with minimum intervalley scattering. This increased electron mobility as seen in Figure 5(a) shoves the velocity to reach velocity overshoot condition as observed in Figure 5(b) in comparison to 50 nm HOI MOSFET [25]. Figure 5(c) clearly depicts the drift velocity variations for three layers of the channel in this novel 22 nm DG-SHOI FET. The effect of quantum carrier transport is evident due to the existence of electric field in the system for which band bending is prominently observed in the conduction band energy level of Figure 4. The notch detected at SiGe-Si (bottom Si layer) interface of the conduction band as in Figure 4, owes to internal electrostatic potential in the tri-layered system which regulates electron accumulation influencing in enhanced carrier transport. The charge carrier mobility in the tri-layered channel depends upon the strain induced in it and the inversion charge impelled by the two gates.

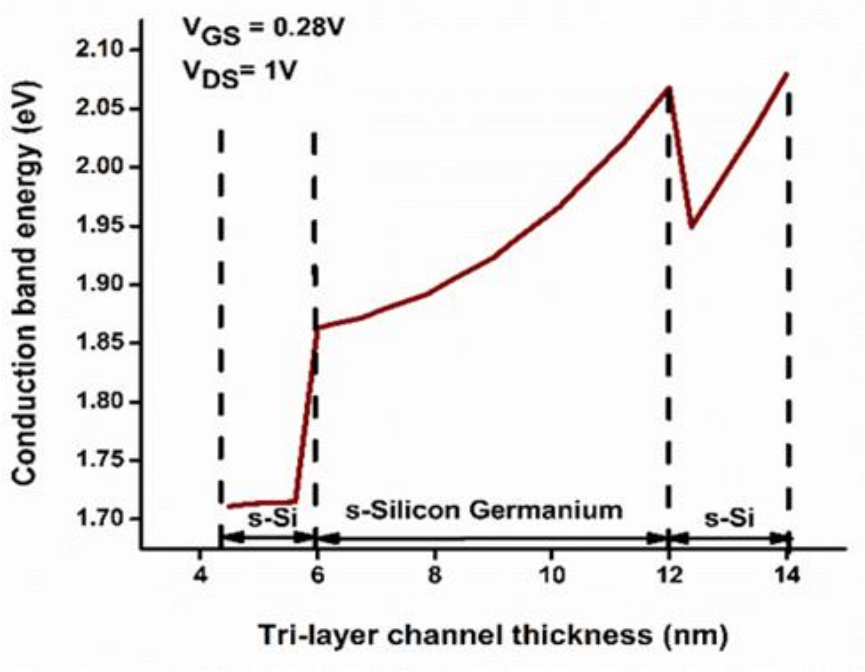
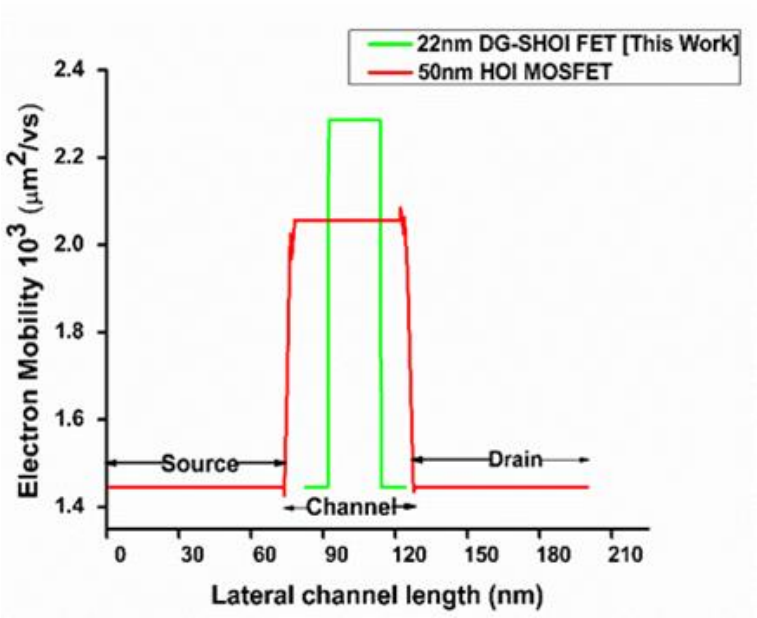


Figure 4. Conduction band energy level along tri-layer channel thickness for DG-SHOI FET.

The strain when implemented in the short channel device the bandgap becomes narrower as the constituent atom befits heavier and they are tightly confined in all three directions. The transverse effective mass decreases due to

smaller difference between lower and upper sub bands in the quantum well. The electron mobility is inversely proportional to the transport effective mass. The maximum electron velocity is attained by charge carrier in inversion layer as another gate also provide equal potential to the other side of the channel. Therefore, maximum carriers are confined in the s-Si layers and relentless electron mobility is observed along lateral channel direction as observed in Figure 5(a). Though, mobility enrichment is observed but in the novel design of DG-SHOI FET the leakage is well within the ITRS 2015 standards [27] as revealed in Figure 6 in comparison to other existing devices.



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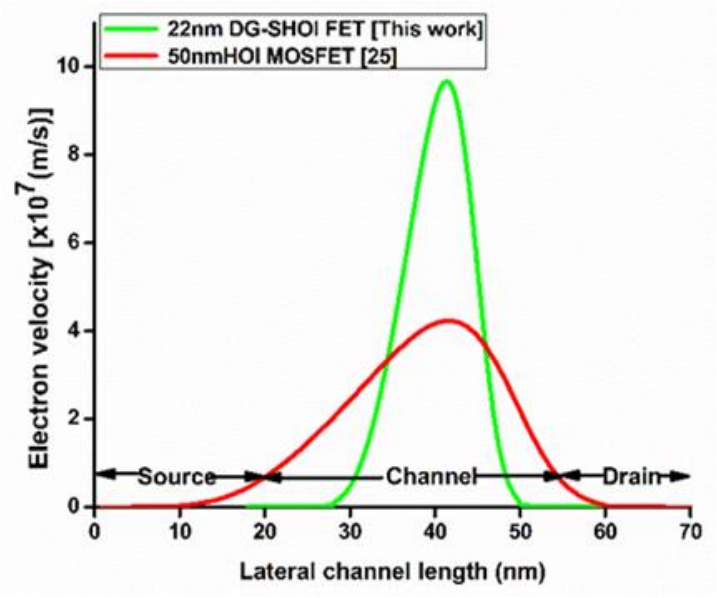

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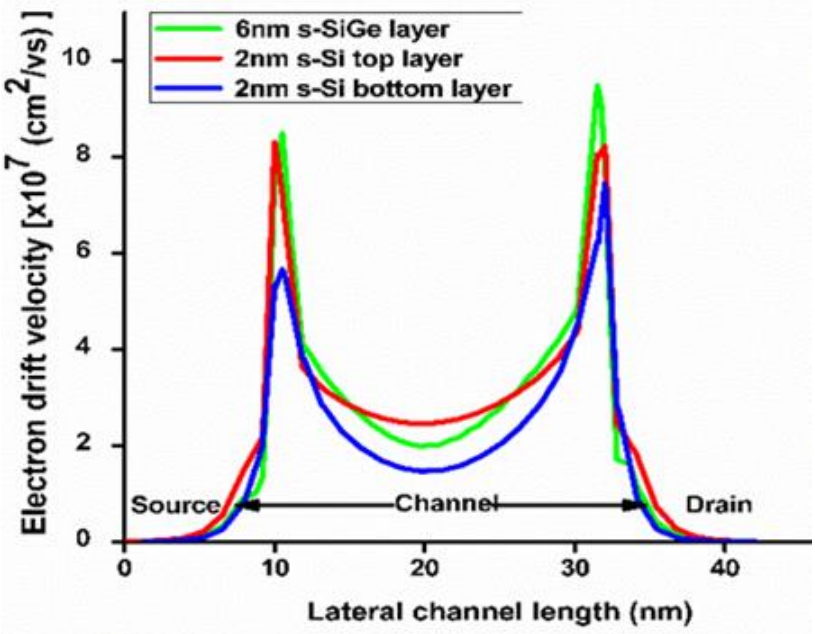

(c)

Figure 5 (a) Comparison of Electron mobility of DG-SHOI FET on 22 nm channel length with 50 nm HOI MOSFET (b) Examination of electron velocity along the channel length. (c) Study of electron drift velocity within three layers (s-Si/s-SiGe/s-Si) in DG-SHOI FET.

The electron and drift velocity are observed along the channel length by applying gate bias voltage (V_{GS} = 0.28V) at two gates. The strong inversion layer is developed by coupling of two gates at s-SiGe interface layer, which is sandwiched between two s-Si layers so majority charge carries resides in s-SiGe layer and high electron velocity is pragmatic as shown in Figure 5(b). The maximum charge carriers flow from source to drain due to extreme drift velocity acquired by electrons as a result of ballistic transport in the short channel (length and width) device so that less intervalley scattering and maximum drift velocity (8.0 x 10^7 cm^2/s) is attained by the carriers as perceived in Figure 5(c). The current voltage transfer characteristics (I_D-V_{GS}) at V_{DS} = 0.5 V of novel 22 nm channel length DG-SHOI FET is analysed and compared with 50 nm channel length HOI MOSFET [25] and the conventional 22 nm DGSOI FET [17] in Figure 6. It is evident that the HOI MOSFET provides better performance at lower voltage while at V_{GS} > 0.28 V the current of DG-SHOI FET merges indicating boosted performance with less scattering and excavated mobility a fact conserved due to quantum carrier confinement and tunnelling effect in the system. The inset of Figure 6 hence pinpoints a lesser leakage for this novel device of 22 nm gate

length in comparison to the 50 nm HOI MOSFET though both the leakages are within acceptable range as per the ITRS 2015 [27]. This is due to the declining of the threshold voltage roll off by 10.6% for quantum carrier confinement compiled with implementation of narrow channel width in the device.

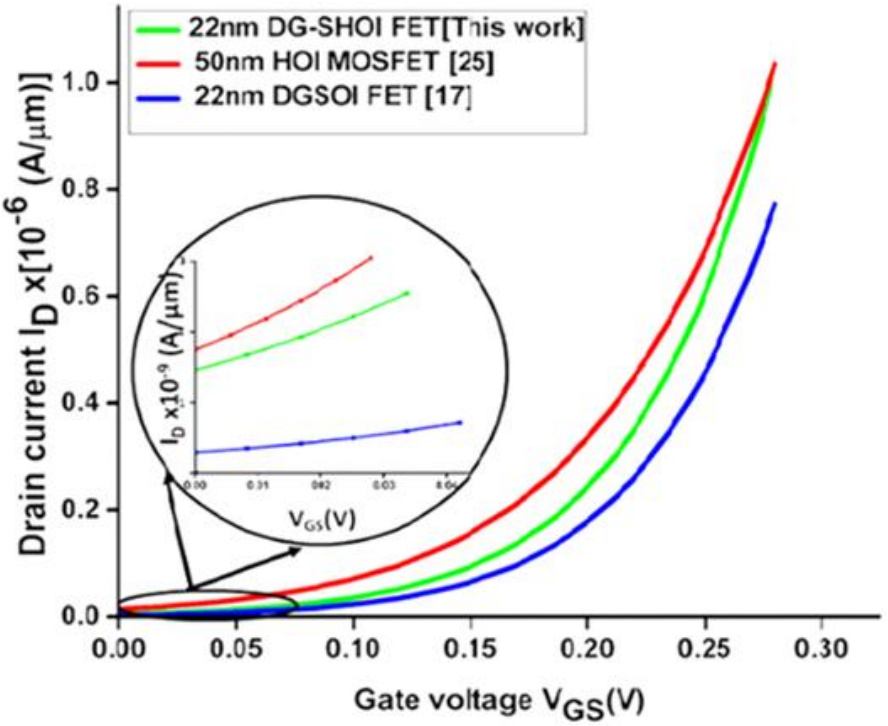

Figure 6. I_D–V_{GS} transfer characteristics of DG-SHOI FET compared with HOI MOSFET and DGSOI FET for determining subthreshold leakage current variation.

The low leakage as observed in DG-SHOI FET is substantiated with increase in mobility and is further witnessed from Figure 7, which obviates the assessment of transconductance ($g_{m(max)}$) to DIBL for the FET devices. As the device is detected to have less subthreshold leakage in Figure 6, the transconductance is alleged to maximize for DG-SHOI FET in comparison to other devices at very low DIBL providing boosted device performance. The improvement in transconductance by 87.6% for newly designed 22 nm channel length DG-SHOI FET as noticed in Figure 7 instil velocity overshoot condition with simultaneous decrease in DIBL. This is a huge gain for the novel DG-SHOI FET with respect to HOI MOSFET [25] that suffered from the trade-off due to short channel effects at nano-regime (below L_g = 50 nm). The potential barrier lowering exponentially increases the source to drain leakage current; therefore, DIBL becomes a crucial parameter measuring the performance of the device at 22 nm technology node. But, with DIBL reduction and increased transconductance

the 22 nm DG-SHOI FET proves to be quite beneficial, thus provide enhanced carrier mobility due to quantum carrier confinement and ballistic transport across the device, which is overlaid in Figure 8 with augmented drain current characteristics. These effects and observations are caused by nominal threshold voltage roll off and the occurrence of reduced scattering events under the influence of biaxial strain which owes to band bending and splitting of conduction band energy levels in the hetero tri-layered channel structure of the novel device.

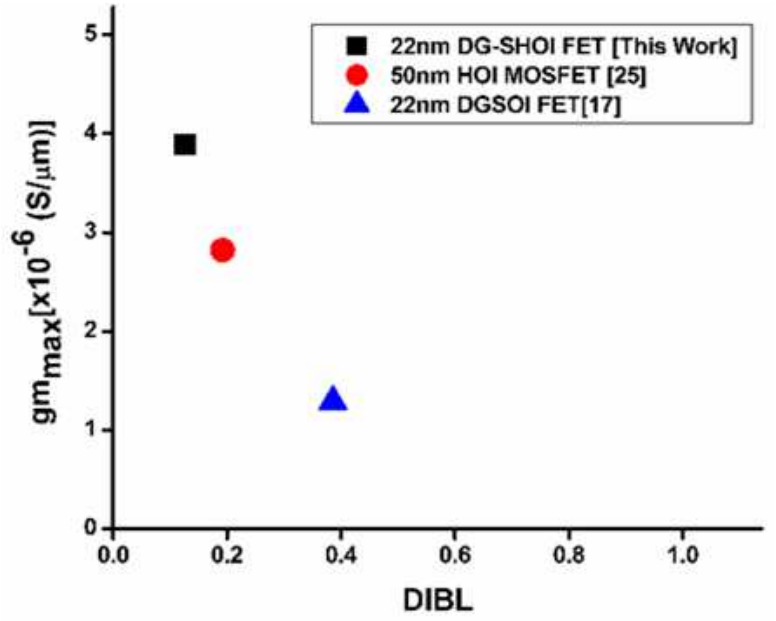

Figure 7. Comparison of transconductance with DIBL for DG-SHOI FET, DG-SOI FET and HOI MOSFET devices.

The self-heating effect (SHE) is an aspect that degrades device performance from the expected yield for strained channel devices and that mostly affects the saturation region of the characteristics, but on implementing a thinner base layer (s-SiGe is 6 nm for DG-SHOI FET) the effect is immensely annulled as low thermal conductivity of ultrathin thermally stable SiGe consents accumulated heat to dissipate through the layers [41, 42]. So an enhancement of ~56% in drain current is observed without degradation due to SHE for the 22 nm gate length DG-SHOI FET in comparison to DGSOI FET as shown in Figure 8. This enriched current is supplemented due to the enactment of the biaxial strain, which induces boosted electron mobility leading to velocity overshoot condition for sub-nano device.

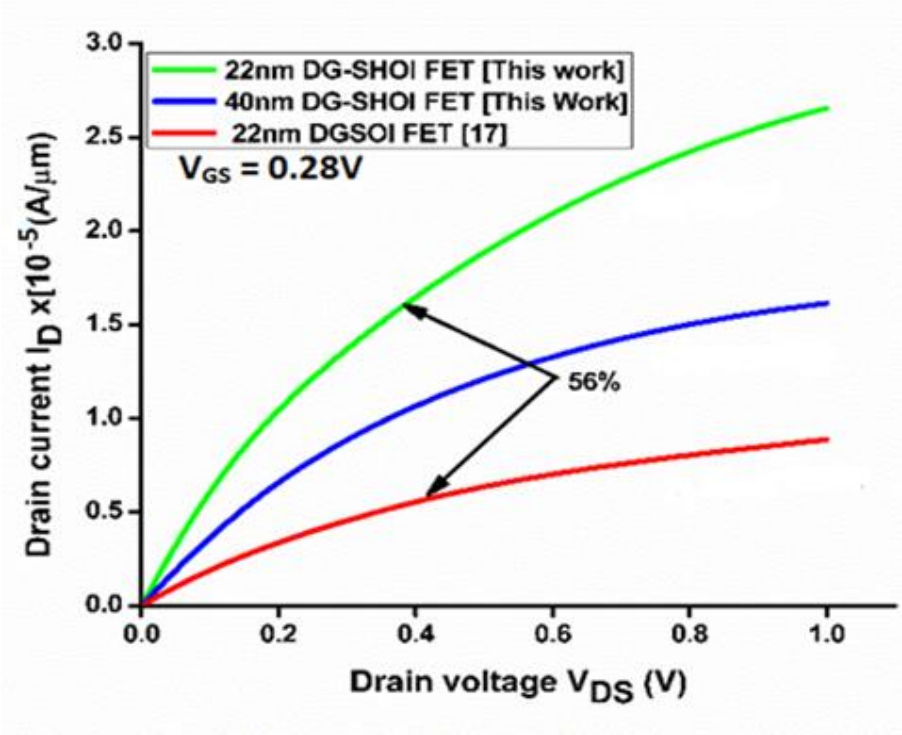

Figure 8. I_D -V_{DS} output characteristics of DG-SHOI FET compared with DGSOI FET for drain current showing 56% enhancement in device performance.

The mobility of charge carries in strained channel is increased as well as the drive current which is inversely proportional to the channel length so that the transconductance of DG-SHOI FET increases as detected in Figure 7 while reducing the channel length to 22 nm on application of the same gate bias (V_{GS}) as on 50 nm HOI MOSFET. As the channel length is reduced to 22 nm the potential barrier from source to drain is also reduced, so that threshold voltage of the novel device gets decreased minimizing V_{th} roll off leading to velocity overshoot condition. The change in threshold voltage at high drain bias (V_{DS}) is measured in terms of DIBL. This clearly elements to low subthreshold leakage and DIBL, thereby contribute in rousing the drain current of the device. The potential barrier of electrons in the depletion region is maintained by the additional gate and minimizes the barrier lowering effect in the device; accordingly subsidizes the reduction in current leakage of the device in comparison to HOI MOSFET. Hence, the novel design of 22 nm DG-SHOI FET proves to be the most beneficial device by being able to reduce the leakage providing enhanced drain current when implemented as exhibited in Figure 8, which is directly attributed to quantum carrier confinement effect in nano-regime quantum well-barrier structure developed by the narrow-width channel in the tri-layered channel system

installing biaxial strain in the device, thus instigating for improved mobility with velocity overshoot condition leading to ballistic transport of carriers in the device.

4. CONCLUSION

The novel DG-SHOI FET on 22 nm channel length is designed and developed here for the first time at nanometer scale channel width of 100 nm. The characteristic of DG-SHOI FET is compared with 22 nm DGSOI FET and with the previously developed 50 nm HOI MOSFET. The novel device performance is observed to have enriched extensively for drive current by 56% with acceptable leakage current of ~2 nA, as a result a highly beneficial structure is designed and implemented with the formation of quantum well structure within the narrow channel region. The increased band gap due to strain augments mobility of electrons in channel and strong inversion layer is developed by placing additional back-gate while forming this vertical double-gate structure. The carrier scattering is supressed by maintaining equipotential on two gates and instigating ballistic transport in nanoscale dimension. The decline in DIBL, high transconductance (87.6%), high electron mobility and drift velocity are evidently observed, which enhances the strength of drain current with V_{th} = 0.218V and minimal threshold voltage roll-off with quantum carrier confinement in well-barrier channel of the device. Thus, the newly designed 22 nm channel length DG-SHOI FET is implemented to afford minimal leakage with acceptable short channel effects and provide a fast operating (56% enriched) device as observed on induction of biaxial strain along with quantum carrier confinement in the s-Si layers of the tri-layered heterostructure channel system of the device.

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Consent to participate: Authors would like to give their consent to participate.

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Figures

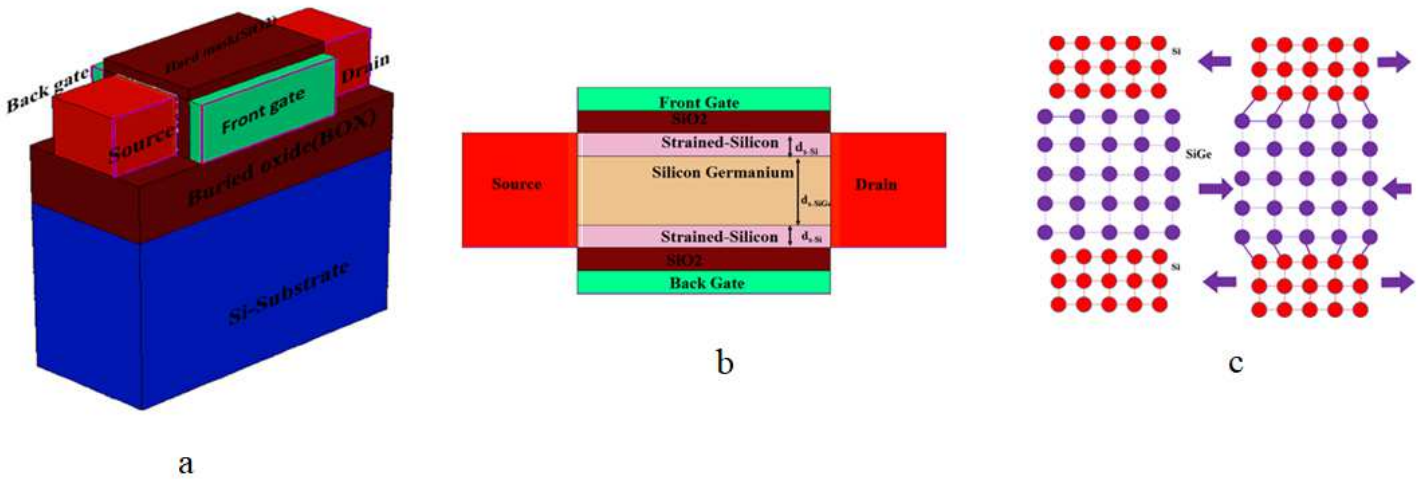

Figure 1

(a) A schematic structure of DG-SHOI FET on 22 nm channel length. (b) A cross sectional view of channel region along with source and drain in DG-SHOI FET. (c) Atomic structure layout for strained system within tri-layered channel.

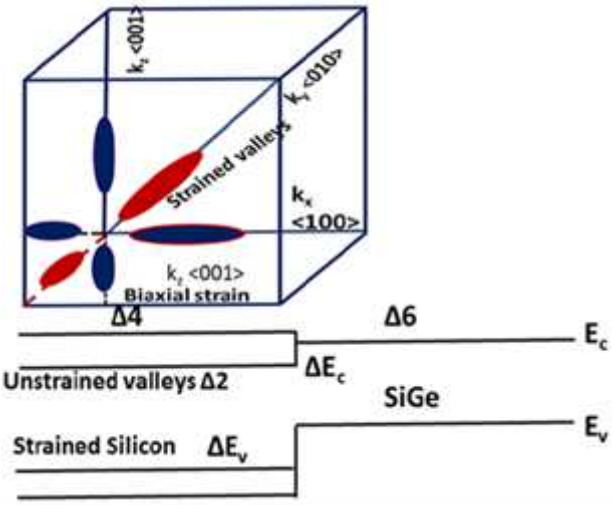

Figure 2

Schematic illustration of band structure deformation with biaxial strain.

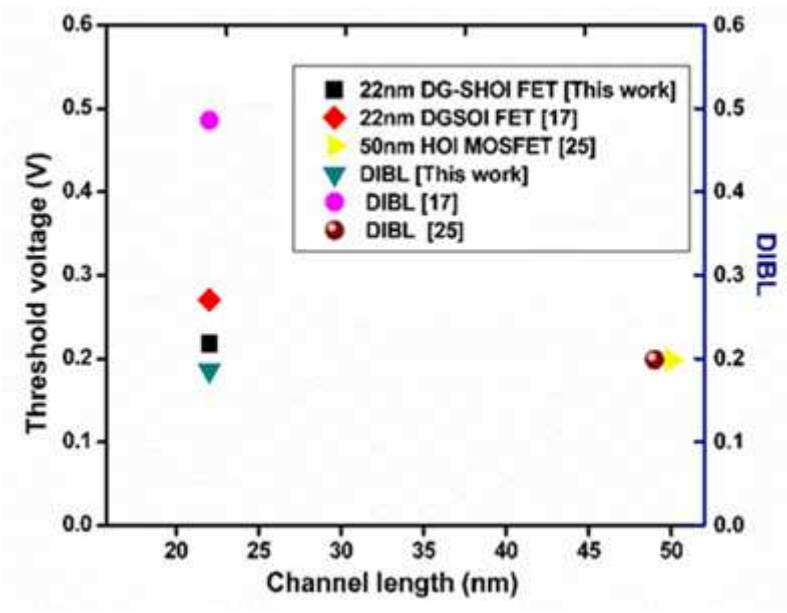

Figure 3

Threshold voltage and DIBL compared among DG-SHOI FET, DGSOI FET and HOI MOSFET devices.

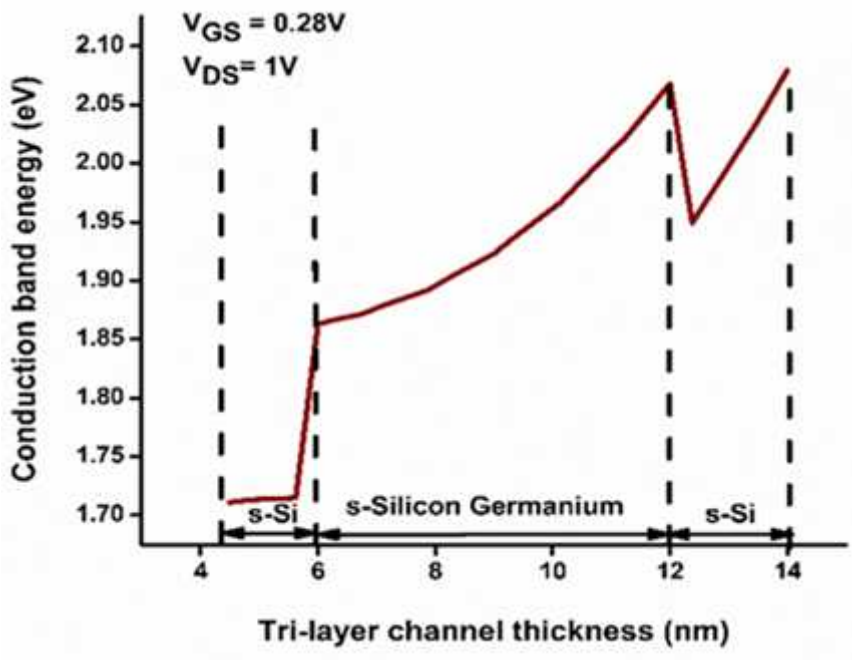

Figure 4

Conduction band energy level along tri-layer channel thickness for DG-SHOI FET.

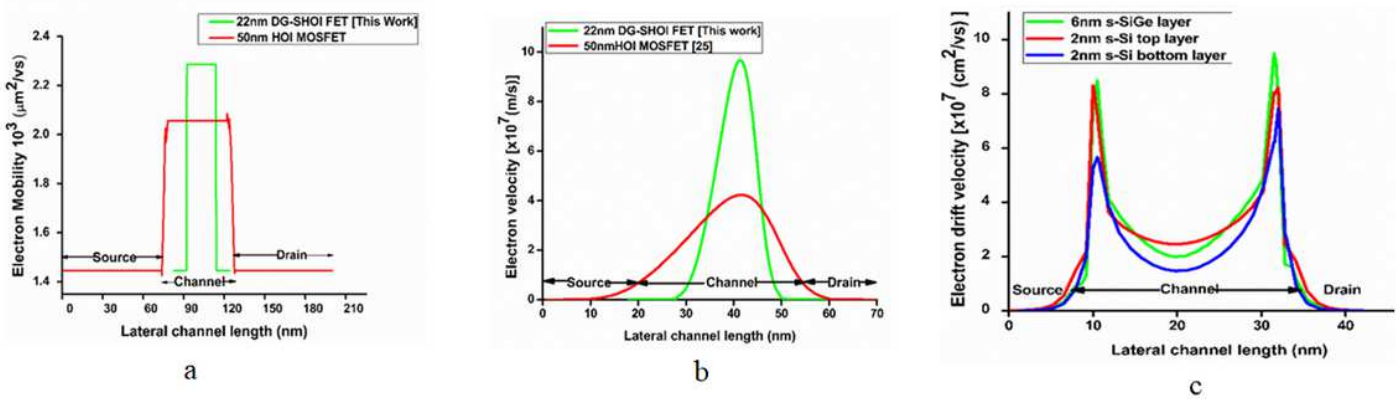

Figure 5

(a) Comparison of Electron mobility of DG-SHOI FET on 22 nm channel length with 50 nm HOI MOSFET (b) Examination of electron velocity along the channel length. (c) Study of electron drift velocity within three layers (s-Si/s-SiGe/s-Si) in DG-SHOI FET.

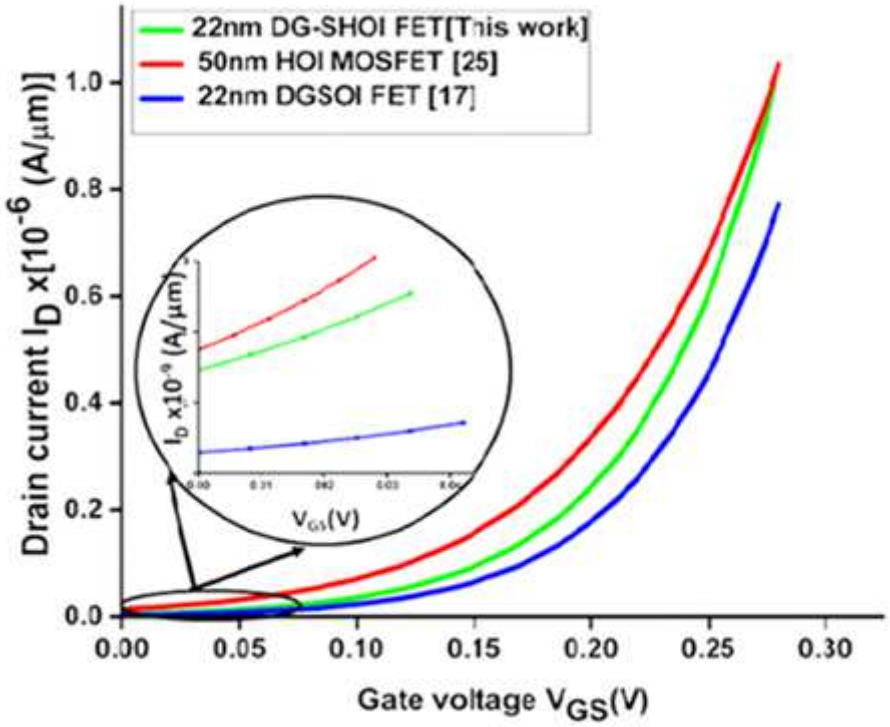

Figure 6

ID–VGS transfer characteristics of DG-SHOI FET compared with HOI MOSFET and DGSOI FET for determining subthreshold leakage current variation.

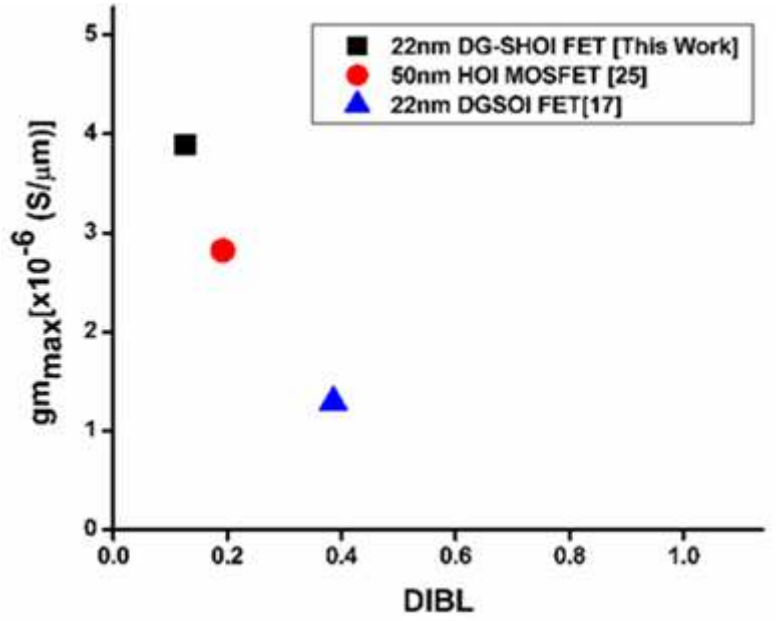

Figure 7

Comparison of transconductance with DIBL for DG-SHOI FET, DG-SOI FET and HOI MOSFET devices.

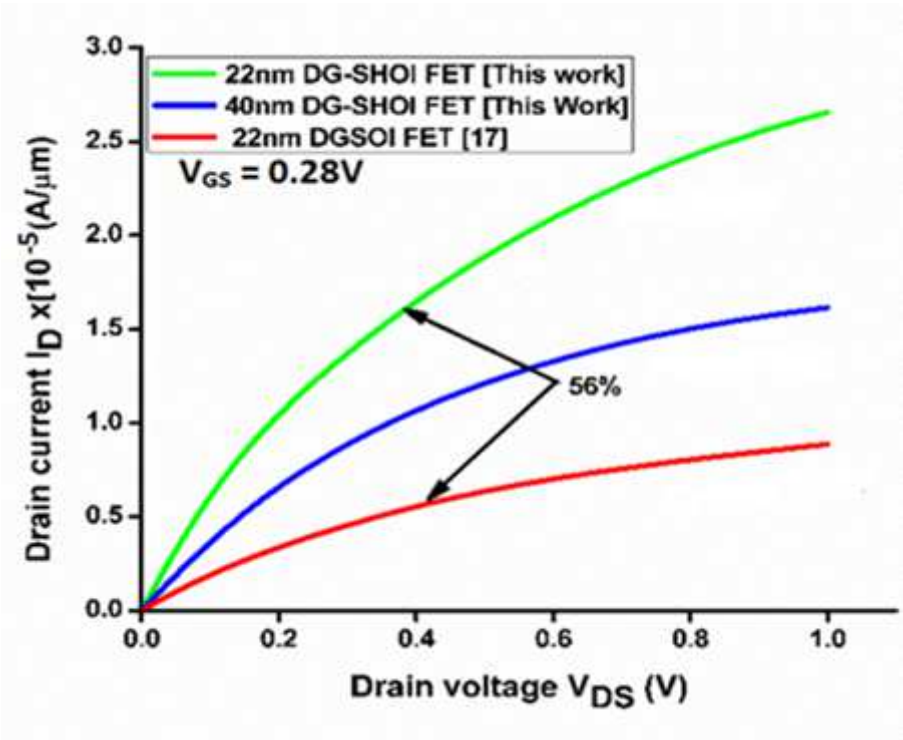

Figure 8

ID -VDS output characteristics of DG-SHOI FET compared with DGSOI FET for drain current showing 56% enhancement in device performance.