

# Effect of Gate Metal Work-function on Junctionless (JL) Nanowire GAA MOSFET Performance

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## Research Article

**Keywords:** CMOS, Nano, MOSFET, Work-Function, Metal

**Posted Date:** April 16th, 2021

**DOI:** <https://doi.org/10.21203/rs.3.rs-371047/v1>

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# Abstract

Metal gate technology is one of the promising methods used to increase the drain current by increasing the electrostatic controllability. Different metals have different work-function that controls the device performance very closely as gate to source voltage is the basic inputs for these. In this paper the dependency of gate metal work-function on device performance (both for nMOS and pMOS) is extensively investigated. The gate metal work-function value is taken as 4.2eV to 5.1eV with one increment to see the change in potential profile. With this condition, the  $I_{on}$  current,  $I_{off}$  current, threshold voltage, transconductance also calculated for these structures. A decrease value in drain current ( $1e-6$  to  $1e-7$  A) is observed for both the cases with increase in work-function of gate metal. However, the Off current is getting better ( $1e-7$  to  $1e-18$  A) while moving towards higher metal work-function values. As a result of which the  $I_{on}/I_{off}$  ratio increases which leads to higher device performances.

## Introduction

Every electronic integrated circuits depends on the semiconductor device called MOSFET. It is the most common transistor in digital circuits, a very large number of MOSFETs are used in a single memory chip or microprocessor. It is a 3 terminal device with Drain, Source and Gate as terminals. The technology of the MOSFET depends upon the channel length of the device [1–3]. The dielectric layer separates the gate terminal with channel that connects the source and drain terminals. When the gate voltage increases, then the charge carriers will move from source to drain terminal through the channel. The ON and OFF conditions of the MOS transistor depends on the charge carriers [4–7]. These charge carriers can be controlled by the gate voltage. If there is no applied voltage is given to the gate terminal, the current flow will be very less due to minority carriers [8, 9]. Threshold voltage of MOSFET is defined as the minimum voltage at which the device starts conducting is known as the threshold voltage. There are different types of MOSFETs developed according to the applications like Planar double gate, Omega gate, FINFET and Gate All Around MOSFET. All these MOSFETs will have gate dielectric material between the gate terminal and channel. As the device dimension is further decreases it cause the hot-carrier effects and will degrade the device performance [10–14].

As the device dimensions have entered into nano-scale, so the Nanoscale CMOS explored itself with various nonplanar device structures for better electrostatic control over the channel. Out of those structures, double gate, FinFET, Triple gate and gate all around ( Triangular, Rectangular and Cylindrical) have attracted much more attention compared to others [15–17]. In case of gate all around (GAA) MOSFET, the channel is fully surrounded by the gate from almost all the direction to enhance the electrostatic controllability [18, 19]. So the decrease in channel length or width will lead to change in gate control over the channel. This is the reason why this GAA structure is considered as the most suitable device for extreme scaling. However, process complexities will be there while fabricating short wires and the gate definition under the body are solved [20–22]. But in near future, GAA MOSFET is considered as the work horse due to its tight control over the channel to reduce short channel effect. In particular, these structures are having good subthreshold characteristics and almost ideal value for subthreshold swing

[23–26]. It is having better electrostatic controllability compared to other double or trigate devices [27–30]. GAA MOSFET based on Silicon are considered as the best alternative to the planar MOSFET because of better gate bias control. This will leads to the suppression of various short channel effects [31–34]

As CMOS technology continues to scale, there are different effects arises by doped polysilicon like high resistance, compatibility with high-k gate dielectrics and gate electrode depletion. To overcome this problem, metal gate electrode is introduced. To suppress the degree of Short Channel Effects, metal gate electrodes will require work functions that can be tuned to a desired value [35–38]. It is observed that poly-Si transistors exhibit severely degraded channel mobility. The reason behind it is due to the coupling of low-energy surface optical phonon modes arising from the polarization [39–42]. To obtain the high performance CMOS logic applications, metal gate electrodes with correct work function are required [43–47]. To operate the nMOS and pMOS properly, the work-function is adjusted in between 4.2eV to 5.1eV. The work-function in between 4.5 to 4.8eV suits best to design a proper n/p MOS [48–51].

## Device Design And Simulation

Sentaurus device simulator from SYNOPSIS is a state of the art semiconductor simulator to carry out the device simulation in nano scale regime [52]. This includes various physics for transportation with necessary physics. The simulator is equipped with structural device editor for device design, sdevice to give physics and biasing and inspect /svisual to visualize. It consists of quantum based physics to carry out the simulation for sub 10nm devices also. This simulator is designed to study the behavior of advanced semiconductor devices. This is a state of the art EDA tool that simulates both 2-D as well as 3-D structures. The simulation here is carried out for both nMOS and pMOS nanowire MOSFET with gate length of 60nm. Further the size is reduced up to 30nm to match the threshold voltages. The doping concentration of source/ drain and channel sections are doped with same concentration to make it a junctionless device.

Sentaurus Workbench is a dedicated graphical environment for creating, managing, executing and analyzing TCAD simulations effectively. Apart from those, Sentaurus TCAD is loaded with various physics to perform device simulation in nanometer region also. It is equipped with quantum based physics if the device dimension is shrinking down to 10nm also. The simulation is carried out for both junction and junction less nanowire GAA MOSFET. The threshold voltage,  $I_{on}$  and  $I_{off}$  matching also carried out for inverter realization.

Table 1  
Device dimensions of the proposed model (for both Junction and Junctionless MOSFET)

Type	Channel length (nm)	Source and drain length (nm)	work function (eV)	Channel doping ( $\text{cm}^{-3}$ )	Source and drain doping ( $\text{cm}^{-3}$ )	Oxide thickness (nm)	Channel Thickness (nm)
JL-nMOS	60	20	4.2–5.1	$1\text{e}+18$	$1\text{e}+18$	2	10
JL-pMOS	60	20	4.2–5.1	$1\text{e}+18$	$1\text{e}+18$	2	10
nMOS	60	20	4.2–5.1	$1\text{e}+16$	$1\text{e}+20$	2	10
pMOS	60	20	4.2–5.1	$1\text{e}+16$	$1\text{e}+20$	2	10

The Sentaurus TCAD generated structure and its cut sectional view is represented in Fig. 1 for the JL-GAA MOSFET. The doping concentration of source, drain and channel is kept as  $1\text{e}+18$  to make it as junctionless. The oxide ( $\text{SiO}_2$ ) thickness for all the structures is kept as 2nm and the channel thickness as 10nm. The gate metal work function is varied from 4.2eV to 5.1 eV, in order to study the performance variation with the influence of work-function value. The analysis included initially the variation in surface potential and ends with transconductance analysis.

## Results And Discussions

The energy band diagram is the best source to understand any semiconductor device working. The band bending in semiconductor device depends on the gate bias that we are giving at the gate electrode. The energy band diagram moves up and down as the electrostatic potential moves up and down. The potential distribution near the interface of channel and dielectric can be observed from Fig. 2. The work-function of the gate metal are considered as 4.2 eV to 5.1 eV and the corresponding surface potential developed is illustrated in the figure clearly. A built in potential is developed near the source side denoted by  $V_{bi}$  and creates a slope near the source channel interface. Same kind of behavior is observed near channel drain interface and add up drain voltage to built-in potential to make it  $V_{bi}+V_{ds}$

The value of built in potential is around 0.48 V and applying a drain voltage of 0.05 volt, at drain end it became 0.485 V. Similar to the source channel interface, there is a slope starts near channel-drain interface and ends near the drain by adding drain voltage to built in voltage. The electrostatic potential profile goes down as the gate metal work-function is increasing. The developed potential near the channel and oxide interface is a flat and almost uniform throughout. However, near source-channel and drain-channel junction it is different due to different region and different biasing. Similar kinds of things are obtained with high drain bias also. In Fig. 3, the application of little gate bias is pulling the potential curve little bit up and for lower work function it is observed above the built in potential. However, the

property of adding drain voltage to the built in potential towards drain side remains the same. With an increase in drain bias, the uniformity in surface potential gets disturbed and the shifting is observed more towards drain side. This can be easily observed from Fig. 3. With the increase in gate bias, the potential curve will lift up and will create potential minima towards the curve near source side. However, drain current will be added up to the built in potential value if the drain voltage is further increased. With a further increase in gate voltage, the curve will lift up again and the minimum point in this surface potential curve will be considered as potential minima for threshold voltage calculation. The metal work-function plays a vital role for potential profile formation and threshold voltage calculation.

From the figure, the impact of gate material and its work-function on electrostatic potential distribution is well observed. The effect of drain bias in device potential curve along with work-function from 4.2eV to 5.1eV is shown in Fig. 3. Similarly the potential distribution for different work-function for pMOS is illustrated in Fig. 4. The gate voltage for this case is kept 0V with a drain bias of 0.05V

From the figure, it can be observed that the potential profile is lifted up for low work-function and becomes flat with increase in metal work-function. The potential profile is similar to that of nMOS and it also carries the same value as  $V_{bi}$  towards source and  $V_{bi}+V_{ds}$  towards drain. The gate voltage applied for this case is -0.2 V where as the drain voltage is little bit higher i.e 0.5V. The distribution of electrostatic potential from source to drain through the channel can be we observed from Fig. 5.

Figure 6 indicates the transfer characteristics of the proposed JL-nanowire GAA MOSFET (n-MOS) for different metal work-function values. From the figure, it can be observed that with increase in metal work-function value, the transfer characteristic curve is shifting its position with lower value of work-function, although the On current is high but the Off current is not up to the level. Apart from this, with increase in metal work-function from 4.8eV, the On current also getting lower values as shown in Fig. 6. The exact analysis of On and Off current can be done through Fig. 7, where the transfer characteristics are in logarithmic form. A higher value of  $I_{On}/I_{Off}$  ratio is achieved when grater value of work-function is taken into consideration.

Similar investigation is carried out for pMOS in order to understand the effect of metal work-function value on device performances. The gate voltage for this case is taken as -1V with a variation in metal work function from 4.2eV to 5.1eV. The result thus obtained is illustrated in Fig. 8 with a drain bias of 0.5V. Inorder to get a clear insight, the transfer characteristic is represented in logarithmic scale and the  $I_{On}/I_{Off}$  ratio is well observed. From the Fig. 9, the  $I_{On}$  and  $I_{Off}$  current with different work-function value is illustrated and the improved switching ratio is observed for higher work-function value.

The work is further extended to match the threshold voltage for both the nMOS and pMOS in order to realize inverter circuit. The threshold voltage matching is done by matching the threshold voltage by calibrating the metal work-function and device channel length. The threshold voltage is calculated for different gate length matches at a point where nMOS is 60nm where as pMOS is 47 nm. The work-function value for nMOS is 4.3 eV and pMOS is 4.461eV. The threshold voltage at this point are almost

similar that leads to an efficient CMOS inverter design. For all these cases, the On current and Off current also kept almost same.

**Table 2**

**Threshold voltage for different gate length and metal work-function (for Junctionless pMOS)**

S.No	Channel Length	Work Function	Drain Voltage	Gate Voltage	Threshold Voltage
1	60	4.704	0.5v	-1.0v	-0.550091
2	30	4.704	0.5v	-1.0v	-0.099271
3	50	4.4	0.05v	-1.0v	-0.549723
4	50	4.4	1.0v	-1.0v	-0.099673
5	47	4.461	0.5v	-1.0v	-0.149724

**Table 3**

**Threshold voltage for different gate length and metal work-function (for Junctionless nMOS)**

S.No	Channel Length	Work Function	Drain Voltage	Gate Voltage	Threshold Voltage
1	60	4.46	0.5v	1.0v	0.25054
2	60	4.3	0.05	1.0v	0.10086
3	60	4.3	1.0v	1.0v	0.150277
4	60	4.3	1.5v	1.0v	0.15047
5	60	4.3	0.5	1.0v	0.15023 (close to 0.14972- PMOS)

## Conclusion

Selection of gate metal with proper work-function is a state of the art engineering technique to produce highly efficient semiconductor devices. In this paper, we have investigated the effect of gate metal work function on device performance. The gate metal work function is varied from 4.2eV to 5.1 eV and the

electrostatic potential thus obtained is investigated extensively. The shape of the potential curve due to different metal work-function values and their effect on drain current and threshold voltage also studied. The observation thus concludes that in order to design a state of the art semiconductor device, metal work-function plays a vital role and by tuning the values, threshold voltage can be matched.

## **Declarations**

## **Acknowledgement**

Not Applicable

## **Funding statement**

There is no funding for this research work.

## **Conflict of Interest**

The authors declare that they have no conflict of interest.

## **Author contributions**

Manoj Angara- Simulation, Methodology and Writing original draft Preparation

Biswajit Jena- Conceptualization, Investigation

S. Rooban- Reviewing and editing

## **Availability of data and material**

The authors confirm that the data given in this study are available within the article or in below mentioned references.

## **Compliance with ethical standards**

This article does not contain any studies with human participants or animals performed by any of the authors.

## **Consent to participate**

All authors freely agreed and gave their consent to participate on this work.

## Consent for Publication

All authors freely agreed and gave their consent for the publication of this paper.

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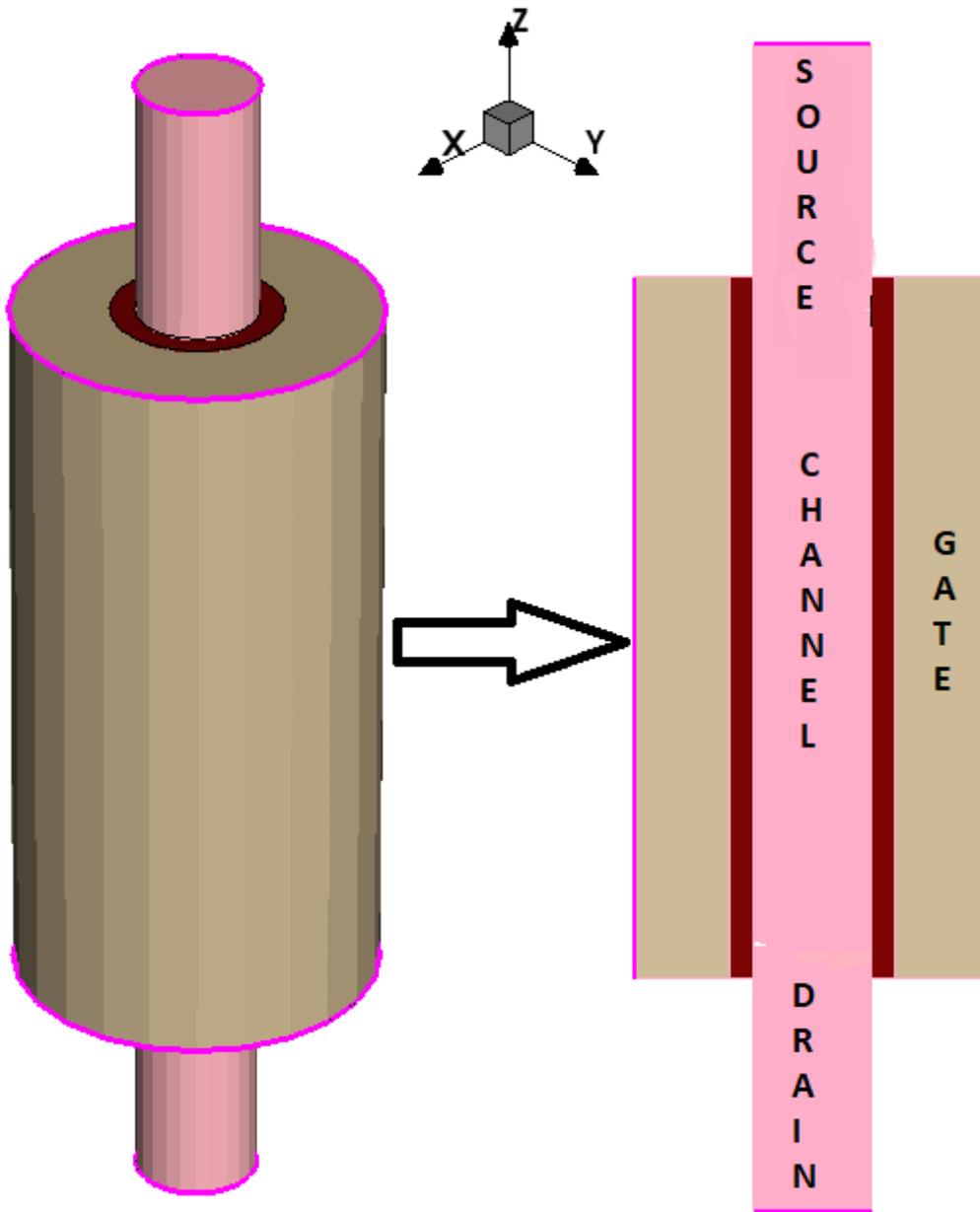
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## Figures



**Figure 1**

(a) Three dimensional (b) Cut sectional view of proposed JL-Nanowire GAA MOSFET structure

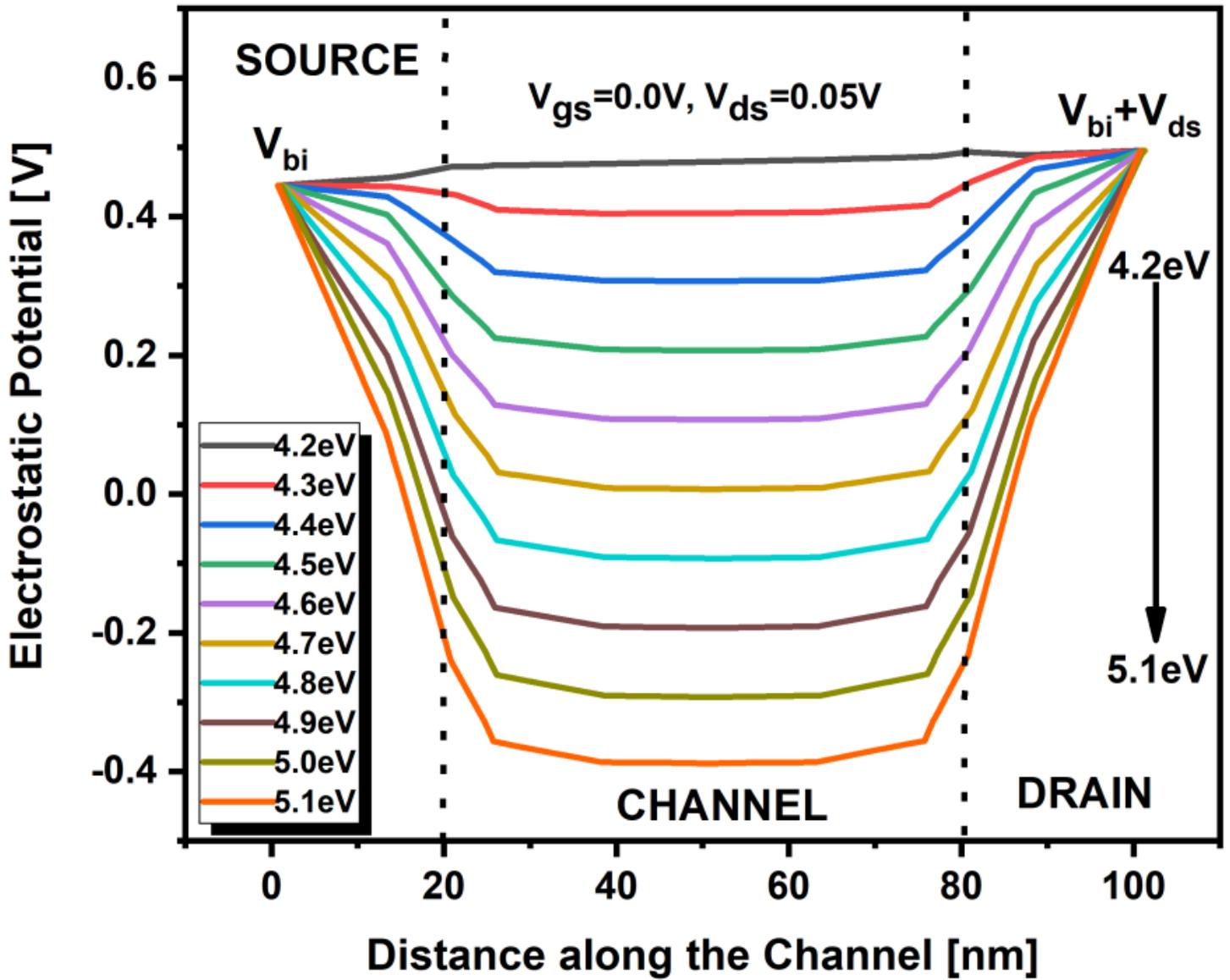


Figure 2

Electrostatic potential distribution in JL-GAA MOSFET (n-type) with zero gate voltage and small drain voltage (50 mV).

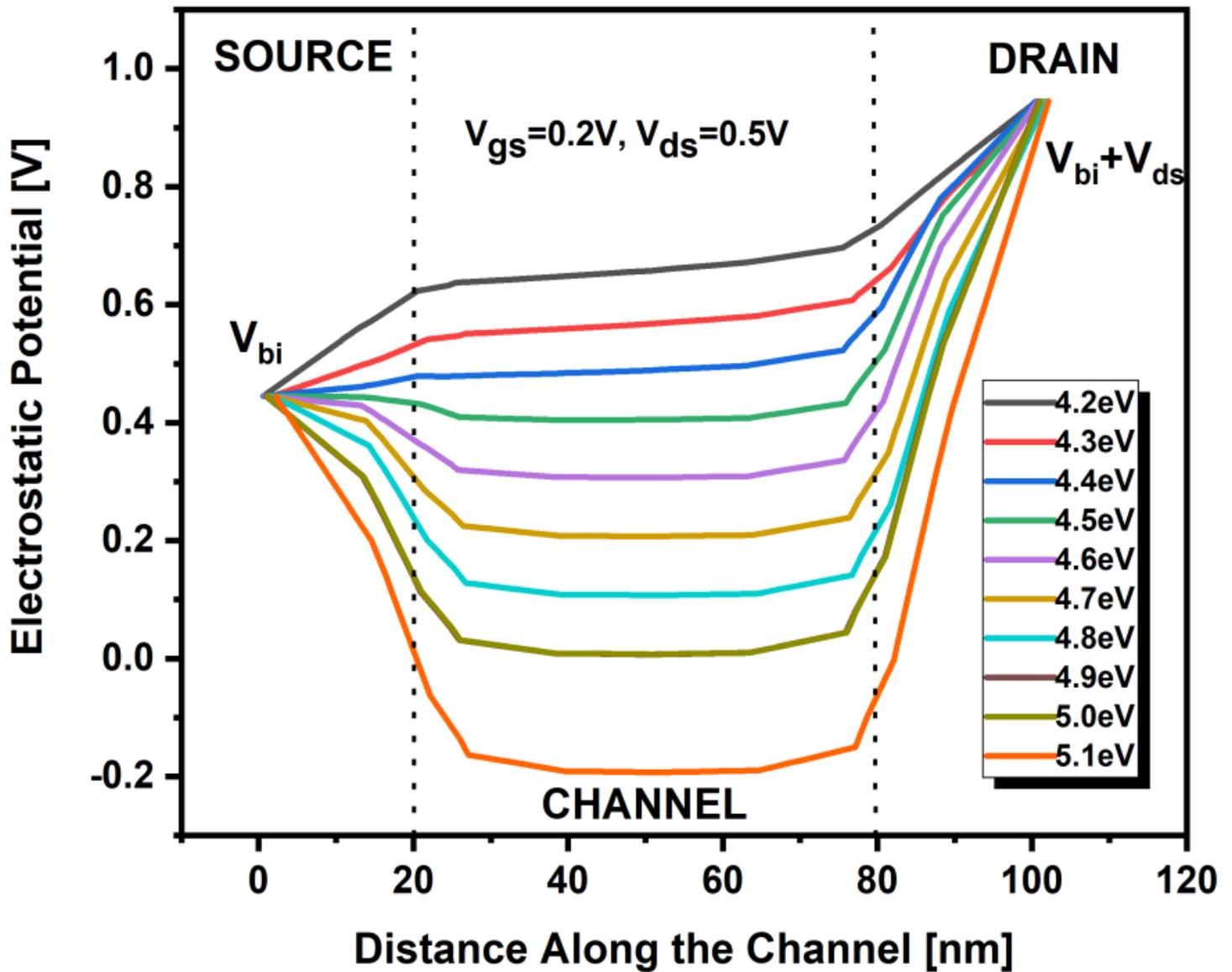


Figure 3

Electrostatic potential distribution in JL-GAA MOSFET (n-type) with small gate voltage (0.2V) and large drain voltage (0.5 V).

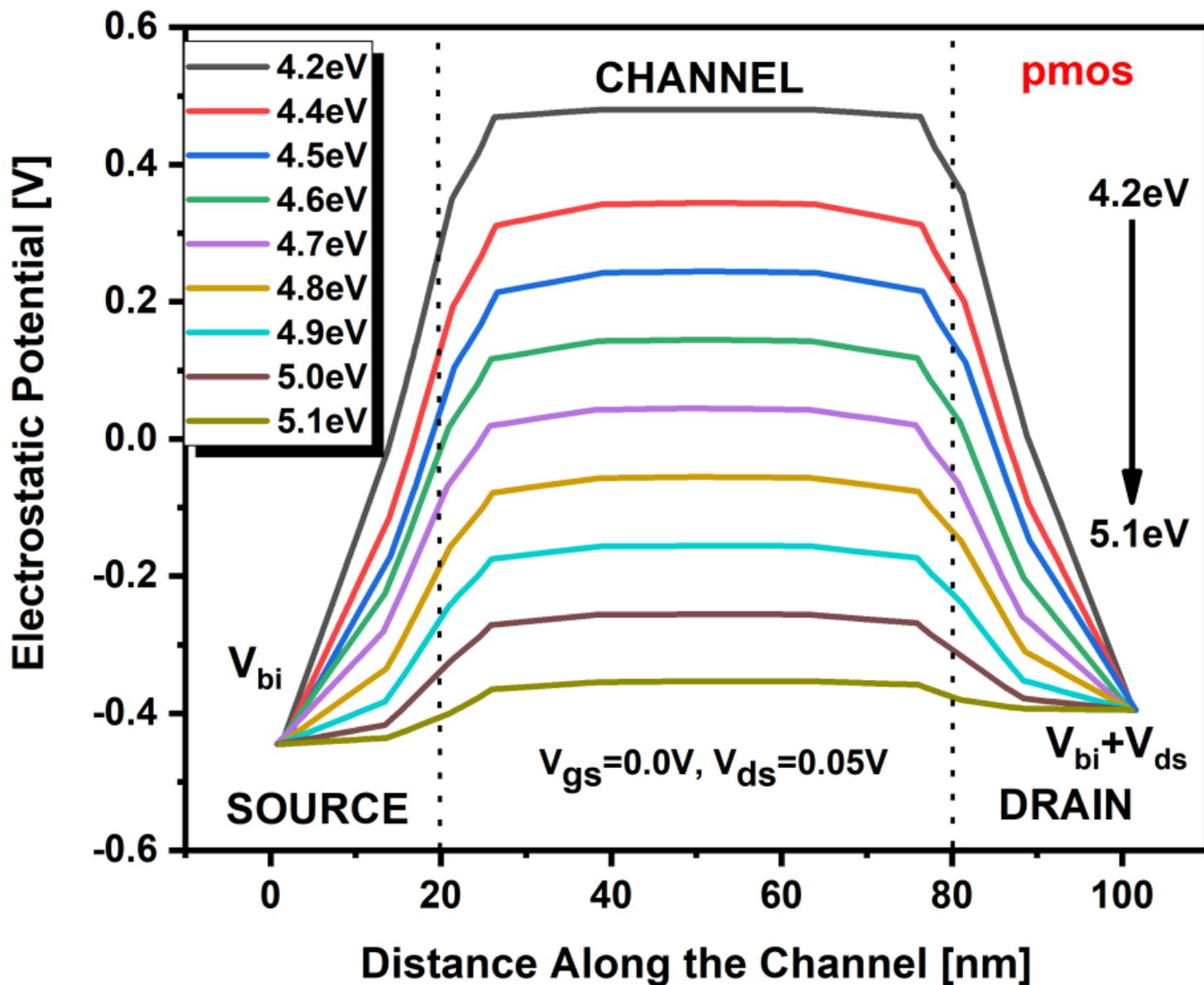


Figure 4

Electrostatic potential distribution in JL-GAA MOSFET (p-type) with zero gate voltage (0V) and small drain voltage (0.05 V).

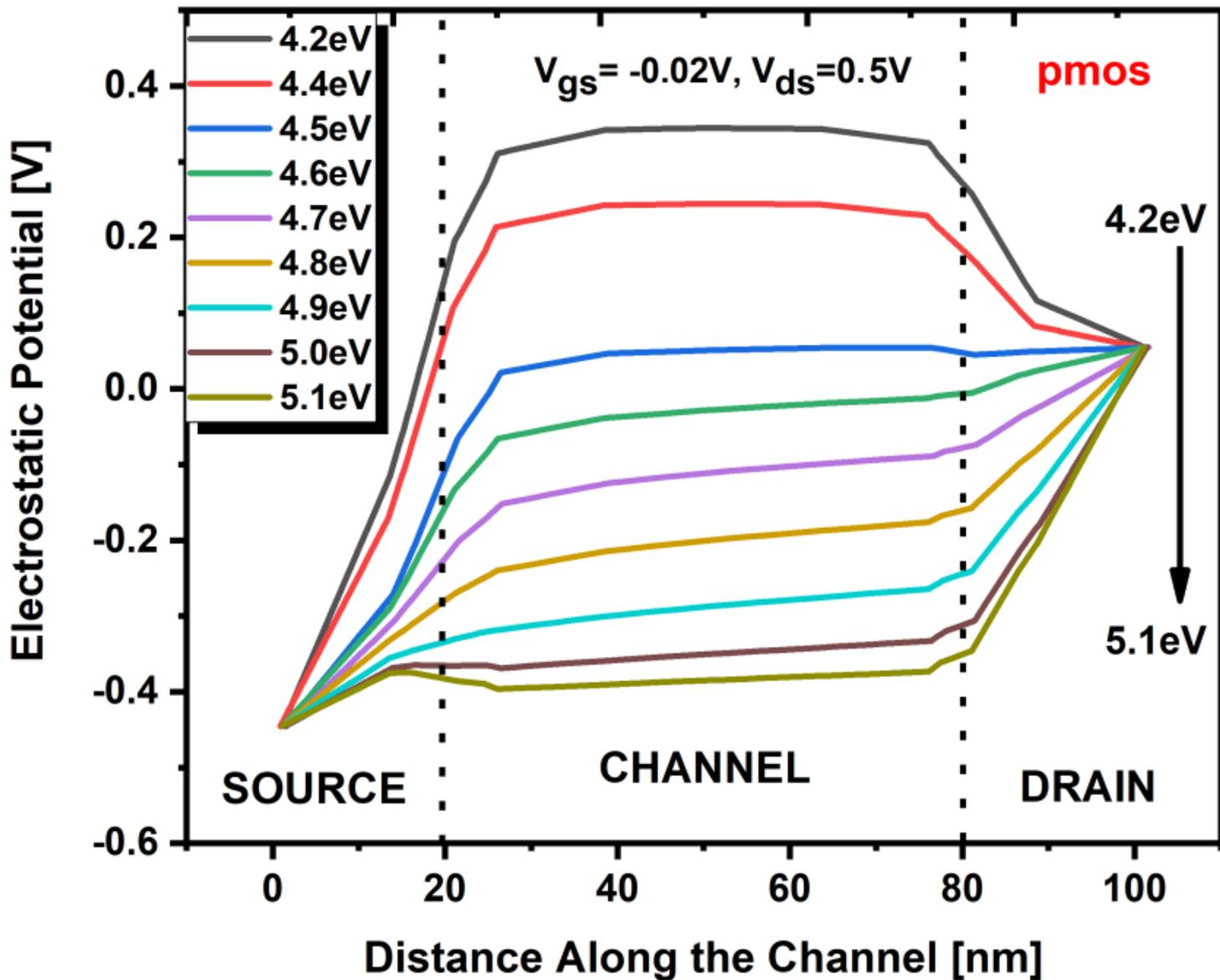


Figure 5

Electrostatic potential distribution in JL-GAA MOSFET (p-type) with small gate voltage (-0.2V) and large drain voltage (0.5 V).

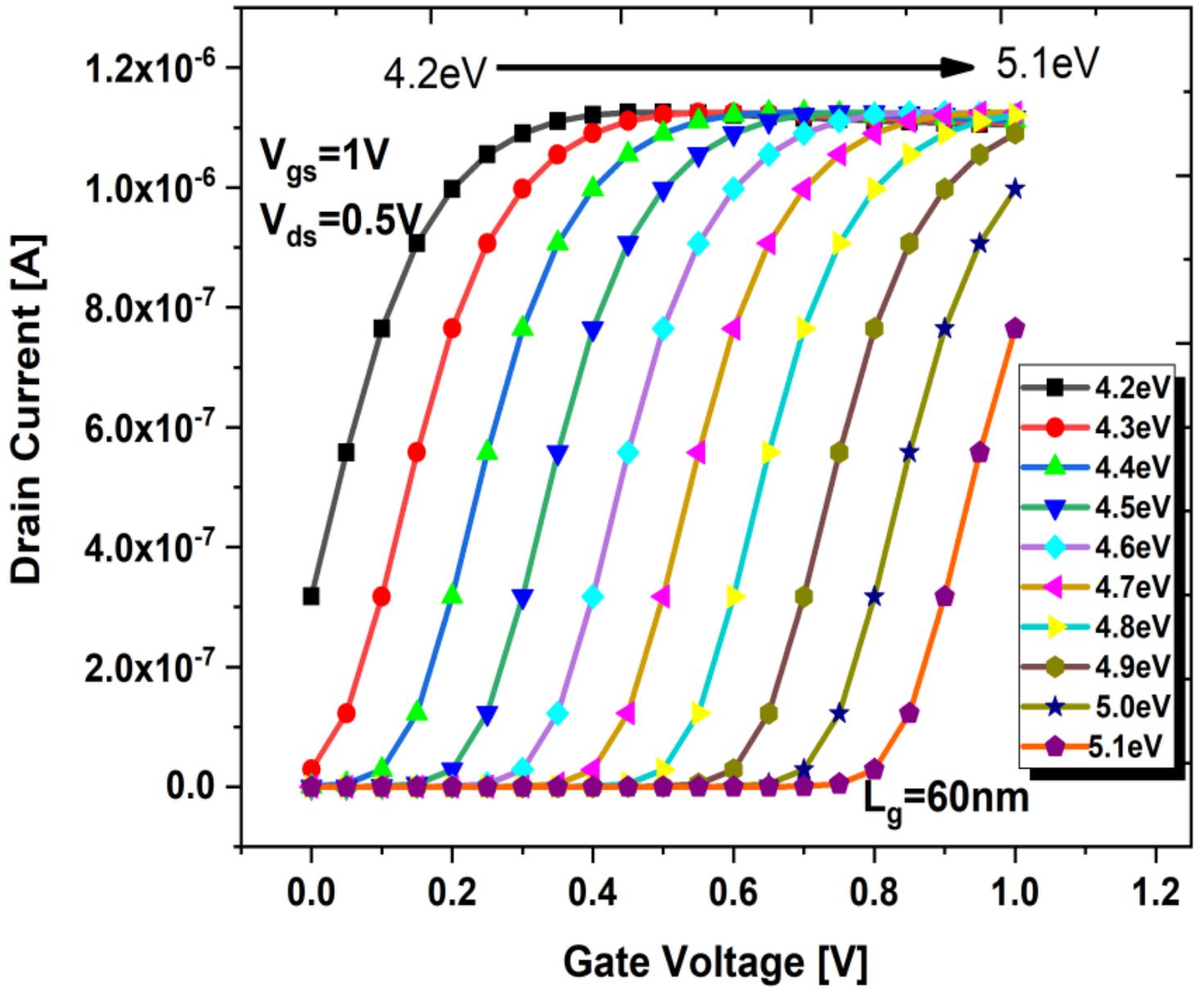


Figure 6

Transfer characteristics of JL-GAA MOSFET (n-type) with a gate voltage of 1V and drain voltage of 0.5V for different metal work-function value.

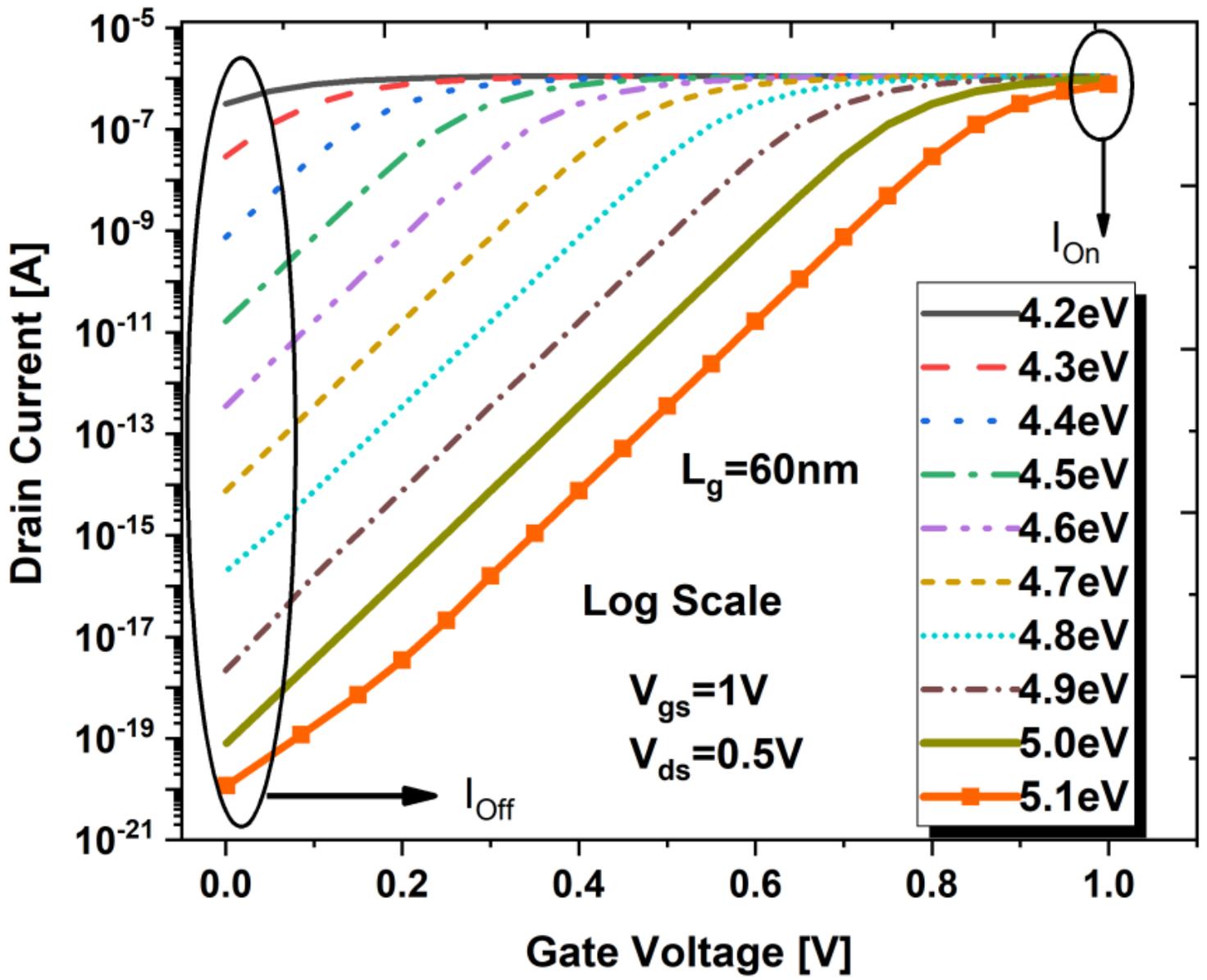


Figure 7

Transfer characteristics of JL-GAA MOSFET (n-type) with a gate voltage of 1V and drain bias of 0.5V for different metal work-function value in logarithmic scale.

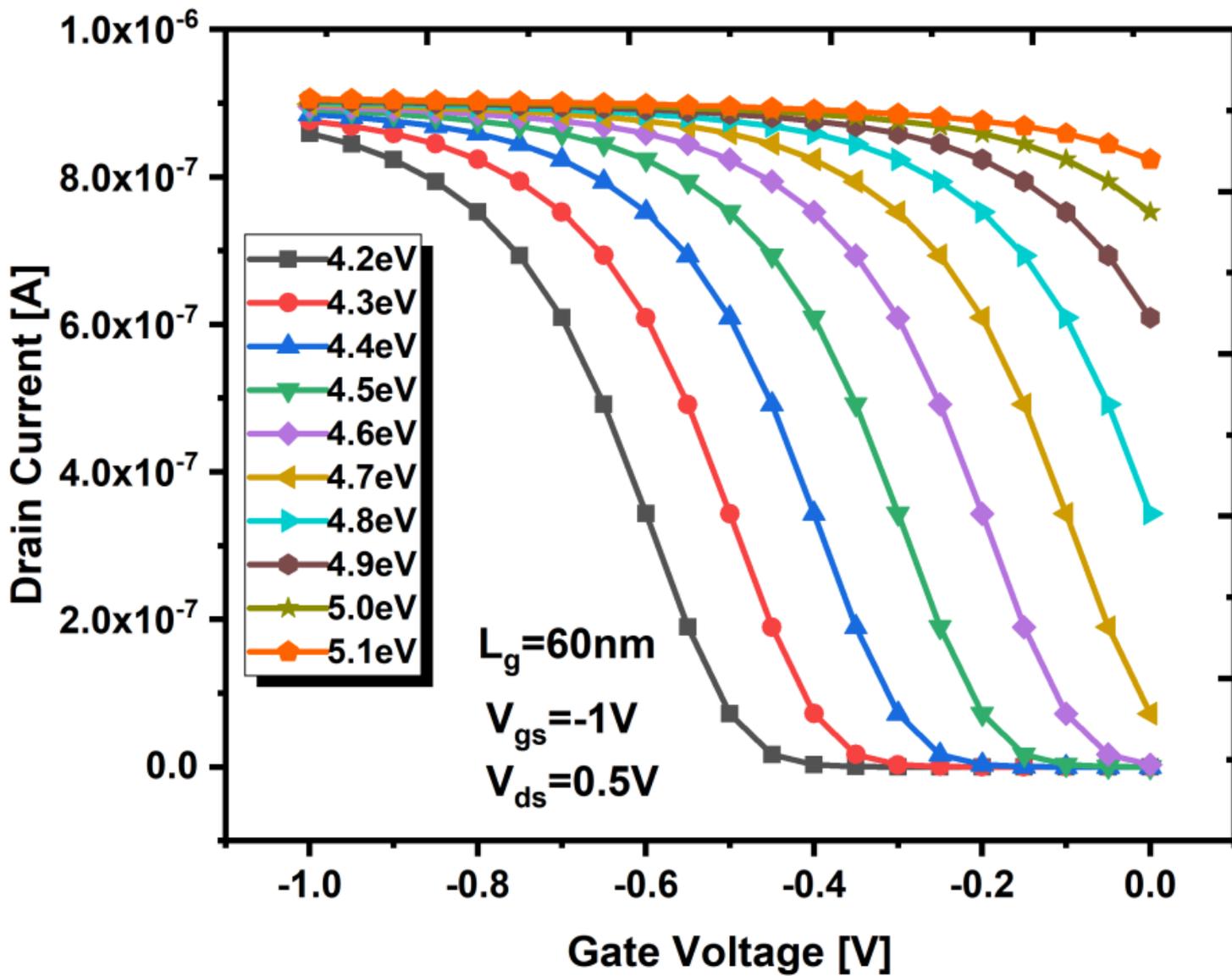


Figure 8

Transfer characteristics of JL-GAA MOSFET (p-type) with a gate voltage of -1V and drain bias of 0.5V for different metal work-function value.

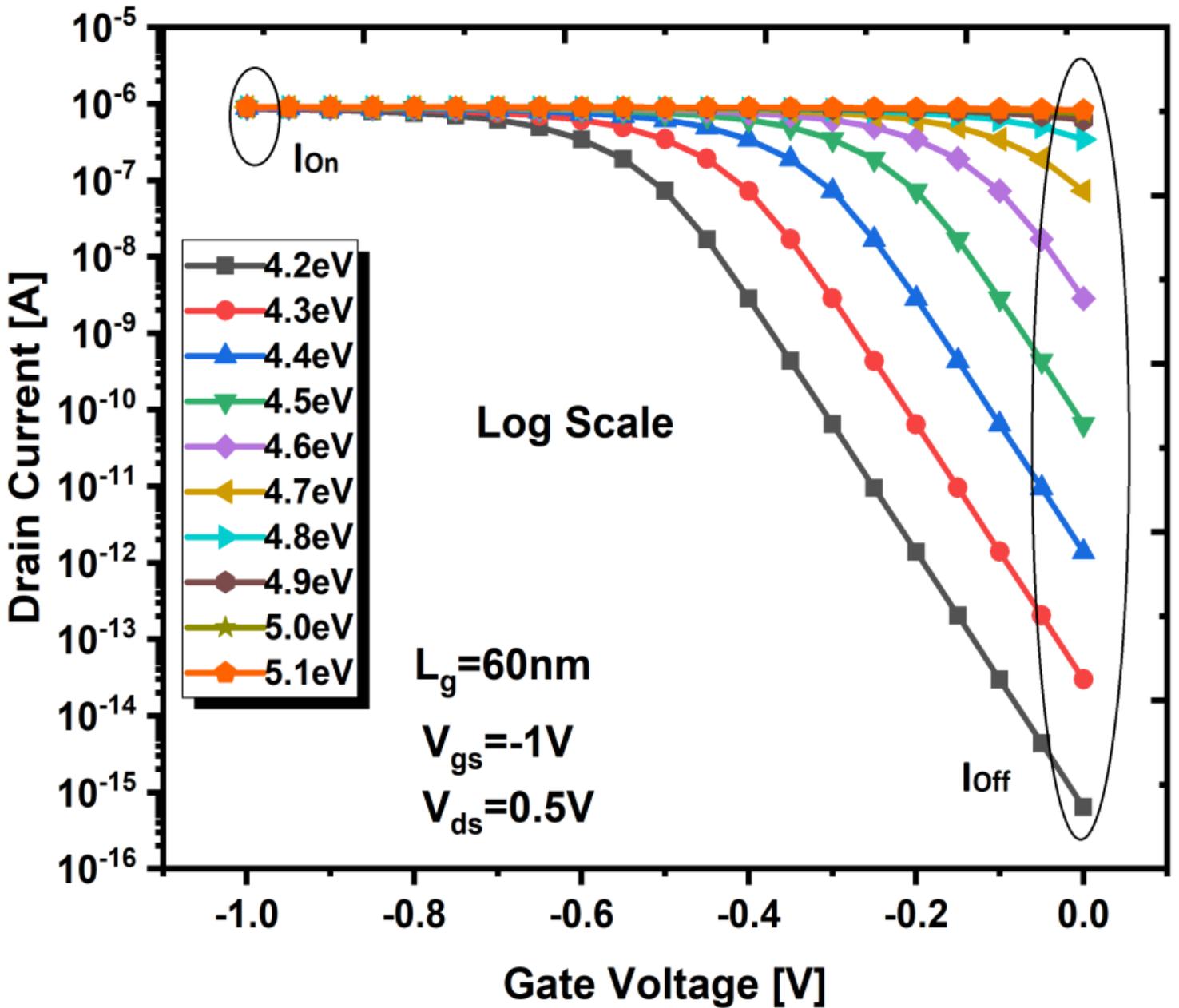


Figure 9

Transfer characteristics of JL-GAA MOSFET (p-type) with a gate voltage of -1V and drain bias of 0.5V for different metal work-function value in logarithmic scale.