Design And Simulation of An Electro-Optic Even Parity Bit Error Detection System

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Research Article

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Design and Simulation of an Electro-optic Even Parity Bit Error Detection System

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Abstract: In the present day, optical communication technology is proving to be one of the potential replacements to the current electronic-based systems due to its much higher data transmission rate with low loss and electromagnetic interference. This paper designed and simulated our proposed circuit of a digital photonic even parity bit error detection system that is widely employed for the long-range digital signal transmission. Silicon photonic micro-ring resonators are used as their core component. Each of the rings is configured to operate as a digital logic XOR mode by taking advantage of the silicon waveguide's resonance shifting properties. Dynamic response characterization was carried out by simulating the proposed circuits at the data rate of 1-Gbps, with the data sampling rate of 1.6-THz. A clear timing waveform was generated to confirm that the proposed circuit operates as the parity bit error detection system.

1. Introduction

In general, every current electronic circuit being distributed and used by the consumer's electronic devices, such as PCs, digital televisions, smartphones, and many more. Such electrical circuits use electrical signals to beas the medium of communication between circuit components. They are delivered via copper-type interconnects either along with the circuit board or via electrical wires. It is also generally known that electrical wires are prone to different transmission losses, either via heat emission or material compounds themselves. Therefore, this is not a feasible routeto transmit digital information at a very high speed as such devices have the above-mentionedlimitations. The alternatives to the current electrical interconnect are under-research in recent years. Amongst the many innovative ideas, optical networks emerge as one of the most promising digital data transmission media as it utilizes optical characteristics to transmit very high data [1, 2]. Photonic integrated circuit (PIC) uses this optical medium as its means of digital interconnects between circuit elements and maintaining the current electronic designs as much as possible. These circuit elements are often photonic devices that act as some sort of switch, which replaces the electronic transistors required for logical switching in the current electronic circuits. PIC is also often built with silicon materials as its base in order for it to be manufactured efficiently with the current CMOS fabrication technology [3, 4].

In electronics, there are generally two categories of digital electronic circuits: i) combinational and ii) sequential logic circuits. Combinational logic circuits generate output instantaneously according to their inputs, with the absence of any kinds of feedback loops. Inside combinational logic circuits can also be further categorized into arithmetic and logical functions, data transmission, and code converters. A bit error detection circuits are part of the combinational logic circuit family, which consists of a pair of parity bit generator and parity bit checker circuits. Its parity bit generator generates a single bit defining the number of logical "1"'s in the data transmission lines at that specific instance and transfers them together with the data lines. At the receiving end, the parity bit checker combines both data as well as a parity bit to generate if the received bits are correctly received or if it has been tempered. Plenty of research outputs have been made regarding this parity bit error detection circuit, including deep analysis on the magnitude errors caused by the circuits [5-7].

The rapid research development of silicon photonics saw it being used in several forms of digital logic circuit designs. Logic gates utilizing single-mode Fabry-Perot Laser Diode (FP-LD) have been proposed [8, 9]. However, silicon micro-ring resonators are instead being used due to FP-LD comes with the drawback that the presented designs are not viable to be manufactured at the microscale CMOS fabrication process. A single design of silicon micro-ring resonators can be configured to produce several types of digital logic gates such as AND, NAND, OR, and NOR gates [10]. Alternative designs for directed OR/NOR and AND/NAND logic circuits have also been proposed [11], with the resonator implementation into many other forms of digital circuits such as tuneable digital D flip-flop [12-14], half adder [15], digital encoders and bit magnitude comparators [16, 17]. Wavelength division multiplexing (WDM) systems have also been shown to be designed with micro-ring resonators [18, 19].

This paper presents the utilization of a designed silicon micro-ring resonator, configured and set up in such a way that it operates as a digital photonic even parity bit error detection system. The ring resonator uses its silicon ring waveguide electro-optic properties. Its PIN diode design reacts to the change in electrical signals being fed into it, with tuning to operate as digital logic XOR mode. This work also shows the circuit behavior in the time

domain and injected predetermined digital information signals at the data rate of 1-Gbps with timing waveforms as its result for analysis.

2. Design Principle of the Proposed Error Detection Circuit

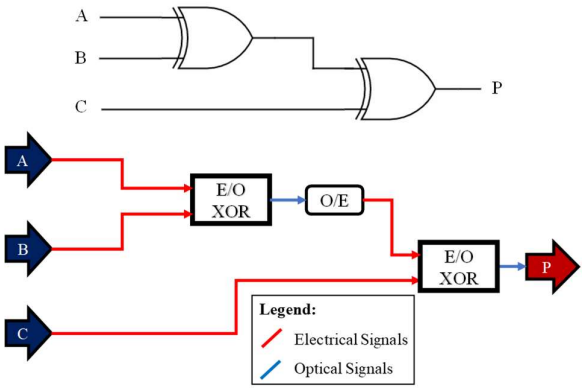

Fig. 1. A logic circuit (on top) and proposed design (on bottom) of the bit generator.

In a 3-bit even parity bit error generator logic circuit, there are two digital logic XOR gates used, where the output of the first one is being fed into the second gate to generate the parity bit. Fig. 1 shows our proposed circuit design, where the two XOR gates are now replaced with two silicon micro-ring resonators operating as digital logic XOR mode. When the input 'A' is at digital logic '**0**', parity bit outputs in accordance to the Inv(A $\oplus$ B) and when the input 'A' is at digital logic '**1**', the parity bit output generates according to A $\oplus$ B. The entire operation of the circuit is as shown in Table 1, when if we observe, the number of '**1**'s in each row is counted as even number, which is in accordance with the name of the circuit even parity bit generator.

Table 1 Even Parity Bit Generator Truth Table.

3-bit Message			Parity Bit
A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

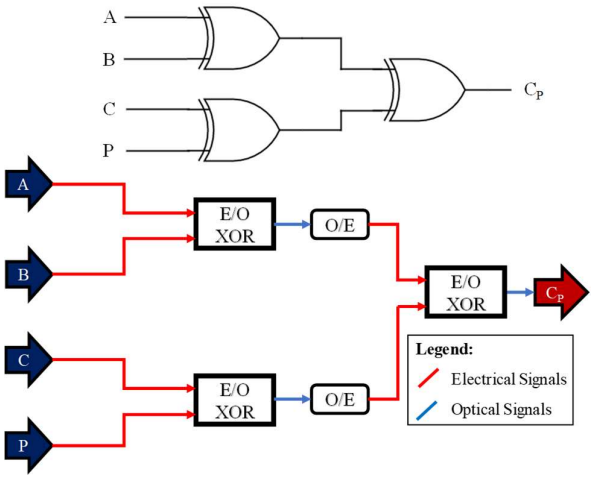

Fig. 2. A logic circuit (on top) and proposed design (on bottom) of the bit checker.

A 3-bit even parity checker has three digital logic XOR gates, where the first two XOR gates output is then fed into the third XOR gate, to generate a parity check (C_P) bit. It is similar to our proposed bit generator, and we replaced the digital logic gates with silicon micro-ring resonators operating as digital logic XOR mode. The equation representing the operation of the bit checker output is $C_P = (A \oplus B) \oplus (C \oplus P)$ and the entire operation bit by bit for the circuit is as shown in Table 2, where C_P is only at digital logic state '**1**' when the total number of logic state '**1**'s for the received four bits is an odd number, indicating that the received information contains an error.

Table 2 Even Parity Bit Checker Truth Table.

4-bits Message Received				Parity Check
A	B	C	P	CP
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Element labeled O/E can be seen in both Fig. 1 and Fig. 2, which stands for optical to the electrical converter. It converts an optical output power of 5-dBm to the electrical signal of 0.2-V linearly, performed by pairing the PIN photodetector serially with the electrical attenuator. The PIN photodetector converts the received optical signal and outputs the electrical signal while the electrical attenuator drops the voltage down to 0.2-V, which is the necessary voltage for one of the inputs of the electro-optic XOR gate.

3. Design Architecture of the Silicon Micro-Ring Resonator

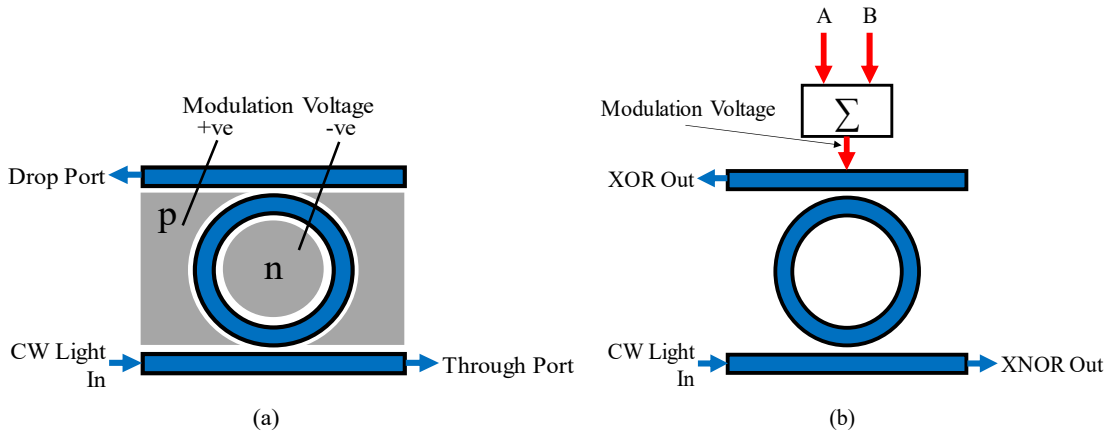

Fig. 3. (a) Architecture of silicon micro-ring resonator. (b) Schematic setup for XOR and XNOR mode operation.

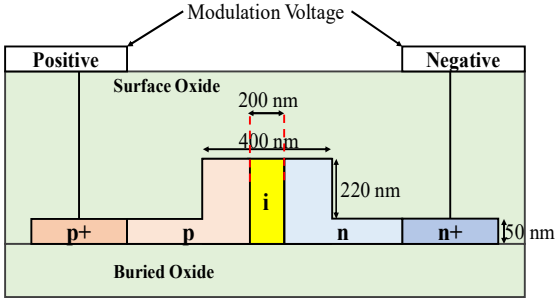

Fig. 4. Cross-section view of the PIN-diode ring waveguide.

The silicon ring waveguide used is as shown in Fig. 3(a), while its inside is built in the structure of PIN-diode with its cross-section as shown in Fig. 4 [20]. The rib-type ring waveguide is formed on top of a buried oxide of SiO_2 with its thickness of 1-µm. The waveguide's core layer is 440-nm in width and 220-nm in height, and its slab thickness is defined as 50-nm. According to the doping region, the entire waveguide is doped as shown in Fig. 4, with an intrinsic region of 200-nm is kept in the middle for optimal free carrier diffusion to occur. The regions of *p* and *n* have the doping concentration of cm^{-3} per 1-µm, while p+ region is doped at cm^{-3} per 1-µm and n+ region is doped at cm^{-3} per 1-µm. Electrical contacts are placed on top of the slabs, connected to the outside electrical modulation voltage source, where p+ region is connected to the positive terminal, and the n+ region is connected to the negative terminal forward-biased free carrier injection to occur. The entire waveguide is then covered with a surface oxide of 1-µm in thickness, leaving the electrical positive and negative terminals on top.

The ring itself, as shown in Fig. 3(a), is constructed with a ring length of 31.8-µm, with its initial Finite-Difference Time-Domain simulated effective index of 2.77, its group index of 3.961, its coupling coefficient of 0.5 as well as its propagation (FDTD) loss of 5.93-dB/cm. The change in the effective index is also found from the FDTD simulation, which is shown in Fig. 5, where no significant change in the effective index is observed when the voltage applied is within the range of 0-V up to 0.7-V, but a linear change in the effective index can be seen when the voltage is 0.8-V up to 1.4-V [21]. This can then be effectively used to operate the ring resonator as digital logic XOR mode by selecting specified voltage levels.

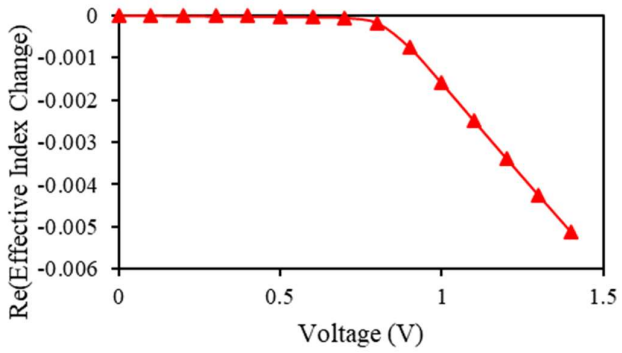

Fig. 5. Change in effective index versus modulation voltage applied to the ring.

Fig. 3(b) shows our setup for the ring resonator operating as digital logic XOR mode, where an electrical adder is used to add the voltage levels of the two electrical signals and finally fed it into the ring resonator. Based on our analysis, the designed ring resonator can operate as digital logic XOR mode by using the voltage levels of 0.9-V, 1.1-V, and 1.3-V, which in turn gives the resonance spectra at the drop port as shown in Fig. 6. We selected the working wavelength for the entire operation to be 1550.3-nm, which is the resonance wavelength when the voltage applied to the ring is 1.1-V. When the voltage applied is 0.9-V, at working wavelength, the optical output power observed is -11.7-dB (assumed logic state '*0*'). When the voltage is increased to 1.1-V, the optical power observed at the drop port is now -2.15-dB (assumed logic state '*1*'), and when the voltage applied is further increased to 1.3-V, the shift in resonance causes the optical power output at working wavelength to be -11.2-dB (assumed logic state '0'). Referring to Fig. 3(b), by applying a constant voltage source of 0.9-V, together with the electrical inputs A and B, each of which has the amplitude of 0.2-V, we can achieve the XOR mode operation using only a single silicon micro-ring resonator, which is shown by the truth table in Table 3.

Table 3. Truth Table of micro-ring resonator voltage selection for XOR mode operation.

	Inputs			**Output**
Constant Voltage	**A**	**B**	**Total Voltage**	**At 1550.3nm**
(V)	**(0/1) (V)**	**(0/1) (V)**	**(V)**	**(0/1) (V)**
0.9	'0' (0V)	'0' (0V)	0.9	'0' (-11.7dBm)
0.9	'0' (0V)	'1' (0.2V)	1.1	'1' (-2.15dBm)
0.9	'1' (0.2V)	'0' (0V)	1.1	'1' (-2.15dBm)
0.9	'1' (0.2V)	'1' (0.2V)	1.3	'0' (-11.2dBm)

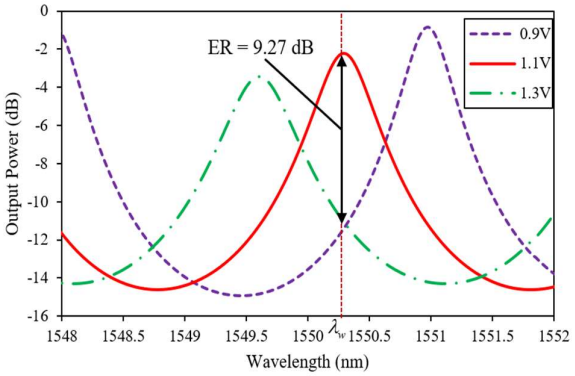

Fig. 6. Resonance spectra at the drop port of the ring resonator at specific modulation voltage.

4. Dynamic Response Test

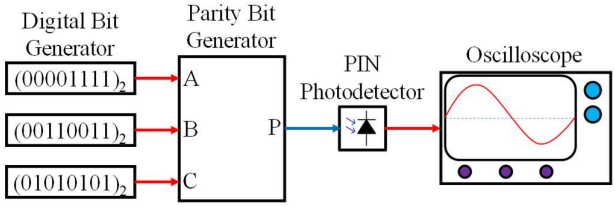

Fig. 7. Simulation block setup for the bit generator.

The proposed circuits were then tested in one of the commercially available photonic simulation software, Lumerical software. The ring resonators are injected with a single wavelength light source of 1550.3-nm with an optical power of 5-dBm. Three digital bit generators are used to generate predetermined bit information with the amplitude of 0.2-V, where the input A received the repeating $(00001111)_2$, while input B received a repeating $(00110011)_2$ and finally input C is injected with repeating $(01010101)_2$. A single PIN photodetector is used to convert the optical output signal P to an electrical signal, in which 1-dBm of optical light power is linearly converted into 1-V of the electrical voltage signal. The entire setup for the bit generator circuit simulation is as shown in Fig. 7.

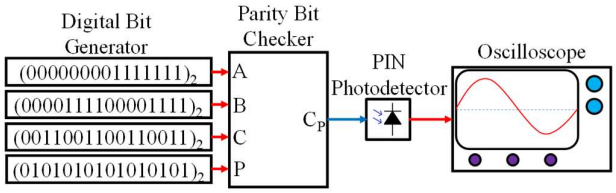

Fig. 8. Simulation block setup for the bit checker.

In the case of bit checker simulation setup, we used four digital bit generators, where input A received a looping information signal of $(0000000011111111)_2$. In contrast, input B received the digital information signal of repeating $(0000111100001111)_2$, with input C is injected with a repeating information signal of $(0011001100110011)_2$. Finally, the parity bit input signal is generated with repeating information of $(0101010101010101)_2$. The entire setup for the bit checker circuit simulation is as shown in Fig. 8.

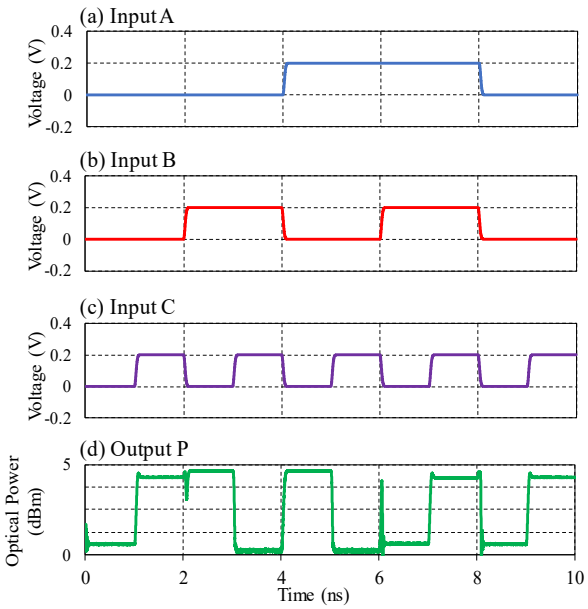

Fig. 9. Timing waveform for the proposed bit generator.

Fig. 9 shows the timing waveforms obtained from simulating the parity bit generator circuit at the data rate of 1-Gbps with the data sampling rate of 1.6-THz and the time frame shown here of 10-ns. The electrical input signals are generated at the amplitude of 0.2-V with its rise and fall time of 0.05-ns. The generated optical parity bit signal has the maximum optical power of 4.7-dBm, with its rise and fall time of 0.06-ns and its response of 0.0106-ns. Based on the output waveform generated, it can be concluded that the proposed circuit design for the even parity bit generator is working according to the bit generator truth table, as shown in Table 1.

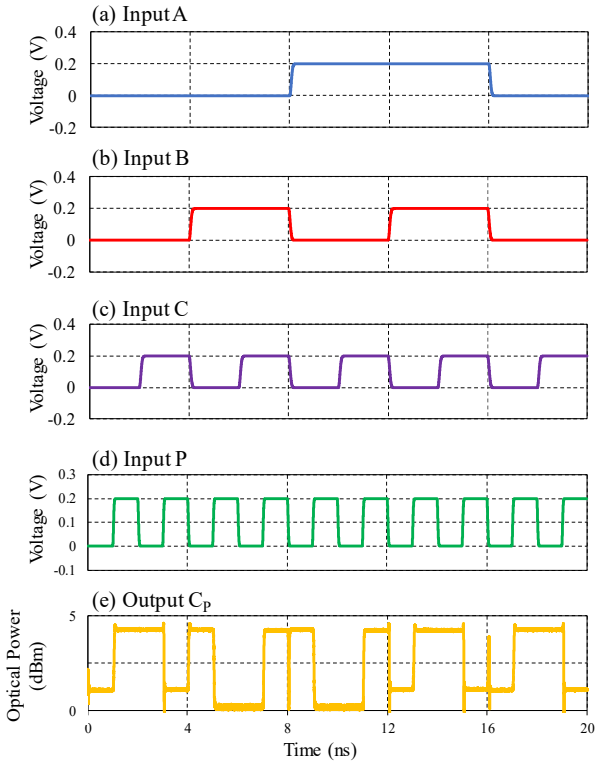

Fig. 10. Timing waveform for the proposed bit checker.

Fig. 10 shows the timing waveforms obtained from simulation of the parity bit generator circuit at the same data rate of 1-Gbps with a different time frame of 20-ns. The electrical input signals are generated with the same amplitude of 0.2-V with its rise and fall time of 0.05-ns. The generated optical parity check signal has the maximum optical power of 4.5-dBm, with its rise and fall time of 0.06-ns and its response of 0.0191-ns. Based on the output waveform generated, it can also be concluded that the proposed circuit design for the even parity bit checker is also working according to its truth table, as shown in Table 2.

5. Conclusion

This paper presented the circuit design of a digital photonic even parity bit generator as well as a checker, which makes up one complete parity bit error detection system. The core device used for the design is the photonic micro-ring resonator built with silicon materials, which in turn exhibits the shift in optical domain resonance via the electro-optic effect. We have designed a customized micro-ring so that the shift in resonance can be incorporated for electro-optic logic gates mode operation, which in this case, is the XOR mode operation. This is proved by analyzing the effective index of the waveguide's core, where we had observed no apparent change in effective index when the voltage applied to the ring is 0-V up to 0.7-V, and an almost linear change in effective index is observed when a voltage of 0.8-V up to 1.4-V is applied. We have also detailed using the designed micro-ring resonator to operate as a digital logic XOR mode by selecting resonance cavities within 1549-nm up to 1552-nm in wavelength, which was generated by voltages of 0.9-V, 1.1-V and 1.3-V applied to the ring. This work also detailed the XOR gates inside the parity bit generator. The checker was replaced with silicon micro-rings operating as an electro-optic XOR mode. Finally, the proposed design was simulated with the predetermined digital information bit sequences at the data rate of 1-Gbps at the time window of a maximum of 20-ns to both generator as well as checker circuits, where clear and accurate optical output signals were observed, following their truth table logic operation.

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Figures

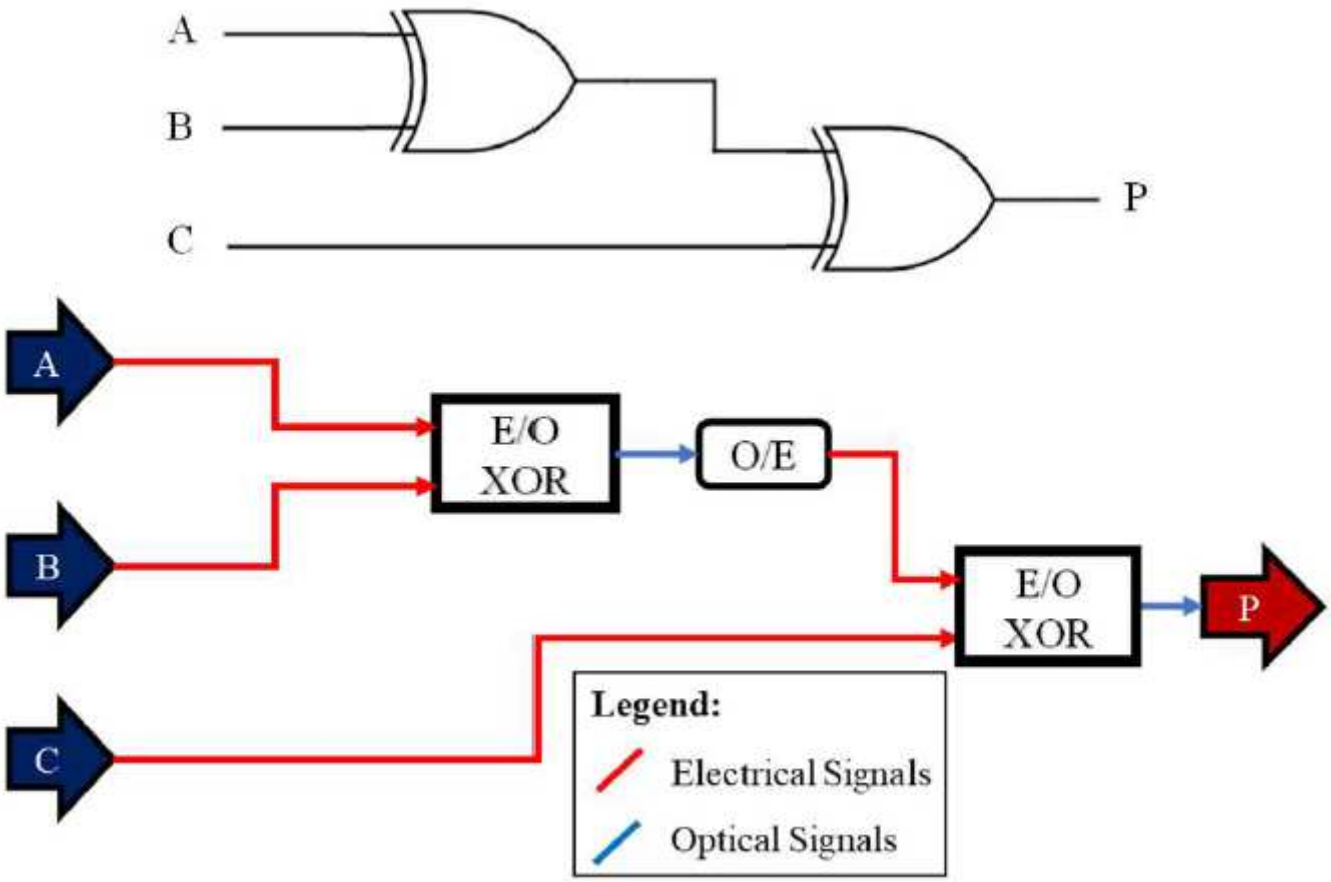

Figure 1

A logic circuit (on top) and proposed design (on bottom) of the bit generator.

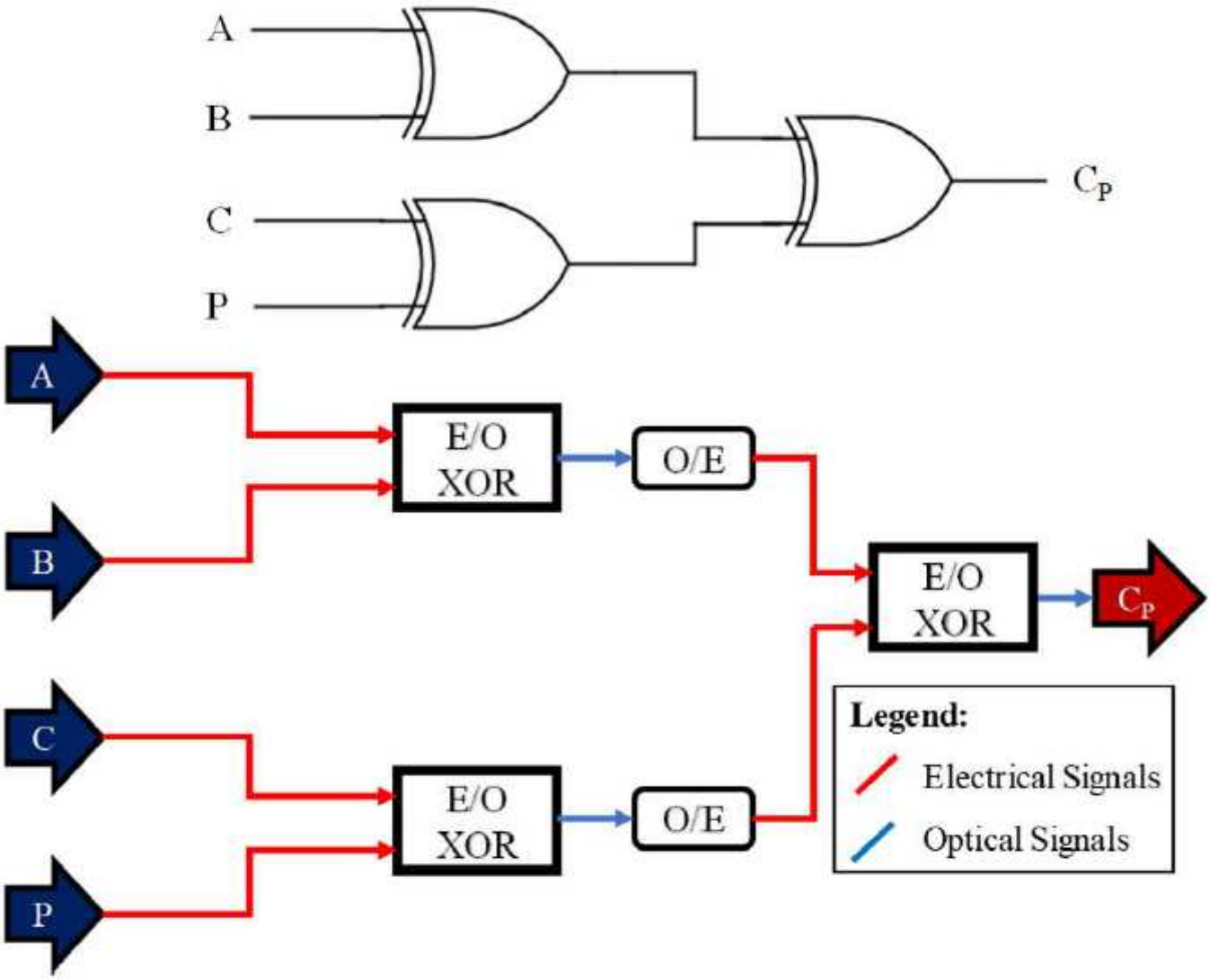

Figure 2

A logic circuit (on top) and proposed design (on bottom) of the bit checker.

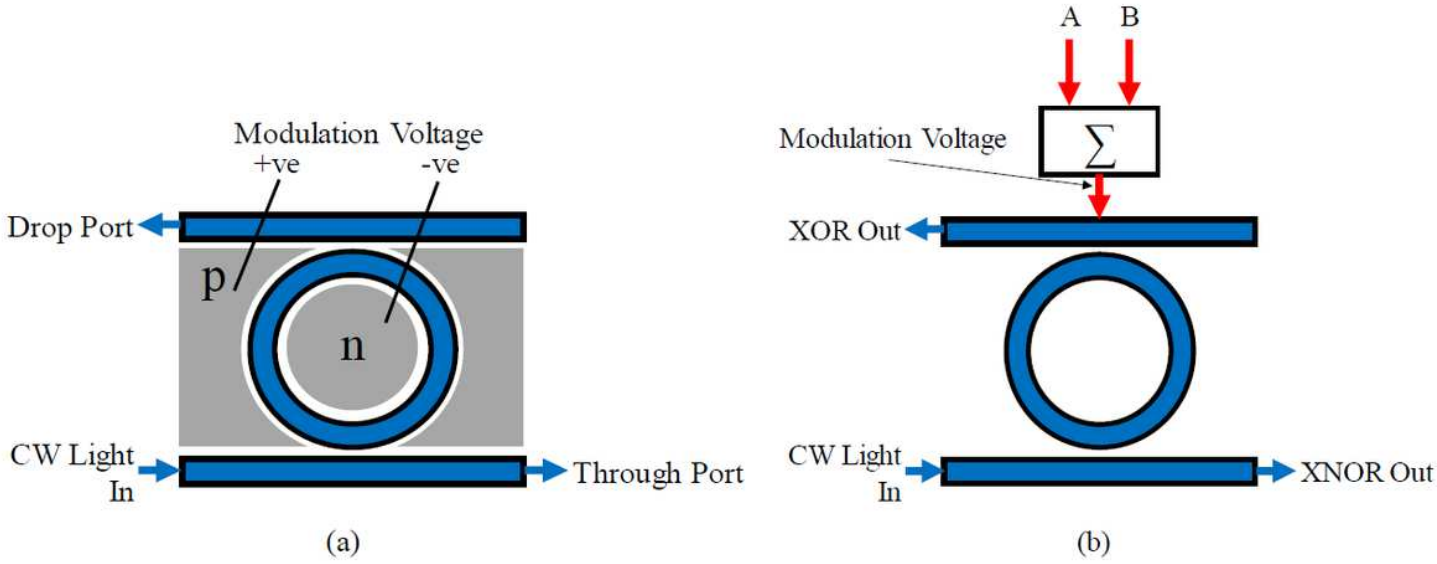

Figure 3

(a) Architecture of silicon micro-ring resonator. (b) Schematic setup for XOR and XNOR mode operation.

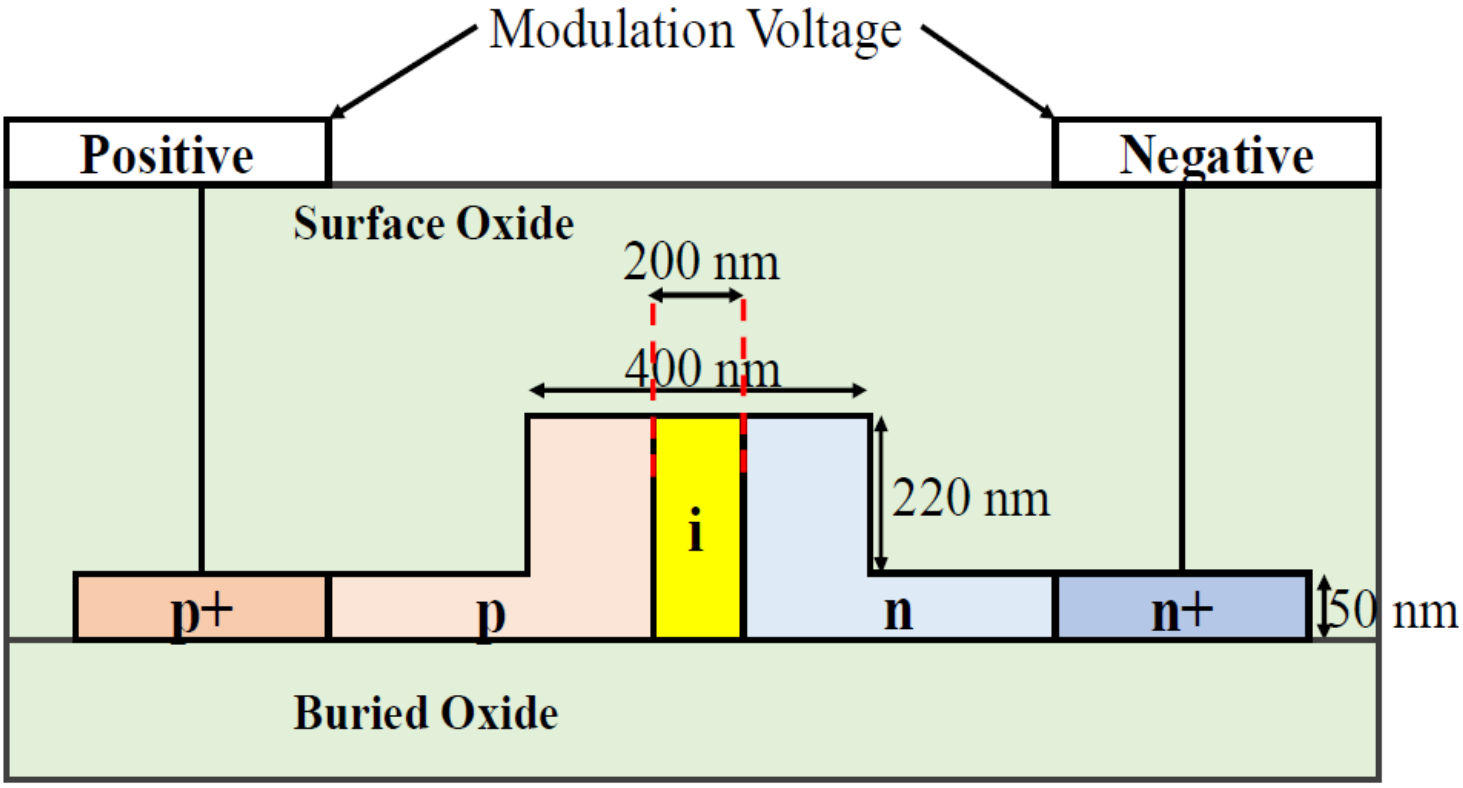

Figure 4

Cross-section view of the PIN-diode ring waveguide.

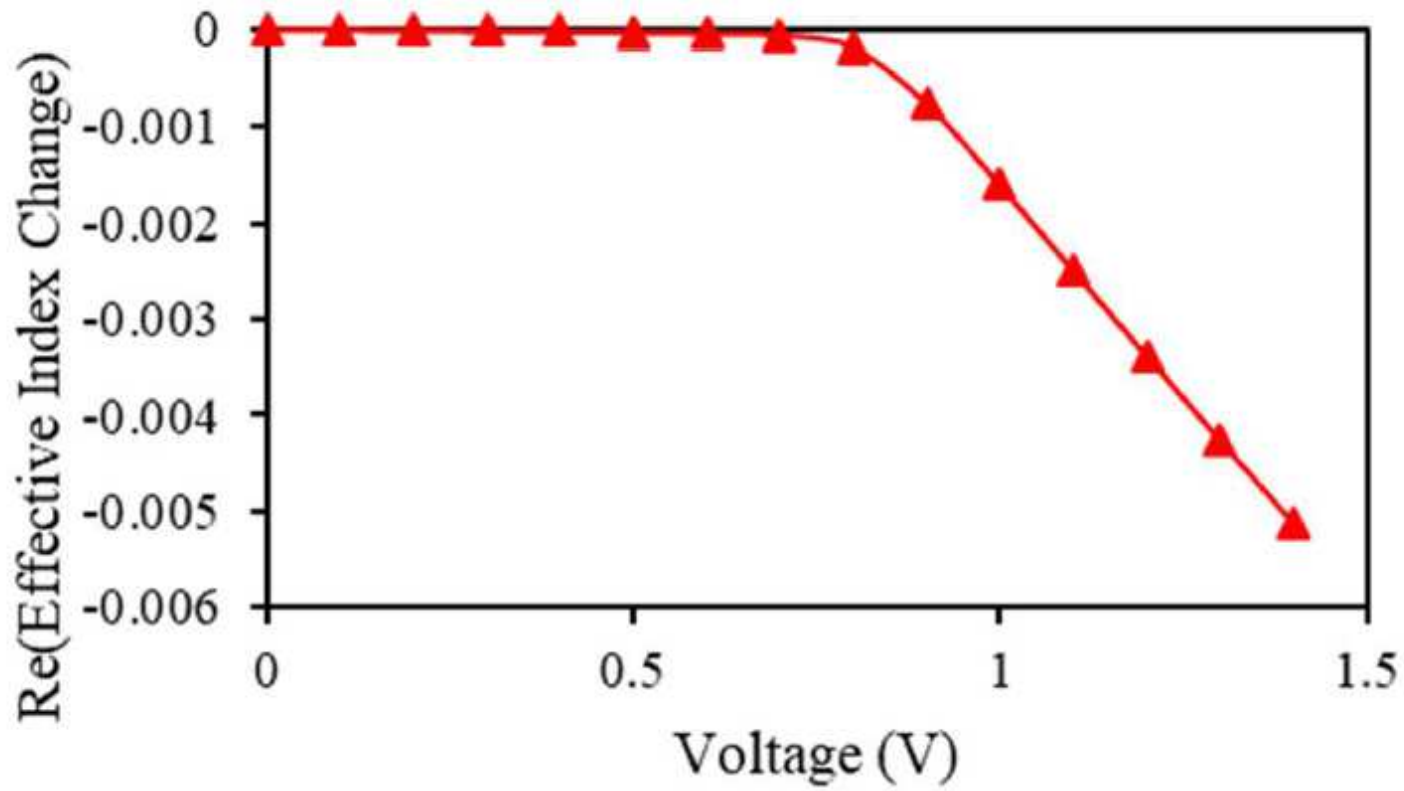

Figure 5

Change in effective index versus modulation voltage applied to the ring.

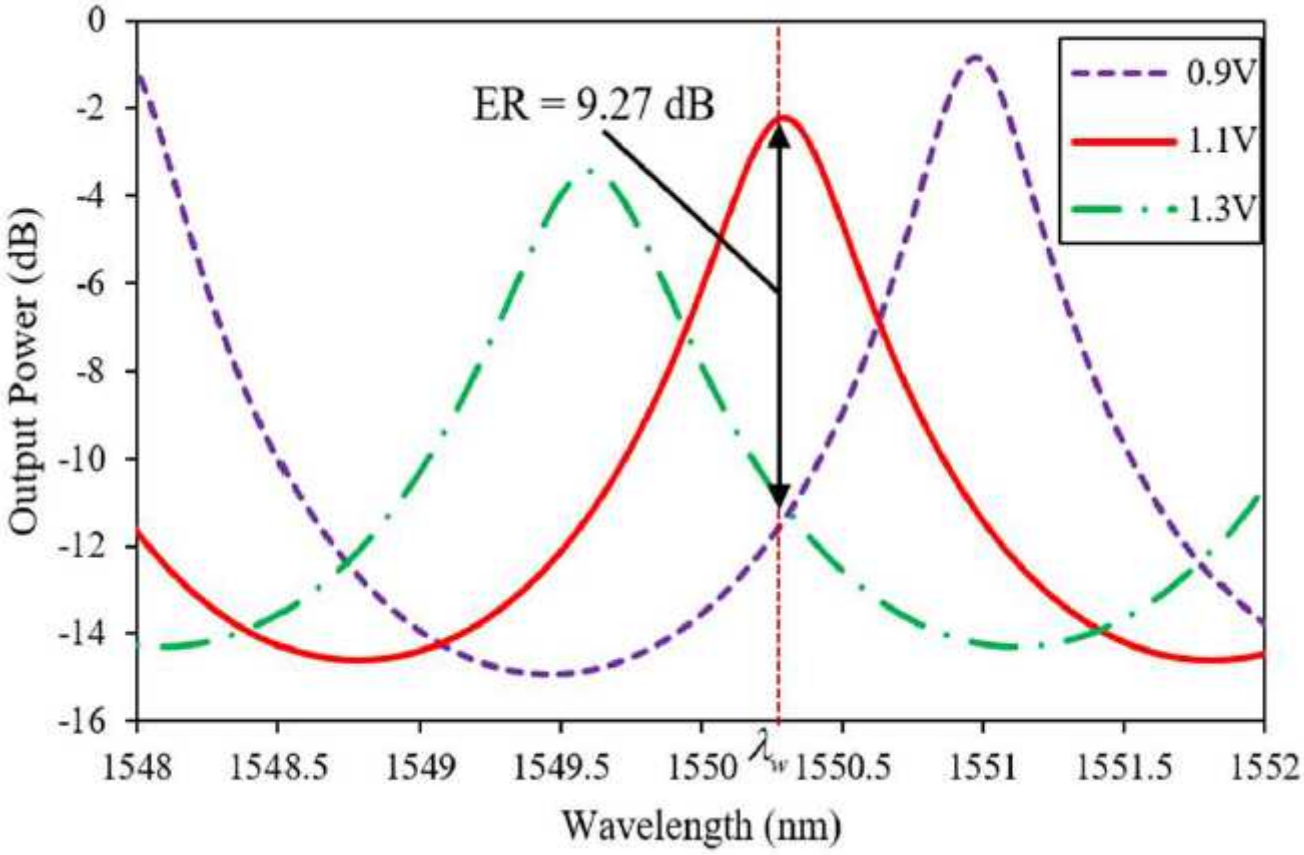

Figure 6

Resonance spectra at the drop port of the ring resonator at specific modulation voltage.

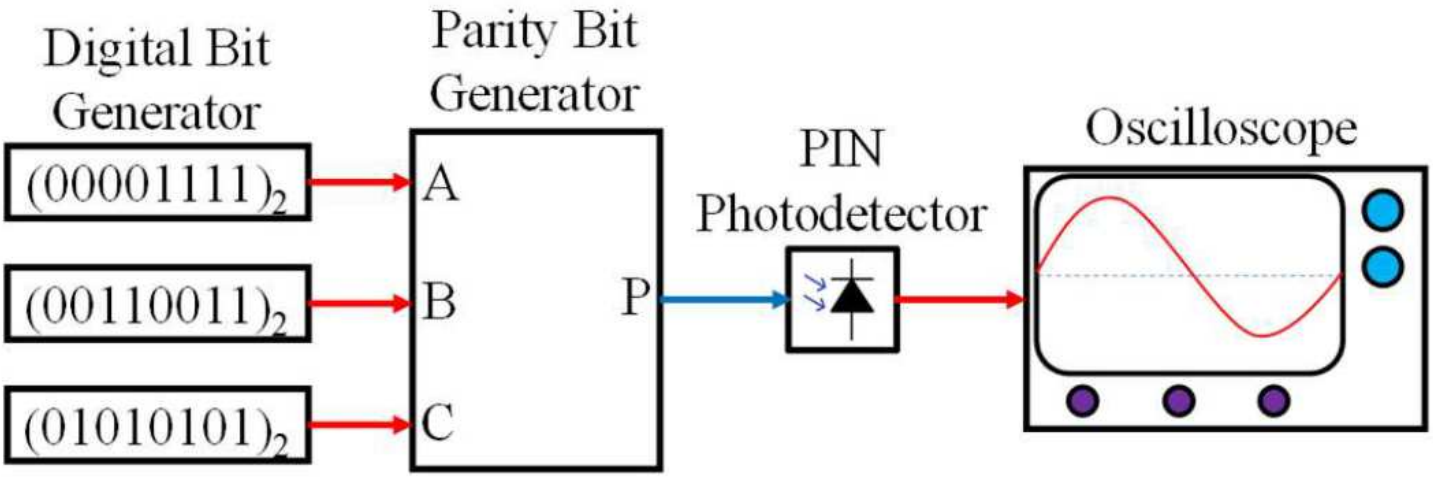

Figure 7

Simulation block setup for the bit generator.

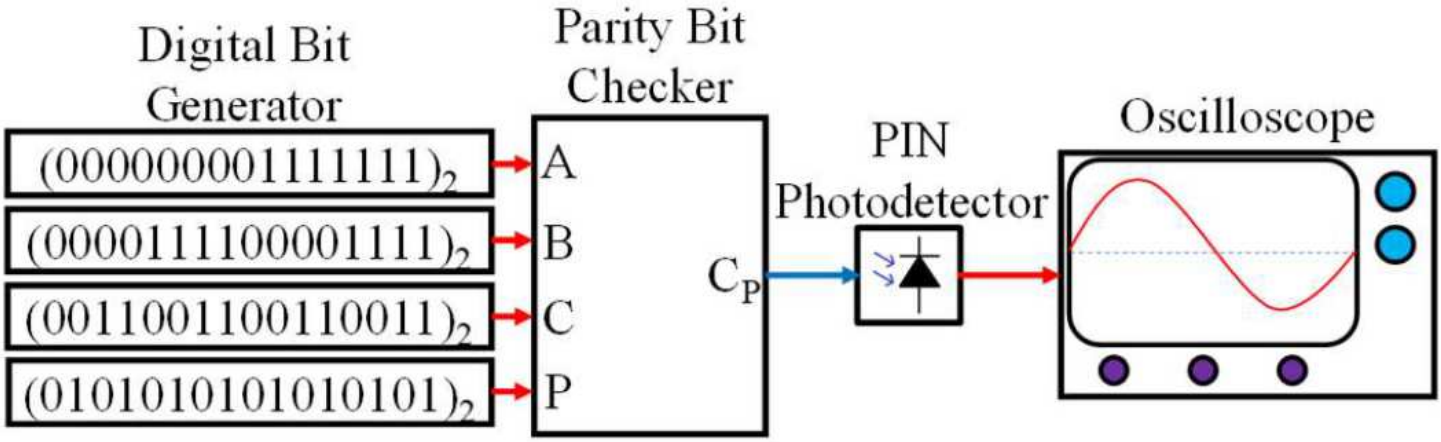

Figure 8

Simulation block setup for the bit checker.

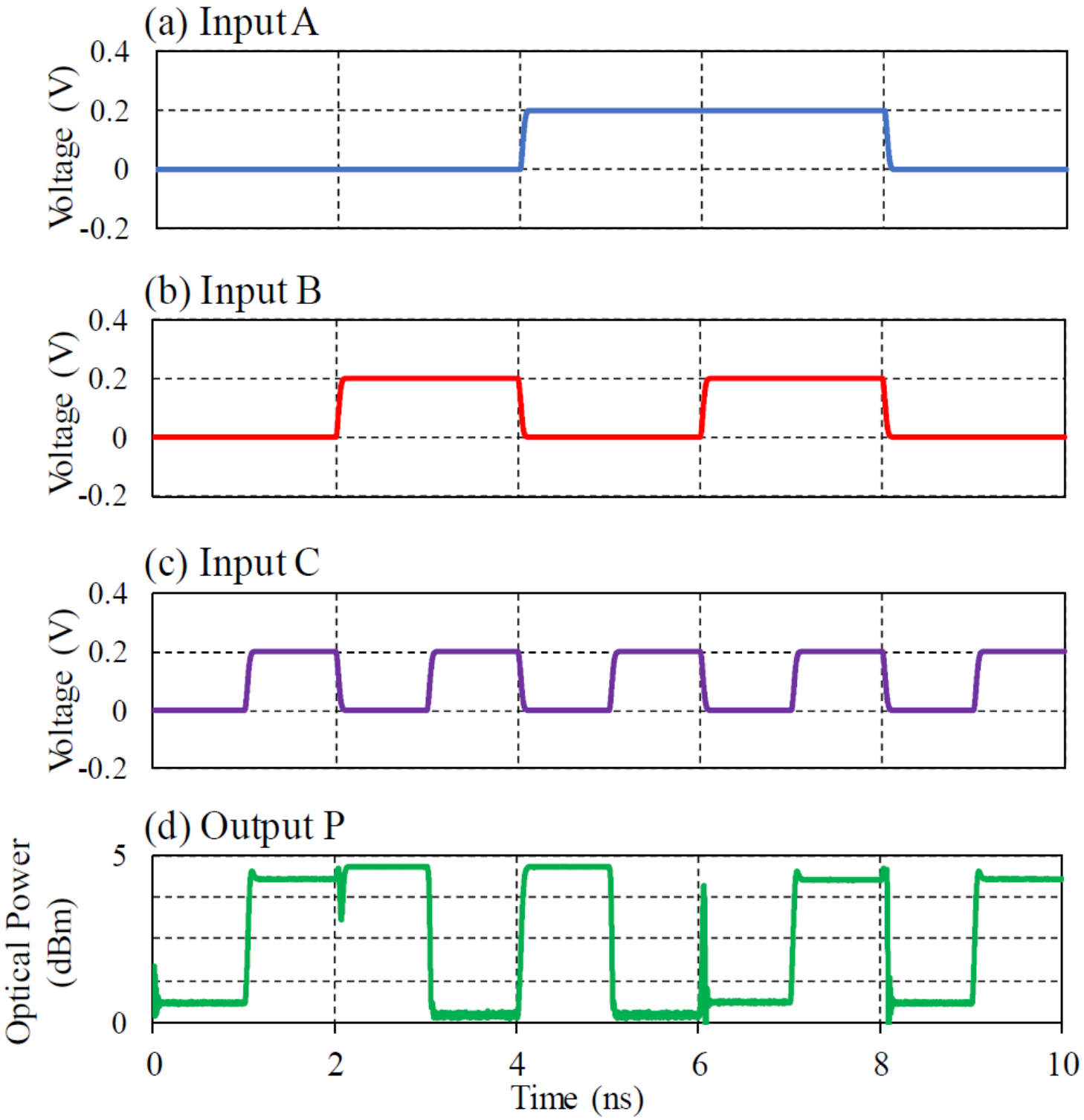

Figure 9

Timing waveform for the proposed bit generator.

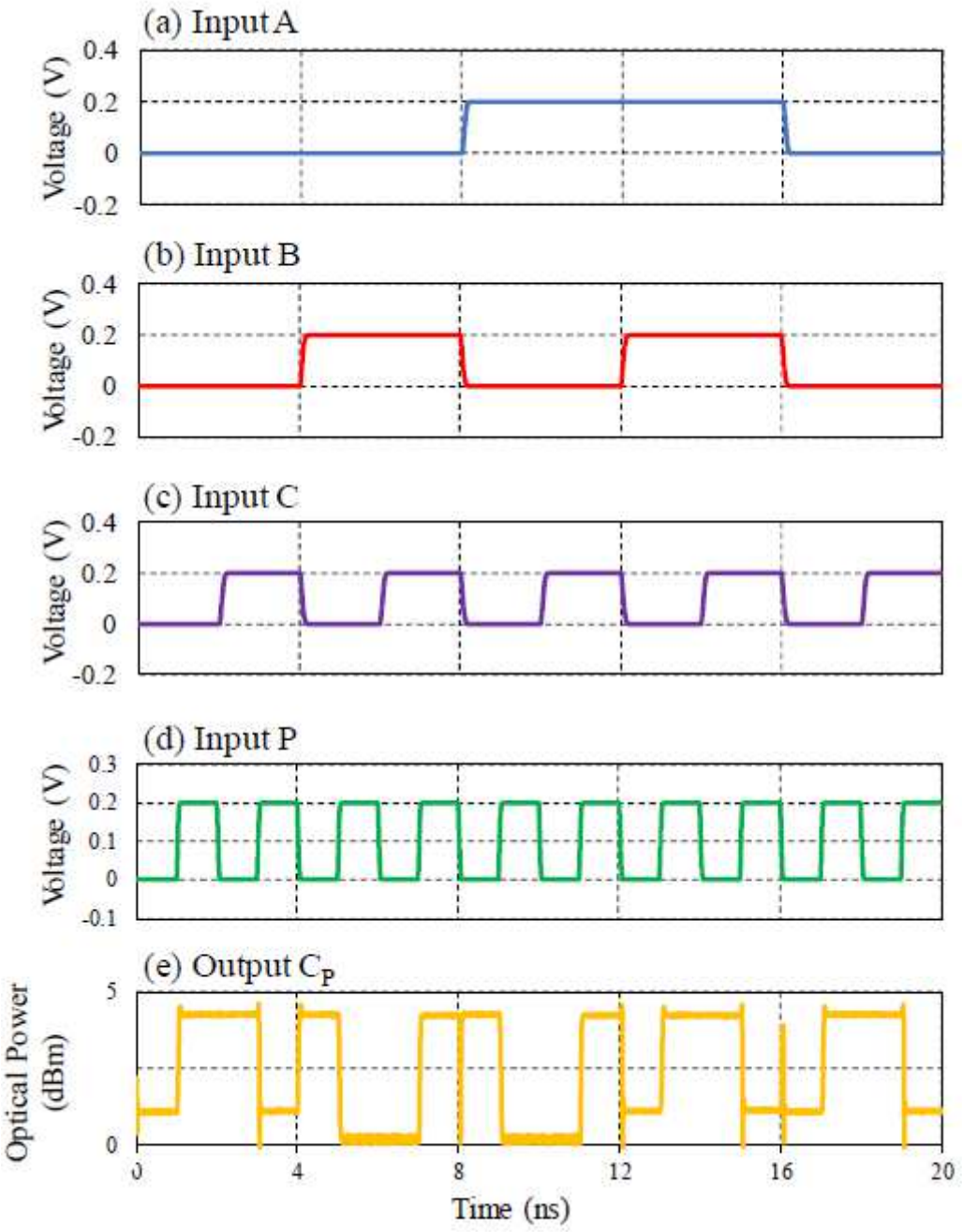

Figure 10

Timing waveform for the proposed bit checker.