A New Switch-Diode Cell-Based Single-Phase cascaded Multilevel Inverters

bidyut mahato (✉ bidyut_mahato@ee.ism.ac.in)

IIT (ISM): Indian Institute of Technology <https://orcid.org/0000-0002-9979-823X>

Saikat Majumdar

IIT (ISM): Indian Institute of Technology

Kartick Chandra Jana

IIT (ISM): Indian Institute of Technology

Ebrahim Babaei

University of Tabriz

Dushmanta kumar Mohanta

BIT Mesra: Birla Institute of Technology

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Abstract

A novel generalized modular MLI topology blends the unique advantages associated with existing MLIs to enhance the output voltage level incorporating a comparatively lesser number of power electronic components for similar performances. The unique features of the proposed topology pertain to lower distortion as well as total standing voltage (TSV) and best level-switch ratio (LSR) amongst the state-of-art MLIs. Extensive simulations using MATLAB/Simulation platforms as well as experimental models of single-phase 7, 9, 11, 13, 15 level inverter validate the superiority of the proposed topology for pragmatic applications in uninterruptable power supplies, photovoltaic farms, wind farms, and fuel cells.

Full Text

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Figures

Figure 1

Proposed asymmetrical MLI topology (a) A generalized Switch Diode Cell (SDC) inverter module, (b) Generalized cascaded MLI with 'm' number of 15-level modules

Figure 2

Practical arrangement of the isolated DC voltage sources with multi-winding transformers-rectifiers.

Figure 3

a. Proposed 7-level inverter b. Control strategy for the proposed 7-level inverter topology

Figure 4

Different operating modes for proposed 7-level inverter module.

(a)

(b)

Figure 5

Switching pulse pattern for each power switches of proposed 7-level inverter having one SDC cell obtained from (a) Simulation at 1 kHz. (b) Experimental set-up at 1 kHz.

Figure 6

Comparison of proposed topology for a) N_v versus N_{ps} for [A]-[ZD]. b) N_v versus N_{DC} for [A]-[ZD]. c) Level Switch Ratio for different ranges, $N_{ps}=7, 10, 15$. d) N_v versus TSV for cascaded module topology (Case-I)

Figure 7

Blocking voltage on each power switch of proposed MLI topology for different voltage levels.

Figure 8

Experimental set-up of the proposed Inverter. (A) Variac arrangements (B) Rectified DC supply from isolated transformer with capacitor filter. (C) Delay board and power circuit arrangements with the driver circuits. (D) DSO, Key sight. (E) RL- Load.

Figure 9

a. Proposed 7-level inverter with 1 SDC. ($V_f = V_{dc} = 107V$; $V_1 = 2V_{dc} = 214V$) b. Proposed 9-level inverter with 2 SDCs. ($V_f = V_{dc} = 55V$; $V_1 = V_{dc} = 55V$; $V_2 = 2V_{dc} = 110V$) c. Cascaded Module 25-level topology. ($V_{1f} = V_{dc} = 10V$; $V_{11} = 2V_{dc} = 20V$; $V_{12} = 3V_{dc} = 30V$); ($V_{2f} = V_{dc} = 10V$; $V_{21} = 2V_{dc} = 20V$; $V_{22} = 2V_{dc} = 30V$)

(a)

(b)

(c)

(d)

Figure 10

Proposed MLI topology with 2 SDC (7-level) obtained at load of $R=65\Omega$, $L=65\text{mH}$ with $V_{pk}=321\text{V}$, $I_{pk}=4.68\text{A}$. (a) Experimental result at $M_i=1$, (b) Experimental result at $M_i=0.5$ (c) Simulation result of load voltage and current (d) %THD for voltage output.

(a)

(b)

(c)

(d)

Figure 11

Proposed MLI topology with 2 SDC (9-level) obtained at load of $R=130\Omega$, $L=50\text{mH}$ with $V_{pk}=220\text{V}$, $I_{pk}=1.68\text{A}$. (a) Experimental result at $M_i=1$, (b) Experimental result at $M_i=0.4$ (c) Simulation result of load voltage and current (d) %THD for voltage output.

(a)

(b)

(c)

(d)

Figure 12

Simulation result of output voltage and load current for the proposed (a) 11-level (b) 13-level (c) 15-level (d) 25-level inverter.

(a)

(b)

(c)

(d)

Figure 13

Experimental results of inverter designed in laboratory for different DC source ratio, (a) 11-level inverter with 2 SDC ($V_f : V_1 : V_2 = V_{dc} : 2V_{dc} : 2V_{dc}$) at load of $R = 123\Omega$, $L = 75\text{mH}$, $V_{pk} = 150\text{V}$, $I_{pk} = 1.2\text{A}$. (b) 13-level inverter with 2 SDC ($V_f : V_1 : V_2 = V_{dc} : 2V_{dc} : 3V_{dc}$) at load of $R = 100\Omega$, $L = 75\text{mH}$, $V_{pk} = 126\text{V}$, $I_{pk} = 1.33\text{A}$. (c) 15-level inverter with 2 SDC ($V_f : V_1 : V_2 = V_{dc} : 2V_{dc} : 4V_{dc}$) at load of $R = 115\Omega$, $L = 75\text{mH}$, $V_{pk} = 133\text{V}$, $I_{pk} = 1.15\text{A}$. (d) 25-level cascaded module inverter with 2 SDCs ($V_{1f} : V_{11} : V_{12} = V_{2f} : V_{21} : V_{22} = V_{dc} : 2V_{dc} : 3V_{dc}$) at load of $R = 120\Omega$, $L = 75\text{mH}$, $V_{pk} = 126\text{V}$, $I_{pk} = 1\text{A}$.

(a)

(b)

(c)

(d)

Figure 14

Harmonic analysis of the simulation results of the output voltage for the proposed inverter (a) 11-level (b) 13level (c) 15-level (d) 25-level.

(a)

(b)

Figure 15

Experimental waveforms for (a) change of modulation index (M_i) ranging from $M_i=0$ to $M_i=1$ (b) change of load from $R=130\Omega$, $L=50mH$ to $R=200\Omega$, $L=50mH$.

Figure 16

Proposed 7-level topology with solar PV integration.