Wideband High Gain Active Feedback Transimpedance Amplifier

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Abstract: This paper presents a new wideband high gain CMOS transimpedance amplifier without using any inductor. In the proposed TIA, gain enhancing path is introduced in the active voltage-current feedback TIA topology to increase both the gain and bandwidth. This path increases the transconductance of the proposed TIA which reduces the input resistance and leads to bandwidth extension. Additionally, for utilizing the benefit of this topology, cascading of common source stage is also done to increase the gain further without deteriorating the bandwidth. Mathematical analysis is also performed to evaluate both the gain and bandwidth enhancement. These analyses are supported by simulations that are done using TSMC 180 nm CMOS technology with the input photodiode capacitance of 0.3 pF. The proposed TIA occupies 0.019 mm² area and consumes 3.2 mW from the power supply of 1.8 V. Simulation results show that the transimpedance gain of the proposed TIA is 57.15 dBΩ over the bandwidth of 6.5 GHz. The input noise is 17.16 pA/√Hz.

Keywords: Active feedback, inductorless, transimpedance amplifier, cascade.

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1. Introduction

The significant increase in the demand of high data rates has motivated researchers to explore optical communication systems that are suitable to handle this requirement. Transimpedance amplifier (TIA) is the very crucial front-end block at the receiver link of optical communication systems. TIA converts small input photodiode current into an amplified voltage level. Therefore, gain is an important parameter of TIA and it should be as high as possible. Few design techniques are reported in the literature to enhance the gain which includes positive feedback technique [1], self cascode structure [2-3] and cascading of buffer stages [4]. Positive feedback increases the gain by reducing the overall output conductance, however, it has stability issues. Self cascode structure also increases the gain but it enhances the voltage headroom. Cascading of stages increases the gain but at the cost of power dissipation and bandwidth. Apart from gain, bandwidth is also an important parameter which

is limited due to large input photodiode capacitance. Various bandwidth enhancement techniques are reported such as inductive peaking [5-6], capacitive degeneration [7-8], capacitive feedback [9-10], negative capacitance [11], common gate (CG) [12] and regulated cascode (RGC) [13-14]. Both the inductive and capacitive compensation increase the bandwidth but they occupy the large chip area. CG topology also gives a wide operating frequency range but yields relatively higher noise. RGC is the most common topology to design TIA due to its low input impedance, high stability and wide bandwidth but it has higher power dissipation and headroom voltage.

In this work, active voltage-current feedback TIA topology [15] is used which provides low input and output impedances. In this topology, the gain enhancing path is introduced in such a way that it increases both gain and bandwidth. This path increases the transconductance and thereby, reduces the input resistance which leads to bandwidth extension. Moreover, a common source (CS) stage has been cascaded to use the advantage of this topology to increase the gain further without deteriorating the bandwidth.

Active voltage-current TIA topology (AVCF) is discussed in Section 2. The proposed TIA design is presented in Section 3. Noise analysis and simulation results are discussed in section 4 and 5, respectively. Section 6 concludes the paper.

2. Active voltage-current TIA

The TIA circuit based on active voltage-current feedback topology is shown in Fig. 1 in which transistor M_1 provides feedback path and decreases the output and input resistances [15]. In this circuit, transistor M_1 itself converts the current into a voltage whereas other topologies use resistor to do the same. The drain current of transistor M_1 is given by [15]:

$$I_{d2} = g_{m1} V_o = g_{m1} V_{in}. \quad (1)$$

The input and output resistances are given in Eq. (2), and Eq. (3) respectively [15].

$$R_{in} = \frac{1}{g_{m1}}. \quad (2)$$

$$R_o = \frac{1}{(1 + R_1 g_{m1}) g_{m2}}, \quad (3)$$

where R_1 is the total resistance at the input port due to both current source CS_1 and the output resistance of transistor M_1 . The transimpedance gain of the circuit is given by [15]:

$$Z(s) = \frac{R_1 R_2 g_{m2}}{R_1 R_2 C_1 C_2 s^2 + (R_1 R_2 C_1 (g_{m2} + g_{mb2}) + R_1 C_1 + R_2 C_2) s + R_1 R_2 g_{m1} g_{m2} + R_2 (g_{m2} + g_{mb2}) + 1}, \quad (4)$$

where C_2 and R_2 are the sum of parasitic capacitance and intrinsic resistance at the output port respectively. C_1 is the total capacitance at the input port. From Eq. (4), the transimpedance gain at low frequency has been deduced as:

$$Z(0) = \frac{R_1 R_2 g_{m2}}{R_1 R_2 g_{m1} g_{m2} + R_2 (g_{m2} + g_{mb2}) + 1} \quad (5)$$

Fig. 1. Active voltage-current TIA [15].

Since the output impedance of TIA (shown in Fig. 1) is very low, therefore, cascading of the gain stage can be done without affecting the bandwidth. The number of gain stages can be chosen based on the trade-off that exists between gain, power consumption and noise.

3. The proposed TIA

The circuit of the proposed TIA is shown in Fig. 2 in which C_{pd} is photodiode capacitance and I_{in} is photodiode current. The active voltage-current feedback (AVCF) TIA is formed by transistors M_1 and M_2 in which transistor M_1 is providing voltage-current feedback. In AVCF TIA, modification has been done by introducing gain enhancing path which includes resistor R_p and transistor M_p . This path not only increases the gain but also extends the bandwidth. It also increases the transconductance of the amplifier which leads to decrement in the input resistance. Additionally, a common source (CS) stage (M_3 and R_D) has also been cascaded with TIA to increase the gain further. This cascaded voltage gain stage does not affect the bandwidth due to the low output resistance of TIA as mentioned in section 2. The small signal analysis of the proposed TIA is done to show the gain enhancement and bandwidth extension.

Fig. 2. The proposed TIA.

The small signal equivalent circuit of the proposed TIA is shown in Fig. 3 in which g_{mi} (where $i = 1, 2, 3, P$) are the transconductance of transistors M_i (where $i = 1, 2, 3, P$) respectively. C_{in} is the total capacitance at the input node which consists of gate-to-source

capacitance (C_{gs0}) of transistor M_p and the capacitance of photodiode. R_1 is the total resistance at the input node and R_2 is the total resistance at the V_o (shown in Figure 2) node. The transfer function of the proposed TIA can be computed by applying Kirchhoff's current law (KCL) at nodes V_1, V_2, V_3 , and V_{out} mentioned in Fig. 3. Body bias effect is neglected because $g_{mp,2} \gg g_{mbp,2}$. C_{gs0} is the sum of the gate-to-source capacitances of M_1 and M_3 and C_{gdm} is the sum of the gate-to-drain capacitances of M_p and M_2 .

The transimpedance gain of the proposed TIA is calculated as:

$$Z(s) = \frac{V_{out}}{I_{in}} = Z(0) \frac{(1 - a_1 s)(1 - b_1 s)}{(a_2 s^2 + b_2 s + 1)} \quad (6)$$

where $Z(0)$ is transimpedance gain at low frequency and is obtained as:

$$Z(0) = - \frac{R_2 R_p R_1 R_D g_{m1} g_{m3} (1 - g_{mp} r_{op})}{(R_1 g_{mp} + g_{m2} R_2) R_p - g_{m2} r_{op} R_2 + R_p}. \quad (7)$$

Fig.3. Small signal equivalent circuit of the proposed TIA.

Assuming $g_{mr} \gg 1$, Eq. (7) can be estimated as:

$$Z(0) = \frac{R_1 R_2 R_p R_D g_{m1} g_{m3} g_{mp} r_{op}}{(R_1 g_{mp} + g_{m2} R_2) R_p - g_{m2} r_{op} R_2}. \quad (8)$$

By comparing Eqs. (5) and (8), it can be concluded that gain is enhanced by introducing path (M_p and R_p) and the common source stage (M_3 and R_D).

The coefficients of Eq. (6) are found to be:

$$a_1 = \frac{C_{gd3}}{g_{m3}} \quad (9)$$

$$b_1 = \frac{C_{gd1}}{g_{m1}} \quad (10)$$

$$a_2 = \frac{R_1 R_p r_{op} C_2 C_{gs2} + R_2 R_p r_{op} C_3 C_{gs2} + R_1 R_2 R_p C_1 C_2 - R_2 R_p r_{op} C_1 C_{gdm}}{(R_1 g_{mp} + g_{m2} R_2) R_p - g_{m2} r_{op} R_2} \quad (11)$$

$$b_2 = \frac{R_1 R_P r_{op} C_{gs2} g_{mp} + R_1 R_2 R_P C_2 g_{mp} + R_P r_{op} C_{gs2} + R_2 R_P C_1 - R_1 R_2 R_P C_1 g_{mp}}{(R_1 g_{mp} + g_{m2} R_2) R_P - g_{m2} r_{op} R_2} \quad (12)$$

where $C_1 = C_{gs0} + C_{gs2} + C_{gd1}$, $C_2 = C_{in} + C_{gd1}$ and $C_3 = C_{gs0} + C_{gd1}$.

The dominant pole can be calculated as:

$$P = \frac{(R_1 g_{mp} + g_{m2} R_2) R_P - g_{m2} r_{op} R_2}{R_1 R_P r_{op} C_{gs2} g_{mp} + R_1 R_2 R_P C_2 g_{mp} + R_P r_{op} C_{gs2} + R_2 R_P C_1 - R_1 R_2 R_P C_1 g_{mp}}. \quad (13)$$

The input resistance of the proposed TIA is obtained as:

$$R_{in} = \frac{(1 + r_{op} g_{mp})(r_{op} + R_P)}{(g_{m1} + g_{mp})(r_{op} + R_P) r_{ol} r_{op} + r_{op} g_{mp} + 1}. \quad (14)$$

On comparing Eqs. (2) and (14), it can be observed that the input resistance of the proposed circuit is reduced by introducing path (M_p and R_p) which isolates input photodiode capacitance and thereby, extends the bandwidth. In the proposed circuit, biasing is provided in such a way that the transistors are operated in a saturation region. Aspect ratios of transistors are selected in order to minimize the trade-offs between bandwidth, gain and noise.

4. Noise analysis

The input of the transimpedance amplifier is photodiode current which is very small in magnitude. Therefore, noise becomes an important parameter for TIA which has to be analysed. Main sources of noise in TIA are flicker and thermal noise [16]. The small signal equivalent circuit for noise analysis is shown in Figure 4.

The total input-referred noise of modified ACVF-TIA is obtained as:

$$\overline{I_{n,total}^2} = \overline{I_{n,M1}^2} + \overline{I_{n,M2}^2} + \overline{I_{n,Mp}^2} + \overline{I_{n,R1}^2} + \overline{I_{n,R2}^2} \quad (15)$$

where $\overline{I_{n,M1}^2}$, $\overline{I_{n,M2}^2}$, $\overline{I_{n,Mp}^2}$ and $\overline{I_{n,R2}^2}$ are the noises due to transistors M_1 , M_2 , M_p , and M_4 . These can be estimated as:

$$\overline{I_{n,M1}^2} = \frac{1}{g_{m1}^2} (4KT\omega^2 C_{gs1}^2 (\gamma_{gd01}) + \frac{g_{m1}^2 K_F}{W_1 L C_{ox}}) \quad (16)$$

$$\overline{I_{n,M2}^2} = \frac{1}{g_{m2}^2} (4KT\omega^2 C_{gs2}^2 (\gamma_{gd02}) + \frac{g_{m2}^2 K_F}{W_2 L C_{ox}}) \quad (17)$$

$$\overline{I_{n,Mp}^2} = \frac{1}{g_{mp}^2} (4KT\omega^2 C_{in}^2 (\gamma_{gd0p} + \frac{1}{R_p}) + \frac{g_{mp}^2 K_F}{W_p L C_{ox}}). \quad (18)$$

$$\overline{I_{n,R1}^2} = \frac{4KT}{R_1} \quad (19)$$

$$\overline{I_{n,R2}^2} = 4KT\gamma g_{d0,R2}(1+M)\omega^2 C_{gs0}^2 \quad (20)$$

γ is noise factor of transistor, K_F is process dependent constant, and g_{d01} , g_{d02} and g_{d0p} are zero-bias drain conductance [17] of transistors M_1 , M_2 and M_p respectively. First and the last terms in Eqs. (16) – (18) are thermal and flicker noises due to transistors respectively.

Fig. 4: Small signal equivalent circuit for noise analysis

After substituting the values of $\overline{I_{n,M1}^2}$, $\overline{I_{n,M2}^2}$, $\overline{I_{n,Mp}^2}$, $\overline{I_{n,R1}^2}$ and $\overline{I_{n,R2}^2}$ in Eq. (15), the total input-referred noise is given by:

$$\begin{aligned} \overline{I_{n,total}^2} = & \frac{1}{g_{m1}^2} (4KT\omega^2 C_{gs1}^2 (\gamma g_{d01}) + \frac{g_{m1}^2 K_F}{W_1 L C_{ox}}) + \frac{1}{g_{m2}^2} (4KT\omega^2 C_{gs2}^2 (\gamma g_{d02}) + \frac{g_{m2}^2 K_F}{W_2 L C_{ox}}) + \\ & \frac{1}{g_{mp}^2} (4KT\omega^2 C_{in}^2 (\gamma g_{d0p} + \frac{1}{R_p}) + \frac{g_{mp}^2 K_F}{W_p L C_{ox}}) + \frac{4KT}{R_1} + 4KT\gamma g_{d0,R2}(1+M)\omega^2 C_{gs0}^2 \end{aligned} \quad (21)$$

From Eq. (21), it can be seen that the value of the resistance R_D and size of transistor M_1 must be large enough to minimize the noise of the proposed TIA. At higher frequency, noise increases due to the effect of dominating term ωC . However, the total noise of the proposed TIA would be slightly higher than that given in Eq. (21) due to cascading of the common source stage.

5. Simulation result

Simulations of the proposed TIA are done using TSMC 180 nm CMOS technology at the power supply of 1.8 V using Mentor Graphics Eldo simulation tool. The values of circuit parameters of the proposed TIA are mentioned in Table 1. For the comparison purpose, AVCF-TIA has also been simulated using the same technology and tool with similar circuit parameters as that of the proposed TIA.

Table 1: Circuit parameters of the proposed TIA.

Parameters	Values
Aspect Ratio	$M_1 = 15/0.18\mu\text{m}$, $M_2 = 50/0.18\mu\text{m}$ $M_3 = 40/0.18\mu\text{m}$, $M_p = 30/0.18\mu\text{m}$
Bias voltage	$V_{B1} = 1.2\text{V}$, $V_{B2} = 0.6\text{V}$
Resistance	$R_D = 800\Omega$, $R_P = 500\Omega$
Capacitance	$C_{pd} = 0.3\text{pF}$

Fig. 5. Comparison of the frequency response of AVCF, AVCF with CS stage and the proposed TIA.

Fig. 6. The frequency response of the proposed TIA at different values of the photodiode capacitor.

Fig. 5 shows the comparison between the frequency responses of AVCF TIA, AVCF TIA with CS stage and the proposed TIA. It can be depicted that the gain of the proposed TIA is enhanced from 47 to 57.15 dB Ω and bandwidth is extended from 1.7 to 6.5 GHz with 3.2 mW power dissipation.

Fig. 7. The frequency response of the proposed TIA at different temperatures.

Fig. 8. Input-referred noise of the proposed TIA.

The frequency responses for different photodiode capacitance ($C_{pd} = 0.1\text{pF}$, 0.2pF , 0.3pF and 0.4pF) and at different temperatures are illustrated in Fig. 6 and Fig. 7, respectively. It can be seen from Fig. 6 that the bandwidth is reducing with the increasing values of photodiode capacitance. However, the variations in the bandwidth with photodiode capacitance are very low. From Fig. 7, it can be observed that both the gain and bandwidth are reducing with the increase in temperature. Fig. 8 shows the input-referred noise of the proposed TIA which is around 17 pA/ $\sqrt{\text{Hz}}$. Fig. 9 presents the dc transfer characteristics of the proposed TIA which shows an almost linear relationship between input and output.

Fig. 9. DC response of the proposed TIA.

Fig. 10. Transient response of the proposed TIA.

The transient response of the proposed TIA is shown in Fig. 10. It can be observed that the output voltage swing is around 10 mV for 10 μ A input current. The Monte Carlo simulation is carried out by applying a set of 200 samples for mismatches in the width of the transistors

of the proposed TIA and is shown in Fig. 11. The minimum and maximum gains of the proposed TIA are 56.2 dB Ω and 57.9 dB Ω , respectively.

Fig. 11. The frequency response of the proposed TIA using Monte Carlo simulation.

Fig. 12. The frequency response of the proposed TIA at different process corners.

Fig. 12 shows the frequency response of proposed TIA at different process corners. Since the proposed TIA consist of only NMOS, therefore, they have only two process corners that are slow (S) and Fast (F). It can be observed that by varying process corners S to F, bandwidth varies from 6.4 to 7.3 GHz while gain is almost same. Fig. 13 shows the layout of the proposed TIA which depicts that the proposed circuit occupies 0.0197 mm² chip area. The post-layout and pre-layout simulations are depicted in Fig. 14 which shows that the gain is the same as that of pre-layout simulation but the bandwidth is slightly reduced.

Fig. 13. Layout of the proposed TIA.

Fig. 14. Post-layout simulation of the proposed TIA.

Table 2 illustrates the comparative results of existing TIAs and the proposed TIA. It can be observed that the bandwidth, gain, power dissipation and noise of the proposed TIA are better than all other TIAs mentioned in Table 2 except [15]. However, the gain and bandwidth of TIA presented in [15] are higher than the proposed TIA but at the cost of noise, chip area and power dissipation. Furthermore, the chip area of the proposed TIA is also lesser than all other TIAs except [21]. But, other parameters of the proposed design are better as compared to [21]. Additionally, the proposed TIA shows supremacy over other existing TIAs in terms of Figure of merit (FOM), expressed by:

$$FOM = \frac{Bandwidth(GHz) \times Gain(dB\Omega) \times C_{PD}(pF)}{power(mW) \times voltage(V)}$$

Table 2: Comparative results of existing TIAs and the proposed TIA.

Ref.	[15]	[18]	[19]	[20]	[21]	This work
Year	2017	2009	2013	2015	2018	2020
PD capacitance(fF)	300	250	250	250	500	300
Supply Voltage (V)	1.8	1.8	1.8	1.5	1.8	1.8
Gain (dBΩ)	59	50	46	55.3	54.4	57.1
BW (GHz)	7.9	6.5	4	6	2.2	6.5
Power (mW)	18	14	31.5	5.7	19.7	3.4
Noise (pA/√Hz)	23	-	18	24.3	-	17.1
Area (mm ²)	0.11	0.09	0.35	0.4	0.003	0.019
No. of inductor	2	1	0	1	0	0
FOM	4.3	3.22	0.81	9.70	1.68	18.19

6. Conclusion

Active feedback based TIA is proposed in which gain enhancing path is introduced to increase both gain and bandwidth. Bandwidth is extended by increasing the transconductance which reduces the input resistance. Moreover, a common source stage is also cascaded which leads to gain enhancement further without reducing the bandwidth. In the proposed TIA, gain and bandwidth both are enhanced along with both low power consumption and chip area. Consequently, it can be concluded that the proposed TIA can be used in numerous optical receiver units where high gain, wide bandwidth, low cost and low noise are required.

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