Design of Universal Logic Gates Using Homo and Hetero-Junction Double Gate TFETs with Pseudo-Derived Logic

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Design of Universal Logic Gates using Homo and Hetero-Junction Double Gate TFETs with Pseudo-Derived Logic

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Abstract

This work explores homo and hetero-junction Tunnel field-effect transistor (TFET) based NAND and NOR logic circuits using 30 nm technology and compares their performance in terms of power consumption and propagation delay. By implementing homo-junction TFET based NAND and NOR logic circuits, it has been observed that NAND consumes less power than NOR gate, since current drawn by PTFET in pull-up network of NOR gate is higher. The delay of homo-junction TFET based NOR logic gate is lesser than that of NAND gate due to its reduced internal capacitances. To meet the enhanced performance of both NAND and NOR logic circuits, shorted and independent double gate hetero-junction (GaSb-InAs) TFETs are designed and implemented. In order to reduce both power consumption and delay further, Pseudo-derived logic is implemented in NAND and NOR logic circuits for the first time. Hetero-junction TFET based NAND with Pseudo-derived logic circuit shows lesser propagation delay of 10^3 times and reduction in power consumption by 0.75 times compared to hetero-junction NAND logic circuit. Hetero-junction TFET based NOR with Pseudo-derived logic shows that the reduction in power consumption is of 10^3 times and less propagation delay than that of hetero-junction NOR logic circuit.

Keywords Tunnel FET · TCAD · logic gates · Pseudo-derived logic · Sub-threshold swing · propagation delay · power consumption.

1. Introduction

Metal-oxide-semiconductor field-effect transistor (MOSFET) has a potential to be used in low power electronic systems. Due to its limitations such as short channel effects and with the down scaling, it did not reach the requirements of low power electronics. The structure of the tunneling field effect transistor (TFET) is almost the same as MOSFET but with different doping materials in source and drain [1]-[3]. Another difference is that the mechanism by which the flow of carriers happens in TFET is quantum tunneling. In TFETs the wave function of electrons disappears on one side of the junction and appears on another side which is called as quantum tunneling. This tunneling feature produces a steep subthreshold swing (SS) of <60mv/decade which is a promising feature for low power high speed electronic applications such as embedded DRAM (Dynamic Random Access memory) [4].

The structure of TFET consists of a p-i-n junction (p-type, intrinsic, n-type), in which the tunneling of electrons in the intrinsic area (channel) is controlled by a gate terminal. As the gate voltage is applied, the band-to-band tunneling (BTBT) happens when the conduction band of the channel goes to the same energy level with the valence band of the p-region [5]-[7]. Due to scaling of technology the channel length is reduced which demanded reduction in oxide layer thickness and thus resulting in increase of gate leakage current. To overcome this issue and to provide better control of the channel, double gate TFETs (DGTFETs) have been introduced [8]-[11]. In TFET structure, the source and drain are doped heavily and the gate controlling the BTBT between the source-channel/ channel-drain regions by means of band bending [12]-[14].

To improve the rate of probability of tunneling, a combinational dopant is used which is Gallium Antimony and Indium arsenide (GaSb-InAs) [15]-[17]. The GaSb-InAs combination has been used for the hetero-junction TFET which gives non-overlapping bandgap. The effective bandgap for tunneling can be decreased even further by using this heterostructure [18]-[20]. To reduce the tunneling barrier, GaSb and InAs were chosen for the source and channel/drain respectively. One more convincing reason to select this combination is that the lattice constants are matched for the materials.

The key element of this work is to implement the NAND, NOR logic gates with lower power consumption and less propagation delay. In this paper, Section 2 gives the device description and parameter space of the device. Section 3 provides the results and discussion where the implementation of NAND and NOR logic circuits using the homo and hetero-junction based TFET is realized. Finally, Section 4 provides the conclusion.

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2. Device Description and Parameter Space

All the device simulations are carried out using TCAD simulator from Synopsys [21]. Figure 1(a) shows the structure of homo-junction based Si TFET. GaSb-InAs hetero-junction TFET structure without and with doping/ meshing is shown in Fig. 1 (b) and Fig. 1(c) respectively. Table 1 gives the parameter space for DG TFETs which is used in the simulation. Doping dependence mobility, high and normal field effects on mobility and velocity saturation are used in the physics section of the simulator. Besides, the Fermi – Dirac statistics and SRH recombination, Hurkx tunneling model is also used in the simulator.

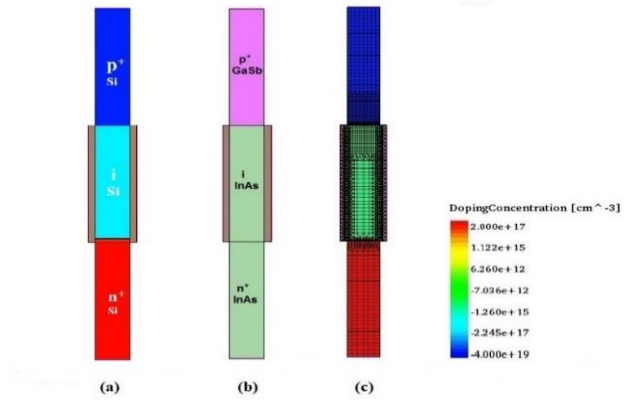

Fig. 1 Simulated structure of DG TFET (a) Si TFET (b) GaSb-InAs TFET without doping (c) GaSb-InAs DG TFET with doping/meshing.

TABLE 1 Parameter Space for DG TFETs.

Geometrical Parameters	Homo-junction (Si) DG TFET	Hetero-junction (GaSb-InAs) DG TFET
Gate length (L_g)	30 nm	30 nm
Channel thickness (T_{ch})	8 nm	8 nm
Front and back gate oxide thickness (T_{ox})	1 nm	1 nm
Source doping concentration	$1 \times 10^{20}\,cm^{-3}$	$4 \times 10^{19}\,cm^{-3}$
Drain doping concentration	$5 \times 10^{18}\,cm^{-3}$	$2 \times 10^{17}\,cm^{-3}$
Channel doping concentration	$1 \times 10^{17}\,cm^{-3}$	$1 \times 10^{15}\,cm^{-3}$

The device dimensions, appropriate models for the device simulator and the DC characteristics obtained are taken from our previous calibrated results [22]. It can be noticed that low-band gap material with low effective mass (m*) can be used to improve the drive current of the device [23]-[24]. The ON current I_{ON} of TFET is based on BTBT mechanism and critically depends on the transmission probability T_{WKB}, of the inter band tunneling barrier [25]. So 'T' can be calculated using the Wentzel-Kramers-Brillouin (WKB) approximation,

$$T_{wkb} \approx \exp \frac{4\lambda\sqrt{2m^* E_g^3}}{3qh(E_g + \Delta\emptyset)} \quad (1)$$

where m^* is the effective carrier mass, E_g is the bandgap, q is the electron charge, λ is the screening tunneling length and describes the spatial extent of the transition region at the source-channel interface, ΔØ is the energy range over which the tunneling can take place or the energetic difference between the conduction band in the source and the valence band in the channel, h is the Planck's constant.

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}} \cdot \sqrt{t_{ox} t_{Si}} \quad (2)$$

where t_{ox}, t_{Si}, ε_{ox}, and ε_{Si} are the oxide and silicon-film thickness and dielectric constants, respectively.

The circuit symbol of homo-junction NTFET and PTFET is shown in Fig. 3(a) and 3(b). The circuit symbol of shorted gate (SG) heterojunction NTFET and PTFET is shown in Fig. 4(a) and 4(b) respectively. The circuit symbol of independent gate (IG) heterojunction NTFET and PTFET is shown in Fig. 4(c) and 4(d) respectively.

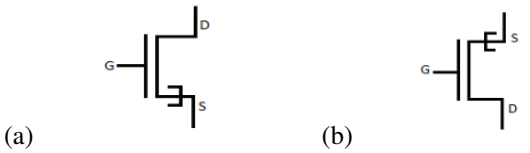

Fig. 3 Symbol of homo-junction (a) NTFET and (b) PTFET

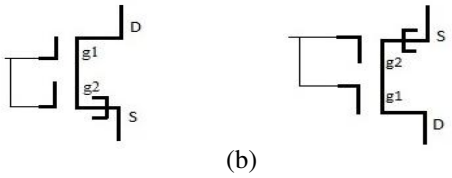

Fig. 4 Symbol of shorted gate (SG) hetero-junction (a) NTFET and (b) PTFET

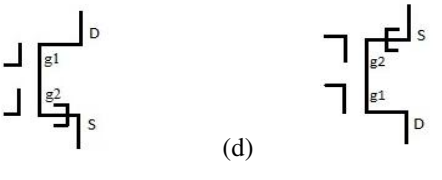

Fig. 4 Symbol of independent gate (IG) hetero-junction (c) NTFET and (d) PTFET

3. Results & Discussion

In this section, the universal logic gates (NAND and NOR) are realized using both homo and hetero-junction based TFETs. The power dissipation and propagation delay are extracted for both homo and hetero-junction TFETs and a performance comparison is made.

3.1. Homo-junction TFET based NAND and NOR logic circuits

This section provides the details of NAND and NOR realization of homo-junction Si based TFET and their corresponding timing diagrams are depicted.

A. Realization of NAND logic function

The realization of homo-junction TFET based NAND circuit which uses 30 nm technology node is shown in Fig. 5(a). In the NAND logic circuit when both inputs are given

as logic low, both PTFETs in the pull up network gets turned on and in the pulldown network both the NTFETs gets open circuited. So the path is created from V_{dd} to the output. When one of the inputs is low, one of the PTFET will get turned on and will pull the supply voltage to the output. Now when both inputs are high, the pulldown network gets short-circuited and pull the output voltage to ground thereby V_{out} becomes logic low or zero. The timing diagram of homo-junction TFET based NAND is as shown in Fig. 5(b).

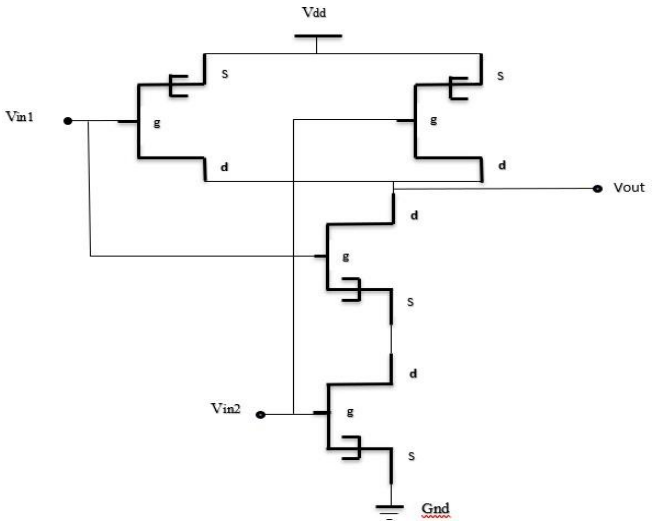

Fig. 5(a) NAND realization using homo-junction TFET.

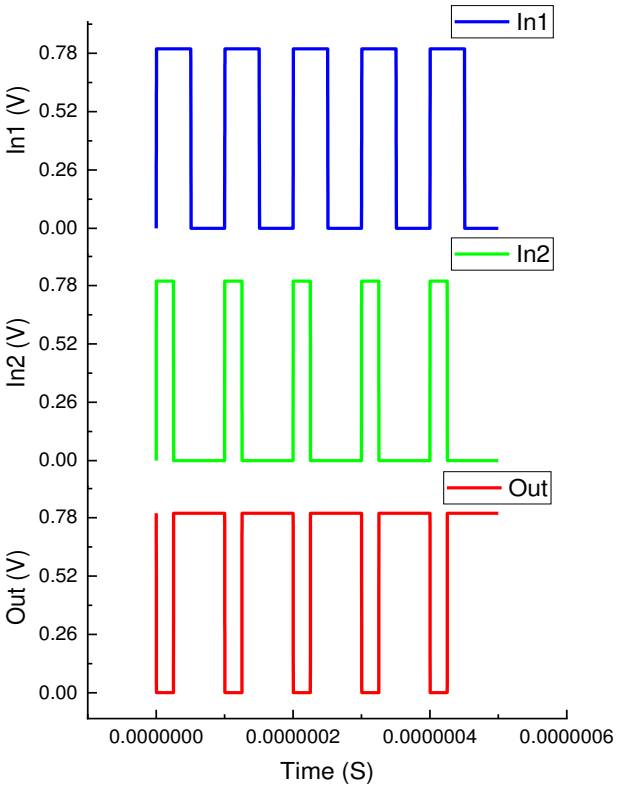

Fig. 5(b) Timing diagram of homo-junction NAND logic function.

B. Realization of NOR logic function

The homo-junction TFET based NOR circuit is as shown in Fig. 6(a). When both inputs are logic high PTFETs in the pull up network are turned off and the NTFETs in the pulldown network get turned on. This results in the output getting pulled to logic zero. Now when both of the inputs are logic low, both PTFETs present in the pull up network gets turned on and thus resulting the output getting logic high. When either of the input is logic high/one, the output is pulled down to logic zero/low, because one of the PTFETs present in the pullup network gets open circuited. The timing diagram of homo-junction TFET based NOR is shown in Fig. 6 (b).

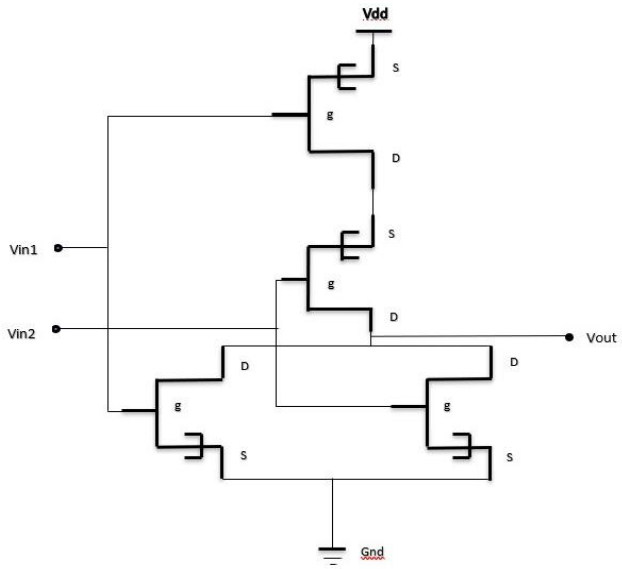

Fig. 6(a) NOR realization using homo-junction TFET.

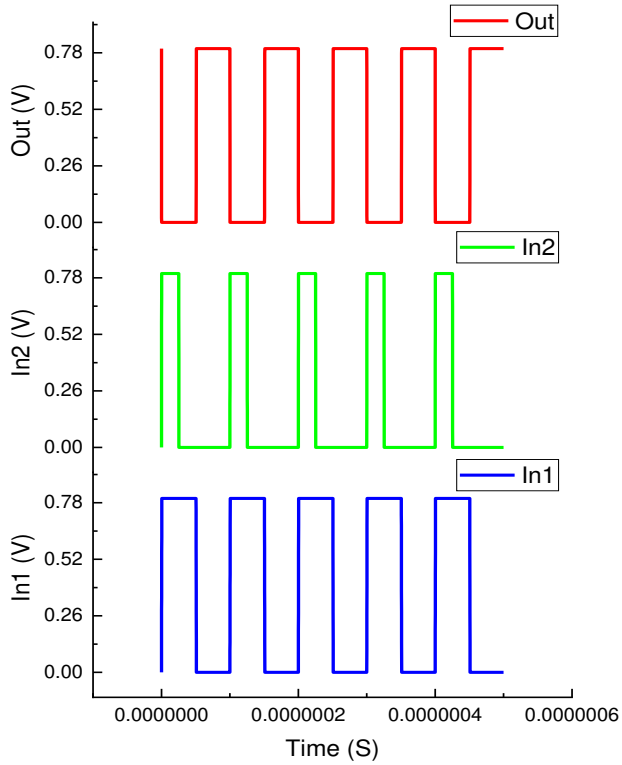

Fig. 6(b) Timing diagram of homo-junction NOR logic function.

3.2. SG Hetero-junction TFET based NAND and NOR logic circuits

This section provides the details of NAND and NOR realization using SG hetero-junction (GaSb-InAs) based TFET and its timing diagram is also plotted.

A. Realization of NAND logic function

The schematic of SG hetero-junction TFET based NAND is shown in Fig. 7(a). The circuit consists of hetero NTFET (HNTFET) in pull-down network and hetero PTFET (HPTFET) in pull-up network connected in series. When both input signals are given logic low, HPTFET gets turned on and forms a short-circuit path between supply V_{dd} and output $V_{out.}$ So the output signal gets logic high. When both inputs are logic high, HPTFET gets turned off and there is no path between supply voltage and output. When either of the input signal is given logic low, that is either V_{in1} or V_{in2} is given logic low, the output signal goes logic high. The timing diagram is as shown in Fig. 7(b).

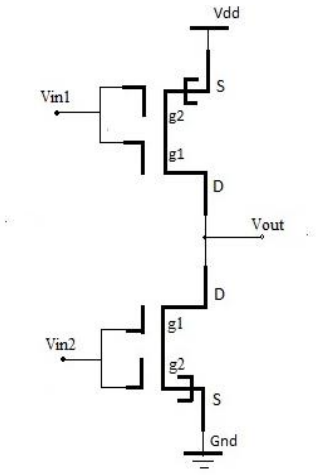

Fig. 7(a) NAND realization using SG hetero-junction TFET.

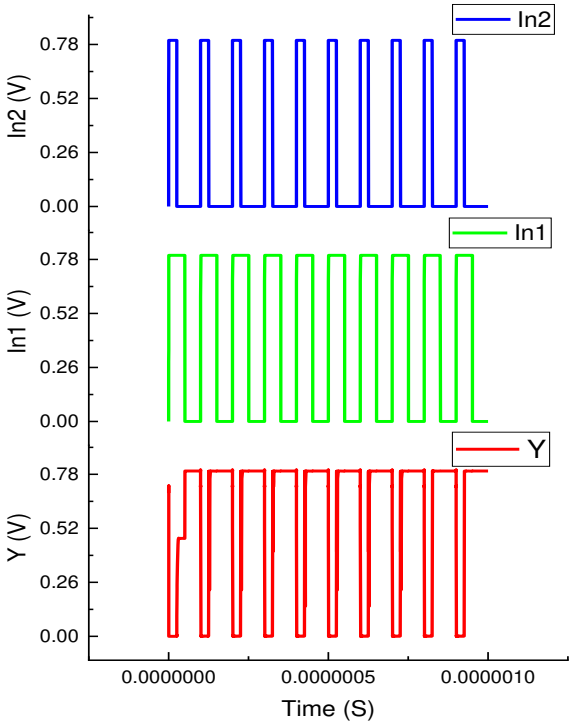

Fig. 7(b) Timing diagram of SG hetero-junction NAND logic function.

B. Realization of NOR logic function

The schematic of SG hetero-junction TFET based NOR logic circuit is shown in Fig. 8(a). Two HNTFETs are connected in parallel, two inputs are given to each of them. HNTFET is connected in series to the parallel combination of HNTFETs to act as a resistor to limit the current into the circuit. When both inputs are given logic high, two HNTEFTs gets turned on and short the supply V_{dd} to the ground, thereby producing logic low output. When both inputs are given logic low, both HNTFETs gets turned off and the supply V_{dd} gets shorted to output, producing logic high output. When either of the input is high, one of the HNTFET gets turned on pulling down the output to logic zero. The timing diagram is as shown in Fig. 8(b).

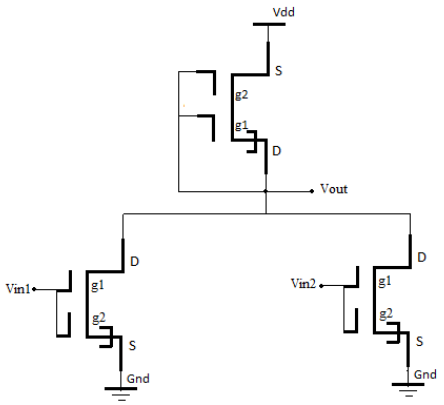

Fig. 8(a) NOR realization using SG hetero-junction TFET.

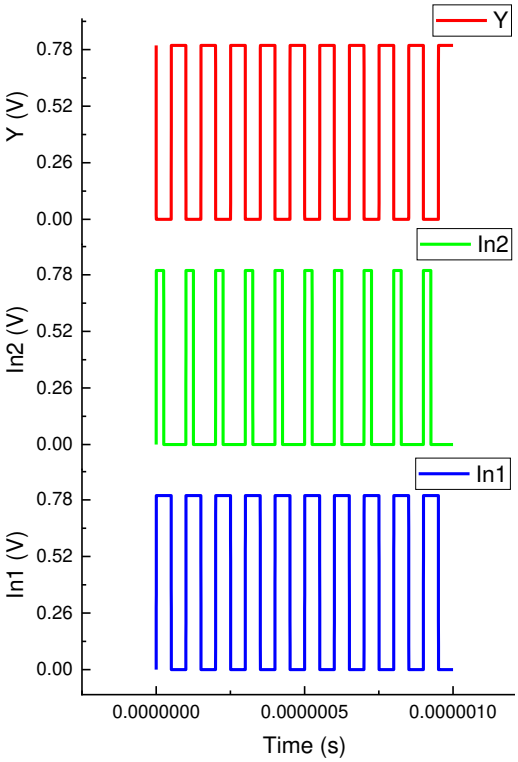

Fig. 8(b) Timing diagram of SG hetero-junction NOR logic function.

3.3. IG Hetero-junction TFET based NAND and NOR logic circuits.

In this section, the details of NAND and NOR realization using IG hetero-junction (GaSb-InAs) based TFET are given along with their corresponding timing diagram.

A. Realization of NAND logic function

The schematic of IG hetero-junction TFET based NAND is shown in Fig. 9(a). When one of the inputs of the gate is given as logic high, it establishes the channel, and the other gate limits the leakage current by isolating source and drain. In the operation of hetero-junction NAND the two gates of the PTFET are tied to each other and are given inputs V_{in1} (input voltage 1) and V_{in2} (input voltage 2) as shown in the Fig. 8(a). When both inputs are logic high, the output will be logic zero. Since the gates of the PTFET are connected to high potential the device gets turned off. While the NTFET gets turned on forming a short circuit path between output and ground. When both of the inputs are given logic low, the output will be logic high since the PTFET forms a short circuit path between supply V_{dd} and output terminal V_{out}. The timing diagram is shown in Fig. 9(b).

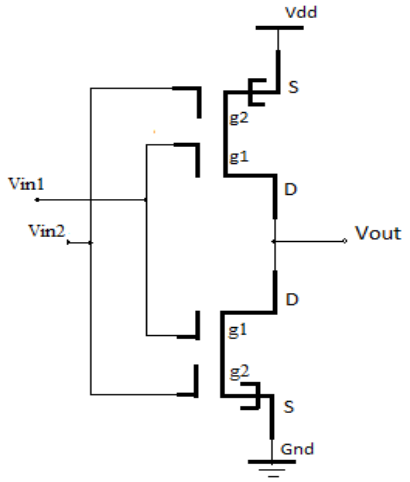

Fig. 9(a) NAND realization using IG hetero-junction TFET

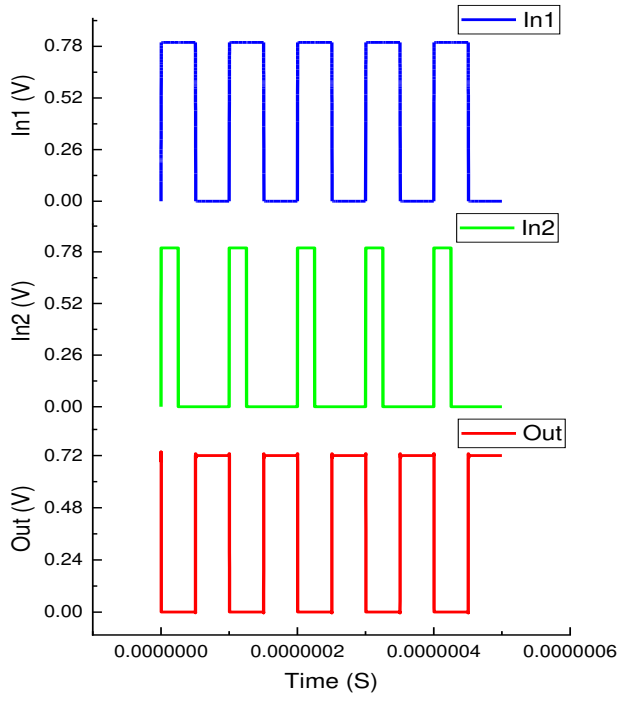

Fig. 9(b) Timing diagram of IG hetero-junction NAND logic function.

B. Realization of NOR logic function

The circuit diagram of the IG hetero-junction TFET based NOR gate is as shown in Fig. 10(a). The HNTFET present between V_{dd} and V_{out} acts as a resistor. When both inputs are logic high, the HNTFET turns on and this leads output to logic low/zero. When both inputs are logic low, the HNTFET will turn off and create a short circuit path between V_{out} and V_{dd} which results in logic high output. When either of the inputs is high, the output will be logic low or logic low/zero as one of the HNTFET gets turned on and closes the path between the supply V_{dd} and ground. The timing diagram of IG heterojunction based NOR logic function is shown in Fig. 10(b).

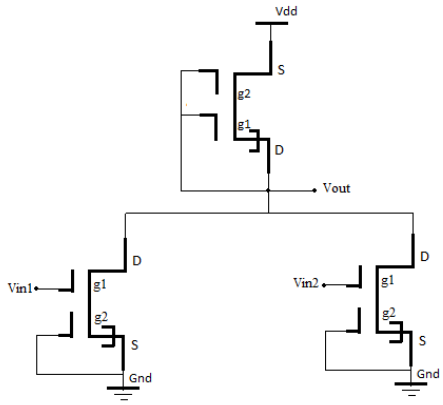

Fig. 10(a) NOR realization using IG hetero-junction TFET.

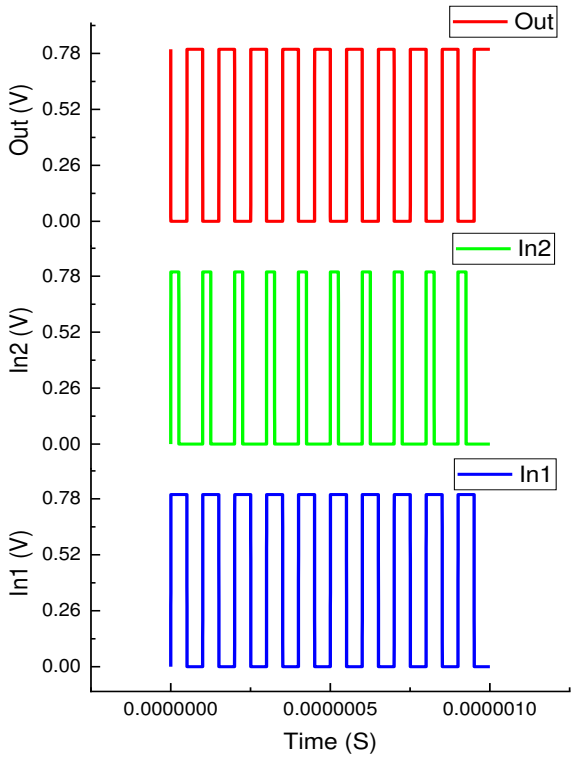

Fig. 10(b) Timing diagram of IG hetero-junction NOR logic function.

3.4. IG Hetero-junction TFET based NAND and NOR logic circuits with Pseudo-derived logic.

This section explores IG hetero-junction TFET based NAND and NOR logic circuits with Pseudo-derived logic. To reduce power consumption and delay, Pseudo-derived

logic circuits are implemented for the first time. The inverter that uses a p-channel device in pull-up has its gate grounded. The n-channel transistor in the pull-down network is given the input signal. This usage of driving the n-channel transistor with the input in pull down network is called as Pseudo logic [26]. In CMOS technology the Pseudo-NMOS logic is the provider of worst-case power consumption. But coming to the case of TFET technology, implementation of this Pseudo logic seems to be a promising logic in reducing the power consumption by making a change in its configuration. In this logic the PMOS transistor is always turned on and it is in the linear region of operation. This means that as PMOS is always on, the resistance of drain-source would be very less and so the time constant RC is low and thus enhancing the speed of operation. The same has been applied to TFET based NAND and NOR logic circuits. But this Pseudo logic has been modified in such a way that HPTFET is not permanently connected to the ground but connected to a pulsating signal which controls the pull-down network. This makes HPTFET turned on only for half cycle of the control signal.

A. Realization of NAND logic function

The schematic diagram of NAND logic function with Pseudo derived logic is shown in Fig. 11(a). The HNTFETs in pull down network are connected in series and a single HPTFET is connected to supply which controls the NAND functionality. When both inputs are logic high, HNTFETs present in the pull-down network gets turned on thus pulling the output to ground. When both inputs are logic low and the control signal is logic high, path between supply voltage V_{dd} and output terminal V_{out} gets closed and pulls V_{out} to the level of V_{dd}. When either of the input is logic high or logic low provided that the control signal is logic high, the output will be pulled down to the logic low value. In contrast to Pseudo logic, a control signal has been supplied to the PTFET in the pullup network which controls the functionality of NAND logic gate. The timing diagram is shown in Fig. 11(b).

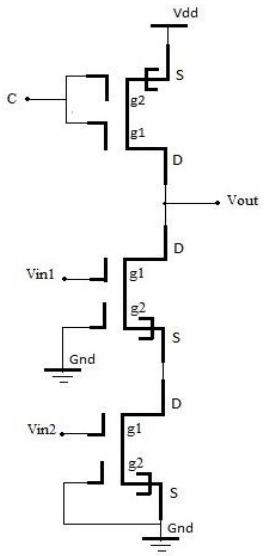

Fig. 11 (a) NAND realization using IG hetero-junction TFET with Pseudo-derived logic.

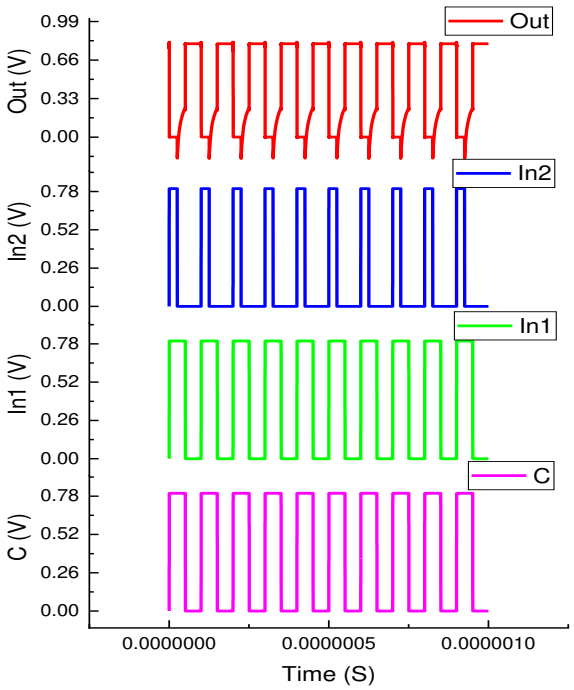

Fig. 11 (b) Timing diagram of IG hetero-junction NOR gate with Pseudo-derived logic.

B. Realization of NOR logic function

The schematic diagram of NOR logic function with Pseudo-derived logic is shown in Fig. 12(a). The HNTFETs in pull down network are connected in parallel and HPTFET is connected to supply which controls the NOR logic functionality. While connecting the circuit with Pseudo-derived logic, the HPTFET has been given a pulse voltage (the pulse input given to the HPTFET in the pull-up network is considered as control signal 'C') such that it does not turn on during the whole operation of NOR logic. When control signal is set logic low, HPTFET turns on and closes the circuit between supply V_{dd} and ground. When both inputs are logic high, irrespective of the control signal (whether it is logic low or logic high) both HNTFETs turn off and the output is pulled to ground. When both inputs are logic zero and control signal is logic low, the output goes logic high. When either of the inputs is high, and the control signal is also high, the output gets grounded. The timing diagram is shown in Fig. 12(b).

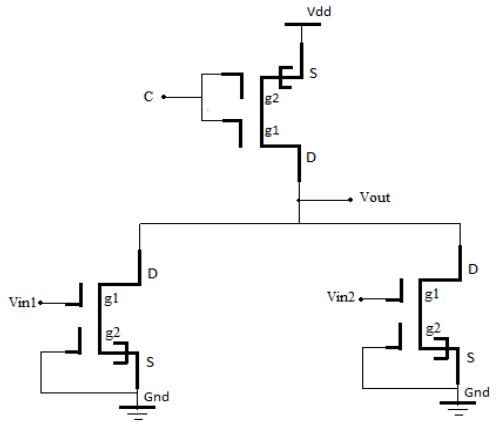

Fig. 12 (a) NOR realization using IG hetero-junction TFET with Pseudo-derived logic.

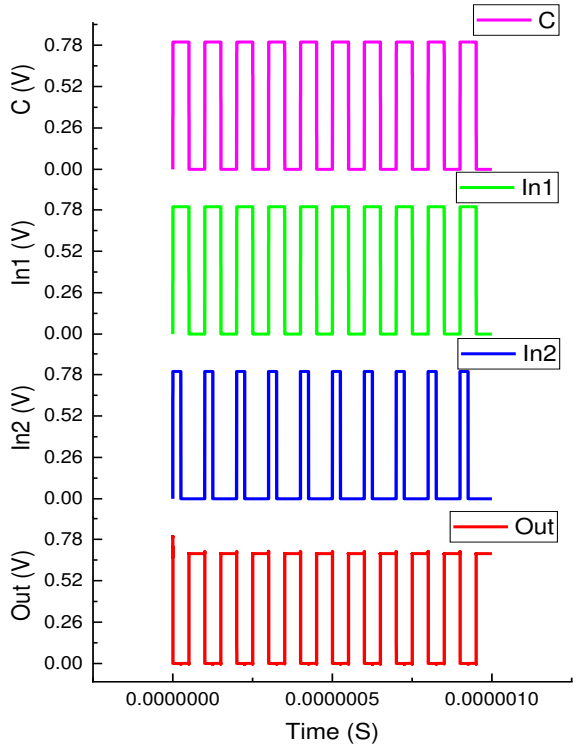

Fig. 12 (b) Timing diagram of IG hetero-junction NOR gate with Pseudo-derived logic.

3.5. Performance Summary of Logic Gates

This section deals with the overall performance comparison of all the logic gates discussed so far. The performance metrics considered here are propagation delay and power consumption. The average power and the propagation delay are measured by performing the transient analysis of logic gates, and the procedure to compute power and delay is explained in the Cadence manual [27]. Table 2 gives the performance summary of both homo and hetero-junction based NAND and NOR logic circuits.

TABLE 2 Performance Summary of Logic Gates

Logic gates	Propagation Delay	Power consumption
NAND (homo-junction TFET)	25.23 ns	79.46 pW
NAND (SG-HTFET)	17.91 ps	1.044 µW
NAND (IG-HTFET)	43.53 ps	38.02 pW
NAND with Pseudo-derived logic	95.51 ps	28.92 pW
NOR (homo-junction TFET)	132.71 ps	3.01 nW
NOR (SG-HTFET)	57.42 ns	39.17 µW
NOR (IG-HTFET)	276.19 ps	79.63 nW
NOR with Pseudo-derived logic	13.06 ps	65.31 pW

In the implementation of homo-junction TFET based NAND and NOR circuits, NAND shows less power consumption than NOR since NAND consumes power only when both inputs are logic high. In NOR circuit, except when both inputs are high, all other states consume power. In the implementation of SG hetero-junction TFET, there is less delay with the increased power consumption. This is because of the substrate being absent in double gate HTFET, which ultimately increases the power consumption.

With the implementation of IG hetero-junction TFET the two different biases applied to the gates offers better control of the channel by controlling the rate of probability of tunneling and substrate leakage current. Due to bandgap energy being lower in GaSb (0.67eV) it provides higher ON current at lower voltages. Due to the band offset being good in the GaSb-InAs hetero-junction, it leads to faster transition and lower path delay in the circuit [28]. Thus, IG HTFET gives less power consumption than SG HTFET.

Further, the performance of HTFET based NAND and NOR gates is improved by with Pseudo-derived logic. In contrast to the Pseudo logic, the HPTFET present in the pull-up network is not permanently grounded instead a control signal was given such that the PTFET is not turned on during the whole time of operation of the circuit. This gives an improved efficiency of consuming power. When the controls signal is given logic low, the supply V_{dd} is connected directly connected to V_{out} which produce logic high output.

Figure 13 (a) & (b) gives the power consumption and propagation delay of homo and hetero-junction TFET based logic gates considered in this study. All power consumption values (in pW) and delay (in ps) values are given in log scale.

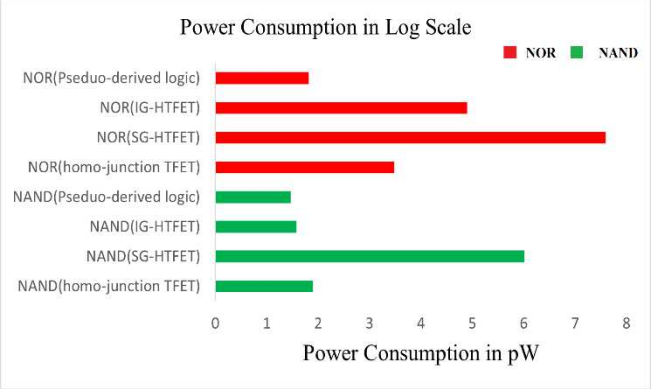

Fig. 13(a) Power Consumption of Logic Gates.

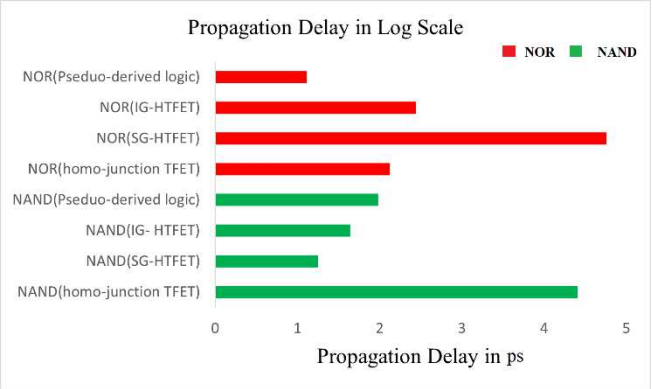

Fig. 13(b) Propagation Delay of Logic Gates.

4. Conclusion

In this study, homo and hetero-junction TFET based universal gates are designed and their performance in terms of power consumption and propagation delay is explored. Homo-junction TFET based NAND and NOR logic circuits offers higher delay/lower power consumption and lower delay/high power consumption respectively. This is because of the high band gap of homo-junction TFET which reduces probability of tunneling. By using SG HTFET, NAND logic function produced a considerable reduction in delay but increased power consumption compared to the homo-junction based NAND logic function. Using IG HTFET, both power consumption and delay are reduced because of the two gates controlling the channel current independently. To reduce delay and power consumption further, Pseudo-derived logic has been implemented for IG HTFET based NAND and NOR logic circuits. In this Pseudo-derived logic circuit HPTFET gets turned only for half cycle of the input reducing the power consumption. The hetero-junction TFET based NAND and NOR logic functions have retained their functionality till 0.28 Volts which proves better control of the channel even at smaller voltages. Hence it can be concluded that Pseudo-derived logic gates excels in performance in both delay and power consumption and thus it can be a potential candidate for ultra-low power applications.

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Figures

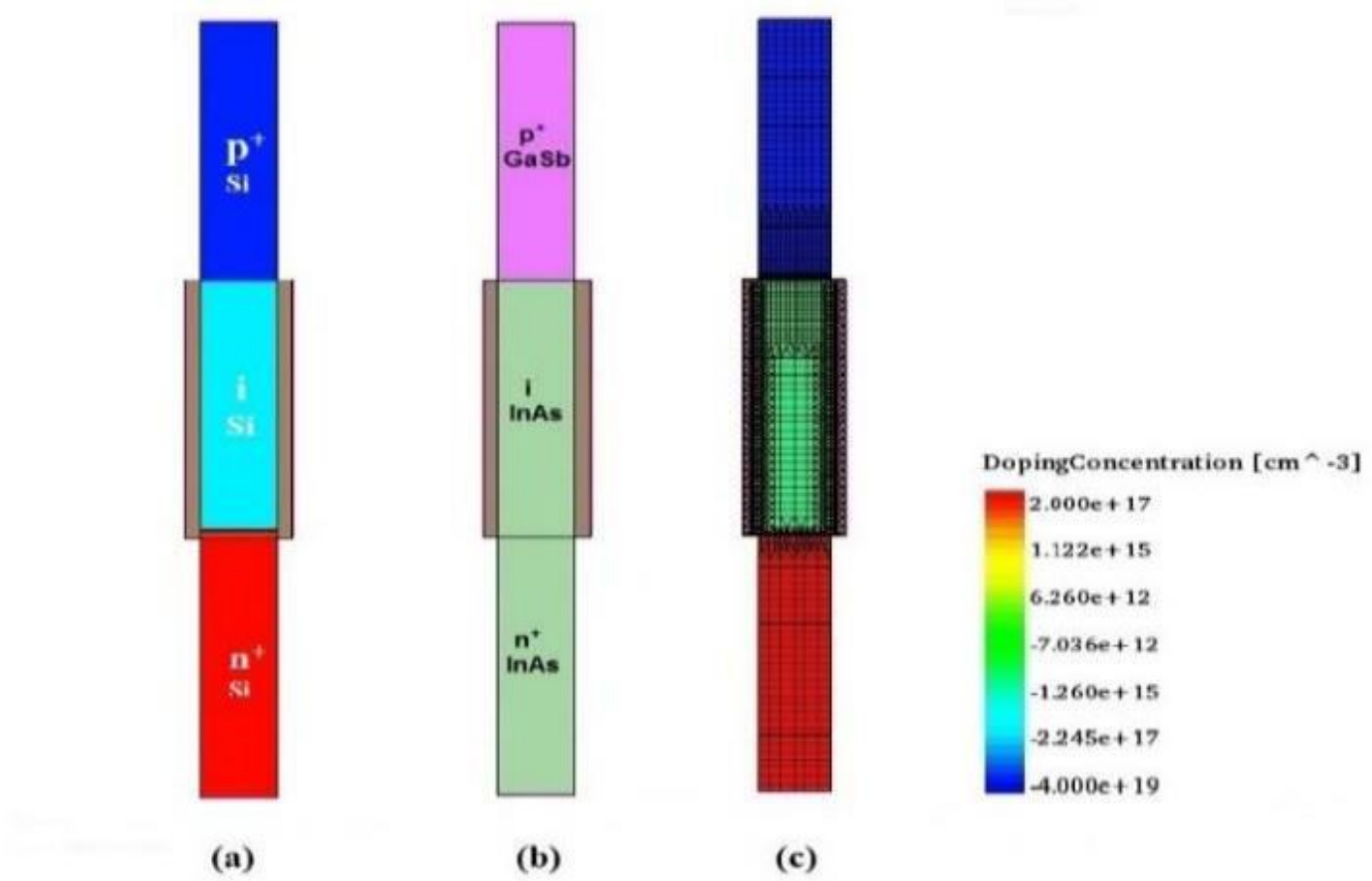


Figure 1

Simulated structure of DG TFET (a) Si TFET (b) GaSb-InAs TFET without doping (c) GaSb-InAs DG TFET with doping/meshing.

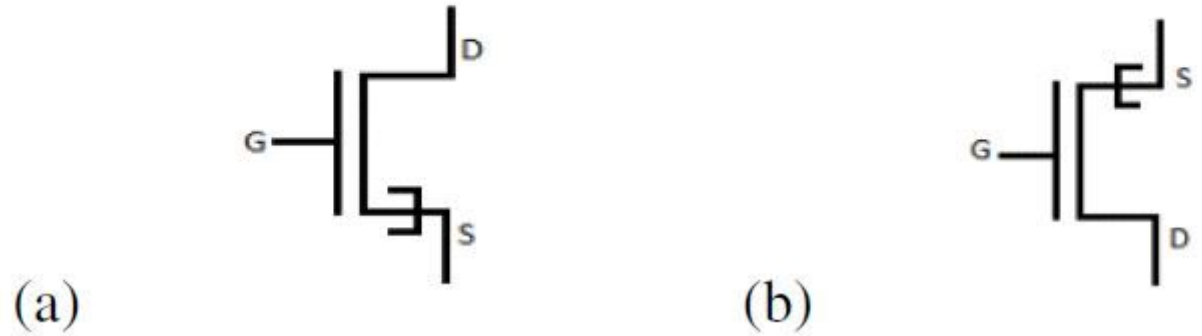


Figure 2

Symbol of homo-junction (a) NTFET and (b) PTFET

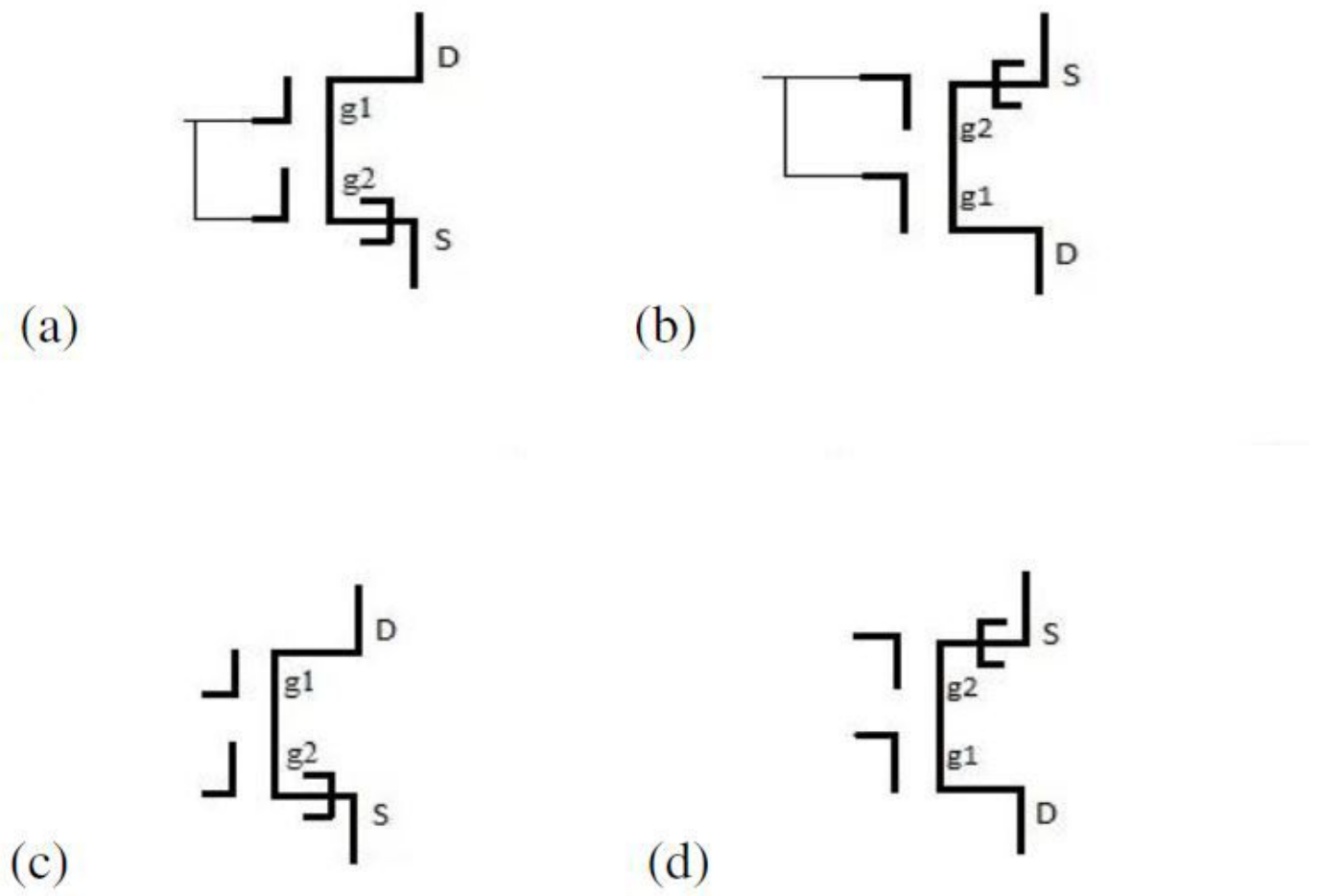


Figure 3

Symbol of shorted gate (SG) hetero-junction (a) NTFET and (b) PTFET Symbol of independent gate (IG) hetero-junction (c) NTFET and (d) PTFET

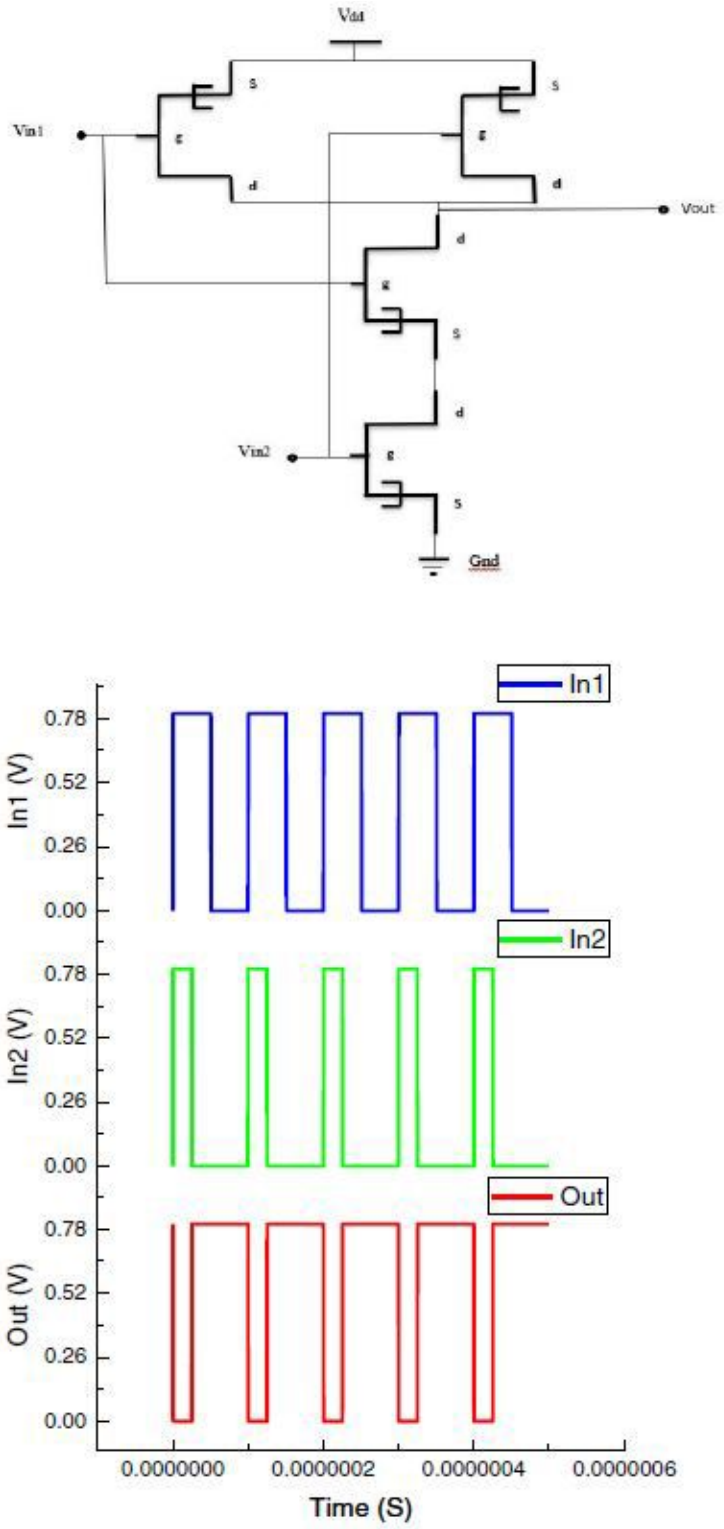


Figure 4

5(a) NAND realization using homo-junction TFET. 5(b) Timing diagram of homo-junction NAND logic function.

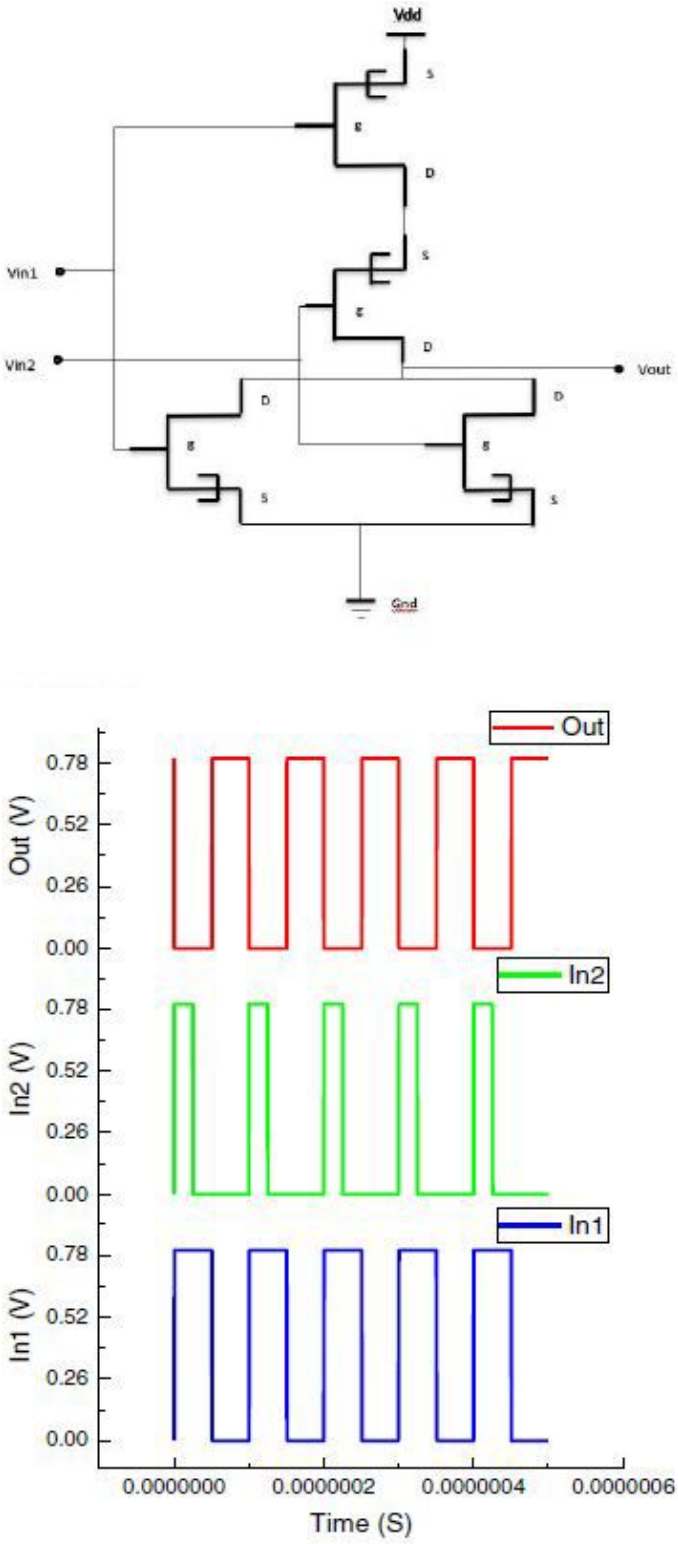


Figure 5

6(a) NOR realization using homo-junction TFET. 6(b) Timing diagram of homo-junction NOR logic function.

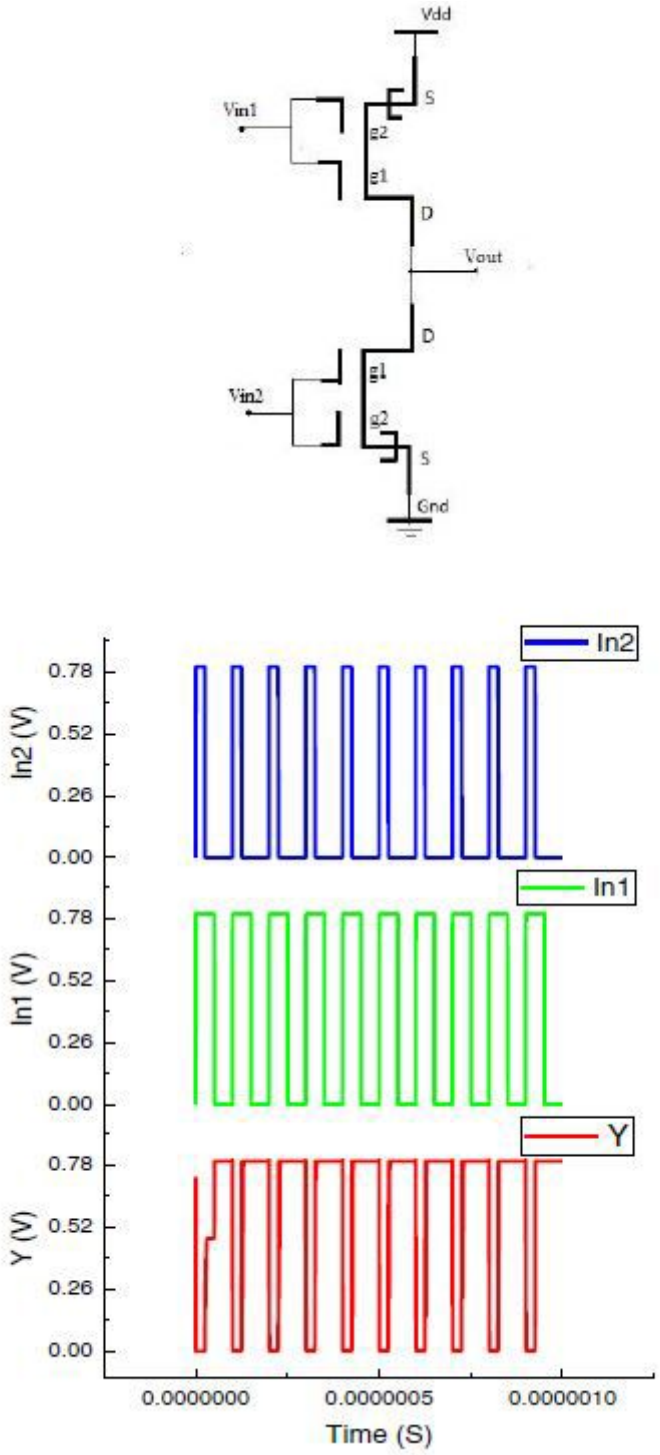


Figure 6

7(a) NAND realization using SG hetero-junction TFET. 7(b) Timing diagram of SG hetero-junction NAND logic function.

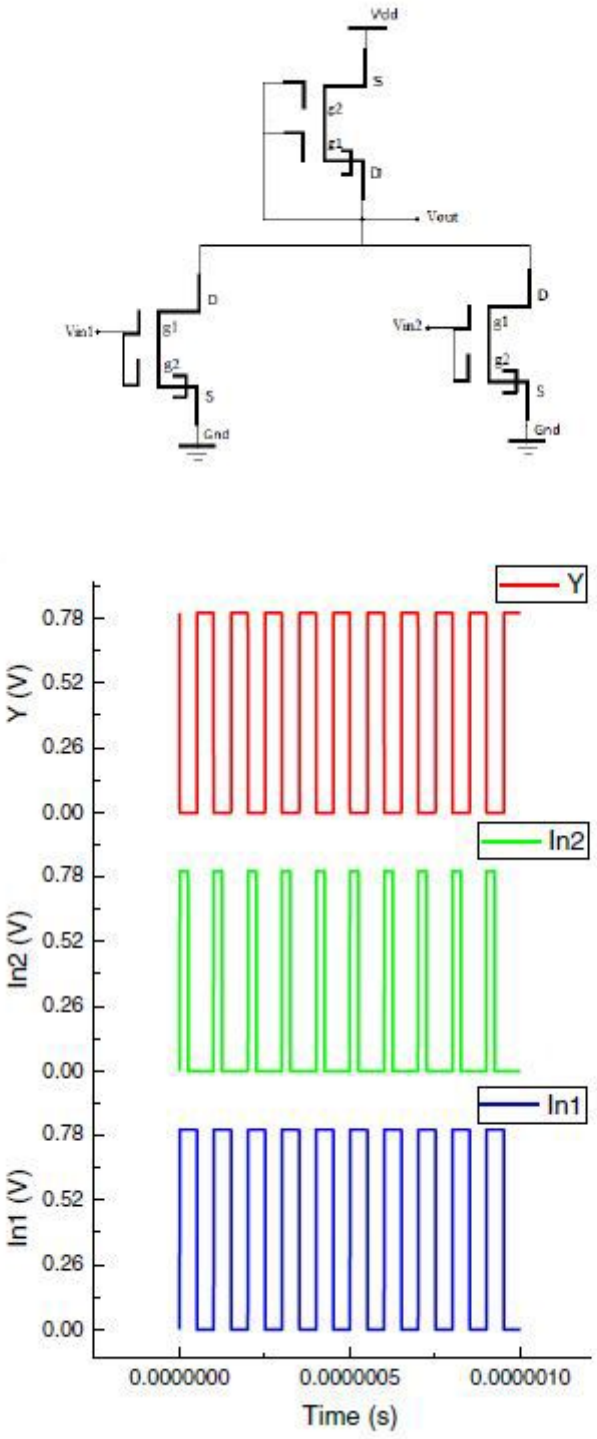


Figure 7

8(a) NOR realization using SG hetero-junction TFET. 8(b) Timing diagram of SG hetero-junction NOR logic function.

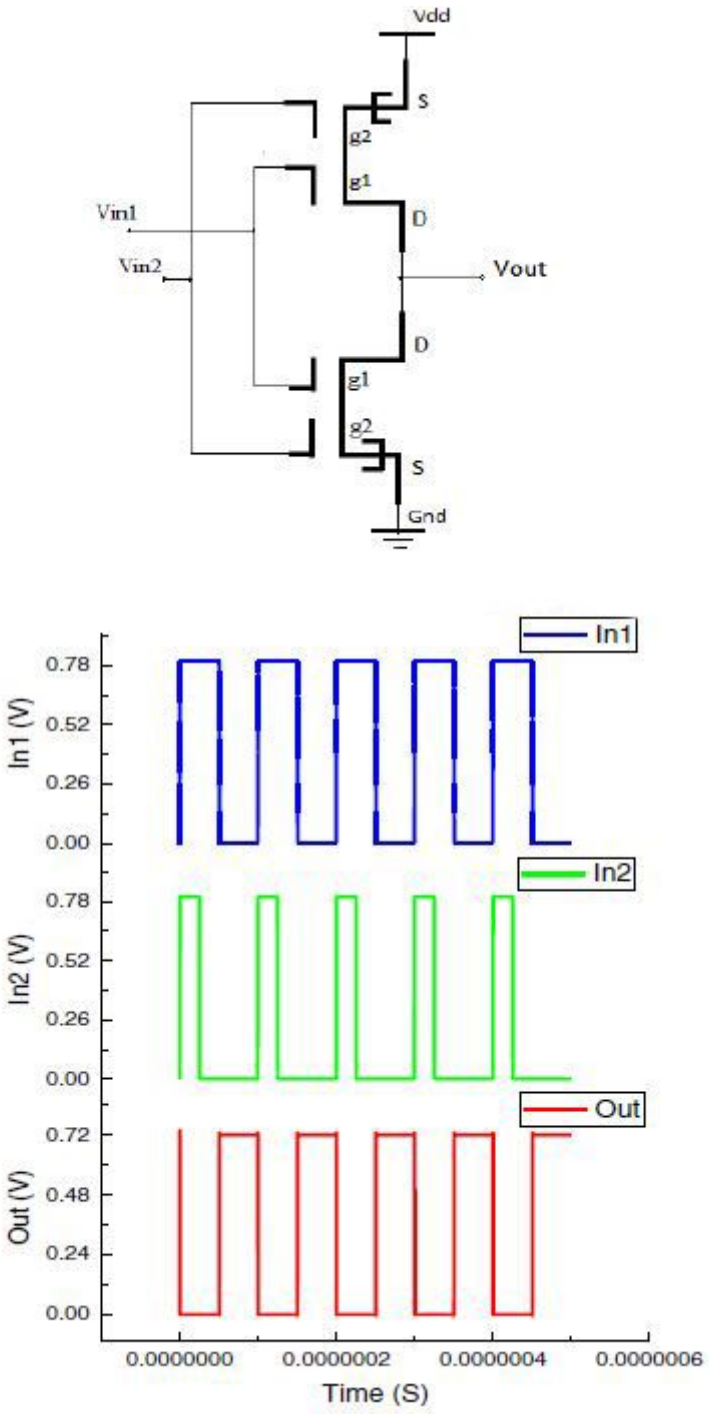


Figure 8

9(a) NAND realization using IG hetero-junction TFET 9(b) Timing diagram of IG hetero-junction NAND logic function.

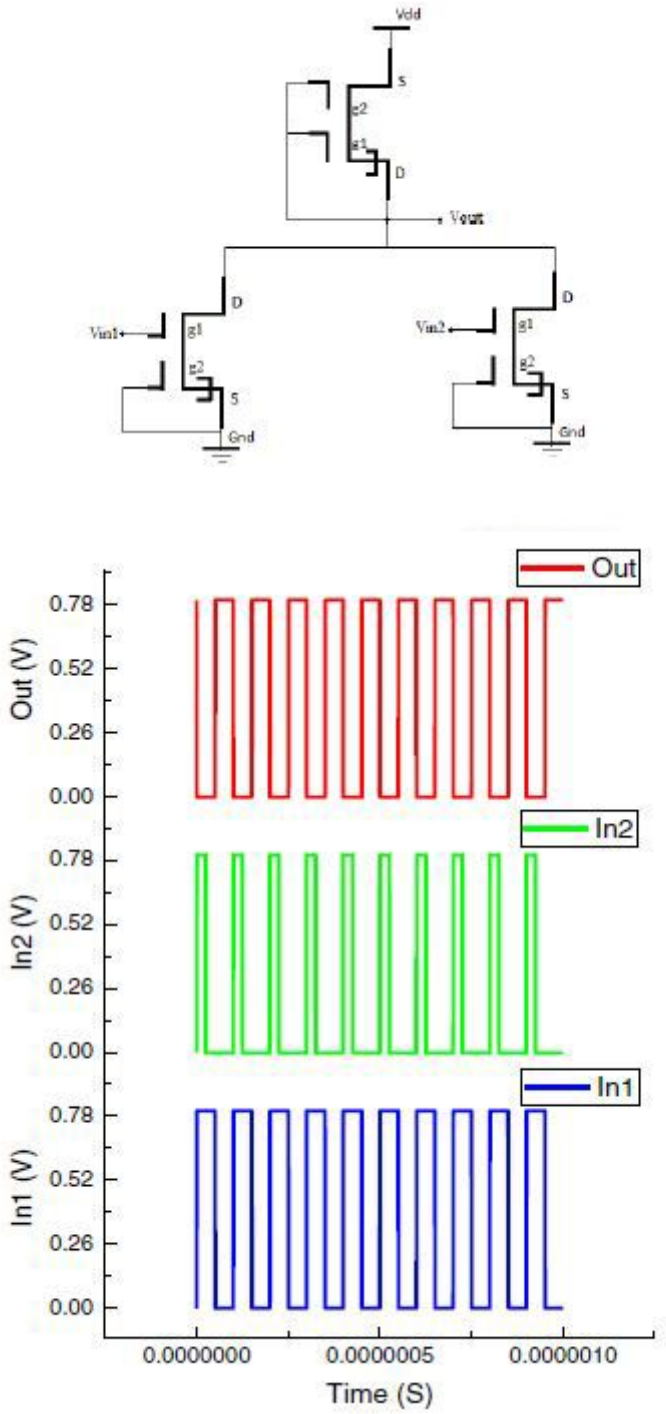


Figure 9

10(a) NOR realization using IG hetero-junction TFET. 10(b) Timing diagram of IG hetero-junction NOR logic function.

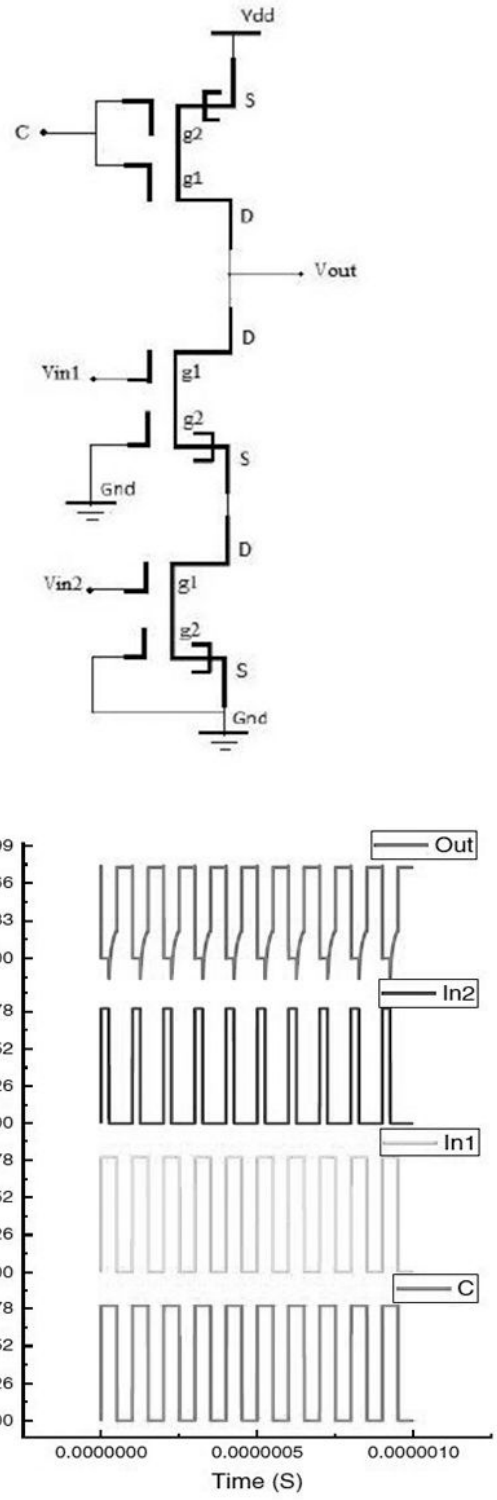


Figure 10

11 (a) NAND realization using IG hetero-junction TFET with Pseudo-derived logic. 11 (b) Timing diagram of IG hetero-junction NOR gate with Pseudo-derived logic.

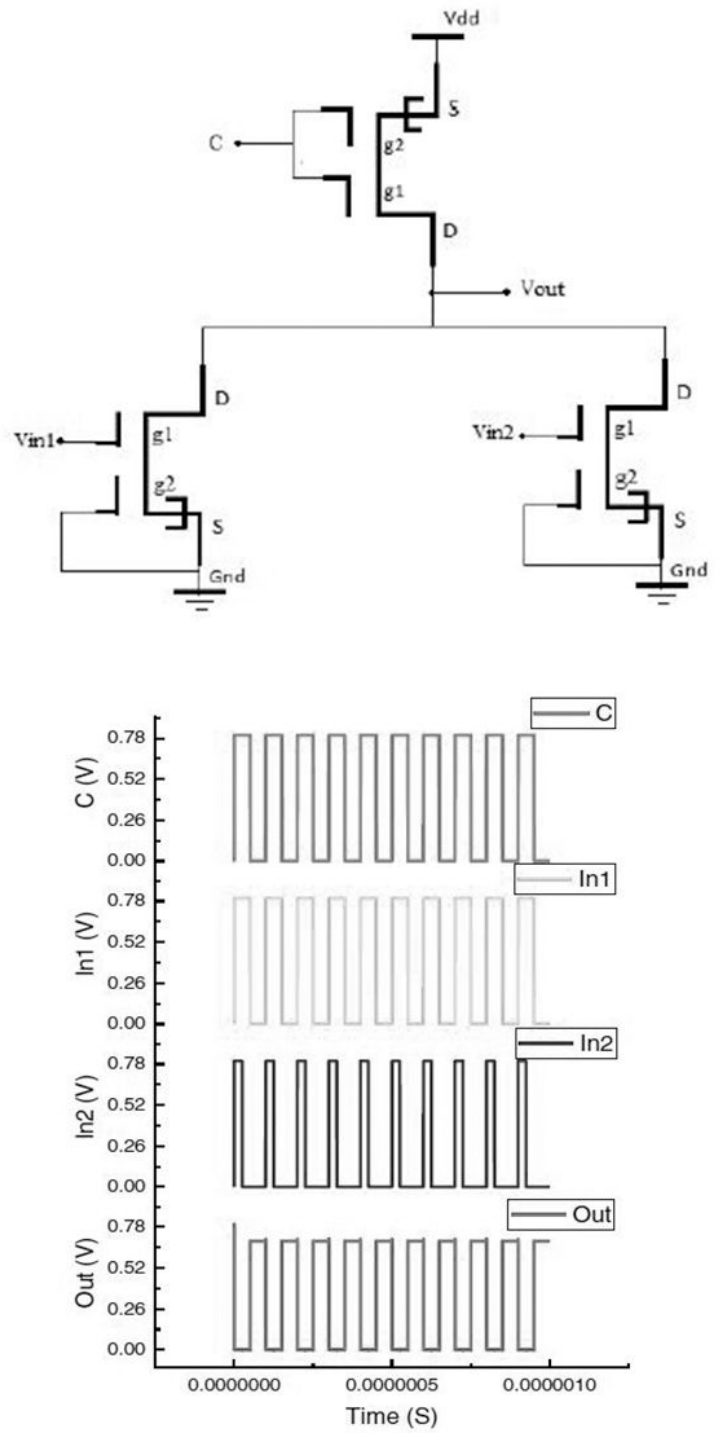
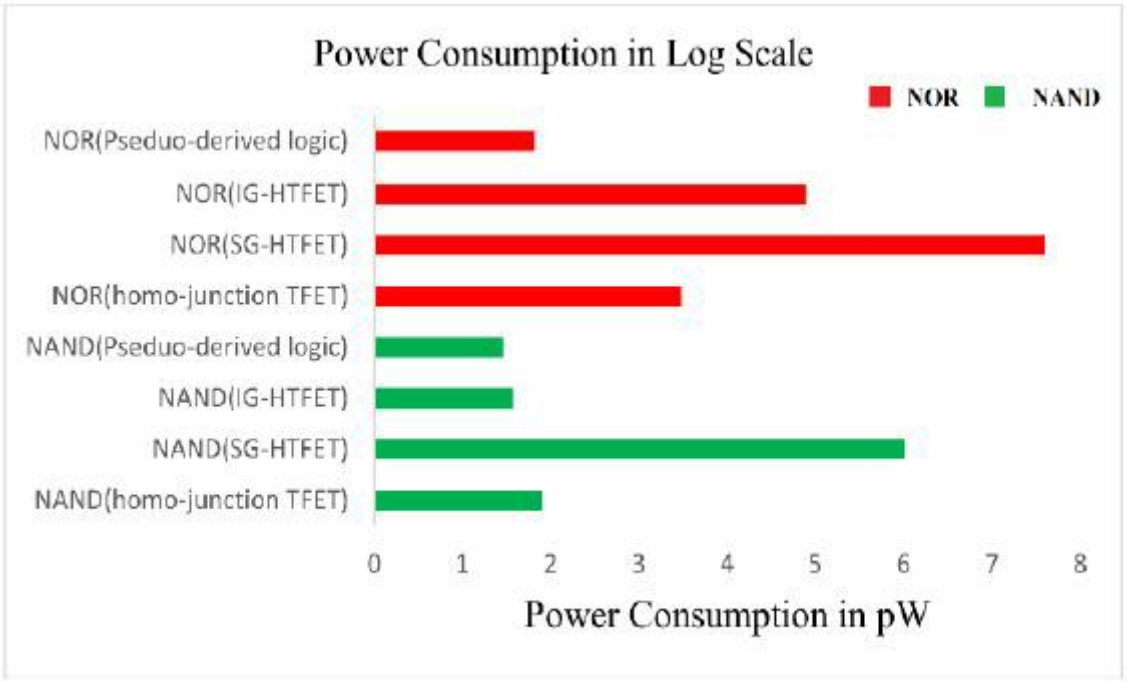


Figure 11

12 (a) NOR realization using IG hetero-junction TFET with Pseudo-derived logic. 12 (b) Timing diagram of IG hetero-junction NOR gate with Pseudo-derived logic.



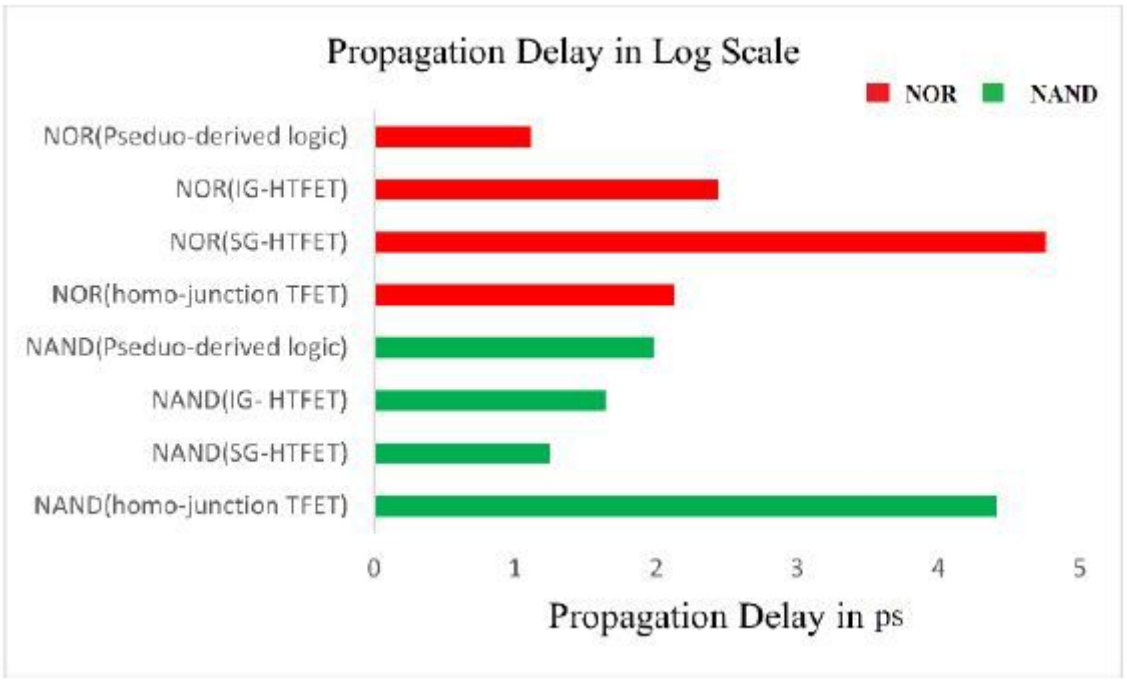


Figure 12

13(a) Power Consumption of Logic Gates. 13(b) Propagation Delay of Logic Gates.