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Kumari Nibha Priyadarshani
NIT Patna: National Institute of Technology Patna
Sangeeta Singh
NIT Patna: National Institute of Technology Patna
Kunal Singh (kunalsingh.ece@nitjsr.ac.in)
National Institute of Technology Jamshedpur

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Ultra Steep Ge-source Dopingless Tunnelling Field Effect Transistor with Enhanced Drive Current

Kumari Nibha Priyadarshani[1], Sangeeta Singh[1], Kunal Singh[2]

[1]Microelectronics & VLSI Design Lab,
National Institute of Technology Patna, India
[2]National Institute of Technology Jamshedpur, India
E-mail: vnskunalsingh@gmail.com

Abstract. Ge-source dopingless tunnelling field effect transistor (Ge-source DLTFET) with the optimization of dielectric oxide thickness under the source and the gate contacts is proposed and investigated by calibrated 2D TCAD device simulation. As the structure is realized using dopingless technique, this enables lower thermal budget, higher immunity towards the random dopant fluctuations (RDFs) effects and velocity degradation effects. The optimization of dielectric thickness has been done to tune the carrier concentrations induced in source and channel regions in order to improve the device performance. The drive current is magnificently enhanced along with I_{ON}/I_{OFF} ratio, peak transconductance and ultra-steep subthreshold slope (SS) is reported for the optimized Si-DLTFET. In addition to this by deploying Ge-source instead of Si source in optimized Si-DLTFET increases ON current slightly and OFF current gets reduced by the order of two as compared to the optimized Si-DLTFET. This improves the I_{ON}/I_{OFF} ratio,the reported drive current for Ge-source DLTFET is 5.1×10^{-4} A/µm, along with I_{ON}/I_{OFF} ratio as 1.54×10^{13}, peak transconductance as 1.26 mS/µm and ultra-steep SS as 1.69 mV/decade. Further, the analog, RF and linearity performance parameters have also been investigated for both the structures and demonstrated notable improvement. The energy efficiency investigationreveals a significant reduction in energy-delay product. This paper indicates thepotentials of optimized Si-DLTFET and Ge-source DLTFET as promising candidates for low power analog and RF applications and Ge-source DLTFET hasbetter device dc performance.

Keywords: Tunnel FET, Optimization, Steep switching, Germanium, high drive.

1 Introduction

Scaling of conventional MOSFET to nano-dimensions helps to achieve better device performance, minimized cost, reduced area, increased drive current and

improved high-frequency response [1, 2]. At the same time, it also leads to some unacceptable drawbacks such as an exponential increase in leakage current, subthreshold slope (SS) is limited to 60 mV/decade and short channel effects (SCEs) [3-6]. This hinders the device applicability in CMOS circuits. Thus, to overcome these problems quantum tunnelling field effect transistor (TFET) works on the principle ofband to band tunnelling unlike drift-diffusion governed current in MOSFET. HenceTFET is emerging as a better alternative to the conventional FET [7-9,36]. TFETcircumvents SS limitation of 60 mV/decade [10], demonstrates lower leakage current,higher immunity towards the SCEs. However, its drive current is also low. Thus,many approaches have been reported to increase the ON current such as dual gate TFET, dopingless TFET, high-k dielectrics, n+ pockets doped TFET, and so on[8-11]. In the meantime, dopingless tunnel field effect transistor (DLTFET) hasbeen reported with an ease of fabrication process as compared to physically dopedTFET because there is no need of expensive diffusion or ion implantation process to realize the ultra-sharp doping profile for source and drain in nanoscale[12-15,33]. In DLTFET, source and drain regions are formed by charge plasmaconcept with the help of suitable electrode work functions i.e. $\varphi_{m,p^+} > \chi_s + E_g/2$and $\varphi_{m,n^+} < \chi_s - E_g/2$, where, χ_s is the electron affinity of bulk semiconductor, E_g is energy band gap of semiconductor whereas, $\varphi_{m,n^+}$and $\varphi_{m,p^+}$are theworkfunction of metals needed to induce n+ doping and p+ doping, respectively[15]. The problem of random dopant fluctuations (RDFs) because of the physicaldoping in conventional TFET, which leads to degradation in the device performance is also eradicated with the concept of plasma doping [16, 17]. Further, it also reduces the bulk trap assisted tunnelling (TAT) induced degradation in subthresholdcharacteristic in comparison to conventional TFET. The charge plasma conceptthas been applied to Si-DLTFET [22] and the base Si device structure in [18].The device structure reported in [22] demonstrated a relatively higher averagesubthreshold slope (SS) of device ~100 mV/decade with supply voltage as 1 V.However, for the basic structure reported in [18] is Si DL-TFET demonstrated average SS as ~ 84.4 mV/decade at a supply voltage of 0.5 V. Further,the authors [18] have used $In_{0.75}Ga_{0.25}N$ and gate engineering for improvementof device performance. The fabrication of InGaN with fixed concentration can bechallenging. Moreover, as the TFET is adopted because of its potential as an ultra-low power device, and power dissipation is minimized by scaling supply voltage.The base silicon [18] Si DL-TFET gives better SS in comparison to [22] at lowersupply voltage. Therefore, the authors in this paper have reproduced the results ofbasic structure [18] i.e. Si-DLTFET for further device performance improvement.Here, considering the base device structure Si-DLTFET of [18] in the presentmanuscript, the optimization of dielectric thickness under both source and gateelectrodes has been carried out here. This optimization of dielectric oxide thickness under source enhances drive current by the order of six and leakage currentalso increases slightly. Moreover, the Ge-source is also deployed in the optimizedSi-DLTFET, this reduces leakage current with retained drive current performance.Here, it is expected that the

considered dopingless realization of the structure alsodemonstrates an inherent advantage of lower thermal budget and tolerance against the velocity degradation effects.

The organization of paper is as follows. Section2 consists of Si-DLTFET, optimized Si-DLTFET and Ge-source DLTFET devicestructures along with design parameters and simulation models. Section 3 coversthe comparative analysis of Si-DLTFET and proposed devices, namely, optimizedSi-DLTFET and Ge-source DLTFET. Section 4 discusses the analysis of effect oftemperature on the proposed structure. Section 5 discusses analog, RF and linearity performance parameters of both the considered device structures. Section 6 containsthe energy efficiency analysis of the proposed structures. Section 7 provides the process flow for fabrication of the proposed device structure. Finally, Section 8concludes our study.

2 Devıce structure and sımulatıon parameters

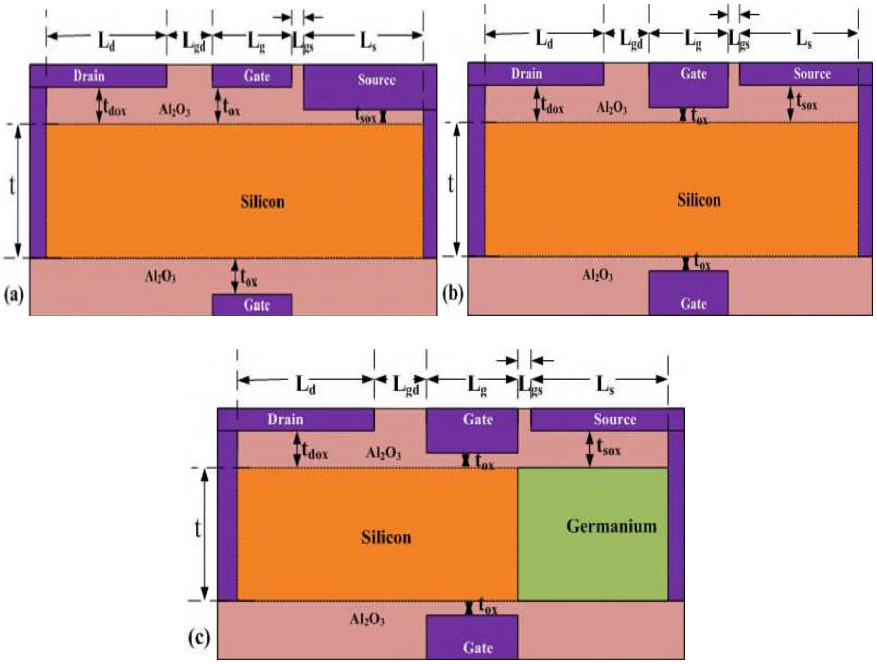


Fig. 1.2D device structure of (a) base silicon structure (Si-DLTFET) [18], (b) optimized Si-DLTFET and (c) Ge-source DLTFET.

2D structure of Si-DLTFET base structure of [18], optimized Si-DLTFET and Ge-source DLTFET have been shown in Fig. 1(a), (b) and (c), respectively. Uniformplasma-induced carrier concentration can be maintained for film thickness

less thandebye length [19-24] (L_D), i.e.$L_D = ((\varepsilon V_T)/qN)^{1/2}$, where, $\varepsilon$is the dielectricconstant of the body material (Si or Ge), V_T is the thermal voltage, and N is thecarrier concentration in the body. Hence, the film thickness has been consideredas 10 nm. Drain and source electrodes have been selected such that it forms n^+plasma drain and p^+ plasma source, respectively. Thereby realizing the n-TFETwithout actual metallurgical doping. For this, the work-function of drain metalis taken as 3.9 eV and for source metal it is taken as 5.93 eV. Suitable sourcemetal can be Pt [25] and drain metal can be Mo [26] highly doped with nitrogenimplant or Hf [25]. The lateral gap between gate and source electrode is 2 nm [18,32] and the lateral gap between gate and drain electrode is 15 nm [18], which ismost suitable for minimum ambipolar current. The oxide taken is Al_2O_3 (ε_r =9.3)as in [18]. The other parameters for device design are listed in Table 1.

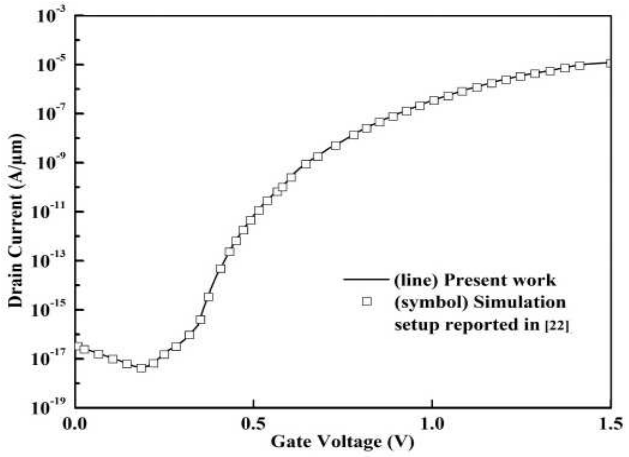


Fig. 2. Calibration of proposed simulation framework with [22]. I_D-V_{GS} characteristics of DLTFET at V_{DS} = 1.0 V.

The device structure simulation has been carried out using 2-D Silvaco AtlasDevice Simulator [28]. It solves Poisson's equation self-consistently with the carriercurrent continuity equation. To consider the effect of structural fluctuation ofenergy band and to model the tunnelling process more precise non-local band to band tunnelling (non-local BTBT) model is considered for simulations. At thesource-channel and drain-channel region quantum tunnelling regions are definedin order to enable forward and reverse tunnelling. Trap assisted tunnelling (TAT)which is dominant in OFF state and ambipolar state has also been considered.The Shockley-Read Hall (SRH) and Auger recombination models are consideredto model the effect of carrier recombination. Concentration dependent mobility(conmob) and field dependent mobility (fldmob) are also considered. The material
and model parameters are listed in Table 2. In order to calibrate and validate oursimulation framework deployed here is at first exhaustively calibrated against data

as reported in [22] as shown in Fig. 2. As the transfer characteristic of two cases are coinciding, it clearly validates simulation framework deployed. Moreover, asthe film thickness of device is 10 nm thus the quantum mechanical effect is notconsidered. Here authors have re-implemented the base Si structure of [18] andoptimized its performance by optimizing the oxide thickness under source and gateand then finally, Ge-source is incorporated in the optimized structure.

Table 1. Parameters used for device structure simulations.

Device Parameters	Si-DLTFET [18]	Optimized Si-DLTFET	Ge-source DLTFET
Body thickness, t (nm)	10	10	10
Gate length, L_g (nm)	50	50	50
Source length, L_s (nm)	100	100	100
Drain length, L_d (nm)	100	100	100
Drain-gate space, L_{dg} (nm)	15	15	15
Source-gate space, L_{gs} (nm)	2	2	2
Gate workfunction, φ_g(eV)	4.5	4.5	4.5
Drain workfunction, φ_d(eV)	3.9	3.9	3.9
Source workfunction, φ_s(eV)	5.93	5.93	5.93
Gate oxide thickness, t_{ox} (nm)	3	1	1
Oxide thickness under the source contact, t_{sox} (nm)	1.2	3	3
Oxide thickness under the drain contact, t_{dox} (nm)	3	3	3

Table 2. Model/Material parameter for device simulation.

Model/Material Parameter	Silicon	Germanium
E_g(eV)	1.08	0.663
χ(eV)	4.17	4
ε	11.8	16
$n_i(cm^{-3})$	1.45×10^{10}	1.73×10^{13}
mass.tunnel	0.25	0.25
m_e.tunnel	0.322	0.216
m_h.tunnel	0.549	0.33

3 RESULTS AND DISCUSSION

3.1 Device performance comparison for different oxide thicknesses under source contact (t_{sox})

In order to accurately compare the effect of oxide thickness under source contact(t_{sox}), the I_D-V_{GS} characteristics of the device (with t_{ox} = 3 nm and t_{dox} = 3

nm)with variation in t_{sox} has been shown in Fig. 3(a). It is observed that with an increase in t_{sox}, leakage current is continuously decreasing. As a remarkable decreasein leakage current is observed around the gate potential of 0.25 V,

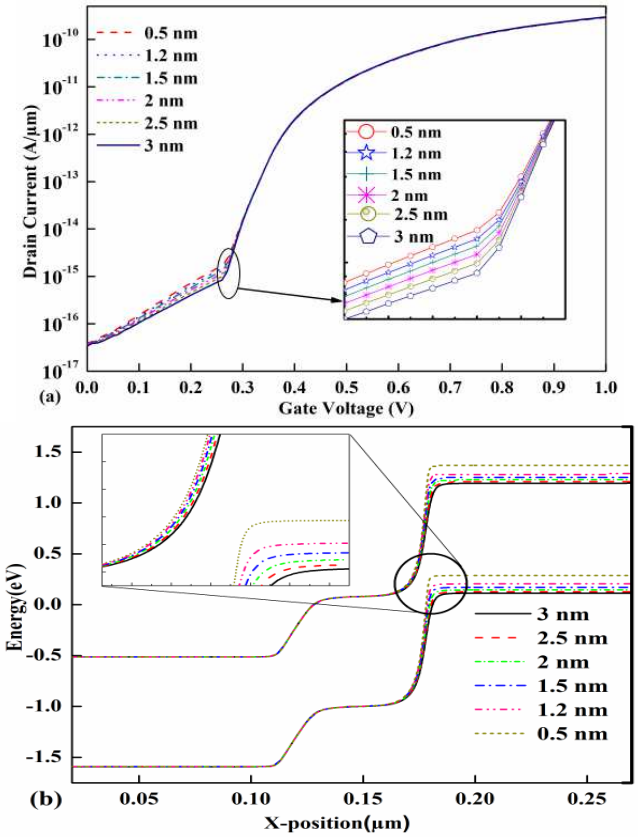


Fig. 3. (a) Transfer characteristic of Si-DLTFET for different oxide thickness under source contact at V_D = 0.5 V and (b) Energy band diagram of Si-DLTFET for change in oxide thickness under source at V_G = 0.25 V, V_D = 0.5 V.

which can be inferred from the energy band diagram for the device at 0.25 V with variation in oxide thickness under source contact shown in Fig. 3(b). It can be observed from the energy band diagram that with an increase in t_{sox} the conduction band and valance band energy levels in source region are shifting downwards.
Thus, it canbe inferred that lesser electron plasma is induced with increasing oxide thicknessbetween the metal and semiconductor. This shifts the source side energy levelsdownwards that leads to decrease in effective tunnelling energy, thus it decreasesthe leakage current. Hence, the device with 3 nm t_{sox} is illustrating better performance as compared to other t_{sox}. The variation of parameters with the change int$_{sox}$ has been shown in Table 3. It can be observedfrom the table that with anincrease in t_{sox}, V_{TH} has been reduced, I_{ON}/I_{OFF} is increased and SS has

beenreduced.

Table 3. Variation of parameters with oxide thickness variations under the source contact for Si-DLTFET (t_{sox}).

	V_{TH} (V)	I_{ON} (μA/μm)	I_{OFF} (fA/μm)	I_{ON}/I_{OFF}	g_m (mS/μm)	SS (mV/ decade)
3 nm	0.618868	0.000297	0.033964	8.75×10^{6}	7.80×10^{-7}	27
2.5 nm	0.619315	0.000295	0.034898	8.47×10^{6}	7.76×10^{-7}	28
2 nm	0.619305	0.000294	0.035683	8.23×10^{6}	7.72×10^{-7}	29
1.5 nm	0.620047	0.000292	0.036911	7.92×10^{6}	7.69×10^{-7}	30
1.2 nm	0.620502	0.000291	0.037290	7.80×10^{6}	7.66×10^{-7}	31.4
0.5 nm	0.620999	0.000289	0.039263	7.36×10^{6}	7.63×10^{-7}	33

3.2 Device performance comparison for different gate oxide thicknesses (t_{ox})

Gate oxide acts as a dielectric layer that sustains very high electric field in order to tune the conductance of the channel. The decrease in gate oxide thickness (t_{ox}) leads to a decrease in the distance between the gate metal and semiconductor (body of device). This decrease in distance results in higher induced plasma doping in gate region thus an increase in output/drain current. Fig. 4(a) shows the electron concentration (at V_D = 0.5V and V_G = 0.5V (ON state)) increases with a decrease in gate oxide thickness. But the electron concentration also increases with a decrease in tox in OFF state as shown in Fig. 4(a). It can be observed from the plot that the increase in electron concentration is higher for ON state as compared to OFF state. Hence, the ratio of increase in ON state current (1.739×10^{6} times) is higher than the ratio of increase in OFF state current (36.8 times) as shown in Fig. 4(b) Thus it leads to an increase in ION as well as I_{ON}/I_{OFF} ratio. The change in parameters with change in tox such as threshold voltage, I_{ON}, I_{OFF}, $I_{ON}/I_{OFF,}$ transconductance and SS are shown in Table 4. The SS has reached to 2.32 mV/decade for gate oxide thickness 1 nm from 27 mV/decade for gate oxide thickness 3 nm.

Table 4. Variation of parameters with variation in gate oxide thickness for Si-DLTFET with t_{sox} as 3 nm.

	V_{TH} (V)	I_{ON} (μA/μm)	I_{OFF} (fA/μm)	I_{ON}/I_{OFF}	g_m (mS/μm)	SS (mV/ decade)
3 nm	0.619	0.000297	0.033964	8.75×10^{6}	7.80×10^{-7}	27
2.5 nm	0.589	0.00549	0.049	1.12×10^{8}	1.34×10^{-5}	14.5
2 nm	0.563	0.182	0.0893	2.03×10^{9}	4.16×10^{-4}	5.98
1.5 nm	0.546	13.7	0.252	$5{:}42 \times 10^{10}$	0.0312	3.22
1.2 nm	0.529	239	0.6	$3{:}98 \times 10^{11}$	0.576	2.17
1 nm	0.504	506	1.25	4.05×10^{11}	1.26	2.32

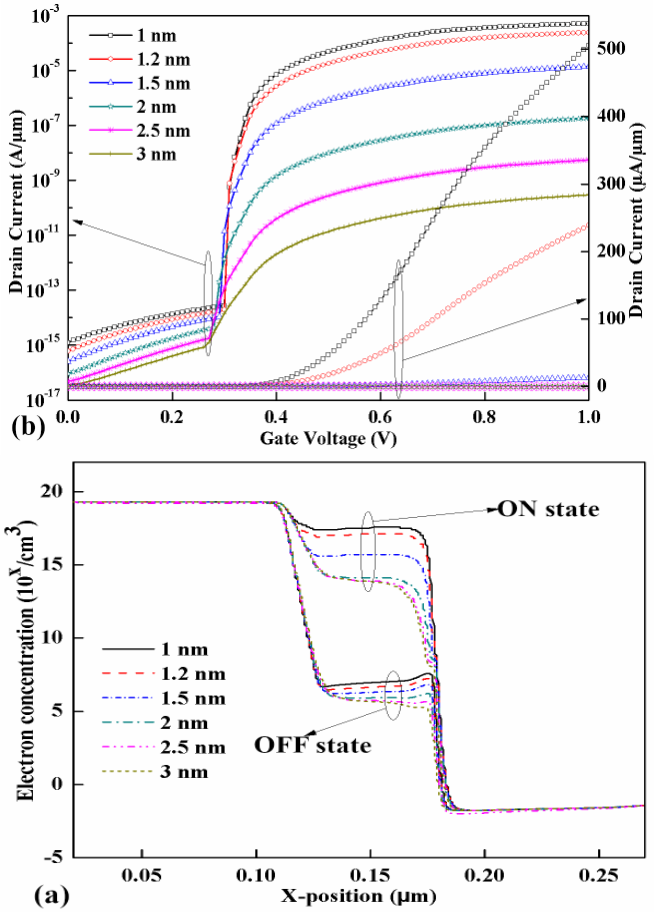


Fig. 4. (a) Electron concentration in ON state (V_D = 0.5 V and V_G = 0.5 V) and in OFF state (V_D = 0.5 V and V_G = 0 V) and (b) Transfer characteristic at V_D = 0.5 V for Si-DLTFET for variation in t_{ox} with t_{sox} as 3 nm.

3.3 Comparison Between Si-DLTFET, Optimized Si-DLTFET and Ge-source DLTFET.

For comparison between Si-DLTFET (base structure of) [18], optimized Si-DLTFET,and Ge-source DLTFET energy band diagram of all three structures at thermalequilibrium and ON state has been shown in Fig. 5(a) and (b) respectively. Thedrain current versus gate voltage plot has been shown in Fig. 6(a). The ON statecurrent for Ge-source DLTFET as well as optimized Si-DLTFET is in the rangeof mA/μm whereas the ON state current for Si-DLTFET [18] is in 10^{-10} A/μm.This difference in ON current can be inferred from ON state electron concentration in the structures shown in Fig. 7(a). It is very clear from the plot that

theincreased electron concentration in gate region for optimized Si-DLTFET and Ge-source DLTFET in comparison to Si-DLTFET is the reason behind the increasedON current. The increase in ON current is 10^6 times of Si-DLTFET.

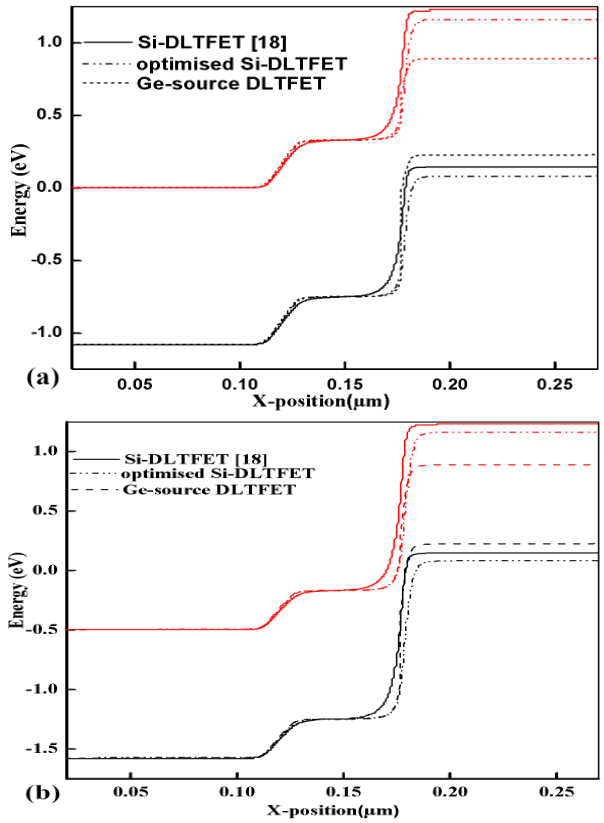


Fig. 5. Energy band diagram of Si-DLTFET [18], optimized Si-DLTFET, Ge-source DLTFET at (a) Thermal equilibrium and (b) ON state V_G = 0.5 V and V_D = 0.5 V.

Also, the OFF state current in Fig. 6(a) is in the range of 10^{-17} A/μm forSi-DLTFET [18] and Ge-Source DLTFET whereas it is in range of 10^{-15} A/μmfor optimized Si-DLTFET. This difference in OFF state current can be well understood by the electron concentration in OFF state is shown in Fig. 7(a). Theincreased electron concentration in gate region for optimized Si-DLTFET is responsible for higher leakage in OFF state. The decrease in electron concentrationin gate region for Ge-source DLTFET is the reason for the decreasein leakagecurrent in OFF state. Moreover, the band gap of germanium is less than the siliconand in off state of device potential barrier between channel and source for case ofGe-DLTFET is more as compared to the optimized Si-DLTFET, therefore lesser e-would be able to cross this potential barrier in Ge-DLTFET. The decrease in gateoxide thickness for optimized Si-DLTFET has led to increase in leakage current,which has been compensated by the use of Ge-source. Also, the

transition from OFF to ON is steeper for Ge-source DLTFET asSS is 1.69 mV/decade similar to reported in our earlier published literature [29].

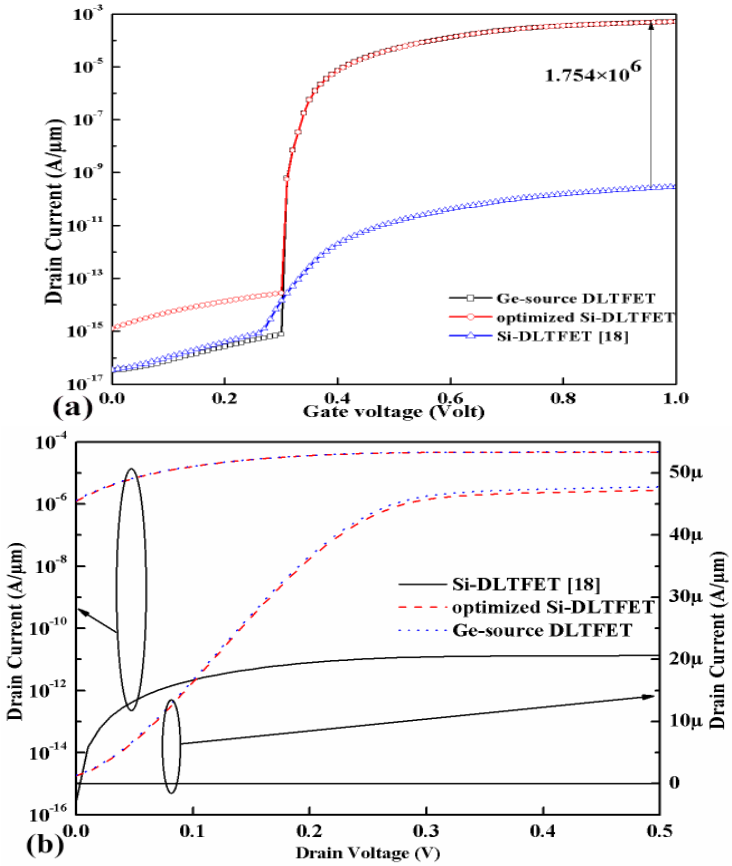


Fig. 6. (a) Transfer characteristic of Si-DLTFET [18], optimized Si-DLTFET and Ge-sourceDLTFET at V_D = 0.5 V and (b) Output characteristic of Si-DLTFET [18], optimized Si-DLTFET and Ge-source DLTFET at V_G = 0.5 V.

The drain current v/s drain voltage has been compared in Fig. 6(b). The maximum drain current for both optimized Si-DLTFET and Ge-source TFET is inthe range of 10^{-5} A/μm and for Si-DLTFET it is in the range of 10^{-12} A/μm.Approximately 10^7 times higher drive current has been achieved as compared toSi-DLTFET. The change in parameters such as threshold voltage, I_{ON}, I_{OFF},I_{ON}/I_{OFF}, transconductance and SS for base structure of Si-DLTFET [18], optimized Si-DLTFET and Ge-source DLTFET and for DLTFET [22] are shown in-Table 5. The Ge-source TFET shows improved device performance in comparisonto Si-DLTFET [18]. Further, Ge-source TFET also reports improvement in

device performance parameters when compared to DLTFET [22](@1V) even at 0.5V supply voltage only. Thus, the reported device structure ensures better performance at ultra-low power applications. Also, the maximum transconductance andSS for these structures have been shown in Fig. 7(b), here very steep SS as well aspeak transconductance has been found for Ge-Source DLTFET (SS = 1.69 mV/decade; g_m = 1.26 mS/µm).Fig. 7(b) shows the I_{ON}/ I_{OFF} ratio for change in oxide thickness and Ge-source DLTFET, the ratio has increased continuously with a decrease in oxidethickness and it is found to be maximum for Ge-source DLTFET.

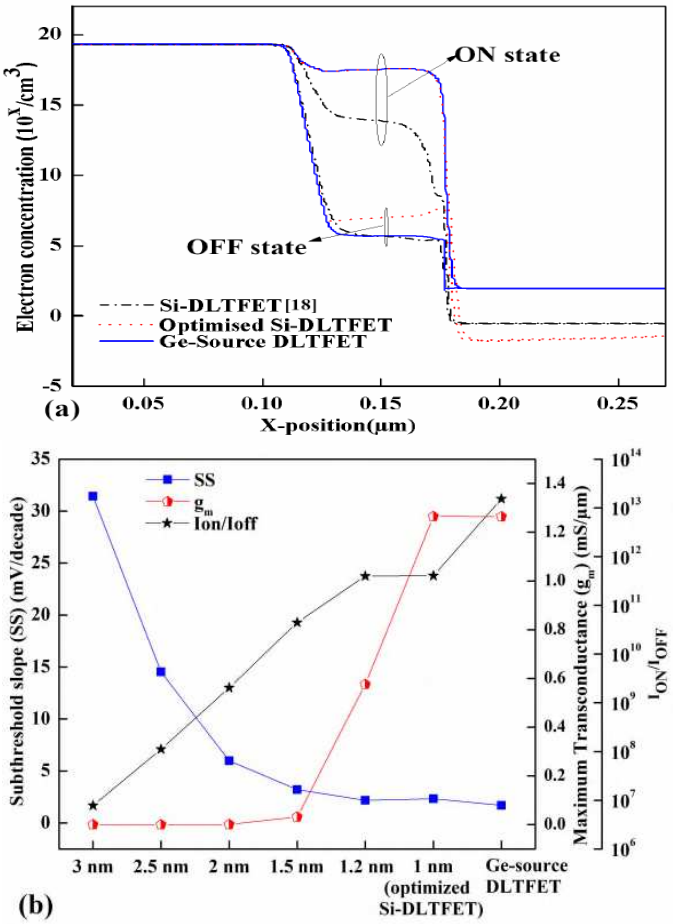


Fig. 7. (a) Electron concentration for Si-DLTFET [18], optimized Si-DLTFET and Ge-source DLTFET in ON state (V_D = 0.5 V and V_G = 0.5 V) and OFF state (V_D = 0.5 V and V_G = 0 V) and (b) SS, peak transconductance and I_{ON}/I_{OFF} ratio for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET.

Table 5. Parameter comparison of DLTFET [22], base structure of Si-DLTFET [18], optimized Si-DLTFET and Ge-source DLTFET.

Parameter	DLTFET [22]	Si-DLTFET [18]	Optimized Si-DLTFET	Ge-source DLTFET
@V_{DD} (V)	1	0.5	0.5	0.5
@$V_{GS,max}$ (V)	1.5	1	1	1
V_{TH}(V)	_	0.620502	0.504	0.503
I_{ON}(µA/µm)	11	0.000291	506	510
I_{OFF}(fA/µm)	0.01	0.037290	1.25	0.0332
I_{ON}/I_{OFF}	1.1×10^{12}	7.80×10^{6}	4.05×10^{11}	1.54×10^{13}
g_m (mS/µm)	_	7.66×10^{-7}	1.26	1.26
SS(mV/decade)	~100 (avg)	31.4 (min)/ ~84.4 (avg)	2.32 (min)	1.69 (min)

4 Effect of temperature

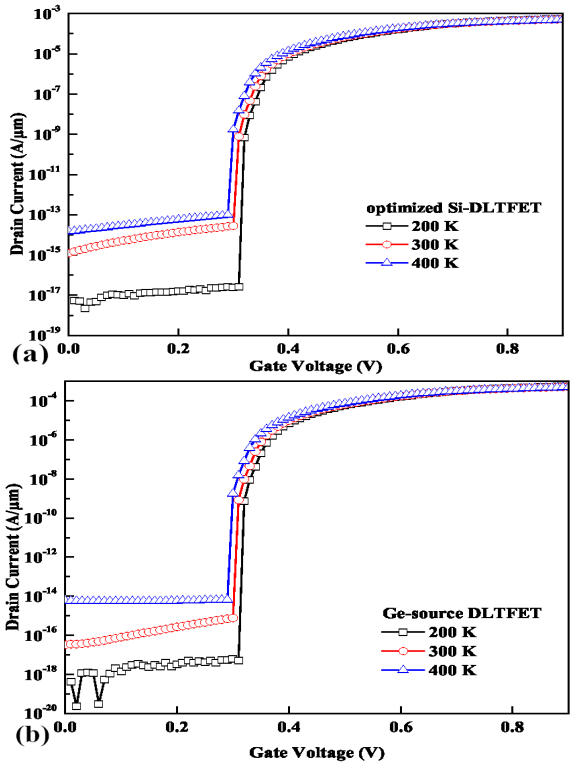


Fig. 8. Effect of temperature variation on performance of (a) optimized Si-DLTFET and (b) Ge-source DLTFET.

Operating temperature effects the tunnelling process. Analysis of the effect of operating temperature variation on proposed devices has been done for 200K to 400K. Fig 8(a) and (b) show the temperature dependence of optimized Si-DLTFET and Ge-source DLTFET respectively. It is evident from the figure that increasing temperature increases the leakage current of the devices. The increase in leakage current is because of increased carrier's thermal generation at higher temperature.

5 Analog, RF and Linearity Performance Parameters.

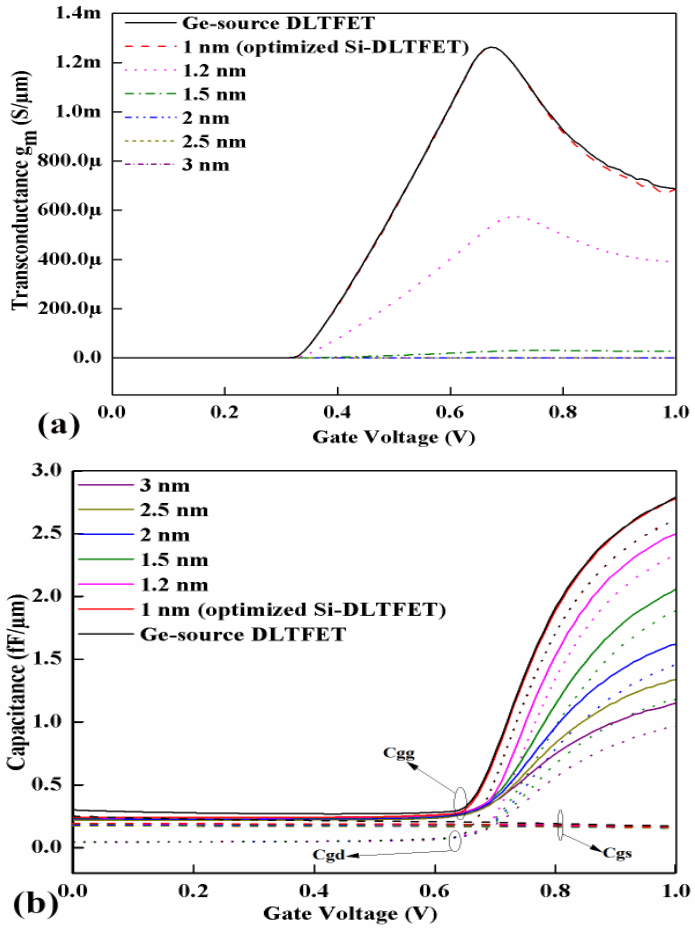


Fig. 9. (a) Transconductance and (b) Capacitance for variation in t_{ox} with t_{sox} = 3 nm inSi-DLTFET and for Ge-source DLTFET.

The most important performance parameter for analog/RF integrated circuit are:transconductance (g_m), intrinsic capacitance, output conductance (g_d), transconductance generation factor (TGF), intrinsic gain (g_m/g_d), cutoff frequency (f_T),gain bandwidth (GBW), transconductance frequency product (TFP), gain frequency product (GFP) and early voltage (V_{EA}). Further, linearity parameters such as second and third order harmonics of drain current (g_{m2} and g_{m3}), VIP_2, VIP_3, third order intercept input power (IIP_3) and third order intermodulation distortion (IMD_3). These parameters have been investigated for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-sourceDLTFET.

Transconductance is the effect of input voltage on output current, defined as

$$g_m = \frac{dI_D}{dV_{GS}}|_{V_{Ds}} \qquad (1)$$

Here, transconductance has been analysed for variation in t_{ox} with t_{sox} = 3 nmin Si-DLTFET and for Ge-source DLTFET at V_{DS} = 0.5 V. From Fig. 9(a), itis observed that the transconductance is increasing with a decrease in t_{ox} becauseof the increase in drain current with a decrease in t_{ox}. While gm for Ge-sourceDLTFET is approximately similar to the g_m for t_{ox} = 1 nm with t_{sox} = 3 nmin Si-DLTFET (optimized Si-DLTFET). Also the gm value has reached its peakat approximately 0.65 V. The increased transconductance leads to better gatecontrollability.

Fig. 9(b). shows total gate capacitance (C_{gg}), gate to source capacitance (C_{gs})and gate to drain capacitance (C_{gd}) for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET. Capacitance values have been extracted using ac small signal analysis. The capacitance between electrode pairs have beencalculated using ac signal frequency (1 GHz) solution with dc gate voltage ramp 0V to 1 V with step size 0.01 V and drain voltage 0.5 V. The capacitance increaseswith a decrease in t_{ox} (with t_{sox} = 3 nm) in Si-DLTFET whereas there is negligiblechange in capacitance with the use of Ge-Source. Fig. 9(b) shows that C_{gd} is adominant component of total capacitance for gate voltage greater than 0.7 V. Forgate voltage less than 0.7 V, C_{gs} is higher than C_{gd}, here C_{gg} mainly depends onC_{gs}.

Another performance parameter is output conductance g_d, defined as

$$g_d = \frac{dI_D}{dV_{DS}}|_{V_{GS}} = (R_o)^{-1} \quad (2)$$

Fig. 10(a) shows illustration of output conductance at gate voltage 0.5 V for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET. This is an important parameter for intrinsic gain of device ($A_V = g_m / g_d = g_m R_o$). Analog circuits require transistors having higher gain i.e. low output conductance. The high output conductance leads to low output resistance and thus high drain currentI_D.

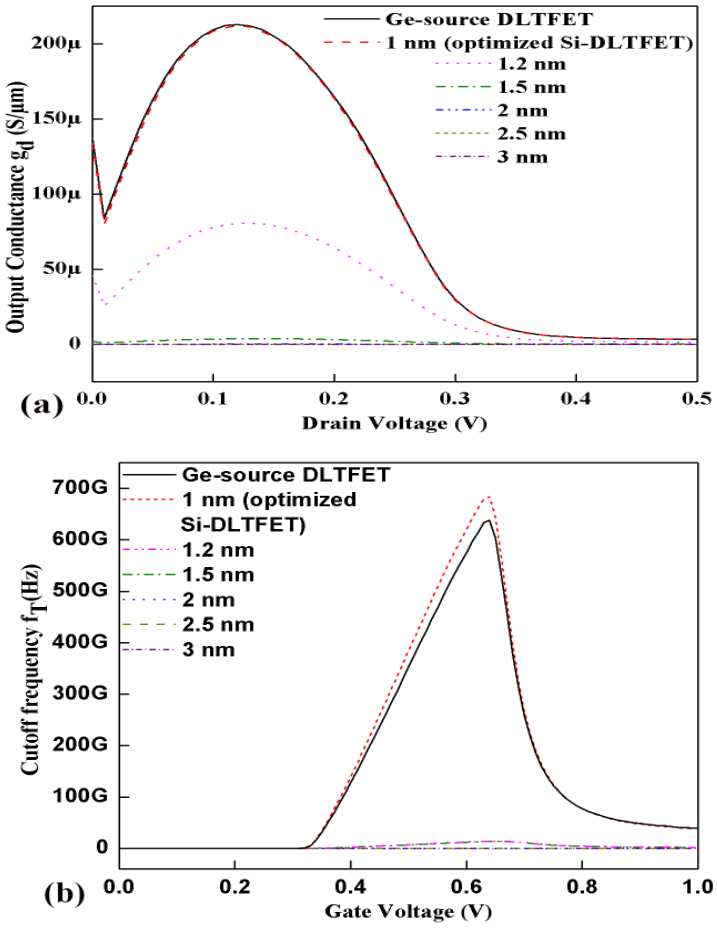
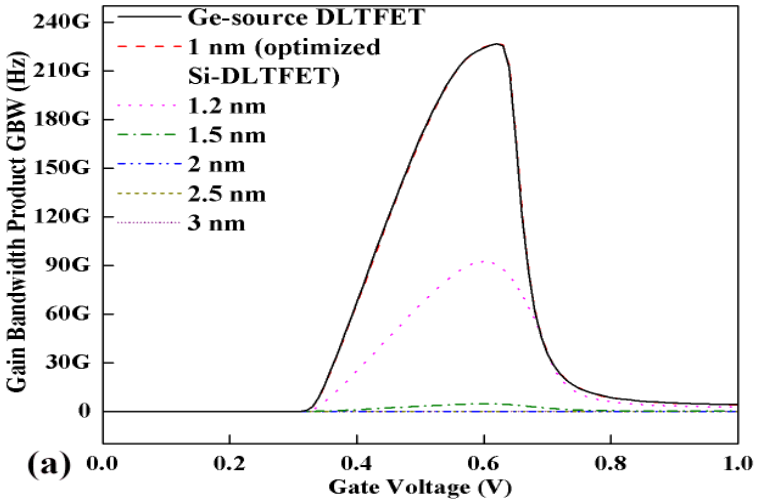


Fig. 10. (a) Output Conductance and (b) Cutoff frequency for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET.

Another important RF performance parameter is cutoff frequency (f_T). It isthe frequency at which output short circuited current gain becomes unity. Afterthis frequency the device will no longer work as an amplifier. The cutoff frequencydepends on g_m and total capacitance.

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1+2\left(C_{gd}/C_{gs}\right)}} \cong \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \cong \frac{g_m}{2\pi C_{gg}} \tag{3}$$



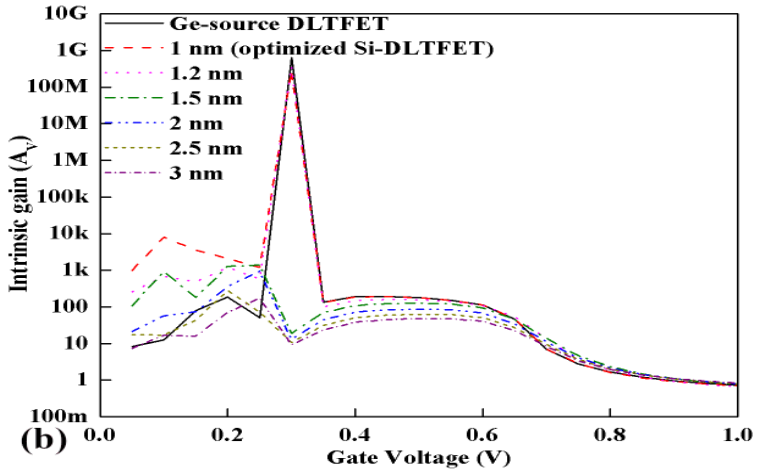


Fig. 11. (a) Gain bandwidth product and (b) Intrinsic gain for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET.

The cutoff frequency for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET andfor Ge-source DLTFET have been illustrated in Fig. 10(b). The cutoff frequencyincreases with increase in the gate voltage up to approximately 0.6 V and suddenlydecreases because of the decrease in g_m value. The cutoff frequency of the devicehas increased with a decrease in t_{ox}. While f_T for Ge-source DLTFET is comparable to the f_T for optimized Si-DLTFET, with cutoff frequency for optimizedSi-DLTFET as 683 GHz and for Ge-source DLTFET as 638 GHz.

Another crucialparameter for RF amplifier is gain bandwidth product. It is the product of openloop voltage gain and the frequency at which gain has been calculated. GBW isalways constant i.e. an increase in gain will lead to the decrease in frequency. The gain bandwidth for a certain dc gain of 10 is defined by

$$GBW = \frac{g_m}{2\pi 10 C_{gd}} \qquad (4)$$

Fig. 11(a) shows GBW for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET andfor Ge-source DLTFET, and it resembles the behaviour of f_T. GBW also increaseswith increase in gate voltage and then suddenly decreases because of decrease ing$_m$ values. GBW is maximum for optimized Si-DLTFET and Ge-source DLTFETi.e. 226 GHz.Another important parameter is intrinsic gain,

defined as

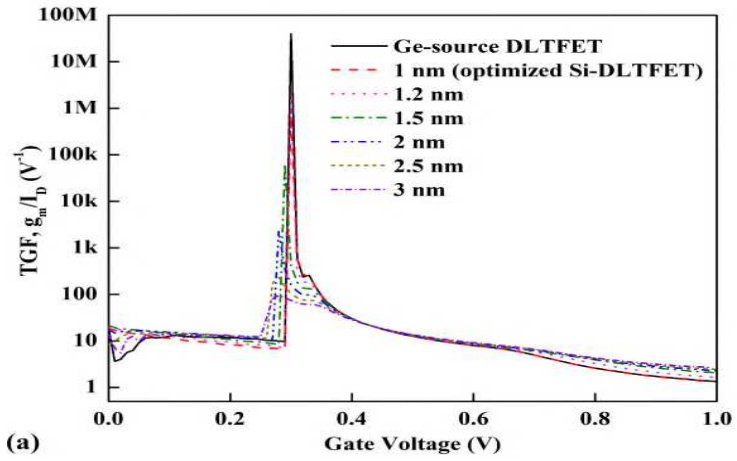
$$A_V = \frac{g_m}{g_d}|_{V_{GS},V_{DS}} \quad (5)$$

where, g_m and g_d are calculated for variation in gate voltage and at constantdrain voltage (0.5 V). Higher gain is required for devices for analog application.Fig. 11(b) shows intrinsic gain for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFETand for Ge-source DLTFET. It can be observed that in ON state the gain hasincreased with decrease in t_{ox} and the gain for optimized Si-DLTFET and forGe-source DLTFET is approximately equal.

In addition, TGF is the effect of current in achieving a desired value of transconductance. It can be defined as [27,30,31]

$$TGF = \frac{g_m}{I_D} = \frac{ln(10)}{SS} \quad (6)$$

Since, SS is extremely small at the transition from OFF to ON. g_m/I_D value isextremely high and it gradually decreases with increase in drain current. The highTGF is well suited for low power analog application. Fig. 12(a) shows the TGFfor variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET,and it can be observed that TGF value is increasing with a decrease in t_{ox} ofdevice also the TGF value for optimized Si-DLTFET and for Ge-source DLTFETis approximately equal.



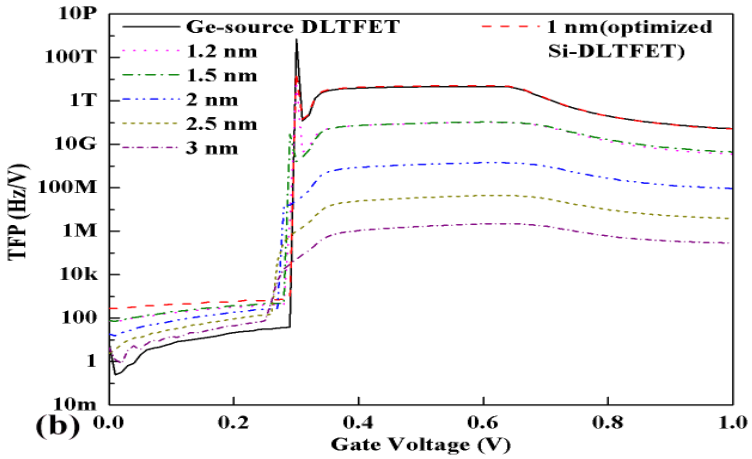


Fig. 12. (a) TGF and (b) TFP for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and forGe-source DLTFET.

Another parameter is TFP defined as [30,31]

$$TFP = \frac{g_m}{I_D} \times f_T = TGF \times f_T \qquad (7)$$

TFP represents trade-off between power and bandwidth and is best suited formoderate to high speed designs. Fig. 12(b) shows TFP for variation in t_{ox} witht_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET. It can be observed that the TFP value is increasing with a decrease in t_{ox} of device also the TFP valuefor optimized Si-DLTFET and for Ge-source DLTFET are approximately equal.Similarly, GFP is defined as [30]

$$GFP = \frac{g_m}{g_d} \times f_T = A_V \times f_T \qquad (8)$$

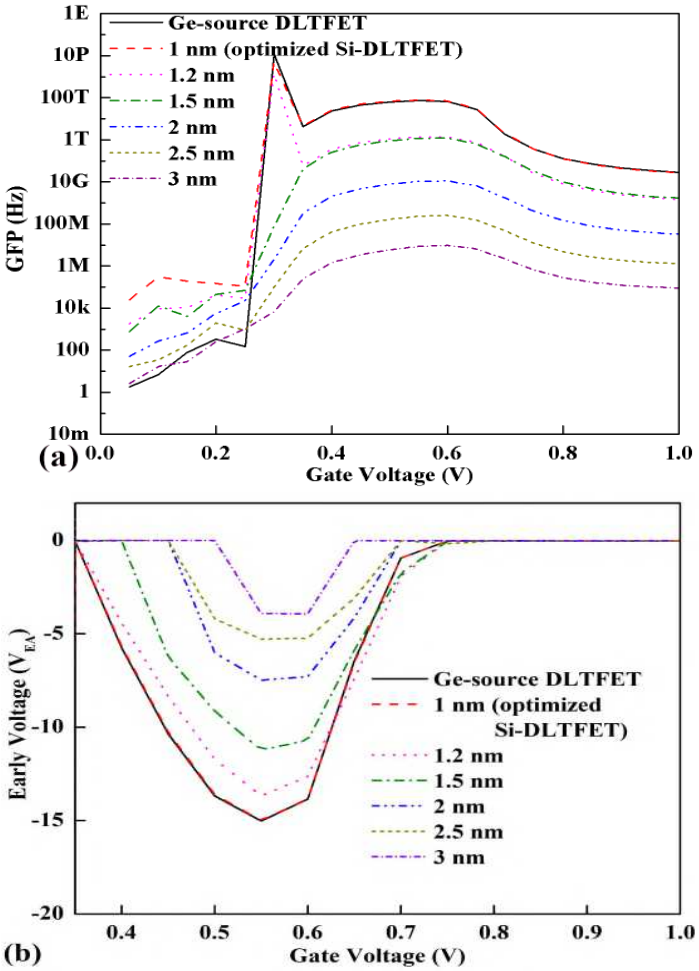


Fig. 13. (a) GFP and (b) Early voltage for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET.

It is an important parameter for operational amplifier at high frequency. Fig. 13(a)shows GFP for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-sourceDLTFET. Both TFP and GFP increase in subthreshold region but after that itattains an optimum value. It can be observed from the GFP plot that GFP valueis maximum for optimized Si-DLTFET and for Ge-source DLTFET.

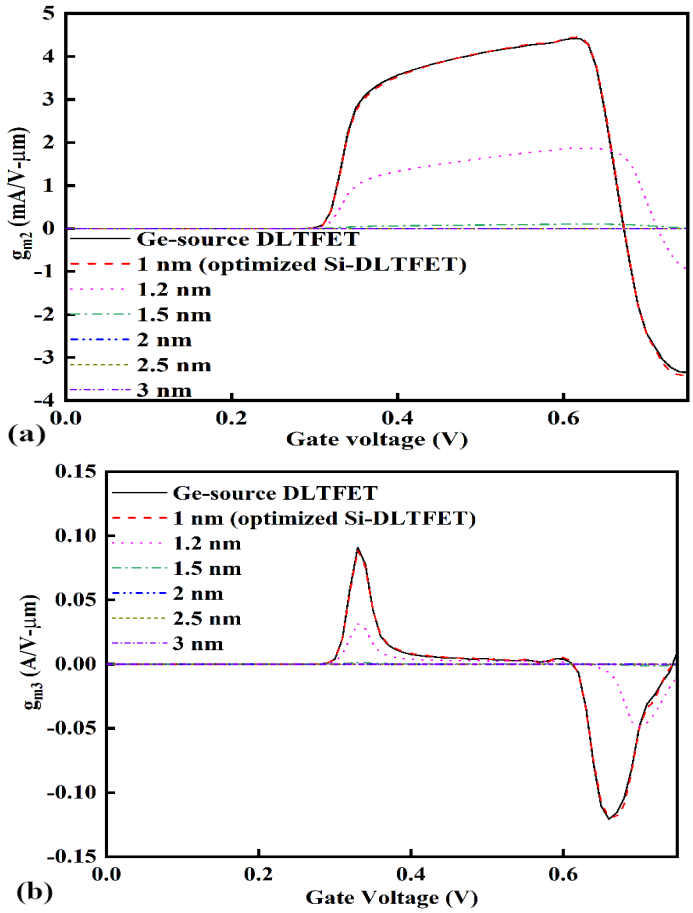


Fig. 14. (a) g_{m2} and (b) g_{m3} for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFETand for Ge-source DLTFET.

Further, in order to estimate the potentials of the device as a constant current source, its early voltage analysis has been done. Early voltage is the measure of independence of drain current on drain voltage in saturation region. Higher the early voltage higher will be the independence of drain current on drain voltage. i.e. the device can work as a constant current source. Early voltage is defined as

$$V_{EA} = \frac{I_D}{R_o} \tag{9}$$

Fig. 13(b) shows early voltage for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET, and it can be observed that magnitude of early voltage increases with increase in t_{ox} and the magnitude of early voltage is maximum

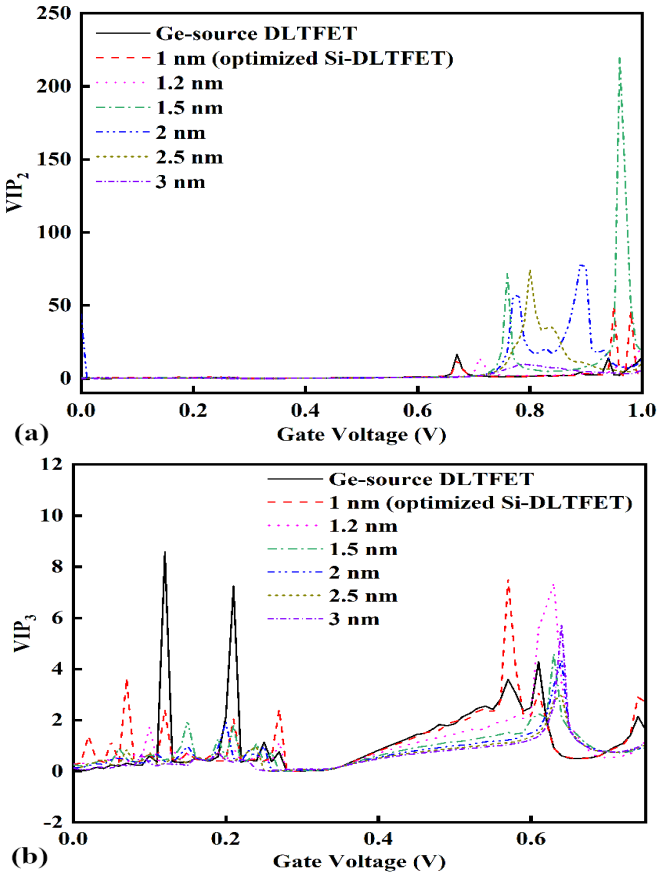


Fig. 15. (a) VIP_2 and (b) VIP_3 for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFETand for Ge-source DLTFET.

for optimized Si-DLTFET and for Ge-source DLTFET. Hence, it can be a better constant current source.

Important linearity parameter is higher order harmonics of drain current, such as second and third order harmonics (g_{m2}& g_{m3}). g_{m2} and g_{m3} is defined as $\delta^2 I_D/\delta V_G{}^2$ and $\delta^3 I_D/\delta V_G{}^3$respectively. Least linearity distortion is expected with least or zero crossover point of higher order harmonics. Fig. 14**.** (a) shows g_{m2} and (b) shows g_{m3} for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET. Further, linearity parameter VIP_2 and VIP_3 has been analysed. VIP_2 is extrapolated gate voltage amplitude at which second order harmonics become equal to fundamental tone of device drain current. Mathematically given as

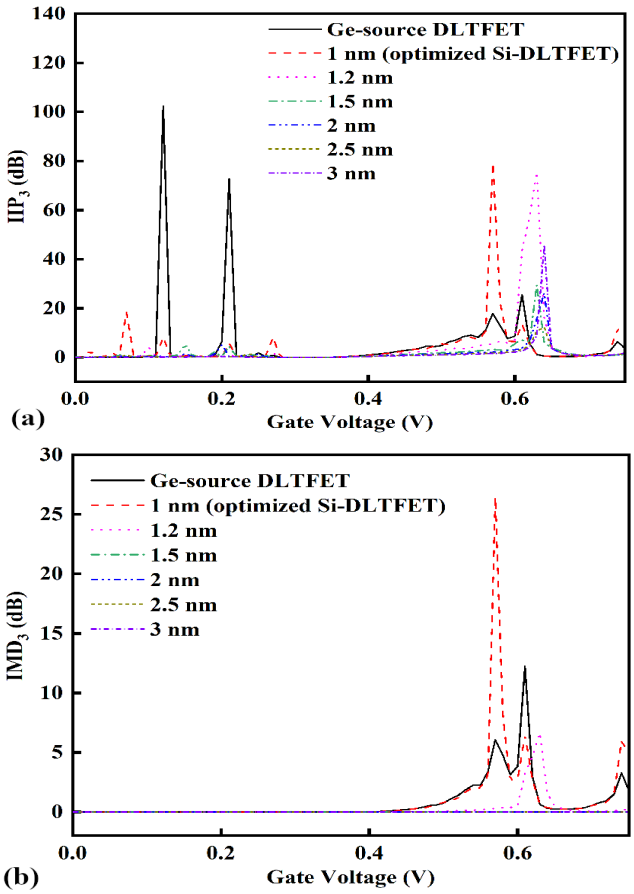


Fig. 16. (a) IIP_3 and (b) IMD_3 for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFETand for Ge-source DLTFET.

$$VIP_2 = \frac{4g_m}{g_{m2}}$$

VIP_3 is extrapolated gate voltage amplitude at which third order harmonics become equal to fundamental tone of device drain current. Mathematically given as

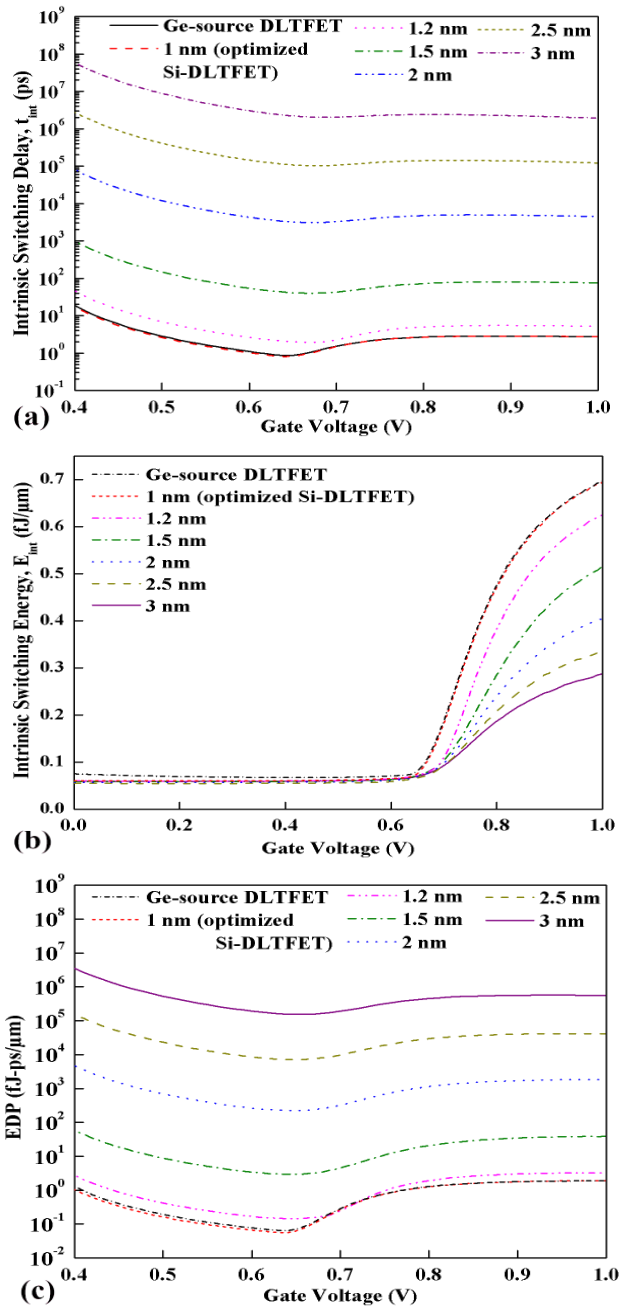


Fig. 17. (a) Intrinsic time delay, (b) Intrinsic switching energy and (c) EDP for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET.

$$VIP_2 = \sqrt{\frac{24 g_m}{g_{m3}}}$$

For least linearity distortion a higher value of VIP_2 and VIP_3 is desired. Fig. 15. (a) shows VIP_2 and (b) shows VIP_3 for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET.

Third order intercept input power (IIP_3) and third order intermodulation distortion (IMD_3) has also been analyzed. IIP3 is the extrapolated input power at which the fundamental tone and the third harmonic of device drain current are equal and is mathematically expressed as

$$IIP_3 = \frac{2}{3} \times \frac{g_m}{g_{m3} R_s}$$

IMD_3 is the extrapolated intermodulation current at which the first and the third order intermodulation harmonic currents are equal and is mathematically given by

$$IMD_3 = \left(\frac{9}{2} \times (VIP_3)^3 \times g_{m3}\right)^2 \times R_s$$

Fig. 16. (a) shows IIP_3 and (b) shows IMD_3 for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET. The desired value of IIP_3 and IMD_3 should be low.

6 Energy efficiency

Finally, to access the energy efficiency of device for low power applications the most important parameter is energy delay product (EDP). EDP is the product of intrinsic switching energy, E_{int} ($C_{gg}V_{DD}^2$) and intrinsic delay, t_{int} ($C_{gg}V_{DD}/I_{ON}$). Fig. 17(a) shows intrinsic time delay, Fig. 17(b) demonstrates the intrinsic switching energy, Fig. 17(c) energy delay product for variation in t_{ox} with t_{sox} = 3 nm in Si-DLTFET and for Ge-source DLTFET calculated at V_{DD} = 0.5 V. The intrinsic delay for t_{ox} = 3 nm with t_{sox} = 3 nm in Si-DLTFET is in the order of 10^{-5} sec and it decreases with a decrease in t_{ox} because of the increase in drain current. The intrinsic delay reaches to the order of pico-sec. The delay for the Ge-source DLTFET is similar to the delay for optimized Si-DLTFET. The intrinsic switching energy increases with a decrease in t_{ox} following the power delay trade-off. The intrinsic switching energy is in the range of $fJ/\mu m$. The product of intrinsic delay

and switching energy i.e. EDP is in the order of $10^6 fJ - ps/\mu m$ for t_{ox} = 3 nm with t_{sox} = 3 nm in Si-DLTFET and decreases with decrease in t_{ox} and reaches the order of 0.5-0.7 $fJ - ps/\mu m$ for optimized Si-DLTFET and is approximately equal for Ge-source DLTFET.

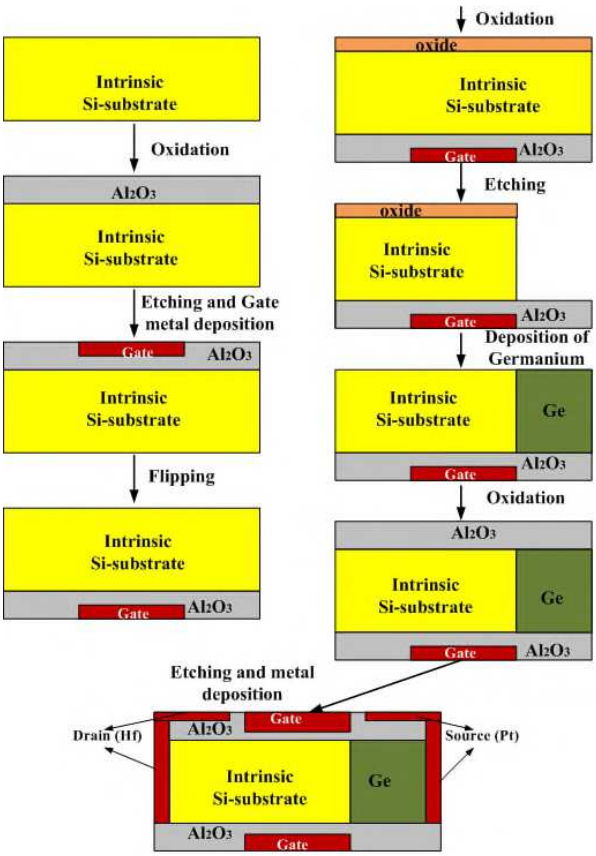


Fig. 18. Proposed process ow for the fabrication of the proposed device structure (Ge-source DLTFET).

7 Proposed fabrication/process flow

The Ge-source DLTFET can be fabricated by the process flow given in Fig. 18. As shown in Fig. 18, on intrinsic Si-wafer Al_2O_3 is deposited as shown, followed by etching of oxide and gate material deposition, now the substrate can be flipped [34], next oxide layer is deposited, followed by selective etching of silicon

substrate [35], next germanium deposition is done and the remaining oxide is etched [35], now Al_2O_3 is deposited, followed by etching and gate, source and drain contact material deposition. There may be some challenges in the actual fabrication of device. However, as there is rapid increase in technology with time, the device will get fabricated with relative ease in future.

8 Conclusion

This work reported the optimization of oxide thickness for Si-DLTFET to improve the device performance parameters. Further, the incorporation of Ge-sourceon DLTFET has been investigated using exhaustive calibrated 2D TCAD device simulation. The simulation results show that the optimized Si-DLTFET has1.739×10^6 times improved ON current whereas Ge-source DLTFET has 1.754×10^6times improved ON current. This increases I_{ON}/I_{OFF} for optimized Si-DLTFET5.19×10^4 times and for Ge-source DLTFET 1.974×10^6 times. The decrease in SSis 92.6% for optimized Si-DLTFET and 94.6% for Ge-source DLTFET as comparedto Si-DLTFET. The increase in peak transconductance for optimized Si-DLTFETas well as for Ge-source DLTFET is 1.645×10^6 times compared to Si-DLTFET.Both proposed structures, optimized Si-DLTFET and Ge-source DLTFET showsan increase in leakage current with an increase in operating temperature. Theanalog, RF and linearity performance parameters have also been investigated for variationin t_{ox} with t_{sox} = 3 nm in Si-DLTFET and Ge-source DLTFET and demonstratesignificant improvement. Furthermore, intrinsic switching delay for both optimizedSi-DLTFET and Ge-source DLTFET is 2-3 ps, intrinsic switching energy is 0.5-0.7$fJ_ps/\mu m$ and energy-delay product in the range of 1-2 $fJ\_ps/\mu m$. Moreover, thereported device is also expected to have a lower thermal budget, immune towardsthe RDF and velocity degradation effects due to its dopingless realization. Hence,our study demonstrates that the optimized Si-DLTFET and Ge-source DLTFETembodies appropriate candidate for low power analog and RF application whereasGe-source DLTFET can be a better candidate for dc device performance.

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References

1. V. Kilchytska, A. Neve, L. Vancaillie, D. Levacq, S. Adriaensen, H. van Meer, K. De Meyer, C. Raynaud, M. Dehan, J.P. Raskin, and D. Flandre, Influence of device engineering on the analog and RF performances of SOI MOSFETs. IEEE Transactions on Electron Devices,50(3), 577 (2003).

2. N. Mohankumar, B. Syamal, and C.K. Sarkar, Influence of channel and gate engineeringon the analog and RF performance of DG MOSFETs. IEEE Transactions on ElectronDevices, 57(4), 820 (2010).
3. H. Masuda, M. Nakai, and M. Kubo, Characteristics and limitation of scaled-down MOSFET's due to two-dimensional field effect. IEEE Transactions on Electron Devices, 26(6),980(1979).
4. S.Bangsaruntip, G.M. Cohen,A. Majumdar, and J.W. Sleight, Universality of short-channel effects in undoped-body silicon nanowire MOSFETs. IEEE Electron Device Letters, 31(9), 903 (2010).
5. J.P. Colinge, FinFETs and other multi-gate transistors, New York: Springer, 73 (2008).
6. T. Nirschl, J. Fischer, M. Fulde, A. Bargagli-Sto, M. Sterkel, J. Sedlmeir, C. Weber,R. Heinrich, U. Schaper, J. Einfeld, and R. Neubert, Scaling properties of the tunnelling field effect transistor (TFET): Device and circuit. Solid-state electronics, 50(1), 44(2006).
7. S.O. Koswatta, M.S. Lundstrom, and D.E. Nikonov, Performance comparison betweenpin tunneling transistors and conventional MOSFETs. IEEE Transactions on ElectronDevices, 56(3),456 (2009).
8. K. Boucart, W. Riess, and A.M. Ionescu, Lateral strain profile as key technology boosterfor all-silicon tunnel FETs. IEEE Electron Device Letters, 30(6), 656 (2009).
9. K. Boucart, and A.M. Ionescu, Double-gate tunnel FET with high-k gate dielectric. IEEETransactions on Electron Devices, 54(7), 1725 (2007).
10. W.Y. Choi, B.G. Park, J.D. Lee, and T.J.K. Liu, Tunneling field-effect transistors (TFETs)with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Letters, 28(8),743 (2007).
11. R. Jhaveri, V. Nagavarapu, and J.C. Woo, Effect of pocket doping and annealing schemeson the source-pocket tunnel field-effect transistor. IEEE Transactions on Electron Devices,58(1), 80 (2010).
12. M.J. Kumar and K. Nadda, Bipolar charge-plasma transistor: a novel three terminal device. IEEE Transactions on Electron Devices, 59(4), 962 (2012).
13. S. Ramaswamy, and M.J. Kumar, Junctionless impact ionization MOS: Proposal andinvestigation. IEEE Transactions on Electron Devices, 61(12), 4295 (2014).
14. S.I. Amin, and R.K. Sarin, Charge-plasma based dual-material and gate-stacked architecture of junctionless transistor for enhanced analog performance. Superlattices and Microstructures, 88, 582 (2015).
15. R.J. Hueting, B. Rajasekharan,C. Salm, and J. Schmitz, The charge plasma PN diode.IEEE electron device letters, 29(12), 1367 (2008).
16. N. Damrongplasit, C. Shin, S.H. Kim, R.A. Vega, and T.J.K. Liu, Study of random dopant fluctuation effects in germanium-source tunnel FETs. IEEE Transactions on Electron Devices, 58(10), 3541 (2011).
17. N. Damrongplasit, S.H. Kim, and T.J.K. Liu, Study of random dopant fluctuation inducedvariability in the raised-Ge-source TFET. IEEE electron device letters, 34(2), 184(2013).
18. X. Duan, J. Zhang, S.Wang, Y. Li, S. Xu, and Y. Hao, A high-performance gate engineeredInGaN dopingless tunnel FET. IEEE Transactions on Electron Devices, 65(3), 1223 (2018).
19. S. Singh, and P. N. Kondekar, A novel electrostatically doped ferroelectric Schottky barriertunnel FET: process resilient design. Journal of computational electronics, 16(3), 685 (2017).
20. J. Hur, D.I. Moon, J.W. Han, G.H. Kim, C.H. Jeon, and Y.K. Choi, Tunneling

effects ina charge-plasma dopingless transistor, IEEE Transactions on Nanotechnology, 16(2), 315 (2017).
21. S. Singh, A.P. Singh and P.N. Kondekar, A novel self-aligned charge plasma Schottkybarrier tunnel FET using work function engineering. Microelectronic Engineering, 168,67 (2017).
22. M.J. Kumar and S. Janardhanan, Doping-less tunnel field effect transistor: Design andinvestigation. IEEE transactions on Electron Devices, 60(10), 3285 (2013).
23. K. Nadda and M.J. Kumar, Vertical bipolar charge plasma transistor with buried metallayer. Scientic reports, 5, 7860(2015).
24. F. Bashir, S.A. Loan, M. Rafat, A.R.M. Alamoud, and S.A. Abbasi, A high-performancesource engineered charge plasma-based Schottky MOSFET on SOI, IEEE Transactions onElectron Devices, 62(10), 3357 (2015).
25. W.M. Haynes, CRC handbook of chemistry and physics. CRC press(2014).
26. P. Ranade, H. Takeuchi, T.J. King, and C. Hu, Work function engineering of molybdenumgate electrodes by nitrogen implantation. Electrochemical and Solid-State Letters, 4(11),G85 (2001).
27. S. Saurabh, and M.J. Kumar, Fundamentals of tunnel field-effect transistors. CRC press (2016).
28. ATLAS User Manual, Silvaco International, Santa Clara, CA (2015).
29. S. Singh, and P.N. Kondekar, A novel process variation immune dopingless zero subthreshold slope and zero impact ionization FET (DL-Z2FET) based on transition metals.Journal of Computational Electronics, 15(1), 67 (2016).
30. S. Singh, P.N. Kondekar, and A. P. Singh, Investigation of analog/radio frequency figures-of-merits of charge plasma schottky barrier tunnel field effect transistor. Journal of Nanoelectronics and Optoelectronics, 12(4), 365(2017).
31. S. Singh, P.N. Kondekar, and R. Sinha, Estimation of analog/radiofrequency figures-of-merits and circuit performance of dynamically reconfigurable electrostatically doped siliconnanowire schottky barrier FET. Journal of Nanoelectronics and Optoelectronics, 12(4), 343(2017).
32. F. Bashir, S.A. Loan, M. Rafat, A.R.M. Alamoud, and S.A. Abbasi. A high performancegate engineered charge plasma based tunnel field effect transistor. Journal of Computational Electronics, 14(2), 477 (2015).
33. S. Singh, A. Singh and P. N. Kondekar,A Novel Self-Aligned Charge Plasma Schottky Barrier Tunnel FET Using Work Function Engineering, Microelectronic Engineering, 168, 67 (2017).
34. S.A. Loan, S. Kumar, and A.M. Alamoud, A novel double gate metal source/drain Schottky MOSFET as an inverter. Superlattices and Microstructures, 91, 78 (2016).
35. S.H. Kim, H. Kam, C. Hu, and T.J.K. Liu, Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}. Symposium on VLSI Technology, 178 (2009).
36. S. Singh, P. N. Kondekar, and N. K. Jaiswal, Label-Free Biosensor using Nanogap Embedded Dielectric Modulated Schottky Tunneling Source Impact Ionization MOS, Microelectronic Engineering, 149, 129 (2016).

Conflict of Interest and Authorship Conformation Form

Please check the following as appropriate:

- All authors have participated in (a) conception and design, or analysis and interpretation of the data; (b) drafting the article or revising it critically for important intellectual content; and (c) approval of the final version.

- This manuscript has not been submitted to, nor is under review at, another journal or other publishing venue.

- The authors have no affiliation with any organization with a direct or indirect financial interest in the subject matter discussed in the manuscript

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Author's name	**Affiliation**
Kumari Nibha Priyadarshani	NIT Patna, Patna, Bihar
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Kunal Singh	NIT Jamshedpur, Jamshedpur, Jharkhand

Figures

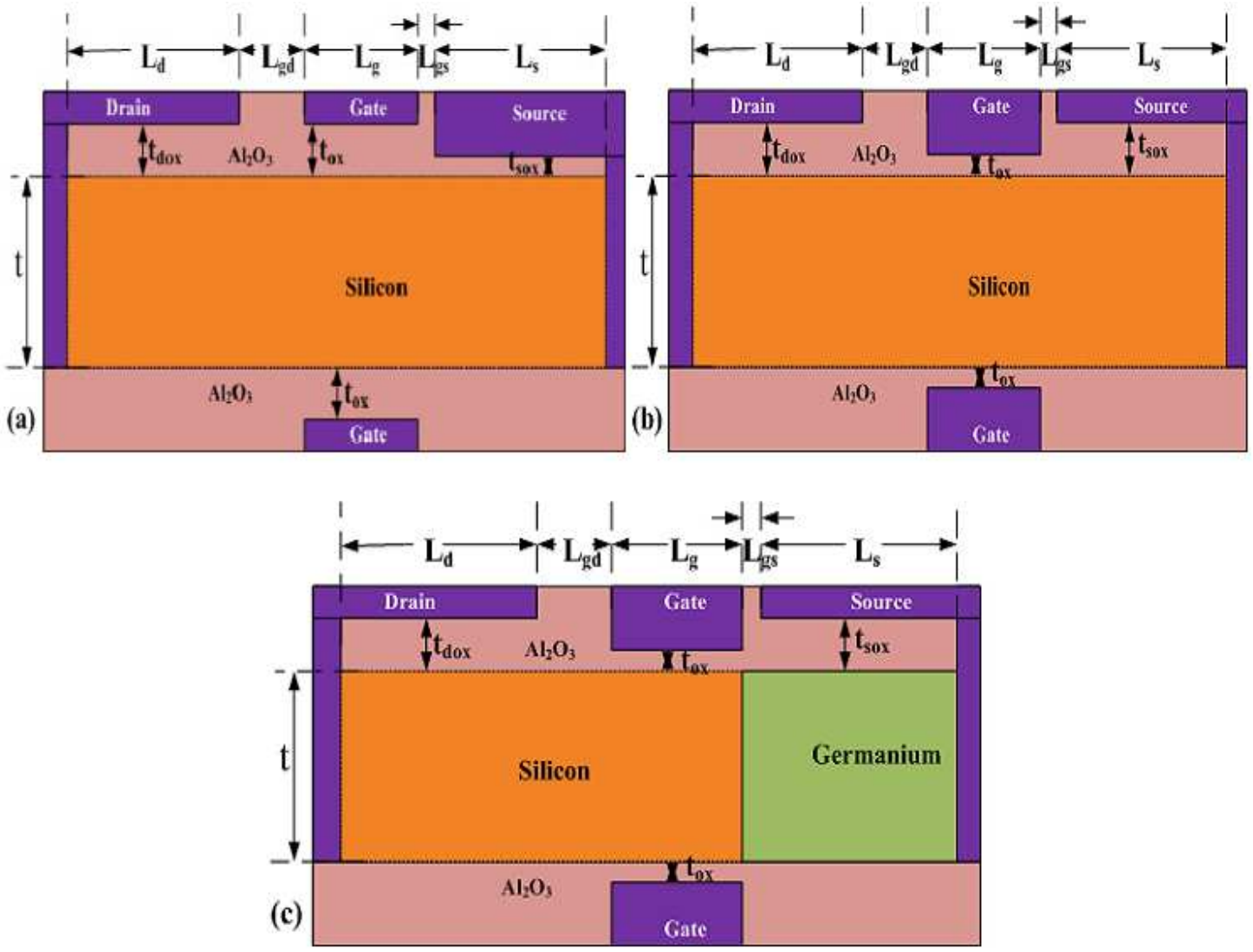

Figure 1

2D device structure of (a) base silicon structure (Si-DLTFET) [18], (b) optimized Si-DLTFET and (c) Ge-source DLTFET.

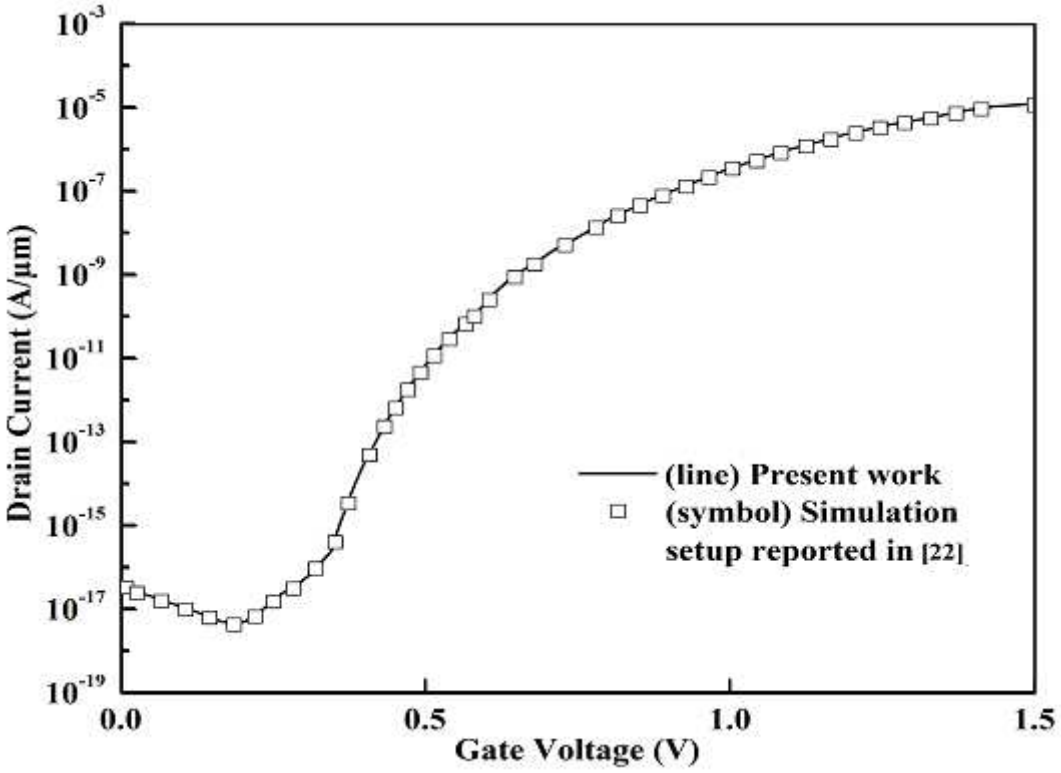

Figure 2

Calibration of proposed simulation framework with [22]. ID-VGS characteristics of DLTFET at VDS = 1.0 V.

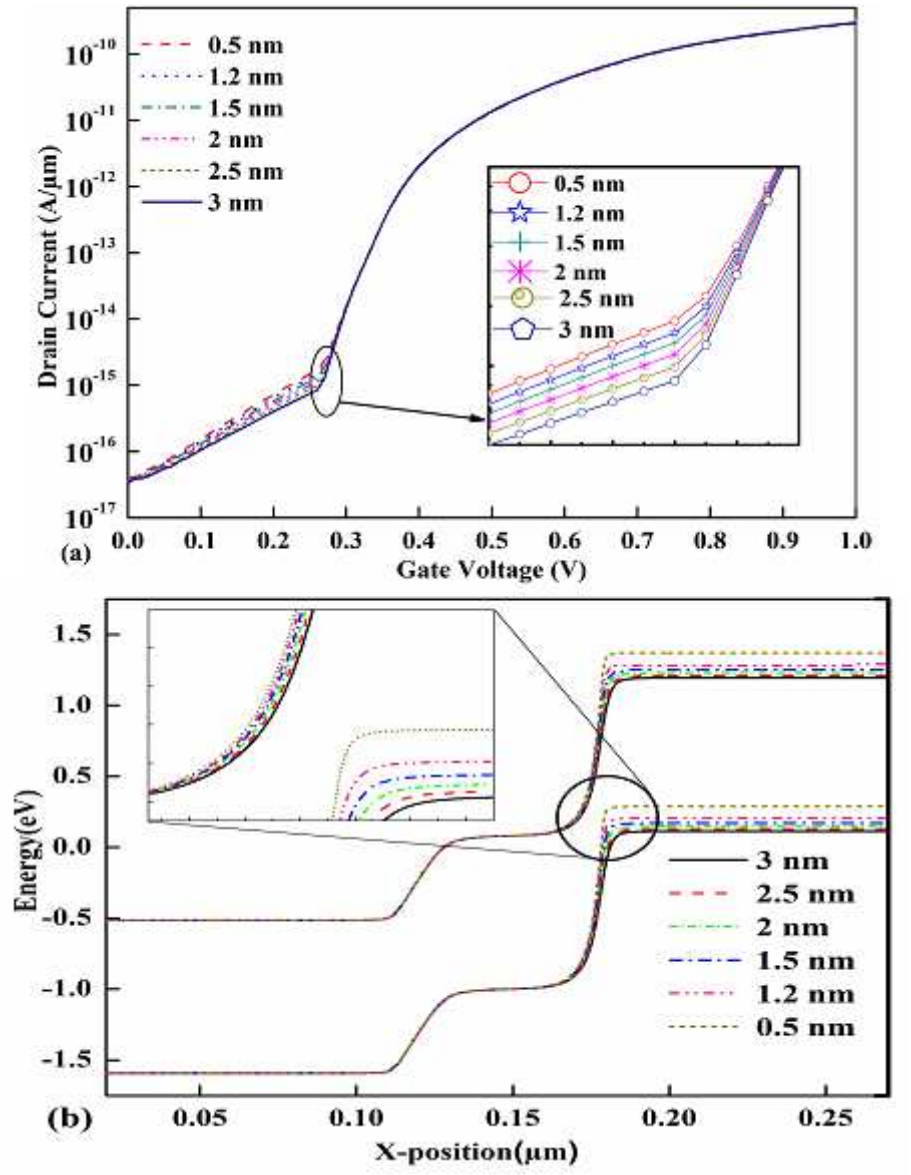

Figure 3

(a) Transfer characteristic of Si-DLTFET for different oxide thickness under source contact at VD = 0.5 V and (b) Energy band diagram of Si-DLTFET for change in oxide thickness under source at VG = 0.25 V, VD = 0.5 V.

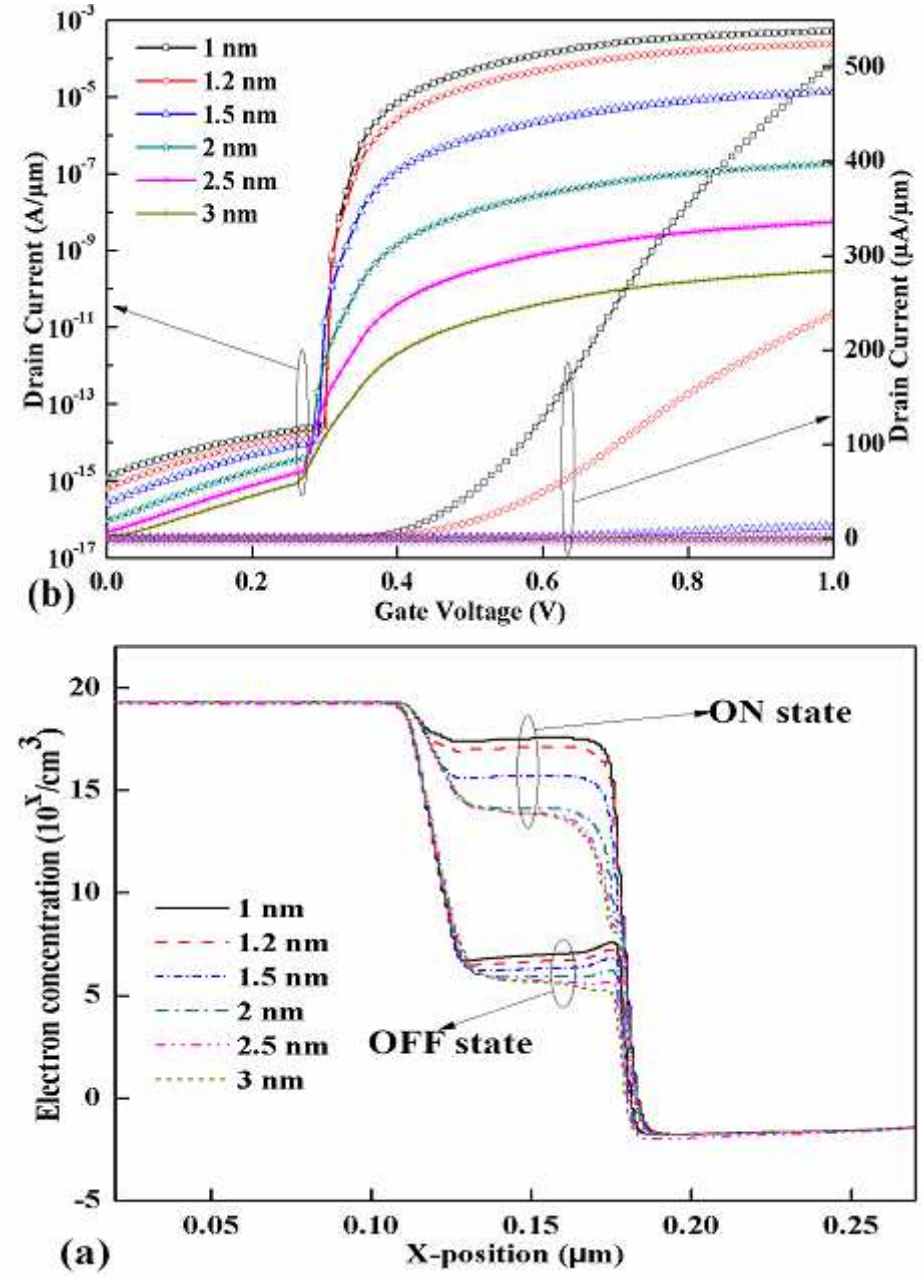

Figure 4

(a) Electron concentration in ON state (VD = 0.5 V and VG = 0.5 V) and in OFF state (VD = 0.5 V and VG = 0 V) and (b) Transfer characteristic at VD = 0.5 V for Si-DLTFET for varia-tion in tox with tsox as 3 nm.

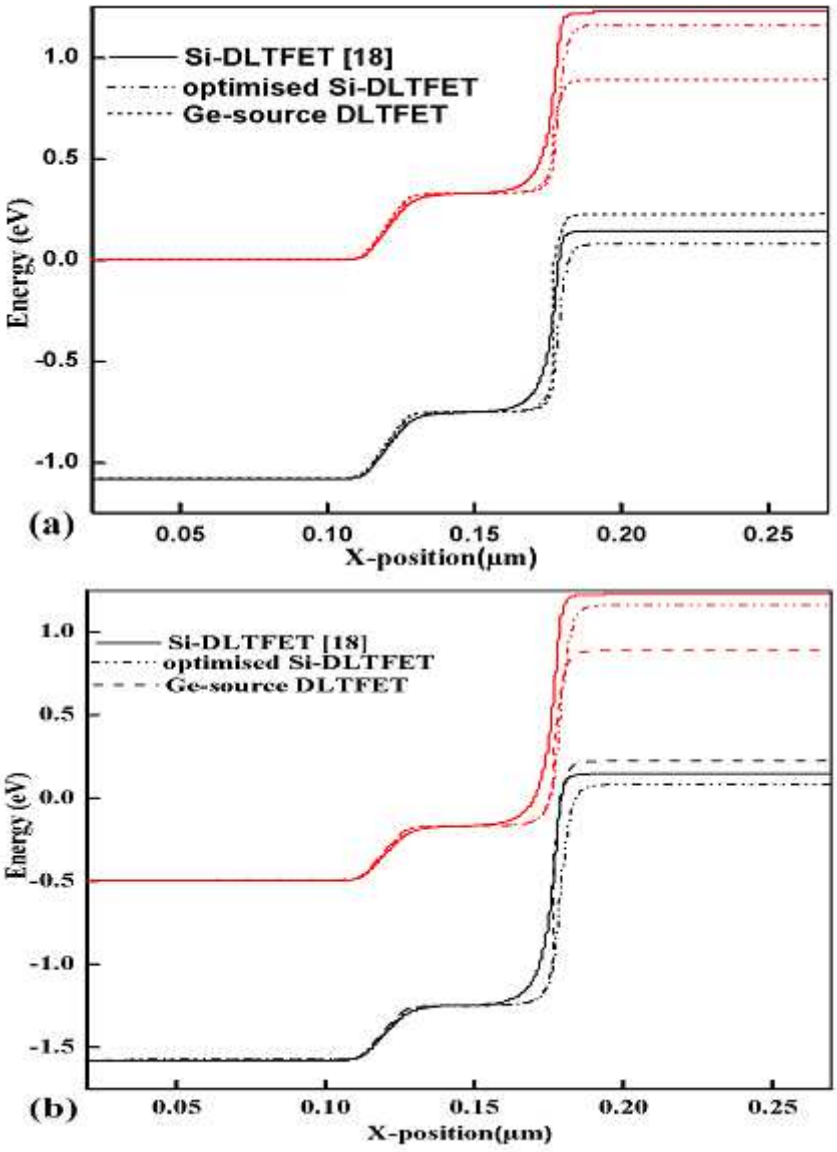

Figure 5

Energy band diagram of Si-DLTFET [18], optimized Si-DLTFET, Ge-source DLTFET at (a) Thermal equilibrium and (b) ON state VG = 0.5 V and VD = 0.5 V.

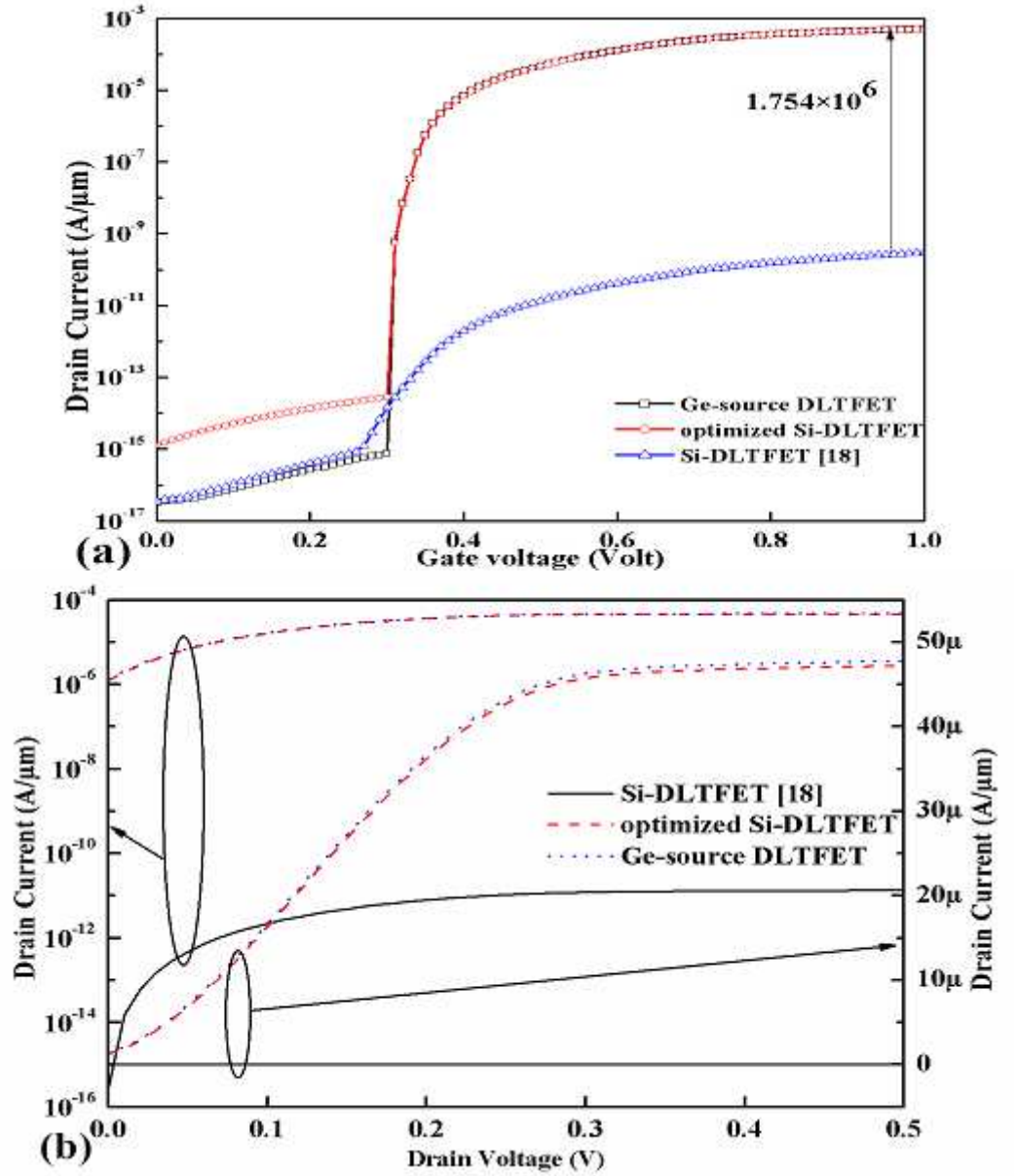

Figure 6

(a) Transfer characteristic of Si-DLTFET [18], optimized Si-DLTFET and Ge-sourceDLTFET at VD = 0.5 V and (b) Output characteristic of Si-DLTFET [18], optimized Si-DLTFET and Ge-source DLTFET at VG = 0.5 V.

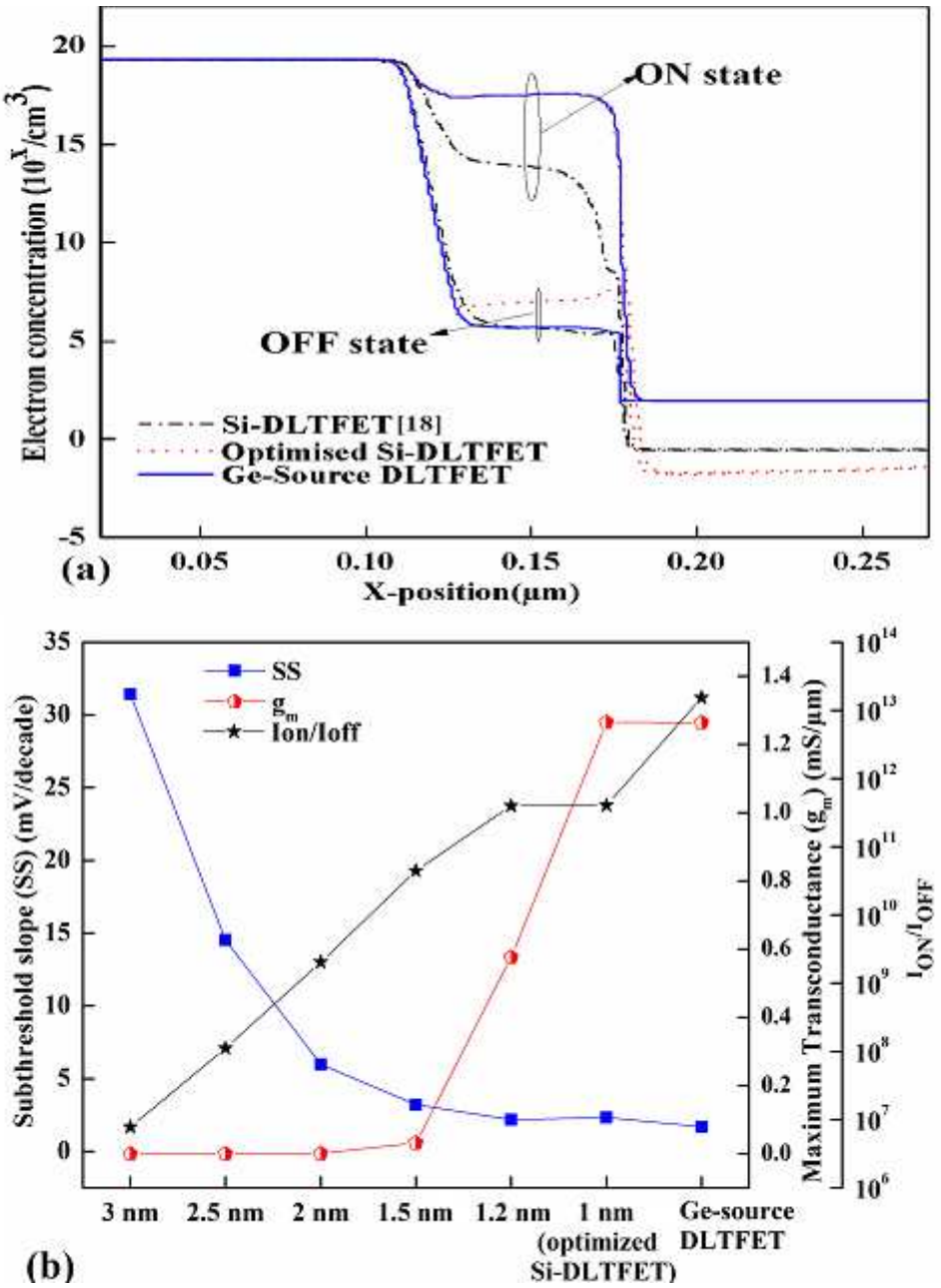

Figure 7

(a) Electron concentration for Si-DLTFET [18], optimized Si-DLTFET and Ge-source DLTFET in ON state (VD = 0.5 V and VG = 0.5 V) and OFF state (VD = 0.5 V and VG = 0 V) and (b) SS, peak transconductance and ION/IOFF ratio for variation in tox with tsox = 3 nm in Si-DLTFET and for Ge-source DLTFET.

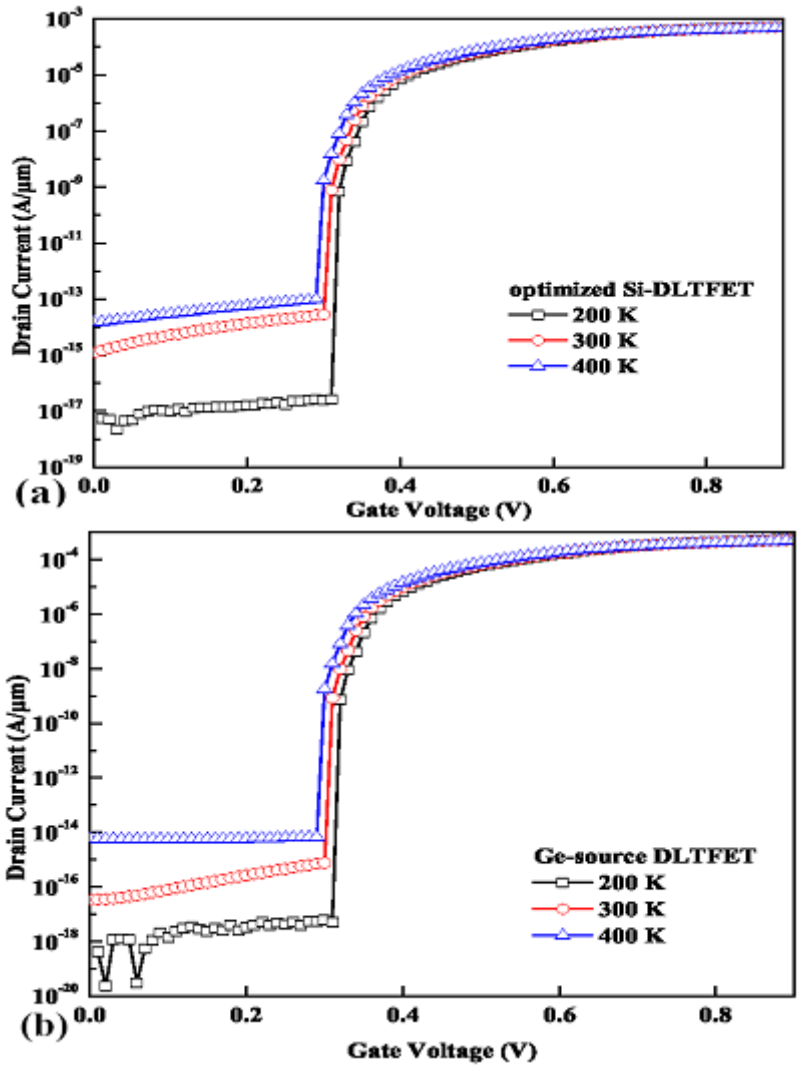

Figure 8

Effect of temperature variation on performance of (a) optimized Si-DLTFET and (b) Ge-source DLTFET.

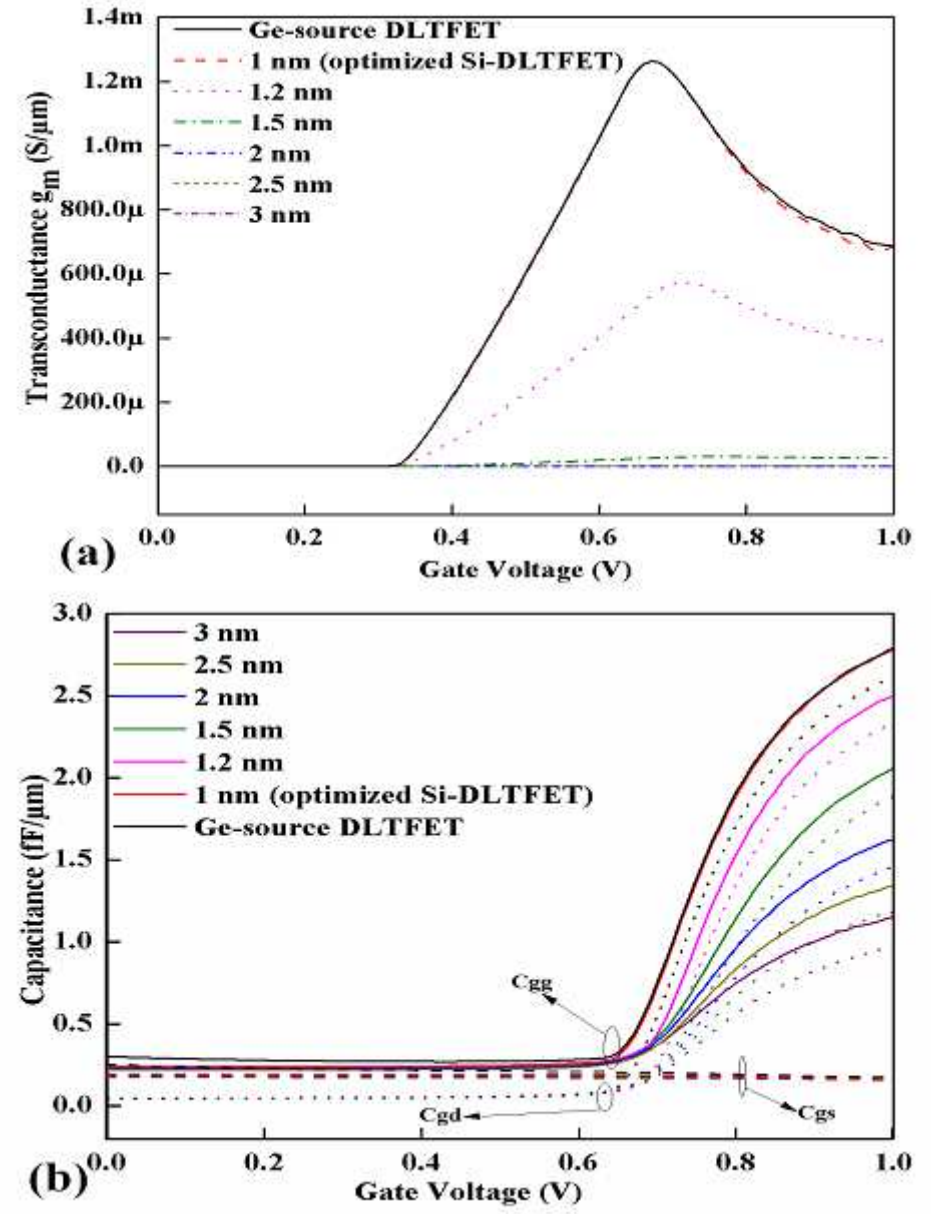

Figure 9

(a) Transconductance and (b) Capacitance for variation in tox with tsox = 3 nm inSi-DLTFET and for Ge-source DLTFET.

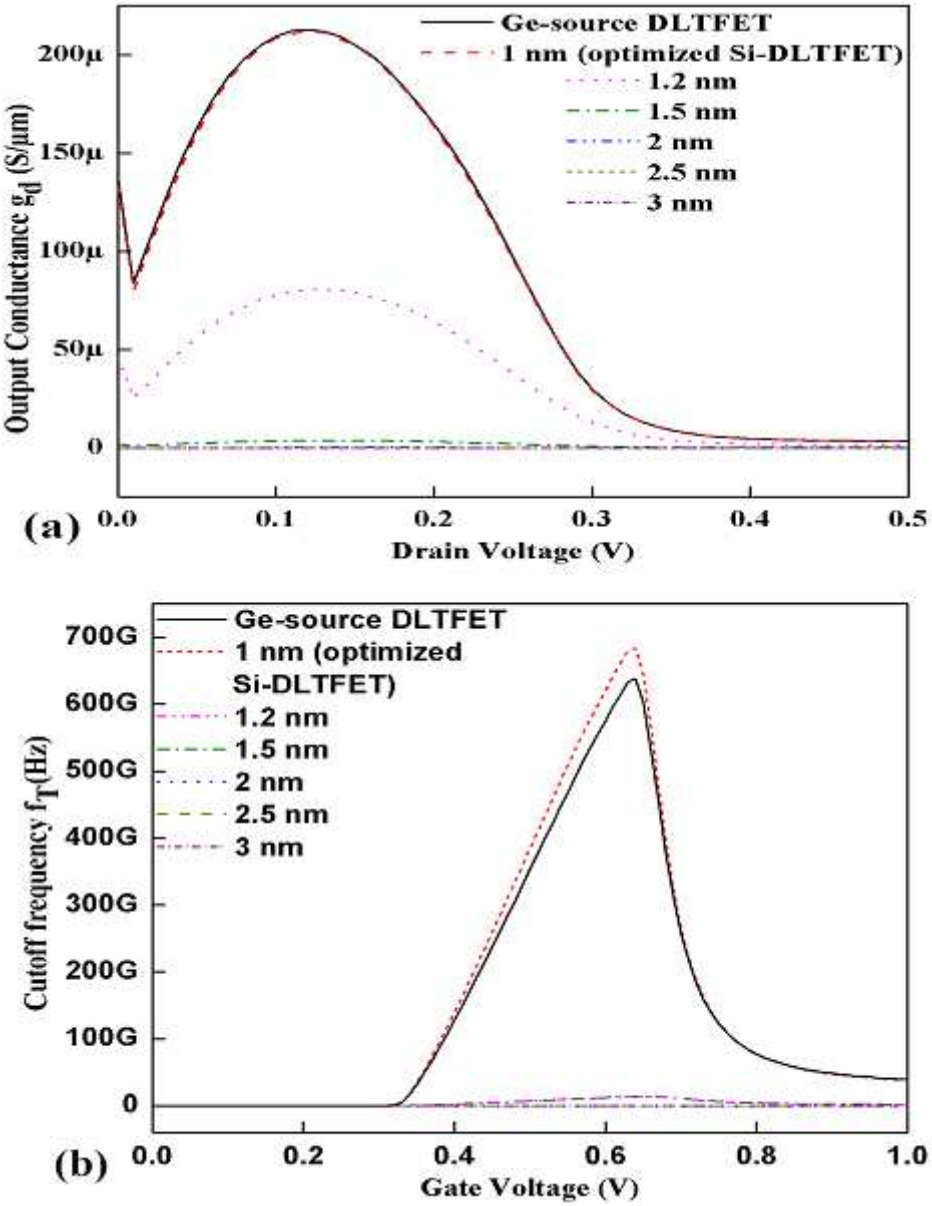

Figure 10

(a) Output Conductance and (b) Cutoff frequency for variation in tox with tsox = 3 nm in Si-DLTFET and for Ge-source DLTFET.

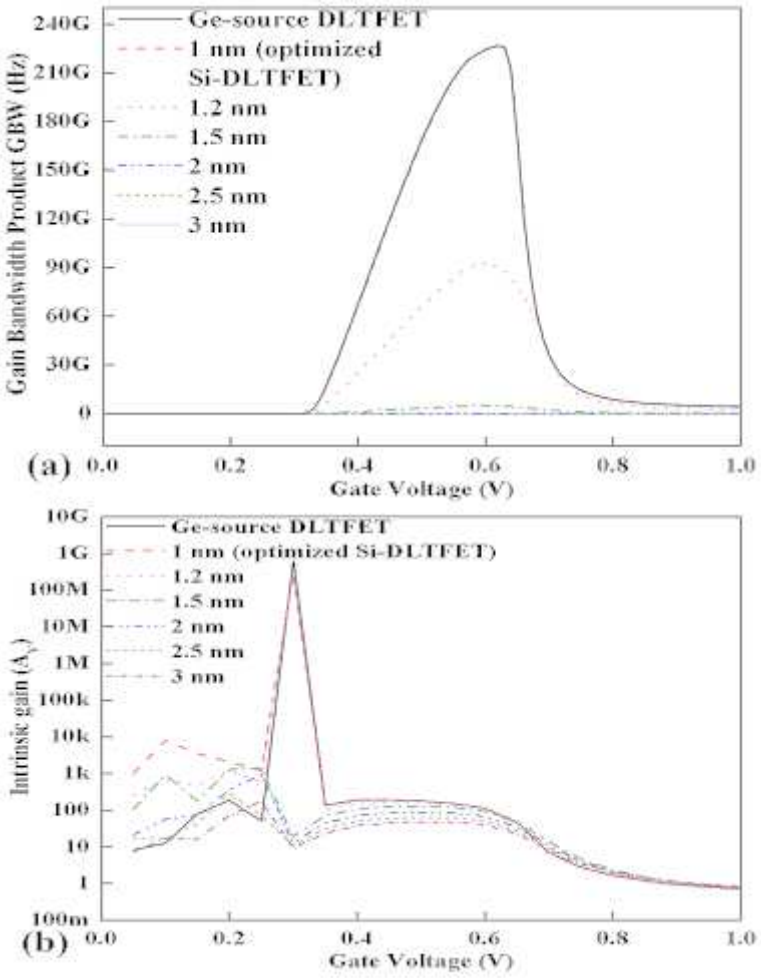

Figure 11

(a) Gain bandwidth product and (b) Intrinsic gain for variation in tox with tsox = 3 nm in Si-DLTFET and for Ge-source DLTFET.

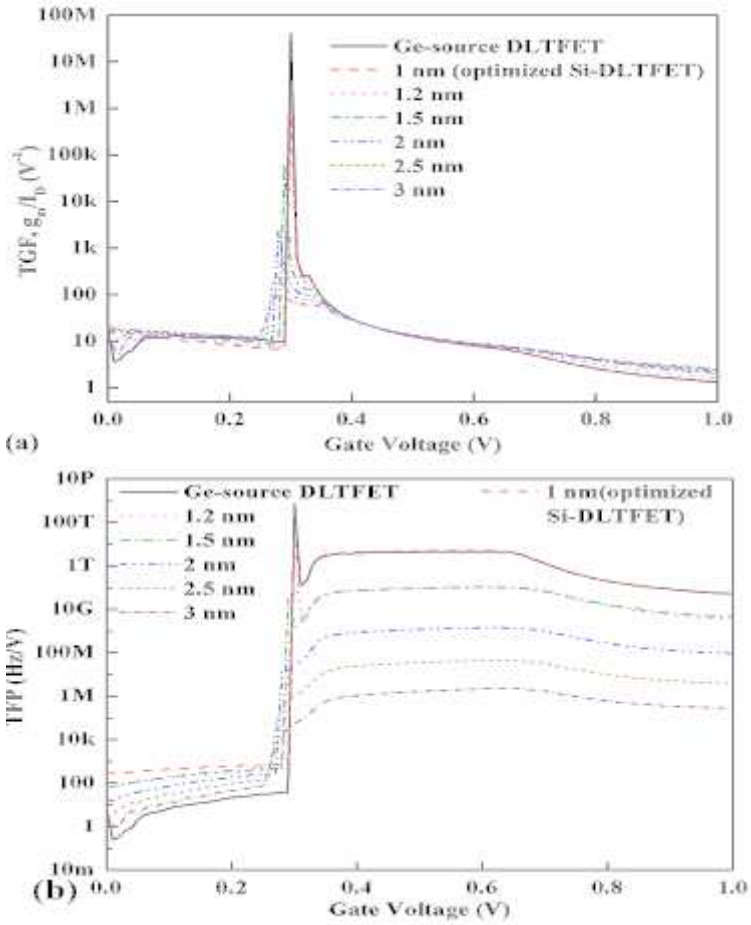

Figure 12

(a) TGF and (b) TFP for variation in tox with tsox = 3 nm in Si-DLTFET and forGe-source DLTFET.

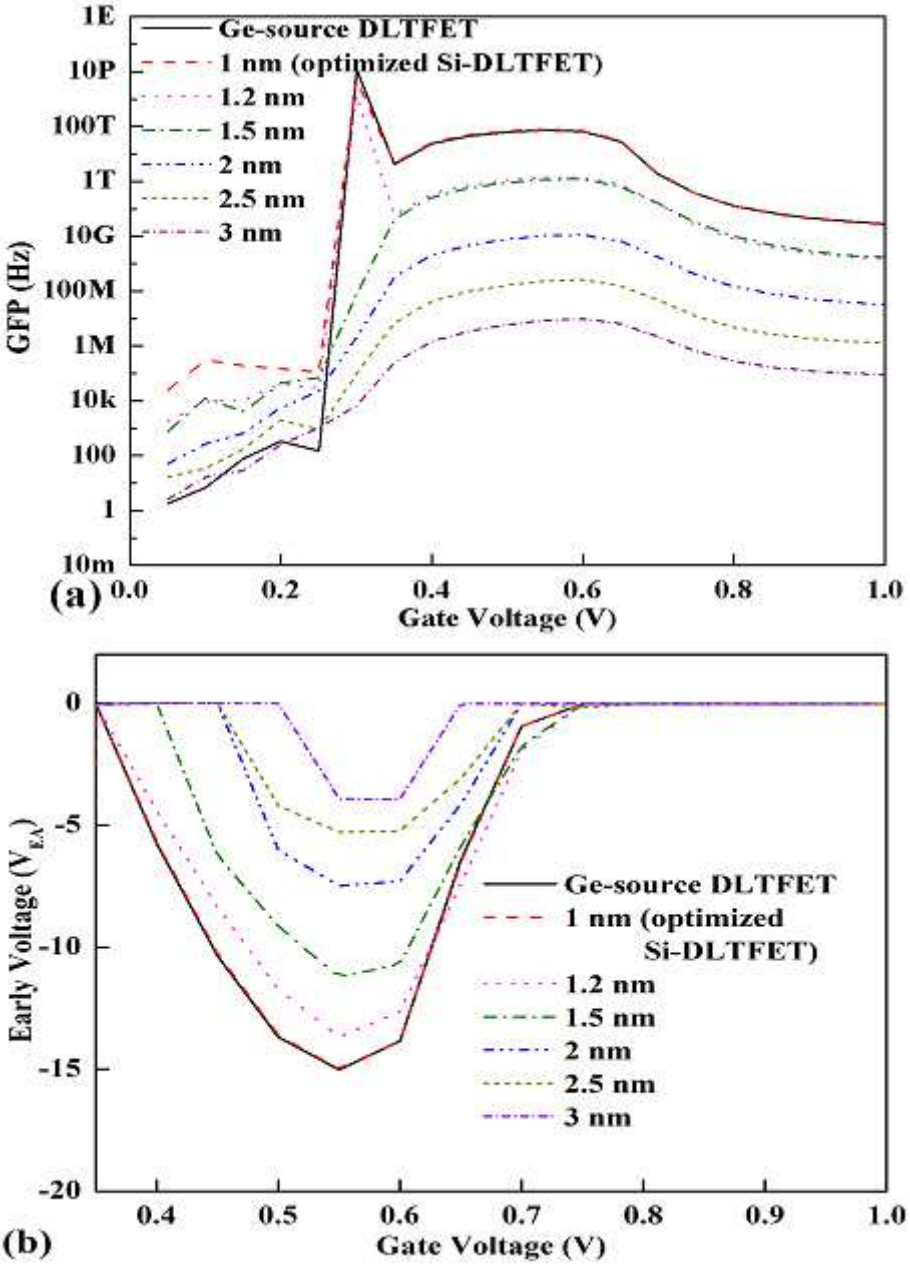

Figure 13

(a) GFP and (b) Early voltage for variation in tox with tsox = 3 nm in Si-DLTFET and for Ge-source DLTFET.

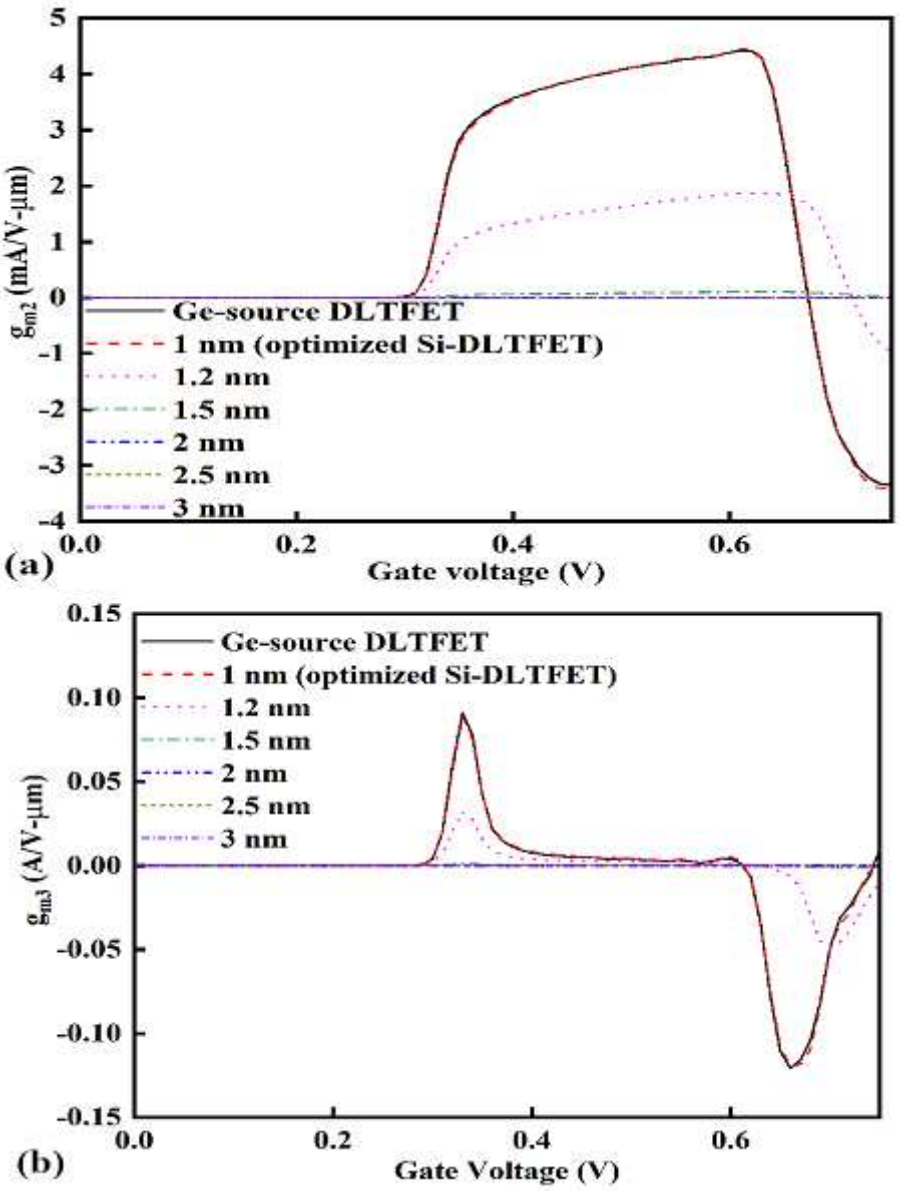

Figure 14

(a) gm2 and (b) gm3 for variation in tox with tsox = 3 nm in Si-DLTFETand for Ge-source DLTFET.

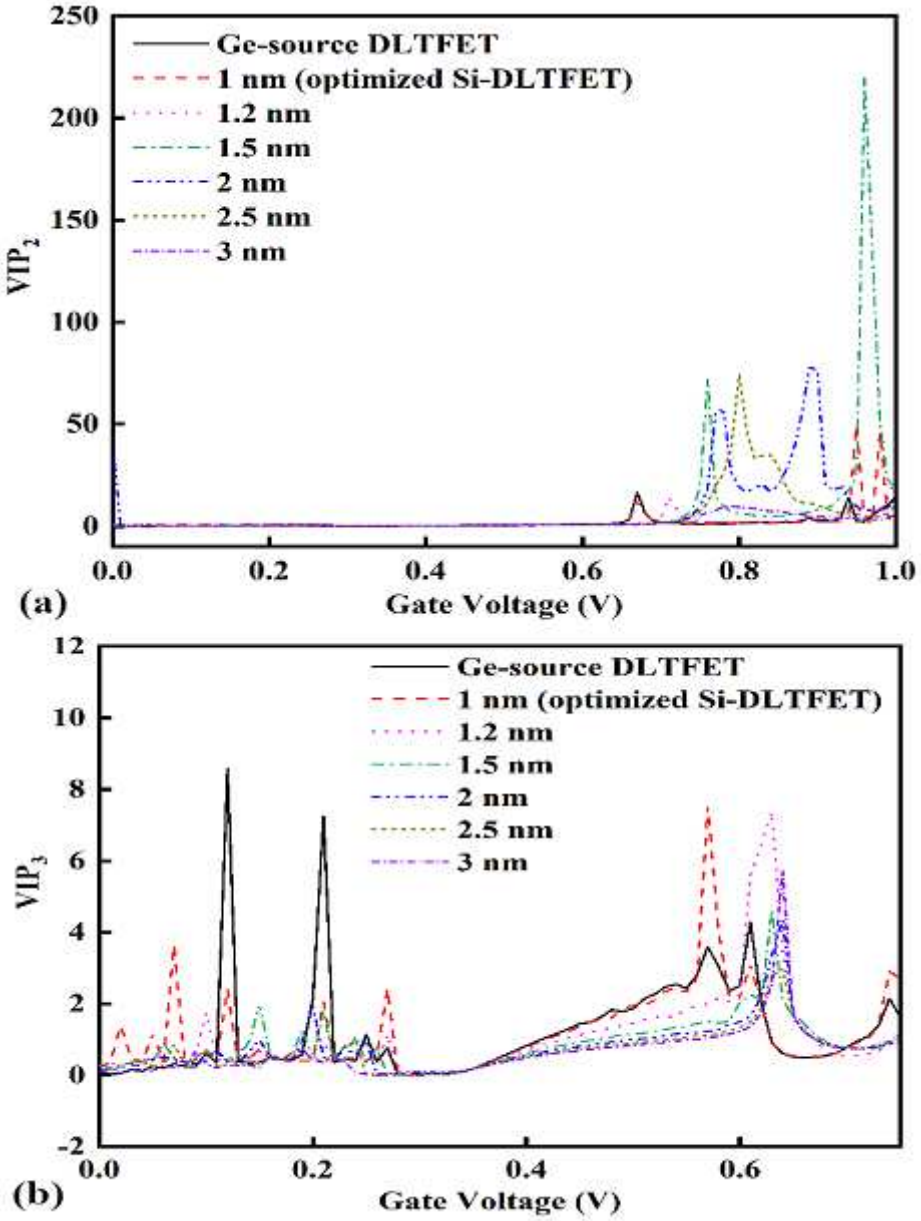

Figure 15

(a) VIP2 and (b) VIP3 for variation in tox with tsox = 3 nm in Si-DLTFETand for Ge-source DLTFET.

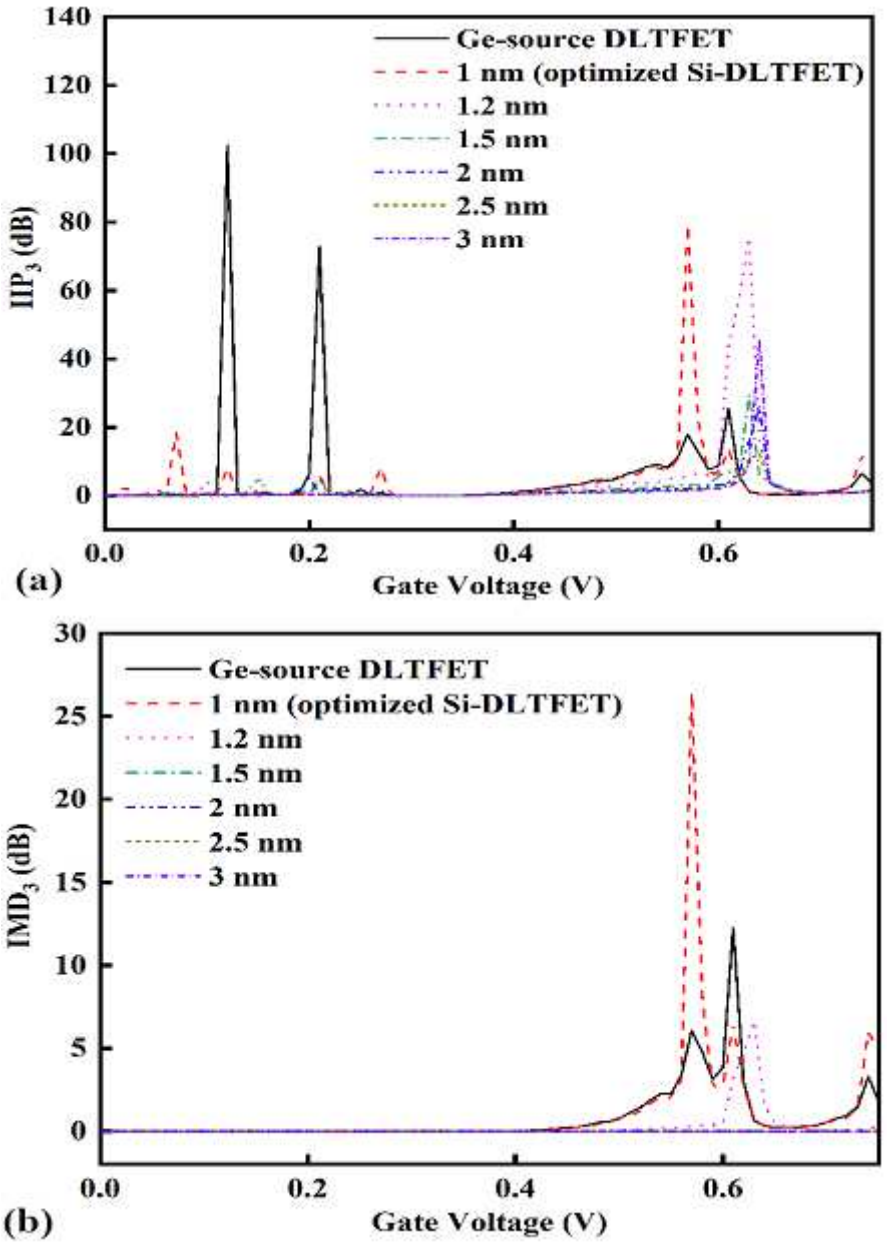

Figure 16

(a) IIP3 and (b) IMD3 for variation in tox with tsox = 3 nm in Si-DLTFETand for Ge-source DLTFET.

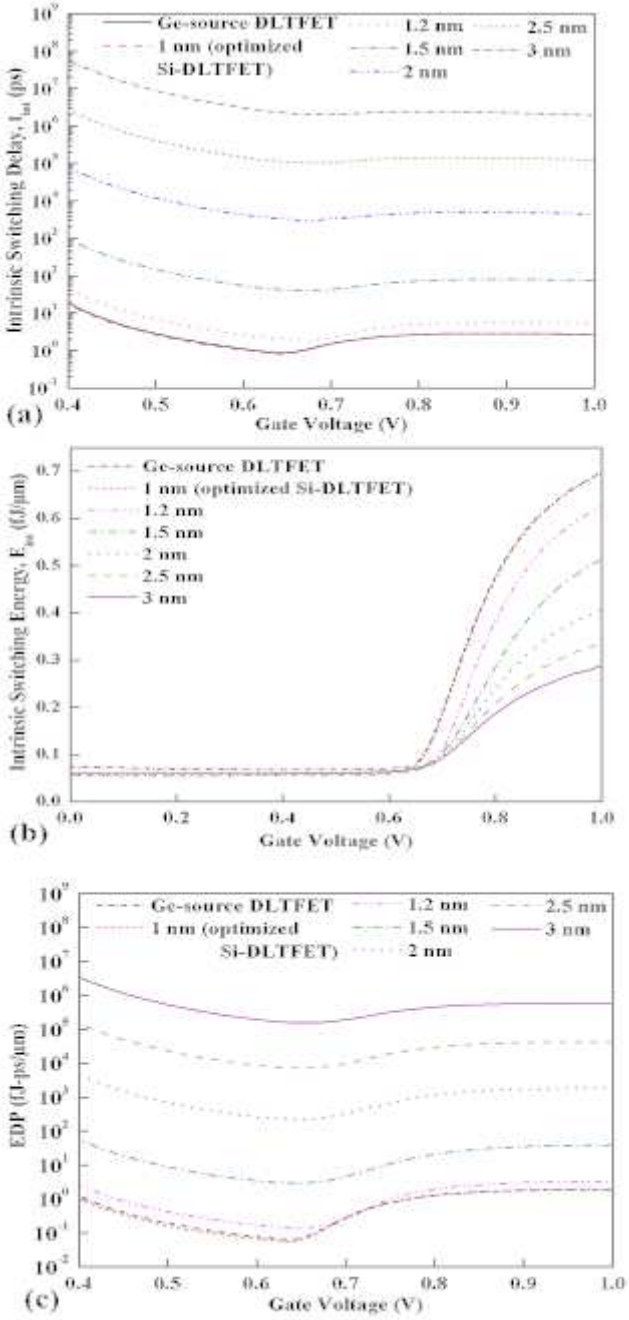

Figure 17

(a) Intrinsic time delay, (b) Intrinsic switching energy and (c) EDP for variation in tox with tsox = 3 nm in Si-DLTFET and for Ge-source DLTFET.

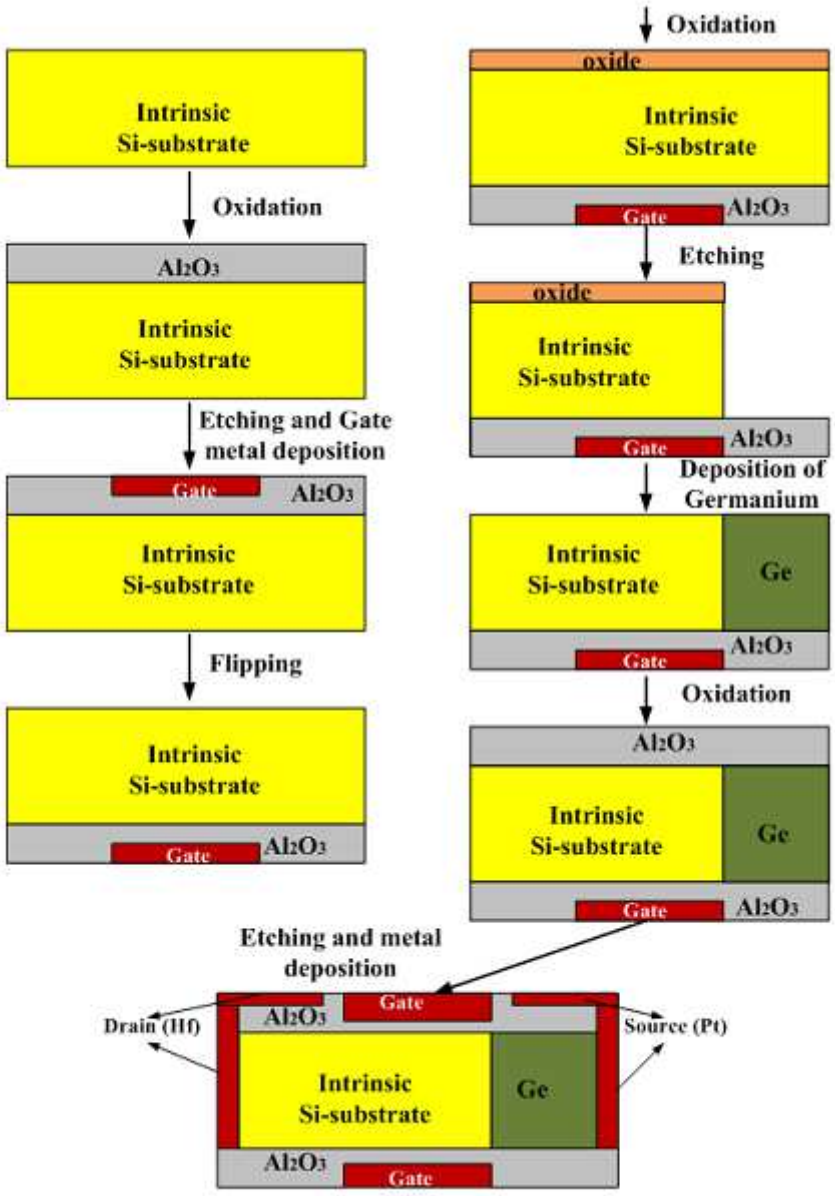

Figure 18

Proposed process ow for the fabrication of the proposed device structure (Ge-source DLTFET).