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Highly passivated TOPCon bottom cells for perovskite/silicon tandem solar cells

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Abstract:

Tunnel oxide passivating contact (TOPCon) silicon solar cells are rising as a competitive photovoltaic technology, seamlessly blending high efficiency with cost-effectiveness and mass production capabilities. However, the numerous defects from the fragile silicon oxide/c-Si interface and the low field-effect passivation due to the inadequate boron in-diffusion in p-type TOPCon (p-TOPCon) reduce their open-circuit voltages (V_{OC}s), impeding their widespread application in the promising perovskite/silicon tandem solar cells (TSCs) that hold a potential to break 30% module efficiency. To address this, we develop highly passivated p-TOPCon structure by optimizing the oxidation conditions, boron in-diffusion and aluminium oxide hydrogenation, thus pronouncedly improving the implied V_{OC} (iV_{OC}) of p-TOPCon to 715 mV and the V_{OC} of double-sided TOPCon bottom cells to 710 mV. Consequently, integrating with perovskite top cells, our proof of concept 1 cm^2 n-i-p perovskite/silicon TSCs exhibit V_{OC}s exceeding 1.9 V and a highest reported efficiency of 28.20%, which paves a way for TOPCon cells in the commercialization of future tandems.

Introduction

Perovskite/silicon tandem solar cells (TSCs) have attracted considerable attention due to their advantages in efficiency and fabrication cost. Recent advancements have propelled this type of TSCs to achieve a record efficiency of 33.9%[1]. Additionally, the shared module structures with single-junction solar cells facilitate the integration of TSCs into module production without the need for additional scaffolds and wires. Silicon solar cells with the

39 Tunnel Oxide Passivating Contact (TOPCon) structure are rising with the advantages of high
40 power conversion efficiency (> 26%)[1] and the potential for mass production upgraded from
41 existing Passivated Emitter and Rear Contact (PERC) cell production lines. These
42 advantages make TOPCon cells become a promising candidate as bottom sub-cells for
43 perovskite/silicon TSCs.

44 In the pursuit of high-efficiency TSCs, texturing the front side of the silicon cell is
45 indispensable as it could significantly reduce the refection of incident photons and extend
46 the propagation length of photons in the absorbers[2, 3, 4]. TOPCon bottom cells contribute
47 lower voltage in TSCs compared to mainstream silicon heterojunction bottom cells, which
48 could be ascribed to the weak passivation of the textured p-type side. Although p-type
49 TOPCon (p-TOPCon) structures on planar substrates have exhibited high passivation with
50 implied open-circuit voltage (iV_{OC}) over 730 mV[5, 6, 7], the p-TOPCon on textured
51 counterparts still suffer low passivation quality. This is primary due to the high defect density
52 in and/or near the ultrathin silicon oxide (SiO_x) interlayer, resulting from the high defect
53 density on textured surface before oxidation, and the formation of destroyed SiO_x and boron-
54 based clusters formed during boron in-diffusion[8]. The rounding etching process on the
55 textured surface indeed reduces surface defects but significantly enhances reflectance[7, 9].
56 Therefore, the textured surface is kept intact but an additional Si/SiO_x stack was inserted to
57 reduce boron corrosion on the SiO_x/c-Si interface[10]. With a common AlO_x/SiN_x capping
58 layer, the sample showed an iV_{OC} of 710-720 mV. Further enhancement was achieved with
59 a multilayer hydrogenation stack, effectively suppressing defect density and acquiring an
60 iV_{OC} above 720 mV. However, the additional insertion and multilayer structure increases
61 complication of production line, leading to higher costs.

62 In this work, industry-compatible fabrication methods, such as ambient-pressure
63 thermal oxidation (APTO) and in-situ plasma-enhanced chemical vapor deposition
64 (PECVD), are employed to prepare highly passivated p-TOPCon structures and double-sided
65 TOPCon bottom cells on industrial textured wafers. The use of thermal oxidation avoids
66 damages from ion-bombardment during the high-power plasma oxidation[11, 12], and in-situ
67 PECVD realizes single-side deposition and doping with high versatility. Chemical and field-
68 effect passivation are significantly promoted through mitigating ultrathin SiO_x distortion by
69 stronger oxidation, enhancing boron in-diffusion by employing a higher thermal budget, and
70 suppressing high residual defect density by strengthened hydrogenation. Consequently, the
71 iV_{OC} of p-TOPCon exceeds 715 mV with single-side saturated current density below 13
72 $fA\cdot cm^{-2}$, and the V_{OC} of bottom cell approaches 710 mV. Employing the optimized TOPCon
73 bottom cells, 1 cm^2 n-i-p monolithic perovskite/silicon TSCs achieve high V_{OC}s of 1.9 V and
74 a highest reported efficiency of 28.2%.

75

76 Results

77 High passivation of p-TOPCon on textured wafers

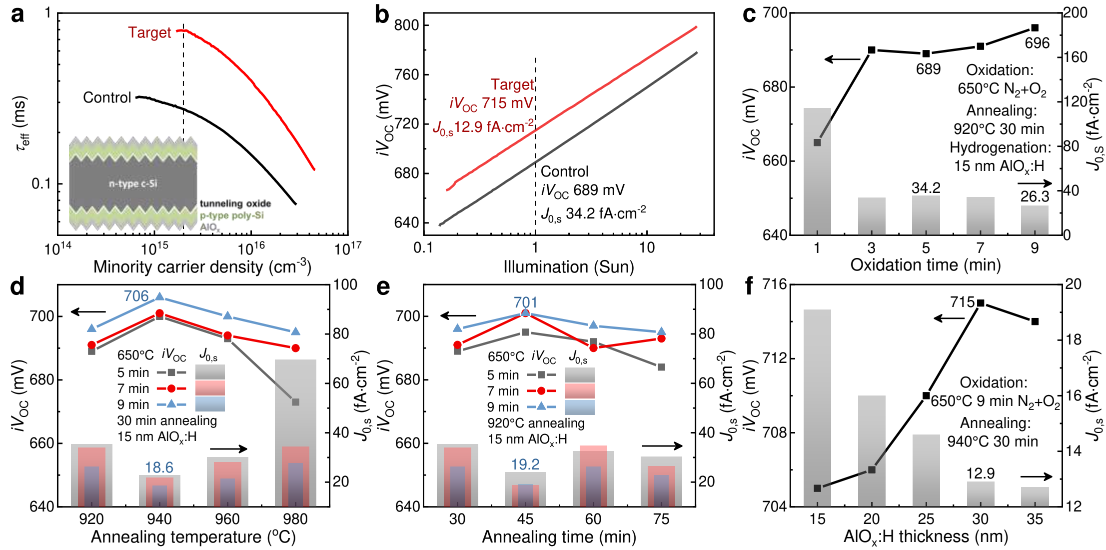


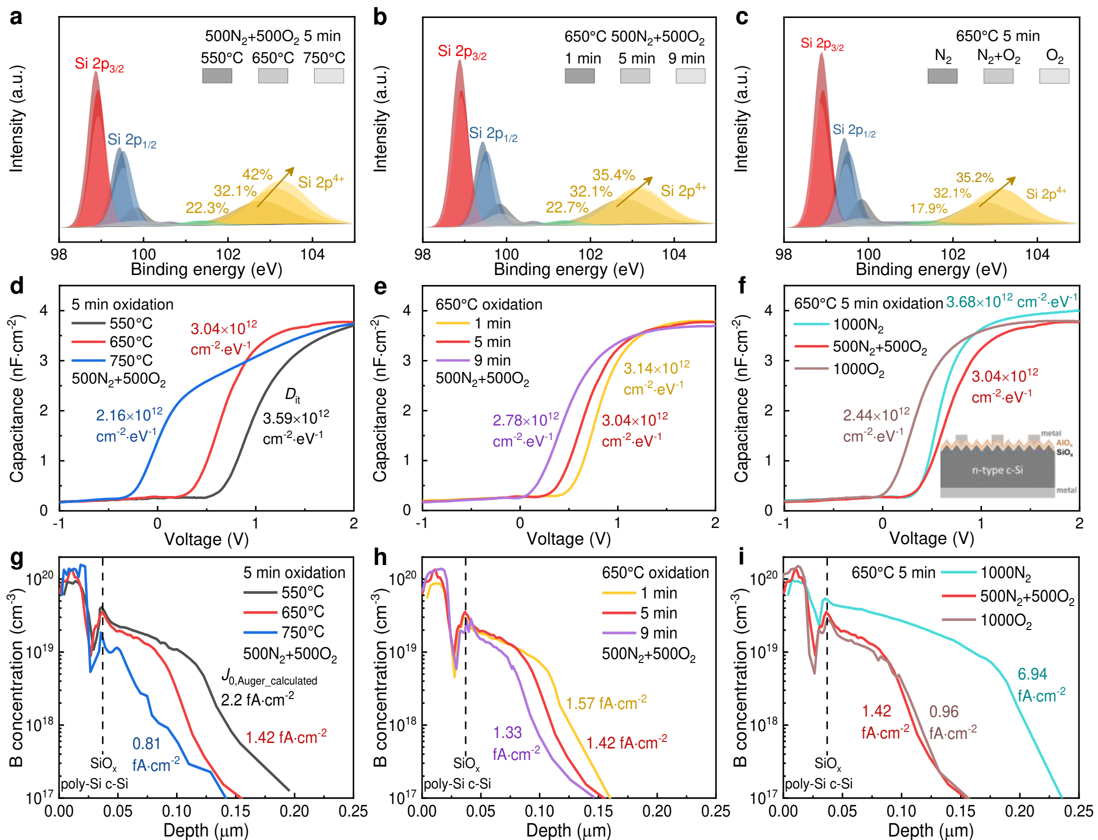
Fig. 1 (a) Effective carrier lifetime curves and (b) illumination intensity-dependent iV_{OC} curves of control (in black) and target (in red) samples. The insert in (a) is a structure sketch of double-sided p-TOPCon on textured wafers. The promotion of textured p-TOPCon passivation by optimizing processes step by step: (a) extending oxidation time, (b) elevating 30 min annealing temperature, (c) extending 920°C annealing dwell time, and (d) increasing hydrogenated AlO_x thickness. The solid curves with closed symbols are for iV_{OC} and hollow columns are for $J_{0,s}$. The added values are iV_{OC}s and corresponding $J_{0,s}$s. The "N_2+O_2" refers to 500 sccm N_2 + 500 sccm O_2.

The inserted sketch in Fig. 1a illustrates the structure of the passivation sample. The wafers were textured to form sub-micrometer-sized random pyramids on both sides, which were capped by p-type poly-Si films to form TOPCon, and followed by hydrogenated aluminum oxide (AlO_x:H) as the hydrogenation coatings. This specific pyramid size was employed to meet the requirements of perovskite top cells. Fig. 1a and b displays the effective carrier lifetime (τ_{eff}) curves over minority carrier density and iV_{OC} curves under different illustration intensities, respectively. The fabrication processes of the basic samples include a 650°C/5 min oxidation, 920°C/30 min annealing, as well as a 15 nm AlO_x:H hydrogenation, according to Refs.[7, 8, 13]. The basic sample exhibits a τ_{eff} of 300 μs and a $J_{0,s}$ of 34.2 fA·cm^{-2} at minority carrier densities of 1×10^{15} and 5×10^{15} cm^{-3}, respectively, together with an iV_{OC} of 689 mV under 1 Sun illustration. This passivation is lower than that of reference published by Hamelin in 2017[8]. To provide a clear understanding of the challenges in passivating textured c-Si wafers, these basic processes were also performed on a double-sided planar wafer, demonstrating a significantly higher passivation with an iV_{OC} of 716 mV, a $J_{0,s}$ of 5 fA·cm^{-2}, and a τ_{eff} of 1161 μs.

The optimization of the textured p-TOPCon sample can be summarized in three key aspects: varying thermal oxidation conditions for different ultrathin SiO_x layers, enhancing the thermal budget in high-temperature annealing for deeper boron in-diffusion, and capping

105 thicker AlO_x:H layers for stronger hydrogenation. As depicted in Figs. 1c and S2, a strong
106 oxidation condition results in a relatively high iV_{OC} of 690-700 mV. On the base of enhanced
107 oxidation condition, the thermal budget of high-temperature annealing was increased. Figs.
108 1d and e and S3 demonstrate that a 9 min oxidation followed by a 940°C annealing yields a
109 high iV_{OC} of 706 mV. Further extension of oxidation time had an inferior effect. Afterwards,
110 in the aluminum oxide hydrogenation process, the AlO_x:H layer thickness was increased to
111 35 nm to facilitate strong hydrogen injection. As shown in Figs. 1a and b and f, after
112 optimization the passivation level increased apparently, with an iV_{OC} of 715 mV at 1 Sun
113 illustration and a $J_{0,s}$ of 12.9 fA·cm^{-2} at the minority carrier density of 5×10^{15} cm^{-3}. The τ_{eff}
114 in the minority carrier density of 2×10^{15}-3×10^{16} cm^{-3} is also largely higher than the basic one.
115 After capping with silicon nitride (SiN_x), the iV_{OC} further increased to 716 mV. This is the
116 highest passivation level of the p-TOPCon structure on a textured wafer based on *ex-situ*
117 oxidation and *in-situ* doped amorphous silicon, only slightly lower than that of *in-situ* thermal
118 oxidation in an LPCVD facility[10]. This data is tagged as the pink circle in Fig. S1.
119

120 **Passivation mechanism and characteristics**

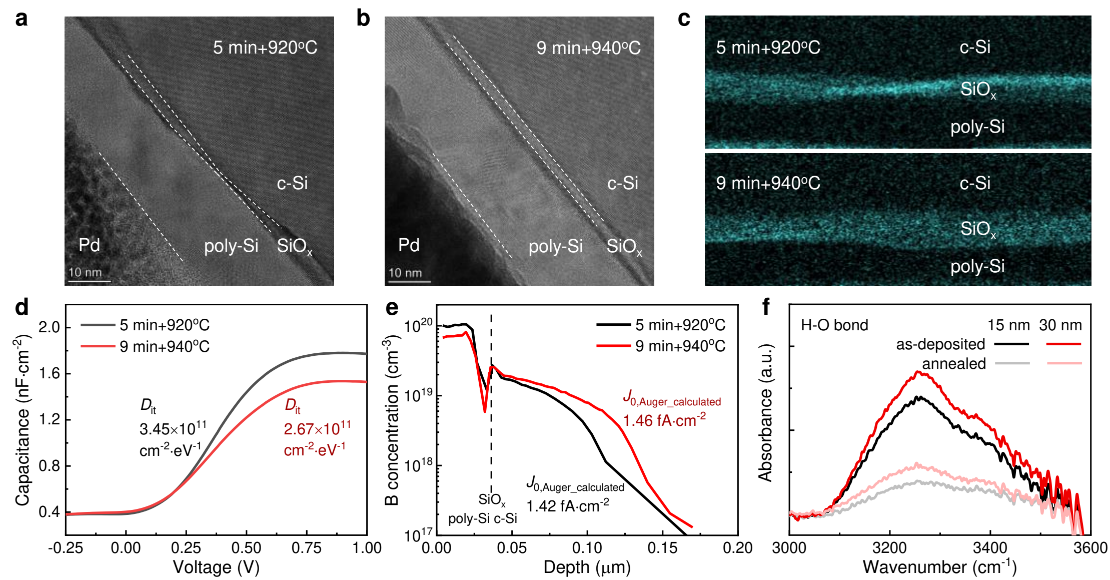


121

122 Fig. 2 The influence of oxidation temperature (left column), oxidation time (middle column), and oxidation
123 ambient (right column) on (a-c) Si chemical state in SiO_x, (d-f) interface state density at SiO_x/c-Si, and (g-
124 i) boron in-diffusion profile. The "N_2+O_2" in c refers to 500 sccm N_2 + 500 sccm O_2. The inserted sketch in

125 f shows sample structure for *C-V* test. The "$J_{0,Auger_calculated}$" in g represents Auger recombination rate

126 calculated using in-diffusion profiles in c-Si.



127

128 Fig. 3 TEM images of Pd/poly-Si/SiO_x/c-Si structures on incline facets of textured wafers for (a) basic and

129 (b) optimized samples, and (c) their local EDS images of O distribution. The comparisons of (d) *C-V* curves,

130 (e) boron in-diffusion profiles, and (f) O-H peaks in AlO_x:H films of basic and optimized samples.

131

132 Firstly, we conduct a comparison of the thicknesses and integration of ultrathin SiO_x

133 layers on textured wafers. For spectroscopic ellipsometry analysis, polished wafers with

134 (111)-orientation were used to redraw the oxide formation on the inclined plane of the

135 textured surface. Table S2 displays the calculated thickness of SiO_x under diverse oxidation

136 conditions, revealing a gradual increase in SiO_x thickness on the (111) wafer with stronger

137 oxidation. Though the calculated thickness may not be highly accurate, it is enough to show

138 the trend in SiO_x thickness. Furthermore, the TEM images in Fig. S4b-d depict that for a 5

139 min oxidation, the SiO_x on textured surface is thinner, less uniform in thickness, and exposes

140 silicon to metal directly at some positions. In contrast, the SiO_x on the planar surface is more

141 uniform in thickness and covers silicon the surface more completely, as shown in Fig. S4a.

142 This observation is in accordance with previous studies[14, 15], suggesting that a strong

143 oxidation process may be necessary to form a thick SiO_x layer with higher uniformity in

144 thickness, providing enhanced protection to the textured silicon surface. The TEM image in

145 Fig. S4f indicates that a 9 min oxidation results in a thicker SiO_x layer than the 5 min oxidated

146 case in Fig. S4c, and it more conformally segregates the wafer surface from the metal Pd.

147 Additional morphology of the 9 min SiO_x on valleys and tips can be found in Fig. S4e-g.

148 Following high-temperature annealing, the 9 min SiO_x remains more uniform and

149 consecutive than the 5 min one, as shown in Fig. 3a and b. The corresponding energy disperse

150 spectroscopy (EDS) mappings of oxygen indicate that during annealing, oxygen diffuses into

151 the adjacent silicon to passivate dangling bonds, and the 9 min SiO_x results in a more uniform
152 diffusion, which contributes to higher passivation.

153 The chemical state of Si in ultrathin SiO_x was checked *via* XPS on SiO_x formed directly
154 on textured wafers. The deconvoluted Si spectra for various oxidation conditions are
155 exhibited in Fig. 2a-c, which shows the oxidation conditions and the corresponding
156 calculated Si^{4+} peak area ratios. Obviously, a higher oxidation temperature, a longer
157 oxidation time, or a higher oxygen ratio leads to a higher Si^{4+} peak proportion, such as 22.7%,
158 32.1%, and 35.4% for 1, 5, and 9 min oxidation, respectively, meaning an increased Si^{4+}
159 concentration in SiO_x. Additionally, a stronger oxidation causes the Si^{4+} peak to shift to a
160 higher binding energy (BE), as indicated by the black arrows. This suggests that the SiO_x
161 layer is more robust after a strong oxidation. It can be deduced that SiO_x formed through
162 enhanced oxidation may be stronger in resisting distortion or damage on SiO_x during high
163 temperature annealing, leaving fewer carrier recombination centres near the SiO_x/c-Si
164 interface.

165 Subsequently, the fixed charge density (Q_f) and interface state density (D_{it}) of the
166 SiO_x/c-Si interface was measured and evaluated using 1 MHz capacitance-voltage (*C-V*) and
167 conductance-voltage (*G-V*) curves for various oxidation conditions on textured wafers. The
168 Q_f and D_{it} were calculated using the data obtained from *C-V* and *G-V* curves with equations
169 1 and 2[16, 17], respectively:

170 $$Q_f = \frac{C_{ox}}{A}\left(\Phi_{ms} - V_{fb}\right) \quad (1)$$

171 $$D_{it} = \left(\frac{2}{qA}\right)\frac{\frac{G_{m,max}}{\omega}}{\left(\frac{G_{m,max}}{\omega\, C_{ox}}\right)^2 + \left(1 - \frac{C_m}{C_{ox}}\right)^2} \quad (2)$$

172 where C_{ox} is the high capacitance plateau of the oxide interlayer, Φ_{ms} is the difference in
173 metal and semiconductor working functions, V_{fb} is the flat band voltage, A is the aera of the
174 metal disk, q is the electron element, $G_{m,max}$ is the measured highest conductance, ω is the
175 angular frequency, and C_m is the capacitance corresponding to the measured highest
176 conductance. The *C-V* curves and corresponding D_{it} values in terms of oxidation conditions
177 are plotted in Fig. 2d-f. With similar C_{ox}, the *C-V* curve shifts to a lower voltage position for
178 stronger oxidation, leading to a lower V_{fb} and thus lower Q_f of the ultrathin SiO_x/AlO_x stack.
179 This suggests that stronger oxidation results in fewer defects at the SiO_x/c-Si interface. The
180 evaluated D_{it} values may show this trend more directly, with 3.04×10^{12} $cm^{-2}\cdot eV^{-1}$ for 5 min
181 oxidation (in red line) verses 2.78×10^{12} $cm^{-2}\cdot eV^{-1}$ for 9 min oxidation (in yellow line) for
182 example. A higher oxidation temperature or O_2 ratio also yields a remarkable decrease in D_{it}.
183 After high-temperature annealing, as plotted in Fig. 3d, D_{it} decreases significantly by an
184 order of magnitude, and D_{it} of the optimized sample is lower than that of the basic one,
185 reaching 2.67×10^{11} $cm^{-2}\cdot eV^{-1}$. This suggests that 9 min SiO_x plus 940°C annealing is

186 effective in eliminating more defects on the textured c-Si surface, yielding a higher chemical
187 passivation effect.

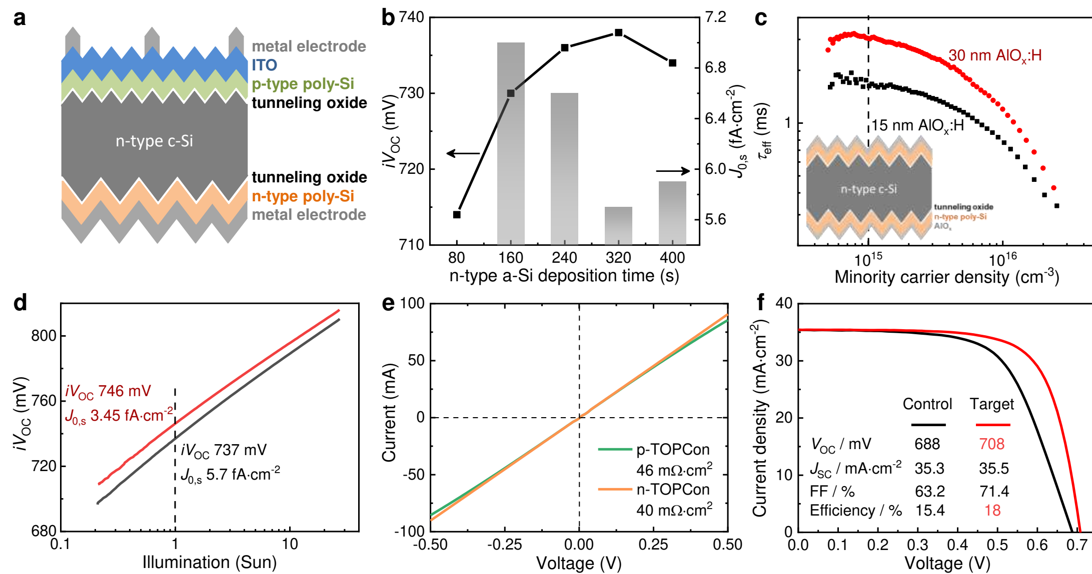
188 In addition to the analysis of the SiO_x layer or SiO_x/c-Si interface, one key property of
189 the TOPCon structure is the dopant in-diffusion profile obtained by electrochemical
190 capacitance-voltage (ECV) measurement. It shows the active dopant concentration at a
191 specific depth, which helps to study of the field-effect and chemical passivation. Fig. 2g-i
192 displays the doping profiles of textured samples with enhanced oxidation strength after
193 920°C annealing, together with their corresponding Auger recombination rates
194 ($J_{0,Auger_calculated}$) calculated based on profiles in c-Si using the EDNA2 program in PV
195 Lighthouse[18, 19]. All of them exhibit the trend that stronger oxidation results in a lower depth
196 of boron in-diffusion in c-Si, suggesting fewer boron dopants penetrate ultrathin SiO_x. This
197 means less damage to SiO_x, benefiting chemical passivation. Moreover, a shallow dopant in-
198 diffusion may simultaneously reduce $J_{0,Auger_calculated}$, improving the effective carrier
199 lifetime[19]. However, the low active boron concentration in c-Si beneath SiO_x may allow more
200 photo-generated electrons to reach the defect-rich SiO_x/c-Si interface, accelerating carrier
201 recombination[20, 21, 22]. At the same time, a lower boron in-diffusion depth may produce a
202 higher contact resistivity, inhibiting the extraction of generated carriers. Therefore,
203 annealing temperature and dwell time were increased based on strengthened oxidation to
204 explore a balance of chemical passivation, field-effect passivation, and contact resistivity.
205 The comparison of boron in-diffusion profiles between basic and optimized samples can be
206 found in Fig. 3e. With low D_{it} from 9 min SiO_x, 940°C annealing leads to deeper boron in-
207 diffusion, which may provide high passivation in both chemical and field-effect aspects.
208 Besides, the calculated $J_{0,Auger_calculated}$ increases only slightly by 0.04 $fA \cdot cm^{-2}$, having a
209 negligible impact on passivation. These factors may be responsible for the high performance
210 of the optimized sample with an iV_{OC} of 706 mV, and a $J_{0,s}$ of 18.6 $fA \cdot cm^{-2}$.

211 It could be deduced from the evolution of p-TOPCon that hydrogenation after high temperature
212 annealing also plays a crucial role in achieving high-level passivation. Therefore, the thickness of
213 the AlO_x:H layer was increased by performing more cycle numbers during ALD to provide
214 sufficient H for passivating p-TOPCon on the textured surface. The cross-sectional SEM images in
215 Fig. S5 of the c-Si/SiO_x/poly-Si/AlO_x:H stacks confirm that a higher ALD cycle number indeed
216 improves AlO_x:H thickness to ~30 nm on the inclined facet of a pyramid. The AlO_x:H layer on the
217 valley or tip also becomes thicker. This guarantees sufficient passivation effect for different parts
218 of the textured surface. Furthermore, as the FTIR data shown in Fig. 3f, the as-deposited 30 nm-
219 thick AlO_x:H layer possesses a larger O-H bond peak than the 15 nm one, and this peak collapses
220 drastically after annealing, meaning that a large number of hydrogens are released to passivate
221 defects[23, 24]. Consequently, the 30 nm-thick AlO_x:H layer attributes to achieve the summit
222 passivation.

223 The V_{OC} of a c-Si solar cell can be expressed by a single diode equation[25, 26, 27, 28]:

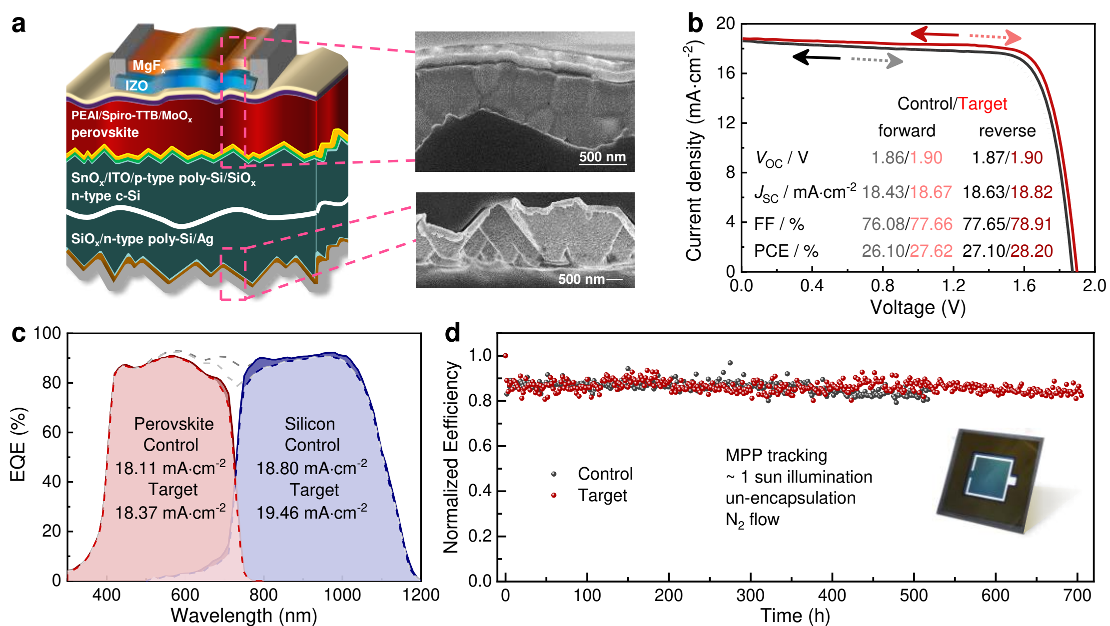
224 $$V_{OC} = \frac{nkT}{q}\ ln\left(\frac{J_L}{J_{0,bulk} + J_{0,emitter} + J_{0,front} + J_{0,rear}} + 1\right) \quad (3)$$

225 where J_L is the illuminated current density, $J_{0,\mathrm{emitter}}$ is the saturated current density of the
226 emitter, $J_{0,\mathrm{bulk}}$ is the saturated current density in the wafer bulk, and $J_{0,\mathrm{front}}$ or $J_{0,\mathrm{rear}}$ is the
227 saturated current density on the front or rear surface. It can be deduced that for a certain
228 temperature, light absorption, c-Si substrate, and p-n junction, a high surface saturated
229 current density, *i.e.*, a high surface carrier recombination rate, will lead to a low V_{OC} for a
230 TOPCon cell. Referring to equation 1, we can evaluate or predict the V_{OC} of a bottom cell to
231 some extent. Under the assumptions that the incident light intensity, the carrier
232 recombination rate in the wafer bulk, and n-TOPCon passivation are stable, the V_{OC}, or the
233 whole passivation, of a bottom cell can be mainly decided by p-TOPCon passivation. The
234 parameters are defined as J_L = 35 mA·cm^{-2}, $J_{0,\mathrm{bulk}}$ = 10 fA·cm^{-2}, $J_{0,\mathrm{n\text{-}TOPCon}}$ = 5 fA·cm^{-2}, and
235 the test temperature is 300 K. For a p-TOPCon with low passivation, the $J_{0,\mathrm{p\text{-}TOPCon}}$ may be
236 40 fA·cm^{-2}, which leads to an V_{OC} of ~703 mV. When $J_{0,\mathrm{p\text{-}TOPCon}}$ decreases to 15 fA·cm^{-2},
237 the calculated V_{OC} will reach ~718 mV.
238
239 **Double-sided TOPCon bottom cells**



240
241 Fig. 4 (a) Schematic structure of an independent n-i-p type double-sided TOPCon bottom cell with sub-micrometer-
242 sized pyramids on the front side and industrial micrometer pyramids on the rear side, respectively. (b) The iV_{OC} and
243 $J_{0,s}$ of n-TOPCon with different a-Si deposition times on industrially textured wafers. (c) Effective carrier lifetime
244 curves and (d) illumination intensity-dependent iV_{OC} curves of 320 s n-TOPCon hydrogenated by 15 nm (in
245 black) and 30 nm (in red) AlO_x:H. The insert in (c) is the structure sketch of double-sided n-TOPCon on
246 textured wafers. (e) *I-V* curves for the optimized p-type (in green) and n-type (in red) TOPCon for the
247 independent bottom cell. (f) The *J-V* curves of basic and optimized independent bottom cells.
248
249 Fig. 4a depicts the structure sketch of an independent n-i-p type double-sided TOPCon bottom
250 cell. The front side features basic or optimized p-TOPCon on a sub-micrometer-sized pyramid

251 textured surface, capped by a thick ITO layer and a grid metal electrode for carrier lateral collection.
252 The rear side incorporates an n-TOPCon on a micrometer-sized pyramid textured surface, capped
253 by a full area metal electrode. To identify the n-TOPCon with high passivation and low contact
254 resistivity, the deposition time of n-type amorphous silicon (a-Si) was tuned from 80 to 400 s,
255 followed by a 940°C annealing and a 15 nm-thick AlO_x:H hydrogenation. As displayed in Fig. 4b-
256 d, sample with a deposition time of 320 s yields an iV_{OC} of 737 mV and a $J_{0,s}$ of 5.7 fA·cm^{-2}. With
257 the optimized 30 nm-thick AlO_x:H hydrogenation, the iV_{OC} and $J_{0,s}$ of the n-TOPCon passivation
258 sample reach 746 mV and 3.45 fA·cm^{-2}, respectively. The low $J_{0,s}$ of n-TOPCon together with highly
259 passivated p-TOPCon contribute to high passivation of bottom cell. Fig. 4e plots the current-voltage
260 (*I-V*) curves of the optimized p- and n-TOPCon measured using Cox-Strack method[29]. The straight
261 curves mean that both TOPCon structures show ohmic contacts, and the p- and n-TOPCon offers
262 contact resistivities of 46 and 40 mΩ·cm^2, respectively. As a result, the independent bottom cells
263 with basic and optimized p-TOPCon structures exhibit *J-V* curves with obvious difference,
264 especially in open-circuit voltage and fill factor, as shown in Fig. 4f. The V_{OC} of the optimized
265 bottom cell is 20 mV higher than the basic one, which may result from a 25 mV difference in iV_{OC}
266 between control and target p-TOPCon as discussed in Fig. 1, as well as a 9 mV increase in iV_{OC} of
267 the n-TOPCon. Additionally, the contact resistivity values of 920°C annealed p- and n-TOPCon
268 may be relatively high, which explain the low fill factor of the basic cell. In summary, the optimized
269 p-TOPCon passivation, coupled with the fabrication process, endows the bottom cell with a
270 marginally increased efficiency.
271
272 **n-i-p monolithic perovskite/silicon TSCs**



273

274 Fig. 5 (a) Sketch structure (left) and cross-sectional SEM images (right) of the optimized tandem device.
275 The scale bars are 500 nm. (b) *J-V* curves and (c) EQE spectra of the two related TSCs. (d) MPP tracking
276 stability of TSCs with the basic and optimized TOPCon bottom cells.

277

278 After demonstrating the effectiveness of the improvements in p-TOPCon and
279 independent Si bottom cell, we fabricated n-i-p type monolithic perovskite/silicon TSCs
280 using the optimized bottom cells (See Experimental Section for more details). The schematic
281 view and cross-sectional SEM images of the TSCs are shown in Fig. 5a. Consequently, a
282 champion efficiency of 28.20% with an V_{OC} of 1.90 V, a fill factor (FF) of 78.91% and a
283 short-circuit current density (J_{SC}) of 18.82 $mA \cdot cm^{-2}$ in 0.9226 cm^2 aperture area was
284 obtained for the optimized device in our laboratory tests (Fig. 5b). Statistics of the
285 photovoltaic parameters imply the improved performance and reproducibility with the
286 optimized bottom cells (Fig. S6). Another tandem cell was sent to Shanghai Institute of
287 Microsystem and Information Technology (SIMIT) for authoritative certification and
288 achieved 27.31% (25.69%) efficiencies with over 1.91 V V_{OC}s in reverse (forward) voltage
289 scanning directions (Fig. S7). Fig. 6c exhibits the external quantum efficiencies (EQEs) and
290 the integrated currents of the champion tandem devices. A 0.26 and 0.66 $mA \cdot cm^{-2}$ integrated
291 current increase is unveiled for perovskite top cell and optimized silicon bottom cell,
292 respectively, which is consistent with the J_{SC} from the J-V measurements. Meanwhile,
293 maximum power point (MPP) tracking tests were conducted to monitor the operation
294 stability of the encapsulated tandems under ~1 sun LED illumination. As shown in Fig. 5d,
295 both types of the tandems demonstrate impressive longevities over 500 h, which indicates
296 the commercialized potential of our tandem devices.

297

298 Discussion

299 In this work, a highly passivated p-TOPCon structure on randomly textured industrial
300 wafers was achieved using industry-compatible techniques, which leads to a high efficiency
301 of an n-i-p type monolithic perovskite/Si TSCs. The enhanced thermal oxidation condition
302 forms more uniform ultrathin SiO_x on textured silicon surface with higher Si^{4+} concentration
303 and blue shift in binding energy, as well as lower interface state density at SiO_x/c-Si. This
304 endows SiO_x with weaker distortion and lower recombination centres after high-temperature
305 annealing, thus resulting in higher chemical passivation. The increased thermal budget of
306 high-temperature annealing deepens boron in-diffusion, which promotes field-effect
307 passivation soundly but Auger recombination slightly. Furthermore, a strengthened
308 hydrogenation process was performed *via* increasing AlO_x:H thickness, passivating more
309 defects and leaving fewer recombination centres a step further after hydrogen injection. As
310 the consequence, the iV_{OC} of p-TOPCon increased to 715 mV, which is the summit
311 passivation for the textured p-TOPCon using *ex-situ* oxidation. Based on the optimized
312 double-sided TOPCon bottom cell, the perovskite/Si TSCs exhibit a high open-circuit
313 voltage of 1.9 V and a remarkable efficiency of 28.2%, which is the top-ranking level for n-
314 i-p type monolithic perovskite/silicon TSCs currently.

315

316 # Methods

317 **Preparation and characterization of passivation samples**

318 The crystalline silicon wafers used in this study were industrial n-type Cz wafers with
319 (100) oriental. The double-side textured wafers with ~155 μm thickness, ~0.8 Ω·cm
320 resistivity, and pyramid size below 1 μm (sub-micrometer-size) (Fig. S8a) were prepared *via*
321 an industrial texturing technique in the lab. Such pyramid size was chosen for the
322 convenience of the fabrication of perovskite top cell. After standard RCA cleaning, ultrathin
323 silicon oxide layers were prepared *via* thermal oxidation on both sides of the wafers. The
324 oxidation conditions were tuned in three dimensions, *i.e.*, temperature (550-750°C), duration
325 time (1-9 min), and oxygen proportion (0-100%). Then, ~40 nm-thick boron doped
326 amorphous silicon was deposited on both sides of wafers using PECVD. Afterwards, high
327 temperature annealing was performed to facilitate silicon crystallization as well as boron
328 diffusion and activation, which was followed by *in-situ* wet nitrogen hydrogenation[30]. The
329 borosilicate glass (BSG) films above poly-Si were removed by dipping in diluted HF
330 solution. Additional hydrogenation process was performed *via* hydrogenated alumina oxide
331 (AlO_x:H) deposition in an atomic layer deposition system (ALD), followed by vacuum
332 annealing in a tube furnace. Finally, silicon nitride (SiN_x) coatings were deposited on both
333 sides of the wafer by PECVD.

334 The passivation properties of planar and textured samples were characterized by
335 implied open-circuit voltage (iV_{OC}) and single-side saturated current density ($J_{0,s}$), which
336 were obtained by Sinton WCT-120 lifetime tester[31, 32, 33]. The contact resistivity of the
337 optimized sample with single-sided p-TOPCon on a textured surface was measured referring
338 the Cox-Strack method[29]. Active boron concentration profiles in poly-Si and c-Si were
339 measured based on the electrochemical capacitance-voltage method (ECV) by WEP Wafer
340 Profiler CVP21[34, 35]. Nano- or micro-structures of samples were observed by scanning
341 electron microscopy (SEM) using Hitachi Regulus 8230.

342 The characterizations of ultrathin SiO_x layer and SiO_x/c-Si interface include the
343 thickness, integrity, and chemical state of SiO_x layer, and the residual interface state density
344 (D_{it}) of SiO_x/c-Si interface. The SiO_x was prepared on polished (111)-oriented wafers for
345 spectroscopic ellipsometry (SE) on Woollam Complete EASE equipment, and on textured
346 wafers for TEM observation on Talos F200X. The measurements of chemical state of SiO_x
347 and D_{it} of SiO_x/c-Si were performed toward the structure of SiO_x above textured wafers, *via*
348 X-ray photoelectronic spectroscopy (XPS) on Axis Ultra DLD and capacitance-voltage
349 method (*C-V*)[17] on Keysight B1500A, respectively. The H content in AlO_x:H film was
350 represented by the integrated area of O-H bond peak, which was measured *via* Fourier
351 Transform infrared spectroscopy (FTIR) on THermo NICOLET 6700.

352

353 **Fabrication and test of TOPCon bottom cells**

354 The c-Si bottom cells with double-sided TOPCon were prepared based on double-side
355 textured n-type Cz (100)-oriental wafers. The bottom cell for tandem cell fabrication has a
356 2.5×2.5 cm^2 wafer size and 1×1 cm^2 work area, while the one for checking bottom cell
357 performance has a 4×4 cm^2 wafer size and 2.2×2.2 cm^2 work area. Initially, SiN_x protection
358 layer was deposited on the textured surface of a single-sided industrially textured wafer (Fig.
359 S8b), which was followed by the texturing process to form a textured surface with pyramid
360 size below 1 μm. Then, the SiN_x protection layer was removed by dipping in diluted HF
361 solution. For the convenience of top cell fabrication, the side with a pyramid size below 1
362 μm was defined as the front side, while another side with industrial large pyramids was the
363 rear side. After RCA cleaning, ultrathin silicon oxide layers were formed *via* thermal
364 oxidation under optimized condition on both sides of wafers. Then, boron-doped amorphous
365 silicon (p^+ a-Si) and phosphorus-doped amorphous silicon (n^+ a-Si) were deposited on the
366 front and rear side, respectively, by PECVD. The following processes were high-temperature
367 annealing, wet nitrogen hydrogenation, AlO_x hydrogenation, and SiN_x deposition, which
368 were similar to symmetric passivation samples. The iV_{OC} and effective carrier lifetime were
369 measured by Sinton WCT-120 lifetime tester[31, 32, 33]. Then, SiN_x/AlO_x stack above the work
370 area was removed by HF dipping. After that, ~10 nm-thick indium tin oxide (ITO) was
371 deposited on the front side as intermediate layer for the 2.5 cm wafer, but ~100 nm-thick
372 ITO as a carrier collection layer for 4 cm wafer. The ITO film was prepared by physical
373 vapor deposition (PVD). The passivation dropped drastically after ITO preparation, but it
374 was recovered by forming gas annealing (FGA). Afterwards, the work area on the rear side
375 was fully covered by a ~100 nm-thick Ag metal electrode prepared by thermal evaporation.
376 Here, an additional process was applied on the 4 cm wafer to form a stack of Al/Ag metal
377 electrode with a grid and fingers above the ITO film using evaporation through a shadow
378 mask. The passivation of the cell sample was monitored by photo-luminescence (PL) after
379 AlO_x hydrogenation and subsequent steps. The performance of the bottom cells, including
380 V_{OC}, J_{SC}, FF, and efficiency (η), was tested by a 4-wire solar cell tester consisting of a
381 Keithley 2400 source meter and a Class AAA solar simulator produced by EnliTech Co.,
382 Ltd, which provided a light intensity of 100 $mW\cdot cm^{-2}$.
383
384 **Fabrication and test of perovskite/silicon TSCs**
385 To fabricate perovskite/silicon TSCs, a 12 nm-thick SnO_2 layer were deposited on the
386 top of silicon bottom cells by a 150-cycle thermal ALD (KE-MICRO, PE ALD-F50R) with
387 the chamber at 120°C and Tetrakis(dimethylamino)tin(IV) (TDMASn) source at 80°C.
388 TDMASn/purge1/H_2O/purge2 times were 0.4/5/1.5/15 s with a constant 90-sccm nitrogen
389 flow. After UV-ozone treatment of the ALD-SnO_2 layer, a SnO_2 nanocrystal solution (Alfa
390 Aesar, 15%) diluted ten times with a mixed deionized water and ethanol (1:1, vol:vol) was
391 dynamically spin-coated on the first SnO_2 layer at 5000 rpm for 35 s. Then, 150°C-30 min
392 post-annealing and 15 min UV-ozone treatment were conducted. A 1.7 M

393 $Cs_{0.05}FA_{0.8}MA_{0.15}Pb(I_{0.75}Br_{0.25})_3$ perovskite precursor solution, fully dissolved into a mixed
394 solvent system comprising anhydrous DMF/DMSO (4:1, vol:vol), was then spin-coated at
395 600/2000/8000 rpm for 6/54/15 s, and 300 μL chlorobenzene as an anti-solvent was dropped
396 onto the center of the substrate 10 s before the end of the rotation procedure. The perovskite
397 absorber layer was annealed at 105°C for 15 minutes. A 5 mg·mL^{-1} PEAI in isopropanol was
398 dynamically spin-coated on the perovskite upper surface at 5000 rpm for 35 s. Spiro-TTB
399 doped with F4-TCNQ as the hole transport layer was thermally evaporated to a 20 nm
400 thickness with a ~14.3 wt.% doping ratio. For the front transparent electrode, 15 nm-thick
401 MoO_x and 100 nm-thick IZO were deposited by thermal evaporation at a 0.2 Å·s^{-1} rate and
402 RF sputtering under a 45 W power, respectively. Silver was evaporated through a shadow
403 mask to a 300 nm thickness with a 1×1 cm^2 active area. Finally, a 100 nm-thick MgF_x was
404 thermally evaporated as the antireflection layer.
405 The cross-sectional SEM images of TSCs were collected using a field-emission
406 scanning electron microscopy (S-4800, Hitachi). The *J-V* measurements were performed
407 through a digital source meter (Keithley 2400) and a solar simulator (94022A, Newport)
408 with illumination calibrated by a standard silicon cell (Bunkoukeiki, BS-520BK). The curves
409 were achieved both in reverse (2.0 to -0.1 V) and forward (-0.1 to 2.0 V) voltage scanning
410 modes with 200 data points. EQE measurements were carried out through a QE system
411 (QEX10, PV measurement, Inc). For perovskite top cell measurement, an infrared light-bias
412 LED with 850 nm peak emission was used to saturate the silicon bottom cells, and a 0.6 V
413 bias voltage was used to build almost short-circuit conditions. For silicon bottom cell
414 measurement, a blue light-bias LED with a 455 nm peak emission was used to saturate the
415 perovskite top cells and a 1 V bias voltage was applied to build an almost short circuit
416 condition. For MPP tracking of tandems, the un-encapsulated devices operated under ~1 Sun
417 LED illumination in a N_2 flow at room temperature. The illumination intensity was calibrated
418 to 100 mW·cm^{-2} with the standard silicon cell from *J-V* measurements.
419

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428

429 ## Author Contributions

430 Z. Ding, C. Kan, X. Yu, Y. Zeng and J. Ye designed the experiments and supervised the
431 project. Z. Ding, C. Kan, S. Jiang, M. Zhang, and H. Zhang performed the material and film

432 preparation and characterization. Z. Ding, C. Kan, S. Jiang, M. Liao and W. Liu fabricated
433 and characterized the devices. Z. Ding and Y. Zeng did the numerical simulations. Z. Ding,
434 C. Kan, Z. Yang, P. Hang, Y. Zeng and J. Ye contributed to data analysis. Z. Ding, C. Kan,
435 P. Hang, Z. Yang, Y. Zeng, X. Yu and J. Ye wrote the manuscript. All authors reviewed and
436 contributed to the final version of the manuscript.
437

438 **Conflicts of interest**

439 There are no conflicts to declare.
440

441 **Data availability**

442 Source data are provided with this paper. All the data supporting the findings of this study are
443 available within this article and its Supplementary Information. Any additional information can be
444 obtained from corresponding authors upon request.
445

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