FIN Junctionless Field Effect Transistor (FIN-JLFET) With Ground Plane For Surpassing Parasitic BJT Action

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FIN Junctionless Field Effect Transistor (FIN-JLFET) with Ground Plane for Surpassing Parasitic BJT Action

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Abstract The leakage mechanism due to lateral band-to-band tunneling (L-BTBT) results in increased off state current and hinders the scaling of the junctionless transistor. The effect of L-BTBT on FIN shaped gate Junctionless field effect transistor(JLFET) with the ground plane (GP) in oxide has been investigated. The proposed device is simulated using 3-D Silvaco TCAD and shows that it can mitigate the L-BTBT and leads to efficient volume depletion which relaxes the requirements of ultra-thin silicon thickness and high workfunction of the gate electrode. The results show significantly reduced OFF-state current and high I_{on}/I_{off} ratio even at scaled gate length beyond 10 nm along with the reduction in drain induced barrier lowering and threshold voltage roll-off. Thus, the proposed device shows better performance at sub-10 nm node.

Keywords Junctionless field effect transistor (JLT), ground plane, lateral band-to-band tunneling (L-BTBT), parasitic BJT, 3D simulation, SOI, FIN shaped gate, SiO₂ BOX

1 Introduction

Trends in the semiconductor industry are towards scaling down the transistor size to reduced delay, power, and increased packing density. However, the scaling of channel length to extreme dimensions puts stringent requirements for doping in sub 10-nm devices as it requires ultrasteep doping profiles [1]. Furthermore, devices having junctions leads to increased power dissipation as junctions are the source of leakage current. Therefore, devices with uniform doping such as junctionless transistor do away with the ultrasteep doping profile constraint and thus holds very promising prospects in the semiconductor technology. The junctionless transistor operates on the principle of modulation of carriers by the gate electrode. A junctionless transistor has constant high doping throughout the device. It can be considered as a gated resistor with high doping [1]. The first device of this

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kind was introduced by J. E. Lilienfeld [2] and was successfully fabricated and demonstrated by J-P. Colinge [1]. Myriads of different structures for junctionless transistor has been reported [3]-[8]. Junctionless transistor faces difficulty in turning off the transistor owing to inefficient volume depletion which results in increased off state current. The device is turned off by gate semiconductor work function difference and requires a thin channel and high metal work function above 5.5eV [10] to successfully turn off the device.

Another source of increased off state current arises from lateral band to band tunneling at the interface of the channel and drain. Because of the significant proximity of the drain and the channel region, the valence band of the channel region overlaps with the conduction band of the drain region and if the tunneling width is small enough, it leads to the lateral band-to-band tunneling (BTBT) leaving behind holes in the channel region for an n-type junctionless transistor. These accumulated holes form a parasitic bipolar transistor (BJT) with the adjoining source and drain region and are the dominant mechanism for increased leakage current in the off state. Moreover, the current dominated by parasitic BJT action may result in loss of gate control once the parasitic BJT is triggered.

The effect of parasitic BJT action due to the lateral band to band tunneling has been earlier reported [9]. After that, the effect of gate induced drain leakage (GIDL) and leakage current mechanism in silicon nanowire transistors [12]-[14] and many other devices have been investigated taking lateral BTBT into account. Numerous architectures have been reported to mitigate the effect of lateral BTBT and resulting in enhanced off state current [15]-[22]. These architectures achieve the intended enhancement either by increasing the tunneling width at the channel drain interface or by reducing the electric field due to field redistribution. Architectures that hinders triggering of parasitic BJT by increasing source to channel barrier height and increasing the effective length of the channel which results in the reduction of the current gain of bipolar BJT and providing the path to the ground for the holes accumulated in the channel region.

Although the performance of multigate junctionless transistor has been analyzed in the past [24]-[27], the effect of parasitic BJT due to lateral BTBT for FINJLFET has not been taken into account. However, from the aforementioned discussion, it is obvious that the lateral BTBT turns out to be a very important effect especially in the nanoscale junctionless transistors where the drain is in significant proximity of channel region and thus cannot be ignored in investigating the performance parameters.

In the present work, the effect of parasitic BJT action due to the lateral band-to-band tunneling is investigated for a FINJLFET. Additionally, to mitigate the parasitic BJT action a ground plane (GP) is added to the oxide layer and its effect in improving the performance is also investigated. The ground plane has been used in past to improve the performance of SOI-MOSFET. The ground plane leads to redistribution of electric field and prevents the penetration of electric field lines that originate from the drain into channel region and thus minimizes the short channel effects such as drain induced barrier lowering (DIBL) as the ground plane acts like a sink to SOI-MOSFET [27].

The rest of this article is organized into three sections: Section 2 deals with the device structural parameters description along with the simulation framework, Section 3 highlights the device dc performance estimation and it also depicts the in-

Fig. 1 Cross-sectional views of the proposed structure (a) along gate direction and (b) along channel direction, and (c) schematic of proposed GP-FINJLFET.

depth device optimization and sensitivity analysis. At the last Section 4 concludes the work.

Table 1 Device parameters considered for GP-FINJLFET during simulation.

Parameters (unit)	Symbols	Values
Channel doping(n-type) ($/cm^3$)	N_D	10^{19}
Gate oxide material	SiO_2	
Gate oxide thickness (nm)	T_{ox}	2
Gate workfunction (eV)	ϕ_m	4.9
Silicon Film Height (nm)	H_s	10
Silicon Film Width (nm)	W_s	10
Gate length (nm)	L_g	20
Ground plane depth (nm)	D_{GP}	10
Ground plane thickness (nm)	t_{GP}	10
Ground plane doping (p-type) ($/cm^3$)	N_A	10^{20}

2 Device Structures and Simulation

The schematic illustration of FIN shaped gate junctionless transistor with the ground plane in SiO_2 BOX (GP-FINJLFET) is shown in Fig. 1. Further, cross-sectional views of the proposed structure along gate direction and along channel direction are shown in Fig. 1(a) and (b), respectively. For the device simulations, Silvaco TCAD [23] was used and the device structure was created in Devedit 3D as shown in Fig.1(c). It is a silicon on insulator junctionless field effect transistor (JLFET) with FIN-shaped gate structure and a ground plane at depth d_{gp} inside the oxide. Because of the triple gate structure which results in better gate control, the requirement of a metal gate with a very high workfunction for efficient volume depletion can be relaxed and in this work, the gate workfunction of 4.9 eV is taken.

Fig. 2 $I_D - V_{GS}$ characteristics of proposed FINJLFET with and without GP and lateral band-to-band tunneling effect.

Fig. 3 Hole concentration plots for (a)GP-FINJLFET with $D_{GP} = 10nm$ and (b)FINJLFET without GP.

The channel doping is taken to n-type and for the ground plane p-type doping is used. The detailed parameters for the device simulation have been tabulated in Table. 1. The Fermi Dirac carrier statistics, Shockley-Reed-Hall, and Auger recombination were employed along with Lombardi mobility model. To account for band gap narrowing effect, slotboom was used. The standard band to band tunneling model was used to account for the lateral band to band tunneling. The tunneling model was calibrated as per the reported work [11].

3 Results and Discussion

As discussed that the band-to-band tunneling effect increases the tunneling current in the OFF-state and reduces the gate control and also hinders the scalability of

junctionless transistor. Fig. 2 compares the characteristics of proposed FINJLFET with and without taking into the effect of the lateral band to band tunneling. It can be observed from the figure that the lateral band to band tunneling causes a significant increase in drain current. This can be attributed to the parasitic BJT that is being triggered due to hole accumulation resulting from lateral band to band tunneling at the channel drain interface. This is further aggravated by high electric field that is present at the channel drain interface resulting in reduced tunneling width leading to a high probability of quantum tunneling. As the parasitic BJT is triggered, it results in the loss of gate control and therefore hinders the scalability of the device. One way to inhibit triggering is to increase the source to channel barrier height in the OFF-state of the device. This is precisely what our proposed structure is providing. The GP spans the length of the device, and it can be considered as the effect of increasing the base width of the parasitic BJT and hence the current due to the parasitic transistor is reduced as it is inversely proportional to the width of the base width of transistor. The GP results in the depletion of the drain extension region which therefore reduces peak electric field at the channel drain interface. This significantly enhances the tunneling width which consequently surpasses the L-BTBT [27]. This leads to a better OFF-state current as compared to the structure without the GP. Moreover, the increased source to channel barrier height in OFF-state inhibits the triggering of parasitic BJT.

The validity of the aforementioned discussion is more apparent by looking at the hole concentration contour plots of FINJLFET with GP and without GP which is shown in Fig.3. From the figure, it is apparent that the GP depth of 10 nm results in reduced accumulated hole concentration and holes accumulate in a larger region as compared to the structure without GP and thus reduced I_{off} due to an increase in the effective base width of the parasitic BJT.

3.1 Ground Plane Depth Variations

The effect of adding the GP can be more clearly interpreted by looking at the results due to variations in depth of GP from the channel. It can be seen from Fig.4 that the optimum depth for the GP is 10 nm and decreasing the depth further results in an increase in OFF-state current. This is attributed to reduced electric field at the channel drain interface and increased source to channel barrier height at the source-channel interface.

Fig.5 shows that the aforementioned reduction of electric field as compared to the structure without GP. The field for different GP depths has also been plotted. In contrast to the FINJLFET without the GP where the peak electric field in OFF-state is concentrated near the channel drain interface, in GP-FINJLFET, the electric field is reduced at the channel drain interface because of redistribution. Because of reduced electric field, the band bending becomes gradual and the tunneling width is increased which mitigates lateral BTBT and reduced hole accumulation in the channel region. Fig.6 shows the effect of GP and depth variations on the band diagram. It can be observed that the GP reduces the source to channel barrier height and thus prevents the triggering of parasitic BJT.

Fig. 4 $I_D - V_{GS}$ characteristics of GP-FINJLFET for different D_{GP} values.

Fig. 5 Electric field profiles of the proposed GP-FINJLFET in the OFF-state for various values of D_{GP} .

Fig. 6 Energy band profiles in the OFF-state for the proposed GP-FINJLFET.

3.2 Effect of Channel Length Scaling

The effect of scaling has been considered in Fig.7, where it can be seen that the device has good scalability even in the sub-10 nm regime. The device exhibits lower hole generation rates because of reduced BTBT even at scaled gate length. Whereas beyond 5 nm gate length, an increase in drain current in OFF-state and loss of gate control is to be expected and more sophisticated simulations like ballistic or quantum-based models called for appropriately model the device behaviour due to quantum effects. Fig.8 compares the drain characteristics of $L_g = 20$ nm and $L_g = 5$ nm with and without GP. It can be seen that the inclusion of GP leads to a significant reduction in the OFF-state characteristics of the device.

Fig.9 shows the I_{on}/I_{off} ratio plots for FINJLFET with GP for different gate lengths. Also, the I_{on}/I_{off} ratio of FINJLFET without the GP has been compared. The addition of GP results in considerable improvement in I_{on}/I_{off} and the proposed structure has a good I_{on}/I_{off} ratio even in sub 10 nm gate lengths. A channel length of 20nm and 5nm GP-FINJLFET gives the I_{on}/I_{off} ratio of order $\sim 10^8$ and $\sim 10^5$ respectively compared to the I_{on}/I_{off} ratio of order $\sim 10^6$ and $\sim 10^2$ respectively for FINJLFET without GP. Thus, the proposed structure in this article provides a very lucrative alternative for scaled devices.

In Fig.10(a) the drain induced barrier lowering (DIBL) has been extracted for our proposed structure. DIBL is calculated as the difference in V_{th} at $V_{DS} = 50$ mV and at $V_{DS} = 1.0$ V. The constant current method of threshold voltage extraction has been used. The DIBL is computed at the constant reference drain current of $10^{-7} A/\mu m$ which is widely used as a reference current for threshold voltage extraction [28]. The threshold voltage(V_t) for scaled gate length has also been

Fig. 7 $I_D - V_{GS}$ characteristics of GP-FINJLFET for different values of gate length L_g

Fig. 8 Comparison of effect of GP for $L_g = 20nm$ and $L_g = 5nm$.

shown in the figure. Moreover, in Fig.10(b) the DIBL and threshold voltage for FINJLFET without GP have been plotted for comparison. It can be observed that the structure with GP shows better DIBL characteristics than the one without GP.

Fig. 9 I_{on}/I_{off} ratio comparison of GP-FINJLFET with FINJLFET for various gate lengths.

Fig. 10 DIBL and V_t roll off for scaled gate length for (a) GP-FINJLFET and (b) FINJLFET without GP.

3.3 Ground Plane Doping Variation

Fig.11 demonstrates the effect of variation of doping concentration on the drain characteristics. It can be observed that the $I_D - V_{GS}$ characteristics are very sensitive to doping variations and a high doping concentration of the order of $\sim 10^{20}/cm^3$ is required to get the optimum results. Reducing the doping concentration of GP leads to a drastic increase in OFF-state current.

Fig. 11 $I_D - V_{GS}$ characteristics of GP-FINJLFET for different doping concentration of GP.

3.4 Channel Width Variation

Fig.12 shows the effect of the width of active layer variation on the drain characteristics of the device. It can be observed that decreasing the width of the channel region significantly reduces the OFF-state current which is due to the reduction in the active region volume that needs to be depleted by the gate electrodes resulting in increased volume depletion. Moreover, a better electrostatic gate control is apparent from the constancy of the $I_D - V_{GS}$ curve in the OFF-state as we scale down the width of the channel region. The ON-state current is slightly reduced as we reduce the width of the channel region owing to reduction in the number of charge carriers available for current transport. However, beyond the width of 6nm, quantum effects like quantum confinement must be taken into account to fully describe the characteristics which have not been considered in this work.

4 Conclusion

A ground plane based FINJLFET is proposed for sub-10 nm for SOI-JLFET. With the use of calibrated simulations, it has been demonstrated that the addition of GP results in a drastic reduction of OFF-state current and increased I_{on}/I_{off} ratio of 10^8 and 10^5 for gate lengths of 20nm and 8nm. Additionally, improved DIBL and threshold voltage roll-off has been observed for GP-FINJLFET which is attributed to the depletion of source drain extension region and reduced parasitic BJT action owing to the GP. This reduction in parasitic BJT action is attributed to suppressed L-BTBT at the drain channel interface. Thus, the proposed GP-FINJLFET shows better performance and is a very promising structure for sub-10 nm scaling.

Fig. 12 $I_D - V_{GS}$ characteristics of GP-FINJLFET for different widths of active layer.

Ethics approval and consent to participate

We comply to the ethical standards. We give our consent to participate.

Consent for Publication

All the authors are giving consent to publish.

Availability of data and material

No associated data.

Competing interests

No conflict of interest to declare.

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Authors' contributions

Bhaskar Kumar has simulated the device structure and developed the computational framework. Bharat Gupta has conceived the idea helped during the writing of final draft and supervised. Sangeeta Singh verified the simulation framework and helped in manuscript preparation. Pankaj Kumar helped in manuscript preparation, simulation and results validation.

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References

1. J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, Nanowire transistors without junctions, *Nature Nanotechnol.*, 5(3), pp. 225–229, Mar. 2010
2. J. E. Lilienfeld, Method and apparatus for controlling electric current, U.S. Patent 1 745 175, Jan. 28, 1930.
3. C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, Junctionless multigate field-effect transistor, *Appl. Phys. Lett.*, 94(5), pp. 053511–053512, 2009.
4. S.Y. Kim, J.H. Seo, Y.J. Yoon, G.M. Yoo, Y.J. Kim, H.R. Eun, H.S. Kang, J. Kim, S. Cho, J.H. Lee, and I.M. Kang, Design and analysis of sub-10 nm junctionless fin-shaped field-effect transistors. *JSTS: Journal of Semiconductor Technology and Science*, 14(5), pp.508–517, 2014.
5. R.T. Doria, M.A. Pavanello, R.D. Trevisoli, M. de Souza, C.W. Lee, I. Ferain, N.D. Akhavan, R. Yan, P. Razavi, R. Yu, and A. Kranti, Junctionless multiple-gate transistors for analog applications. *IEEE Transactions on Electron Devices*, 58(8), pp.2511–2519, 2011.
6. C.-J. Su, T.-I. Tsai, Y.-L. Liou, Z.-M. Lin, H.-C. Lin, and T.-S. Chao, Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels, *IEEE Electron Device Lett.*, 32(4), pp. 521– 523, Apr. 2011.
7. R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn, Comparison of junctionless and conventional trigate transistors with Lg down to 26 nm, *IEEE Electron Device Lett.*, 32(9), pp. 1170–1172, 2011.
8. S. Sahay, and M.J. Kumar, Nanotube junctionless FET: proposal, design, and investigation, *IEEE Transactions on Electron Devices*, 64(4), pp. 1851–1856, 2017.
9. S. Gundapaneni, S. Ganguly, S. and A. Kottantharayil, Bulk planar junctionless transistor (BPJLT): An attractive device alternative for scaling, *IEEE Electron device letters*, 32(3), pp. 261–263, 2011.
10. S. Sahay and M. J. Kumar, Realizing efficient volume depletion in SOI junctionless FETs, *IEEE J. Electron Devices Soc.*, 4(3), pp. 110–115, 2016.
11. S. Gundapaneni, M. Bajaj, R.K. Pandey, K.V. Murali, S. Ganguly, and A. Kottantharayil, Effect of band-to-band tunneling on junctionless transistors, *IEEE Transactions on Electron Devices*, 59(4), pp.1023–1029, 2012.
12. J. Fan, M. Li, X. Xu, Y. Yang, H. Xuan, and R. Huang, Insight into gate-induced drain leakage in silicon nanowire transistors, *IEEE Transactions on Electron Devices*, 62(1), pp.213–219, 2014.
13. R. Trevisoli, R. Trevisoli Doria, M. de Souza, and M. Antonio Pavanello, Analysis of the leakage current in junctionless nanowire transistors, *Applied Physics Letters*, 103(20), p. 202103, 2013.
14. S. Sahay and M. J. Kumar, Physical insights into the nature of gate- induced drain leakage in ultrashort channel nanowire FETs, *IEEE Trans. Electron Devices*, 64(6), pp. 2604–2610, 2017.
15. S. Sahay, and M.J. Kumar, M.J., Controlling L-BTBT and volume depletion in nanowire JLFETs using core-shell architecture, *IEEE Transactions on Electron Devices*, 63(9), pp. 3790–3794. 2016.
16. J. Hur, B.H. Lee, M.H. Kang, D.C. Ahn, T. Bang, S.B. Jeon, and Y.K. Choi, Comprehensive analysis of gate-induced drain leakage in vertically stacked nanowire FETs: Inversion-mode versus junctionless mode, *IEEE Electron Device Letters*, 37(5), pp. 541–544, 2016.
17. S. Sahay, and Kumar, M.J., Spacer design guidelines for nanowire FETs from gate-induced drain leakage perspective. *IEEE Transactions on Electron Devices*, 64(7), pp.3007–3015, 2017.

18. S. Agarwal, S. Singh, B.C. Sahana, and A. Naugarhiya, Gaussian Doped Planar 4H-SiC Junctionless Field Effect Transistor For Enhanced Gate Controllability, *Silicon*, pp.1-10, 2020.
19. M.J. Kumar, and S. Sahay, Controlling BTBT-induced parasitic BJT action in junctionless FETs using a hybrid channel. *IEEE Transactions on Electron Devices*, 63(8), pp.3350-3353, 2016.
20. I.H. Wong, Y.T. Chen, S.H. Huang, W.H. Tu, Y.S. Chen, and C.W. Liu, Junctionless gate-all-around pFETs using in-situ boron-doped Ge channel on Si, *IEEE Transactions on Nanotechnology*, 14(5), pp.878-882, 2015.
21. S. Gundapaneni, S. Ganguly, and A. Kottantharayil, Enhanced Electrostatic Integrity of Short-Channel Junctionless Transistor With High- κ Spacers, *IEEE Electron Device Letters*, 32(10), pp.1325-1327, 2011.
22. V. Thirunavukkarasu, Y.R. Jhan, Y.B. Liu, E.D. Kurniawan, Y.R. Lin, S.Y. Yang, C.H. Cheng, and Y.C. Wu, Gate-all-around junctionless silicon transistors with atomically thin nanosheet channel (0.65 nm) and record sub-threshold slope (43 mV/dec), *Applied Physics Letters*, 110(3), p.032101, 2017.
23. ATLAS User's Manual, Silvaco Int., Santa Clara, CA, 2016.
24. M. J. Kumar and M. Siva, The ground plane in buried oxide for controlling short-channel effects in nanoscale SOI MOSFETs, *IEEE Trans. Electron Devices*, 55(6), pp. 1554–1557, 2008.
25. W. Xiong and J. P. Colinge, Self-aligned implanted ground-plane fully depleted SOI MOSFET," *Electron. Lett.*, 35(23), pp. 2059–2060, 1999.
26. S. Garg and S. Saurabh, Improving the scalability of SOI-based tunnel FETs using ground plane in buried oxide, *IEEE J. Electron Devices Soc.*, 7, pp. 435–443, 2019.
27. A.K. Jain, and M.J. Kumar, Sub-10 nm Scalability of Junctionless FETs Using a Ground Plane in High-K BOX: A Simulation Study, *IEEE Access*, 8, pp. 137540-137548, 2020.
28. A. Ortiz-Conde, F.G. Sánchez, J.J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, A review of recent MOSFET threshold voltage extraction methods, *Microelectronics reliability*, 42(4-5), pp.583-596, 2002.

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Figures

Figure 1

Cross-sectional views of the proposed structure (a) along gate direction and (b) along channel direction, and (c) schematic of proposed GP-FINJLFET.

Figure 2

I_D - V_{GS} characteristics of proposed FINJLFET with and without GP and lateral band-to-band tunneling effect.

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Figure 12

ID - VGS characteristics of GP-FINJLFET for different widths of active layer.

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