Investigation of Variation in Device Design Parameters on the Saturation Voltages of Hetero-junction Nanowire Tunnel FETs

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Research Article

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Abstract

Estimation of the saturation voltages of beyond CMOS devices is essential for the accurate circuit design and analysis. In this work, we look at the influence of device design parameters on the saturation voltage (V_{DSAT}) of a Tunnel Field Effect Transistor (TFET) using 3D TCAD Numerical Simulations. The variation in channel length, underlap at gate-drain, source/drain doping, and the source/channel material are some of the vital optimization parameters in the design and optimization of TFET based circuits. We observe, with the increasing value of drain bias (V_{DS}), TFET device initially enters in the soft saturation state and subsequently a deep saturation state is attained. These voltages are altered with device variability and hence the analog performance. An increase in drain (source) doping increases (decreases) the soft saturation voltage of TFETs. It is also found that an early onset of saturation can be achieved by the gate-drain underlap in TFETs. The impact of short channel lengths is to worsen the perfect saturation phenomenon in Tunnel FETs. In addition, the reduction in nanowire diameter delays the saturation by few millivolts.

I. Introduction

The energy efficiency of VLSI system can be significantly improved with the scaling of supply voltage, V_{DD} by innovating beyond complementary metal-oxide-semiconductor (CMOS) transistors. In this context, ITRS has pointed out Tunnel FET as one of the most promising device having inverse subthreshold slope less than 60 mv/decade, thus enabling aggressive voltage scaling [1]-[5]. Several device structures and band engineering solutions have recently been investigated to achieve high drive currents [6]-[9]. Analog circuit application of Tunnel FETs are recently being explored [10]-[17], and the output current saturation is also discussed in [18]-[21]. TFETs offer high output resistance and small subthreshold swing. The optimization strategies like source/drain doping, gate-drain underlap and source material selection, improves the SS and ON currents of Tunnel FET. On the other hand, the value of V_{DSAT} and the vital analog parameters are also changed with such optimization. The saturation drain voltage is one of the key design parameter for analog circuits. In our previous work, we discussed a phenomenological method to extract the value of the soft and deep V_{DSAT} in lateral tunneling based TFETs and validated against experimentally measured characteristics [32]. Therefore, this work, while addressing the problem raised above, explains the impact of device design parameters on the onset of saturation in TFETs. The device under consideration is a Nanowire TFET (NWTFET) with SiGe source. This will help the circuit designer to optimize and bias device properly. Device level analog performance parameters are fairly good in the soft saturation regime, and attain their best values in the deep saturation regime. We systematically discuss the influence of variation in device design parameters on these two sub-regimes and thereafter, the performance of vital analog parameters is addressed. This paper is prepared as follows. Section II describes the details of device structure and simulation set up. Section III comprehends the impact of device variability viz. nanowire diameter, channel length, source/drain (s/d) doping and gate-drain underlap on the onset of saturation in Tunnel FET. Lastly, the conclusion is drawn in Section IV.

li. Device Structure And Simulation Setup

The 3-D numerical simulations have been performed in self-consistent manner by using *Sentaurus* TCAD of Synopsys Inc [22]. The device structure is taken from our previous work [32], [34] and reproduced here for the convenience of readers. Three dimensional schematic of the target device is shown in Fig. 1(a). The diameter of nanowire is kept 25 nm and the length of gate is set at 50 nm. The work function of gate electrode is selected as 4.17 eV. In these simulations, 3 nm HfO₂ is used as gate dielectric along with an interfacial layer of 1 nm SiO₂. Further, the source material is selected as Si_{0.5}Ge_{0.5} for realizing hetero-junction [23]. In order to improve the electrostatic integrity of the TFET device, high- κ gate dielectric is used [24] on top of interfacial layer of SiO₂. The doping concentration of channel (p-type), drain (n-type) and source (p-type), and is kept at 10^{17} , 5×10^{18} and 10^{20} cm^{-3} respectively. We have calibrated our simulation setup against the experimentally reported device [25], as shown in Fig. 1(b). It includes bandgap narrowing, SRH recombination, non-local band-to-band tunneling, mobility models and Fermi dirac statistics. Wentzel-Kramers-Brillouin (WKB) approximation is used to compute the band-to-band tunneling probability in the reverse bias junctions [31]. It is noteworthy to mention here that SRH recombination model is used to calculate the deep level defects in bandgap in order to estimate the impact of trap assisted tunneling. Philips unified mobility model takes care of doping dependence and bandgap narrowing models deals with effective bandgap.

lii. Implications Of Device Design Parameters On The Saturation Characteristics Of Tunnel Fet

The extraction method of V_{DSAT} along with circuit application is discussed in our previous work [32]. This section elaborates the influence of variation in the vital device design parameters on the onset of saturation. The preliminary findings of this section have been discussed in brief [36], however, a detailed explanation is presented here.

A. Influence of channel length on Saturation

The drive currents in Tunnel FETs are almost independent of channel length. When the channel lengths are extremely short (below 20 nm), the impact of drain-induced barrier thinning (DIBT) is more enunciated in Tunnel FETs. Thus, the saturation behavior in the output characteristics is observed to be degraded [35]. The physics behind this phenomenon is similar to DIBL in MOSFETs. This is due to the control of drain bias on the tunnel junction, i.e at the source-channel region. Therefore, at sub-20 nm channel length, an increase in drain bias (V_{DS}) results in a reasonably small decrease in the conduction band energy of the channel (E_{CC}) beyond its deep saturation point ($V_{\text{DSAT}}^{\text{d}} = V_{\text{GS}}$). The value of E_{CC} does not pin effectively to a specific value, as shown in Fig. 2(c). Furthermore, the height of tunneling window (ΔE_{t}) is also affected by the drain bias beyond deep saturation. However, as with long channel TFETs, in short channel TFETs too, ΔE_{t} becomes non-zero at the onset of saturation and increases for further increase in V_{DS} [Fig 2(a)-(c)]. However, the value of saturation voltage is not affected by DIBT, rather a relative change in the potential of channel impacts this phenomenon, thus, it is similar for both the long and short channel length TFET devices.

In addition, for shorter channel TFETs, the saturation in output characteristics is worsened [Fig. 2(c)], thereby the output resistance and intrinsic gain also degrades. It may be noted that short channel (sub-20 nm) Tunnel FETs are suitable for digital applications, while long channel TFETs are most suitable for analog design due to

reduced impact of DIBT, therefore the benefits in terms of output resistance and intrinsic gain can be fully exploited.

B. Influence of gate-drain underlap on Saturation

The gate-drain underlap is considered to be a promising solution to suppress the ambipolar behavior of TFET devices [30]. This technique basically reduces the drain side tunneling. In this section, we examine the impact of underlap at drain side of gate (gate-drain underlap) on saturation characteristics of TFET. The value of gate-drain capacitance (C_{gd}) is reduced in the gate-drain underlap structures having an underlap of 20 nm at the drain side, as shown in Fig. 3(a).

It is apparent from the Fig. 3 that the value of threshold voltage V_{th}^{MOS} is increased ($\Delta V_{th}^{MOS} = 83\text{mv}$) with the gate-drain underlap. This happens as the electrostatic control of gate over the underlap portion of channel becomes weaker. Consequently, the value of gate bias required to attain a strong channel inversion is comparatively high. Further, the onset of *soft* saturation advances ($V_{DSAT}^S = 0.813\text{ V}$) since the drain is effectively low doped as shown in Fig. 3(b). V_{DSAT} in the *deep* saturation is still equal to the gate bias. This happens as the sweeping of most of the channel charges is done by the drain, when V_{GD} (difference in gate and drain bias) reaches to zero as explained in [32].

C. Influence of source/drain doping on Saturation

The source doping is one of the key design parameters in TFETs. The impact of variation in source/drain doping on the saturation characteristics of TFET is discussed in this section. Three different devices D_1 , D_2 and D_3 with p-type source (n-type drain) doping values of 10^{20} (5×10^{18}), 4×10^{20} (5×10^{18}) and 10^{20} (10^{20}) respectively are considered. Please note that all other parameters are kept same as explained in Section II, other than the doping values. A high source doping in results in the source degeneracy, thus an increase in the junction electric field [29]. Consequently, this results in the increased drain current. Moreover, it is interesting to note that the change in source doping does not affect the value of V_{DSAT}^S to significant level, although the magnitude of drain current increases due to increase in BTBT. This happens as the value of V_{th}^{MOS} of TFET remains independent of the value of source doping [Fig 4(a)]. On contrary to this, an increase in drain doping does not change the drain current of Nanowire TFET, as the tunneling current remains almost unaffected of drain doping [24]. However, as shown in Fig. 4(b), the value of V_{DSAT}^S increases (or V_{th}^{MOS} reduces) with increase in the drain doping. This is owing to the diffusion of more number of inversion carriers from the drain end to the channel. Therefore, a delayed saturation happens due to the decrease in V_{th}^{MOS} , when drain doping is increased. Further, there is no change in V_{DSAT}^d since it is caused by attainment of a flat-band condition in the gate-channel-drain MOS system.

D. Influence of nanowire diameter on Saturation

As the diameter of nanowire is reduced, the electrostatic control of gate over the channel is enhanced. This is due to the penetration of vertical electric field into the channel. Further, the gate voltage required for strong inversion in the channel of nanowire is also reduced for small NW diameter. This in turn, increases the onset of soft saturation in Tunnel FETs. Moreover, in order to deplete the channel for a given gate bias, the amount of drain bias required is generally high, in case of the reduced NW diameters [inset of Fig. 5(b)]. Please note that, E_{cc} of 20 nm diameter Nanowire TFET effective pins at the higher drain bias than the 25 nm diameter [Fig 5(a)].

Therefore, the height of tunneling window will be more in the case of 20 nm diameter Nanowire TFET. This also results in an enhancement of the drive current when compared to larger diameter NWTFTs, as depicted in Fig. 5(b). As a consequence, the value of ΔE_c remains low for a reduced diameter [Fig. 5(a)]. This causes a delay in the output current saturation in TFETs at scaled NW diameters. The deep saturation is always defined as flat band voltage when $V_{DS} = V_{GS}$ and $V_{GD} = 0$. The onset of soft saturation at lower voltage is desirable from analog design point of view, as discussed in Section V. Table I discloses the important conclusions of variation in NW diameter on output current saturation at $V_{GS} = 1.0\text{ V}$ in NWTFT.

E. Influence of homo/hetero-junctions on Saturation

The source material engineering is one of the prominent design parameter in Tunnel FETs based circuit design. Since *Si-Si* homo-junction based devices suffer from low drive currents. From last few couple of years, *SiGe*, *Ge* and *GeSn* based group IV material are widely exploited as source material apart from group III-V based materials. In this study, only the source material is changed from $\text{Si}_{0.5}\text{Ge}_{0.5}$ to *Si*. It is found through numerical simulations, the homo-junction based Tunnel FET saturates at lower drain bias than the hetero-junction. In homo-junction TFETs, the inversion in the channel occurs at higher gate bias than the hetero-junction TFETs. This is by virtue of an abrupt decrease in the bandgap of hetero-junction (*Si-SiGe*). Furthermore, there is a prominent effect of direct and indirect BTBT in *Ge* based devices [31]. Nevertheless, the value of drive current always increases with increasing *germanium* content in the source due to the favorable energy bands for tunneling.

Iv. Conclusion

This paper highlights the influence of device variability on the output characteristics in TFETs. Our observations clearly show that the soft saturation voltage can be altered by device variability. From the analog design perspective, it is always desirable to advance the output current saturation. This can be accomplished by increasing the threshold voltage of MOS system in the TFETs. Further, we have also estimated V_{DSAT} for different source material, NW diameters, s/d doping and gate lengths, which is highly essential in analog circuit design. The conduction band energy of the channel and the height of tunneling window play a vital role in analyzing the underline physics of saturation. An increase in drain (source) doping increases (decreases) the soft saturation voltage of TFETs. It is also found that an early onset of saturation can be achieved by the gate-drain underlap in TFETs. The impact of short channel lengths is to worsen the perfect saturation phenomenon in Tunnel FETs. In addition, the reduction in nanowire diameter delays the saturation by few millivolts. The variability in device-circuit performance was found worst with gate-drain underlap due to an imperfect saturation.

Declarations

Funding (Not Applicable)

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Code availability (Not Applicable, No code is required to submit)

Authors' contributions (In this work, we present, an approach to explain the physics behind the output current saturation mechanism in the Nanowire Tunnel FET. Thereafter, a method to extract the onset of soft and deep saturation voltages (V_{DSAT}) of Nanowire TFET is presented for brief introduction of the reader. Further, the impact of the device design variation in the saturation characteristics. Moreover, the variation of saturation voltage with source/drain doping, gate length, hetero/home junctions, diameter/thickness of silicon film is also addressed from the perspective of analog circuit design. To the best of our knowledge, this kind of study is carried out first time. We believe that the results presented in

this manuscript will be immensely useful for developing future analytical model for analog circuit design using Nanowire TFETs. I, the undersigned declare that the manuscript entitled " Investigation of Variation in Device Design Parameters on the Saturation Voltages of Nanowire Tunnel FETs" is original, (abstract of this has been published in IEEE Silicon Nanoelectronics Workshop 2017, Kyoto, Japan), and is not currently being considered for publication elsewhere.)

Additional declarations for articles in life science journals that report the results of studies involving humans and/or animals

Ethics approval (Not Applicable, No Research is involved for Human Participants and/or Animals)

Consent to participate (Not Applicable)

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37. *Declarations*

Tables

Tables can be found in the Supplemental Files section.

Figures

Figure 1

(a) Isometric view of target 3-D NWTFET with SiGe Source, which is used in this work. (b) Calibration ID-VGS characteristics. For calibration, device design, physical dimensions and doping profiles are borrowed from Ref. [25].

Figure 2

Energy band for SiGe/Si hetero junction Nanowire Tunnel FET (a) 50 nm channel length (b) 20 nm channel length. It is shown that ECC decreases gradually with increase in V_{DS} even after deep saturation condition for short channel TFETs. (c) Imperfect saturation results in short channel TFETs due to pronounced effect of DIBT.

Figure 3

Please see manuscript for full figure caption.

Figure 4

Please see manuscript for full figure caption.

Figure 5

Variation in ECC and ΔEC with VDS for VGS = 1 V. For reduced diameters, the delay in the onset of soft saturation is observed [Inset]. (b) Output characteristics for different nanowire diameters. The channel of Nanowire TFET depletes as VDS increases [Inset].

Supplementary Files

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