Semi Analytical Modelling for Drain-Induced Barrier Lowering Reduction in Dual-Metal Gate all Around FET

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Semi Analytical Modelling for Drain-Induced Barrier Lowering Reduction in Dual-Metal Gate all Around FET

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***Abstract* – In the research paper, the semi-analytical modelling is done for low drain-induced barrier lowering (DIBL) dual-metal gate all around FET (DM GAAFET). Vacuum and silicon nitride are considered in the act of the gate oxide material near drain region for dual-metal vacuum oxide gate all around FET (DM-VO GAAFET) and dual-metal nitride oxide gate all around FET (DM-NO GAAFET) respectively, in which surface potential, threshold voltage, and DIBL are modelled for both the devices. The proposed models are validated by comparing DM-NO GAAFET with DM-VO GAAFET. DM-NO GAAFET shows the better device performance than DM-VO GAAFET as the threshold voltage increased by 10% and DIBL decreased by 50% in simulated as well as analytical results. The obtained results are having very close agreement with simulated results for both the GAAFETs.**

***Index Terms* – DIBL, Hetero-dielectric, Semi-analytical Modelling, and GAAFET**

I. INTRODUCTION

As per today's state-of-the-art technologies, device scaling plays a crucial role to enhance device packing density on a single chip. The scaling of device dimensions increase the device performance to faster speed, less area and low cost, but it also increases short channel effects (SCEs) for the devices. In nanoscale dimension, source comes closer to the drain which reduces gate curb on the channel region and upsurges the influences of drain voltage (V_{DS}) which introduces drain-induced barrier lowering (DIBL) [1],[2]. Therefore, it is essential to improve effective gate control on the channel region to reduce DIBL. To enhance the gate control, multi-gate device structure has been introduced [3-5]. Among all the device structures, gate all around [6],[7] is a most promising and widely used device structure due to its better gate controllability, better SCEs immunity and improved transport properties [8][9].

Moreover, to increase gate control and decrease gate oxide tunneling, SiO_2 has been replaced by the high-κ dielectric material [10],[11] but devices still face the problem of DIBL at nanoscale dimensions. To overcome the issue, alternatives were carried out. Gate material engineering (GME) is one of them proposed by Chiang et al. [12] and Kumar et al. [13]. In GME technique, gate metal work function is tuned so that the metal with high work function accelerates charge carriers near the source region while the low work function metal is chosen at drain region [14],[15]. These expedited charge carriers collected at drain region provide higher I_{ON}. Moreover, a stepped size potential along the channel region has been provided by GME, which is due to the modulation in metal gate work function. This stepped potential provides a better immunity against DIBL.

As far as gate oxide is concerned, hetero-dielectric oxide materials are used at the source and drain region [16], [17]. This technique is called hetero-dielectric oxide. The accelerated charge carriers collected at the drain region. Hence the higher permittivity material has been used near the drain region to reduce gate oxide tunneling.

As the channel length diminishes till the nanoscale regime, the gate drops the control on the channel, which modulate the threshold voltage [18]. But in multi-gate devices, the whole channel region has been accumulated and inverted by gate terminal [19]. Hence, for GAAFET devices, a threshold voltage is calculated by gate voltage at which the minimum channel carriers sheet density Q_{inv} met with the threshold value Q_{TH} [20],[21]. The channel mobile charge carrier density has been used in this paper to model channel potential. Hence the Poisson equation became nonlinear for this charge density. Therefore, to solve such nonlinear Poisson equation, superposition principle [22] has been used.

Further, in this research paper, DM-NO GAAFET device, which is the combination of GME and hetero-dielectric, has been modelled for channel surface potential distribution, threshold voltage, and DIBL. This DM-NO GAAFET device structure has already being proposed by Kumar et al. in [23] to reduce DIBL. All analytical results, meet the good agreement with simulated data. The attained results are then further compared along with DM-VO GAAFET to verify the better performance of DM-NO GAAFET.

The organization of this work as follows: The device structure and simulation set-up along with the considered models are included in section-2. In section-3, semi analytical models for threshold voltage, surface potential, and DIBL are given. The validation of the models and comparative analysis for both the devices are covered in section-4. Section-5 present the summary and conclusion of the work in the last.

II. GAAFET DEVICE STRUCTURE AND MODELS USED FOR SIMULATION

The device structure of DM-VO GAAFET and DM-NO GAAFET are delineated in Fig. 1. It can be infer from Fig. 1 that, in DM-NO GAAFET device, silicon nitride (Si_3N_4) has been adopted as the gate oxide near the drain region to reduce charge carrier tunneling while, in DM-VO GAAFET device, a vacuum has been used as gate oxide to reduce hot carrier effects [24]. Both the devices have been

divided into two regions in which region 1 has been considered near the source region and region 2 has been considered near the drain region as per Fig. 1. The gate material engineering and hetero-dielectric techniques are used in both the devices.

In GME, high work function metal (Φ_{m1}) is adopted in region 1 with Φ_{m1} = 4.9 eV and the low work function metal (Φ_{m2}) is adopted in region 2 with Φ_{m2} = 4.62 eV. To get the desired metal work function, Molybdenum has been used as gate electrode material in which work function can be tuned [25]. In DM-NO GAAFET, silicon nitride has been used just above the silicon structure in region 2 whereas SiO_2 has been incorporated as the gate oxide for region 1 in both the devices.

The doping concentration with 1×10^{20} cm^{-3} has been used in source/drain region with donor impurity while the lower doping profile of 1×10^{16} cm^{-3} is used in channel region with the acceptor impurity. Similar doping concentration are reported by Sahay S. et al. [26]. The length of region 1 and region 2 have been defined by L_1 and L_2 respectively. The total channel length has been shown by L. All the device dimensions for DM-VO GAAFET and DM-NO GAAFET have been depicted in Table-I. The simulated results are matched with the results of [24] at V_{DS} = 0.05V and 1V are shown in Fig. 2.

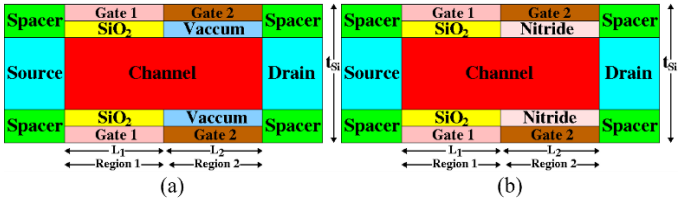

Fig. 1. Cross section view of (a) DM-VO GAAFET [24], (b) DM-NO GAAFET [23] device structure

Visual TCAD Cogenda tool is used to carry out all the 3-D simulation [27]. For simulation, we have considered local band to band tunneling (BTBT), Shockley-Read-Hall (SRH), Philips unified and Lombardi mobility models. To include the degradation of mobility by high electric field and doping, Philips unified, and Lombardi mobility model are included in the present simulations. The effects of charge carriers have been examined by local BTBT model. The effect of charge carrier recombination and Boltzman statistics are calculated using SRH and Drift-diffusion model, respectively. To analyse the impact of highly doped source and drain regions, the Fermi diac statistics model has been incorporated. Since the quantum confinement effect is not the part of our current work, hence the dimensions are not less than 7nm.

III. Semi-Analytical Modeling

As per the device cross-section shown in Fig. 1, the whole gate and oxide length have been divided into two different regions. Since the whole channel region is uniformly doped by acceptor impurity, hence the Poisson equation for the potential $\emptyset_i(r,z)$ can be shown by [22]

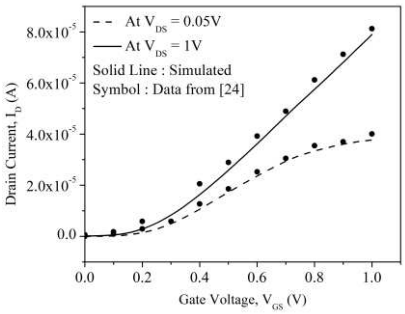

Fig. 2. Simulated results matched with the data of [24] for DM-VO GAAFET at V_{DS} = 0.05V and 1V.

TABLE I
STRUCTURAL PARAMETERS FOR DIFFERENT DEVICE STRUCTURES

Parameters	DM-VO GAAFET		DM-NO GAAFET	
Source/Drain region length (nm)	10		10	
Doping profile for source/drain (/cm^3)	1×10^{20}		1×10^{20}	
Doping profile for channel (/cm^3)	1×10^{16}		1×10^{16}	
Channel length for region 1 and region 2 (nm)	$L_1 + L_2 = L$		$L_1 + L_2 = L$	
	15 + 15 = 30		15 + 15 = 30	
Channel thickness (nm)	20		20	
Gate oxide thickness (nm)	2		2	
Metal gate work functions (eV)	Φ_{m1}	Φ_{m2}	Φ_{m1}	Φ_{m2}
	4.9	4.62	4.9	4.62

$$\frac{d^2\emptyset_i(r,z)}{dr^2} + \frac{1}{r}\frac{d\emptyset_i(r.z)}{dr} + \frac{d^2\emptyset_i(r.z)}{dz^2} = \frac{q.N_a}{\varepsilon_{Si}} \quad (1)$$

Where i = 1, 2 shows the two different regions, N_a is channel doping concentration and $\mathcal{E}_{Si}$ is permittivity of silicon channel.

To solve such non-linear Poisson equation associated with the potential distribution, superposition principle is used [22]. In this superposition principle, the solution of 2D Laplace equation is added with the solution of 1D Poisson equation

$$\emptyset_i(r,z) = V_i(r) + U_i(r,z) \quad (2)$$

Where $V_i\,(r)$ *and* $U_i\,(r.z)$ are the solutions of 1D Poisson equation and 2D Laplace equation respectively.

The boundary condition has given in [22] have been applied to get the solution of Eq. (2). Hance the solution of 1D Poisson and the 2D Laplace equation for different regions are given as

$$V_1(r) = \frac{q.N_a r^2}{4\varepsilon_{Si}} + V_{GS} - V_{FB1} - \frac{q.N_a {t_{Si}}^2}{16\varepsilon_{Si}} - \frac{q.N_a t_{Si} {t_{ox}}'}{4\varepsilon_{ox}} \quad (3)$$

$$V_2(r) = \frac{Q.N_a r^2}{4\varepsilon_{Si}} + V_{GS} - V_{FB2} - \frac{q.N_a {t_{Si}}^2}{16\varepsilon_{Si}} - \frac{q.N_a t_{Si} {t_{ox}}'}{4\varepsilon_{oxj}} \quad (4)$$

$$U_1(r,z) = \sum_{n=1}^{\infty} J_0(\lambda_n r)(A_n e^{\lambda_n z} + B_n e^{-\lambda_n z}) \quad (5)$$

$$U_2(r,z) = \sum_{n=1}^{\infty} J_0(\lambda_n r)(C_n e^{\lambda_n z} + D_n e^{-\lambda_n z}) \quad (6)$$

Where λ_n is the eigen value and given as

$$\lambda_n = \frac{{C_{oxj}}' J_0\left(\frac{\lambda_n t_{Si}}{2}\right)}{\varepsilon_{Si}.J_1\left(\frac{\lambda_n t_{Si}}{2}\right)} \quad (7)$$

$${C_{oxj}}' = \frac{\varepsilon_{oxj}}{{t_{ox}}'} \quad (8)$$

Where A_n, B_n, C_n *and* D_n are the Bessel's coefficient. In Eq. (4), $\mathcal{E}_{oxj}$ is the permittivity of oxide material used in the region 2. In this research work, DM-VO GAAFET is compared with DM-NO GAAFET. If $\mathcal{E}_{ox1}$ is the permittivity of vacuum, which is equal to $1.\mathcal{E}_o$ and used in DM-VO GAAFET while the $\mathcal{E}_{ox2}$ is the permittivity of silicon nitride, which is equal to $7.\mathcal{E}_o$ and used in DM-NO GAAFET. The device structure DM-NO GAAFET shows the higher potential value as per the Eq. (4) and it also verified by Fig. 3. As the $\mathcal{E}_{ox2}$ is higher than the $\mathcal{E}_{ox1}$, it reduces the fifth term of Eq. (4) and increases over all potential for DM-NO GAAFET.

By the addition of the solution of 1D Poisson and 2D Laplace equations, the solution of Eq. (1) will be

$$\emptyset_1(r,z) = \frac{q.N_a r^2}{4\varepsilon_{Si}} + V_{GS} - V_{FB1} - \frac{q.N_a {t_{Si}}^2}{16\varepsilon_{Si}} - \frac{q.N_a t_{Si} {t_{ox}}'}{4\varepsilon_{ox}} + J_0(\lambda, r)(A_1 e^{\lambda_1 z} + B_1 e^{-\lambda_1 z}) \quad (9)$$

The virtual cathode point (VCP) is defined as the minimum potential point at which or after it, the mobile charge carriers have been controlled by the gate electric field [28] and can be calculated as

$$\left.\frac{\partial \emptyset_1}{\partial r}\right|_{z=z_{1,min}} = 0 \quad (10)$$

Substituting the value of $\emptyset_1$ from Eq. (9) to Eq. (10). The VCP will be

$$z_{1,min} = \frac{ln\left(\frac{B_1}{A_1}\right)}{2\lambda_1} \quad (11)$$

Now putting $z = z_{1,\,min}$ and $r = t_{Si}/2$ in Eq. (9) to calculate minimum inversion charge carrier density

$$\emptyset_{1,min} = V_{GS} - V_{FB1} - \frac{q.N_a t_{Si}}{4{C_{ox}}'} + 2J_0\left(\frac{\lambda_1 t_{Si}}{2}\right)\sqrt{A_1 B_1} \quad (12)$$

Similarly the minimum surface potential in region 2 will be

$$\emptyset_{2,min} = V_{GS} - V_{FB2} - \frac{q.N_a t_{Si}}{4{C_{oxj}}'} + 2J_0\left(\frac{\lambda_1 t_{Si}}{2}\right)\sqrt{C_1 D_1} \quad (13)$$

Where

$$z_{2,min} = \frac{ln\left(\frac{D_1}{C_1}\right)}{2\lambda_1} \quad (14)$$

As per the [22], the threshold voltage is considered which is equal to V_{GS} when the minimum surface potential has been considered two times of bulk potential. As per given below

$$\emptyset_{1,min} = 2\emptyset_B \text{ for } V_{GS} = V_{th} \quad (15)$$

Now putting the values from Eq. (15) to Eq. (12) and solve for V_{GS}. To reduce the complexity of computation, $\lambda_1(L_1+L_2) >> 1$, has been considered. The threshold voltage will be

$$V_{th} = \frac{-Y + \sqrt{Y^2 - 4XZ}}{2X} \quad (16)$$

$$V_{th} = \frac{-(\omega_1\omega_4 + \omega_2\omega_3 + 2\alpha\delta) + \sqrt{(\omega_1\omega_4 - \omega_2\omega_3)^2 + 4\delta(\omega_2 + \alpha\omega_1)(\omega_4 + \alpha\omega_3)}}{2(\omega_1\omega_2 - \delta)} \quad (17)$$

Where

$$\alpha = \frac{q.N_a t_{Si}}{4{C_{ox}}'} + V_{FB1} + 2\emptyset_B \quad (18)$$

$$\delta = \frac{1}{{J_0}^2\left(\frac{\lambda_1 t_{Si}}{2}\right)\left[coth\left((L_1+L_2)\lambda_1\right) - 1\right]^2} \quad (19)$$

$$\omega_1 = \eta\left[1 - e^{(L_1+L_2)\lambda_1}\right] \quad (20)$$

$$\omega_2 = \sigma_1 - e^{(L_1+L_2)\lambda_1}\sigma_2 - \gamma \quad (21)$$

$$\omega_3 = \eta\left[1 - e^{2(L_1+L_2)\lambda_1}\right] \quad (22)$$

$$\omega_4 = e^{(L_1+L_2)\lambda_1}\sigma_2 - e^{2(L_1+L_2)\lambda_1}\sigma_1 + \gamma \quad (23)$$

$$\gamma = \frac{4e^{(L_1+L_2)\lambda_1}\, cosh(L_2\lambda_1)\, J_1\left(\frac{\lambda_1 t_{Si}}{2}\right)(V_{FB1} - V_{FB2})}{t_{Si}\left[{J_0}^2\left(\frac{\lambda_1 t_{Si}}{2}\right) + {J_1}^2\left(\frac{\lambda_1 t_{Si}}{2}\right)\right]\lambda_1} \quad (24)$$

$$\eta = \frac{-4J_1\left(\frac{\lambda_1 t_{Si}}{2}\right)}{\lambda_1 t_{Si}\left[{J_0}^2\left(\frac{\lambda_n t_{Si}}{2}\right) + {J_1}^2\left(\frac{\lambda_n t_{Si}}{2}\right)\right]} \quad (25)$$

$$\sigma_1 = \frac{qN_aJ_2\left(\frac{\lambda_1 t_{Si}}{2}\right)C_{ox}{}'t_{Si} + qN_aJ_1\left(\frac{\lambda_1 t_{Si}}{2}\right)\lambda_1 t_{Si} + 4J_1\left(\frac{\lambda_1 t_{Si}}{2}\right)\lambda_1 C_{ox}{}'\varepsilon_{Si}(V_{bi}+V_{FB1})}{\lambda_1{}^2\varepsilon_{Si}C_{ox}{}'t_{Si}\left[J_0{}^2\left(\frac{\lambda_n t_{Si}}{2}\right)+J_1{}^2\left(\frac{\lambda_n t_{Si}}{2}\right)\right]} \quad (26)$$

$$\sigma_2 = \frac{qN_aJ_2\left(\frac{\lambda_1 t_{Si}}{2}\right)C_{oxj}{}'t_{Si} + qN_aJ_1\left(\frac{\lambda_1 t_{Si}}{2}\right)\lambda_1 t_{Si} + 4J_1\left(\frac{\lambda_1 t_{Si}}{2}\right)\lambda_1 C_{oxj}{}'\varepsilon_{Si}(V_{bi}+V_{DS}+V_{FB2}}{\lambda_1{}^2\varepsilon_{Si}C_{oxj}{}'t_{Si}\left[J_0{}^2\left(\frac{\lambda_n t_{Si}}{2}\right)+J_1{}^2\left(\frac{\lambda_n t_{Si}}{2}\right)\right]} \quad (27)$$

As per the Eq. (17), threshold voltage is directly affected by $\omega_1, \omega_2, \omega_3, \omega_4, \alpha$ *and* δ. According to the dependency of C_{ox}' on α which has been given in Eq. (18), α reduces with increase in C_{ox}' (higher value of $\mathcal{E}_{ox}$) and thereby increase V_{th} for DM-NO GAAFET. Moreover, ω_1 and ω_3 are dependent on η and $e^{(L_1+L_2)\lambda_1}$. Since λ_1 increases with increase of C_{ox}' as per Eq. (7), hence it plays important role in η and $e^{(L_1+L_2)\lambda_1}$. From Eq. (20) and Eq. (22), ω_1 and ω_3 decrease with increase in λ_1 and hence increases threshold voltage for DM-NO GAAFET.

As per Eq. (21) and Eq. (23), ω_2 and ω_4 are much dependent on σ_1 and γ coefficients but σ_1 and γ reduces (as per Eq. (26) and Eq. (24) respectively) with increase in λ_1 hence ω_2 and ω_4 also increases with threshold voltage for DM-NO GAAFET.

DIBL for GAAFET can be defined as the threshold voltage difference at low V_{DS} and high V_{DS}. As per the definition, DIBL is directly dependent on the threshold voltage variation at different V_{DS} hence higher threshold voltage device provides smaller DIBL. According to the definition, the formula for DIBL will be

$$DIBL = \frac{V_{TH}(V_{DSlow}) - V_{TH}(V_{DS})}{V_{DS} - V_{DSlow}} \quad (28)$$

Where $V_{TH}(V_{DSlow})$ is the threshold voltage at small V_{DS} = 0.05V whereas $V_{TH}(V_{DS})$ is the threshold voltage at higher V_{DS} = 1V. The expression for DIBL by substituting V_{th} from Eq. (16) to the Eq. (28) will be

$$DIBL = \frac{1}{2X}\left(\frac{4X(Z-Z_0)-(Y^2-{Y_0}^2)}{\sqrt{{Y_0}^2-4XZ_0}+\sqrt{Y^2-4XZ_0}}+Y-Y_0\right) \quad (29)$$

Where Y_0 and Z_0 are the values of Y and Z at V_{DS} = 0.05V. As per the above sub section, DM-NO GAAFET provides higher value of threshold voltage compare to DM-VO GAAFET hence DM-NO GAAFET gives less DIBL and it has also been verified by Fig. 10

IV. Results and Discussion

The surface potential distribution modelling is adapted for different channel length, channel radius, V_{GS}, and V_{DS}. Fig. 3 (a) delineated the surface potential distribution for DM-VO GAAFET and DM-NO GAAFET devices along with the variation in channel length. The $V_{GS} = V_{TH}$ and V_{DS} = 0.05V are used for simulations. The surface potential is calculated 2 nm below the channel-oxide interface in the channel region. In Fig. 3 (a), the surface potential is compared for different channel lengths in region 1 and region 2 in such a way that the length for gate and oxide in region 1 are kept at 10nm and 20nm for L_1:L_2 = 1:2 and L_1:L_2 = 2:1 respectively while the length for gate and oxide in region 2 are kept at 20nm and 10nm for L_1:L_2 = 1:2 and L_1:L_2 = 2:1 respectively. From the Fig. 3 (a), it can be observed that the potential exhibits a step variation at the interface of two regions for both the device structures, which is due to the work function variation at these two region interface.

It can be observed from Fig. 3 (a) that this step sized variation is lower for DM-VO GAAFET and higher for DM-NO GAAFET which is due to the different electric field near the drain region at channel-oxide interface. In DM-NO GAAFET, silicon nitride material is adopted near the drain region to reduce tunneling. The accelerated charge carriers are poised at drain region, but silicon nitride reduces the tunneling of these charge carriers to reduce the electric field. Further, a vacuum region is used in DM-VO GAAFET and thus it has a higher electric field. Moreover, higher stepped size potential distribution provides higher immunity from SCEs [29]. Hence DM-NO GAAFET is more immune for DIBL.

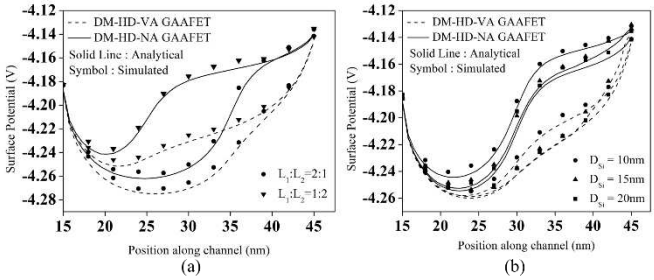

Fig. 3. Surface potential deviation when channel length increases from 15nm to 45nm at V_{DS} = 0.05V and $V_{GS} = V_{TH}$ for, (a) Channel length of 2:1 and 1:2, (b) Channel diameter of 10, 15 and 20 nm.

As channel diameter reduces, it boosts the gate control on the channel region, hence the gate can now control the channel region charge carriers effectively. Fig. 3 (b) exhibits the surface potential variation for different channel length and channel diameter. The voltage levels are kept fixed at $V_{GS} = V_{TH}$ and V_{DS} = 0.05V. In Fig. 3 (b), DM-VO GAAFET and DM-NO GAAFET have been compared for channel diameter of 10nm, 15nm, and 20nm. Analytical results have also been calculated for both the devices at the same channel diameter and found close agreement with simulated results. It can further be observed from Fig. 3 (b) that the potential is distributed in stepped size and this stepped size potential is high for DM-NO GAAFET which is caused by the electric field variation at channel-oxide interface near drain side.

From Fig. 3 (b), it can be observed that the potential is high for 10nm channel diameter while the potential is low for 20nm channel diameter which is caused by the gate control on the channel region for both the devices. Although for 10nm channel diameter, a gate provides excellent control on the channel region compared to 20nm channel diameter for both the devices because of the higher vertical electric field between the gate and channel region [30]. Moreover, at 10nm channel diameter, a gate provides higher immunity from the SCEs due to higher stepped size potential in channel region.

Fig. 4 (a) demonstrates the surface potential distribution along with the channel length at different V_{GS}. V_{DS} is kept fixed at 0.05V whereas channel length and channel diameter are kept fixed at 30nm and 20nm respectively. In Fig. 4 (a), it can be observed that the V_{GS} has been kept fixed at 0.2V, 0.4V, and 1V. Since at V_{GS} = 0.2V, both the devices are in the cut-off region; hence, it provides minimum potential in the channel region. As the V_{GS} increases from 0.2V, devices move to the depletion region and starts conduction. At V_{GS} = 0.4V, devices remain in the depletion region and in the depletion region, the channel begins to form. Hence in this region, surface potential became higher compare to the cut-off region.

At V_{GS} = 1V, devices remain in saturation region which provides higher I_{ON} current for both the devices. The potential distribution is much higher for DM-NO GAAFET at V_{GS} = 0.4V as compare to the potential distribution of DM-VO GAAFET at V_{GS} = 1V. Since in DM-NO GAAFET, silicon nitride has been used as the gate oxide which minimizes the tunneling of charge carriers; hence, it provides the higher surface potential for DM-NO GAAFET at V_{GS} = 0.4V in region 2. Moreover, from Fig. 4 (a), the stepped sized surface potential, and the surface potential in region 2 are higher at every V_{GS} voltage levels. Hence it provides higher immunity to SCEs and higher I_{ON} current.

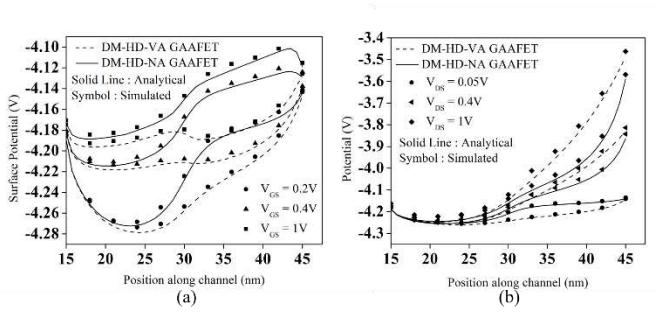

Fig. 4. Surface potential deviation when channel length increases from 15nm to 45nm for channel diameter of 20nm and, (a) V_{GS} = 0.2, 0.4, and 1V, (b) V_{DS} = 0.05, 0.4 and 1V

Fig. 4 (b) shows the deviation in surface potential when the channel length increases from 15nm to 45nm at different V_{DS}. V_{GS} is kept fixed at the threshold voltage level to keep the device in ON-state. In Fig. 4 (b), the surface potential of DM-VO GAAFET and DM-NO GAAFET are compared at V_{DS} = 0.05V, 0.4V, and 1V. The surface potential is high for DM-VO GAAFET as the V_{DS} is increasing from 0.05V to 1V and the vacuum gate oxide is adopted in DM-VO GAAFET. Due to the vacuum gate oxide, an additional electric field also present due to the charge tunneling which causes increment of DIBL in DM-VO GAAFET. However, due to this increased DIBL, V_{DS} has a stronger influence on channel region's charge carriers, and due to this influence, DM-VO GAAFET provides higher surface potential in channel region 2. The surface potential is obtained higher at V_{DS} = 0.05V as the lower V_{DS} is used in DM-NO GAAFET (see in Fig. 4 (b)).

Electric field distribution plays a critical role in device operation and charge carriers movement. Fig. 5 (a) shows the electric field distribution along with the channel length at different channel regions. The oxide length is kept fixed at 10nm for region 1 and 20nm for region 2 at L_1:L_2 = 1:2 while it kept fixed at 20nm for region 1 and 10nm for region 2 at L_1:L_2 = 2:1. From Fig. 5 (a), it can be observed that in device structure L_1:L_2 = 1:2, a small electric field spike is observed at the interface of these two regions. Since the gate length is 10nm in region 1 and the interface of two regions, comes closer to the source region; hence, it gives a small spike at the interface. The electric field increases for DM-VO GAAFET, and it started decreasing for DM-NO GAAFET in the case of L_1:L_2 = 1:2 after electric field spike. The electric field has been increased for DM-VO GAAFET, which is due to the additional electric field that occurs by the tunneling of charge carriers whereas the electric field has decreased for DM-NO GAAFET which is due to the reduction of charge tunneling. The electric field provided by the silicon nitride layer plays important role to reduce overall electric field by the factor of $\mathcal{E}/\mathcal{E}_0$.

The lower value of electric field in DM-NO GAAFET provides lower electric field in drain region, and hence, it gives less DIBL for DM-NO GAAFET. From Fig. 5 (a), it can be seen that the two region interface is close to the drain side for L_1:L_2 = 2:1. Hence it gives a parabolic distribution of electric field till the region interface, and then provides a big spike at the interface. After the spike, the electric field started decreasing for DM-NO GAAFET and gives small electric field at the channel-drain interface and hence reduces DIBL.

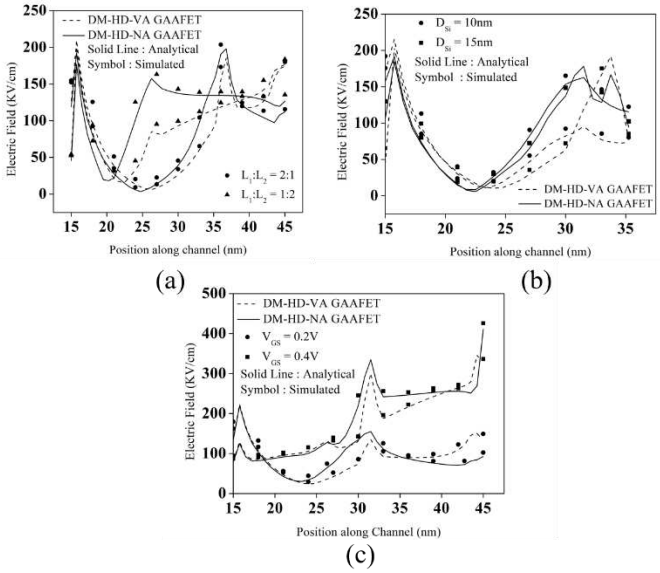

Fig. 5. Electric field deviation when channel length increases from 15nm to 45nm for, (a) Channel length of 2:1 and 1:2, (b) Channel diameter of 10, 15, and 20nm, (c) V_{GS} = 0.2V and 0.4V

Fig. 5 (b) shows the variation in the electric field along with the channel length for different channel diameters. The electric field is higher at 10nm diameter than the electric field at 15nm diameter for both the devices. Since the small diameter channel influenced by the higher vertical electric field, which is provided by the gate terminal. Hence this additional electric field gives better control to the charge carriers available in the channel region.

Fig. 5 (c) shows the electric field variation along with channel length for different V_{GS}. V_{DS} is kept fixed at 0.05V. The electric field is higher for both the devices at V_{GS} = 0.2V. Since devices remained in cut-off mode at V_{GS} = 0.2V which is due to the V_{GS} is smaller than the V_{TH}. In the cut-off mode, there would not be any conducting channel in

source and drain, so a small electric field which is present between Source and Drain, is because of the unwanted charge carriers which move from source region to drain region due to lack of source-channel barrier height [31]. The electric field in cut-off mode is low for DM-NO GAAFET device because this device provides small DIBL.

Further, devices remain in the depletion mode for V_{GS} = 0.4V, which is due to the V_{GS} higher than the V_{TH}. Although, the charge carriers have been depleted by V_{GS} increment in depletion mode. These depleted charge carriers are than move towards the centre of the channel. Moreover, as the charge carriers depleted, fixed acceptor atoms are left behind near the channel-oxide interface. As the V_{GS} increases, it also increases the vertical electric field. However, the fixed acceptor ions also offers limited electric field at channel-oxide interface. Therefore, these two electric fields provide higher electric field for both the devices as per Fig. 5 (c). The electric field spikes present at the metal gate interface due to the variation in an electric field.

The threshold voltage is directly affected by the DIBL. As far as improvement of V_{DS} is concerned, it diminishes the threshold voltage due to the DIBL effect and source-channel barrier height, which further increases sub-threshold leakage current [31]. The threshold voltage deviation has been shown in Fig. 6 (a), when the channel length increases from 20nm to 100nm for channel diameter of 20nm. From Fig. 6 (a), it can be observed that when the channel length increases from 20nm to 100 nm, it increases threshold voltage till 40nm for both the devices and after 40nm, threshold voltage became almost constant. At 20nm channel length, threshold voltage is less due to the SCEs, but at 40nm, SCEs have been minimized.

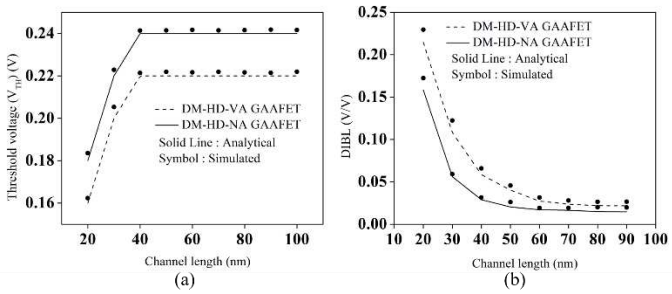

Fig. 6. Modification of (a) Threshold voltage, (b) DIBL, along with the channel length for channel diameter of 20nm.

Moreover, after 40nm, SCEs became insignificant for channel length increment and provided almost constant threshold voltage for both the devices. The value of threshold voltage is high for DM-NO GAAFET, due to the higher immunity against SCEs. The calculated analytical results are more close to the simulated results, which validate the threshold voltage model.

DIBL is an SCE which occurs due to the influence of V_{DS} on the channel region. DIBL is calculated by the threshold voltage difference for lower and higher values of V_{DS}. The formula used for calculation of DIBL is expressed in Eq. (28). Fig. 6 (b) exhibits the variation in DIBL along with the channel length for DM-VO GAAFET and DM-NO GAAFET. The DIBL reduces exponentially till 50nm and after 50nm it became almost constant. Since at 20 nm channel length, the SCEs are more prominent for both the devices and hence, it shows a higher value of DIBL. When the channel length increases from 20nm to 50nm, DIBL has reduced due to the increased channel length. It also increases gate control over the channel region [18]. After 50nm, source and drain became as far enough so that the horizontal electric field component became insignificant, which in general controlled by V_{DS}. Hence it reduces DIBL in both the devices. As per Fig. 6 (b), DIBL offered by DM-VO GAAFET is high whereas low for DM-NO GAAFET, which is due to the minimized charge carrier tunneling. This reduced charge carrier tunneling helps to reduce addition electric field near the drain side and hence reduces DIBL in DM-NO GAAFET. This reduced DIBL helps to lower down leakage current.

V. Conclusion

The semi-analytical modeling and the effect of device engineering are carried out for surface potential, threshold voltage, and DIBL on DM-NO GAAFET and DM-VO GAAFET. The analytical and simulation result shows the better device performance for DM-NO GAAFET to suppress DIBL, and enhanced threshold voltage. DM-NO GAAFET provides more immunity against SCEs due to the more stipe stepped surface potential distribution. Moreover, a limited electric field is observed in DM-NO GAAFET near channel-drain interface due to which DIBL is reduced for DM-NO GAAFET. Since the threshold voltage is higher and DIBL is lower, which provides excellent charge control by gate terminal on the channel region, as per channel length decreases for DM-NO GAAFET.

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