Research Square

Preprints are preliminary reports that have not undergone peer review. They should not be considered conclusive, used to inform clinical practice, or referenced by the media as validated information.

Reconfigurable Two-dimensional Floating Gate Field-effect Transistors for Highly Integrated In-memory Computing

Gwan-Hyoung Lee

gwanlee@snu.ac.kr

Seoul National University https://orcid.org/0000-0002-3028-867X

Cheol Seong Hwang

Seoul National University https://orcid.org/0000-0002-6254-9758

June-Chul Shin

Seoul National University

Taegyun Park

Seoul National University

Dong Hoon Shin

Seoul National University

Hyun-Young Choi

Seoul National University

Kenji Watanabe

National Institute for Materials Science https://orcid.org/0000-0003-3701-8119

Takashi Taniguchi

National Institute for Materials Science Tsukuba Ibaraki https://orcid.org/0000-0002-1467-3105

Yeonwoong Jung

University of Central Florida

Physical Sciences - Article

Keywords: Reconfigurable floating-gate field-effect transistors, highly integrated computing unit, programmable arithmetic and logical operation, two-dimensional semiconductor, van der Waals heterostructure

Posted Date: April 22nd, 2024

DOI: https://doi.org/10.21203/rs.3.rs-4101407/v1

License: This work is licensed under a Creative Commons Attribution 4.0 International License.
Read Full License

Additional Declarations: There is **NO** Competing Interest.

Abstract

With the increasing need for highly integrable and energy-efficient hardware for cutting-edge applications, such as neuromorphic and in-memory computing, reconfigurable devices with multi-functional operations are essential for these applications, enhancing performance and area efficiency. However, traditional reconfigurable devices suffer from limited functionality and circuit incompatibility due to the adoption of multiple gates, leading to increased system complexity and manufacturing costs. This work demonstrates reconfigurable floating-gate field-effect transistors (R-FGFETs) based on van der Waals (vdW) heterostructure to implement highly integrable and reconfigurable circuits for in-memory computing with minimum overhead. By modulating the charge trapping within the graphene floating gate using a single gate terminal, R-FGFETs can attain four distinct electrical conducting states: metallic, n- and p-type semiconducting, and insulating. By incorporating these R-FGFETs into reconfigurable combinatorial computing units, programmable logic and arithmetic operations, including 16 Boolean logic gates, addition, subtraction, and comparison, are feasibly achieved with minimal overhead. Also, a novel method is proposed to address voltage mismatch between input and output through programming voltage-dependent threshold voltage shift, facilitating efficient connections between logic gates. This work offers a potential pathway for highly integrating a reconfigurable processor based on vdW heterostructures, thus providing an area- and energy-efficient solution.

Full Text

The demand for high-performance and low-power computing continuously increases due to rapid advancements in artificial intelligence, where data-centric workloads proliferate[1,2]. Traditional von Neumann architecture that separates the processing and memory units leads to memory bottlenecks, incurring a heavy penalty in performance and energy consumption[3]. In this regard, in-memory computing, which enables data processing and storage within the same memory array, was proposed as a promising approach to address these issues, offering advantages in overall performance and energy efficiency[4,5]. However, enhancing computing performance requires a high integration density of the computing units (CUs), which remains challenging.

In general, in-memory computing hardware primarily consists of a memory array for storing data alongside periphery circuits that selectively manage memory states and function as CUs[6], a unit device that operates specific computations based on Boolean logic functions. Although previous studies on in-memory computing have mainly focused on applications with dense memory arrays consisting of millions of memory devices, the potential penalty of the peripheral circuits has not been considered despite their substantial contribution to the overall cost[7–9]. In addition, achieving logic gates within a memory array requires multiple bias modes, each requiring distinct peripheral circuits and their selections. This operation method increases the chip area portion of peripheral circuitry[10], which is further increased by system flexibility through memory array reconfiguration. Therefore, new concepts of devices and

architectures for high-integration technologies with minimal overheads for the peripheral circuits are urgently required for practical in-memory computing.

Implementing reconfiguration in individual electronic devices can be a highly flexible and area-efficient approach to address the abovementioned challenges, enabling the creation of more complex systems with fewer devices[11,12]. A prominent candidate among these components is a reconfigurable field-effect transistor (R-FET), which can manipulate the polarity between the n- and p-type states by adjusting a control signal[13,14]. Especially, the effective electrostatic tunability in two-dimensional (2D) semiconductors with inherent ambipolar transport, such as WSe_2, BP, and $MoTe_2$, enables the fabrication of transistors with reconfigurable polarities, holding promise for applications in multi-functional logic, security circuits, and neuromorphic computing[12,15–17]. Furthermore, reconfigurable 2D devices coupled with nonvolatile elements were reported to facilitate in-memory computing[18–20]. Moreover, at the circuit level, utilizing reconfigurable components allows for the construction of reconfigurable processors to perform more complex functions through a single configuration. This approach eliminates wasted units that do not contribute to the desired processing tasks, resulting in more compact CUs and improved integrated processor density[21].

This work demonstrates WSe_2 R-FGFETs based on van der Waals heterostructure that can be utilized to integrate reprogrammable circuits for in-memory computing with minimum overhead. As illustrated in Fig. 1a, conventional 2D R-FETs can only change the polarity between n-type and p-type FETs[11,12]. In contrast, R-FGFETs in this work consisting of a WSe_2 channel, hBN tunnel barrier, and graphene charge trap layer can be better functional CU components with two key features: First, R-FGFETs have a channel conduction that can be linearly adjusted by changing the charges trapped in the graphene floating gate layer. This feature allows for four distinct types of electrical conductance operations within a single device, greatly diminishing the need for additional components for circuit reconfiguration and reducing the overall circuit footprint. Second, in contrast to other reconfigurable devices that require multiple gate terminals, the R-FGFETs are designed with a single gate terminal, which minimizes space usage, simplifies circuit layouts, and contributes to lower power consumption as illustrated in Fig. 1b[4,5]. Consequently, these R-FGFETs, serving as the fundamental logic CU in reconfigurable circuits, can perform all logic functions, including 16 Boolean logic operations and arithmetic functions, such as full adder (FA), full subtractor (FS), and comparator, with minimal components of a CU.

Figure 1c shows the schematic device structure of the R-FGFET composed of WSe_2, graphene, and hBN. The WSe_2 is used as a channel because of its unique characteristics of ambipolar transport and electrostatic polarity modulation[22–24]. The hBN is an ultrathin tunneling dielectric layer that provides electrostatic controllability of the WSe_2 channel and efficient charge tunneling into the graphene charge trap layer[25,26]. Graphene is selected as a floating gate because of its high charge storage capacity even at atomic thickness[27,28]. The van der Waals heterostructure was fabricated onto a SiO_2 (285 nm)/Si substrate by pick-up transfer method for 2D layer integration[29], followed by e-beam lithography for Ti/Au

source and drain electrodes. (See Method and Fig. S1 for details of the fabrication process) The optical microscopy image of Fig. 1d shows a representative WSe_2 R-FGFET fabricated in this work. (See Fig. S2 and S3 for information on the used flakes) By modulating the trapped charge density by changing the bias applied to a single gate of Si, these R-FGFETs have reconfigurability among the four electrical states. In addition, the five R-FGFETs, as shown in Fig. 1e, were combined into a CU featuring two parallel R-FGFETs in a series, offering a programmable function that enables the implementation of all 16 Boolean logic gates.

Stable and controllable memory characteristics in these devices are required to implement and maintain configured states of R-FGFETs. So, the device characteristics of WSe_2 R-FGFETs were first examined, as shown in Fig. 2. The transfer curve (I_{DS} - V_{BG}) in Fig. 2a shows that the WSe_2 R-FGFET has ambipolar transport behavior with a high on/off ratio of ~ 10^7 and a large hysteresis of ~ 50 V for both n- and p-type conductance during V_{BG} sweeping of ± 60 V. Note that such an extensive V_{BG} sweeping range was required because of the thick thickness of the SiO_2 thickness (285 nm), which was adopted to alleviate any damaging effect to the insulator layer by the 2D material transfer method. If the practical thickness (~ 15 nm) was used, the required V_{BG} would be $<<$ 15 V, comparable to the current flash memory technology. The large memory window in the transfer curve is attributed to the stored charges within the graphene floating gate[28]. Figure 2b shows that the memory window can be modulated by varying the sweeping range of V_{BG}. The linear increase of memory window with increasing V_{BG} for n- and p-type conductance indicates that the type and density of carriers stored in the floating graphene gate can be precisely controlled. (See Extended Data Fig. 1) The ambipolar nature of the WSe_2 channel can provide both electrons and holes to the floating gate, significantly contributing to the device's reconfigurability. The retention and endurance characteristics of the WSe_2 R-FGFET at a programming pulse time of 100 ms were measured, as shown in Fig. 2c-d and Extended Data Fig. 2–3. The retention measurement of n-type conductance in Fig. 2c shows a high on/off ratio exceeding 10^7 even after programming pulses with no noticeable degradation in performance for up to 10^4 s. The extracted room temperature retention times for both n- and p-type states surpass 10 years, and stable memory operations are observed even at a high temperature of 383 K. (See Extended Data Fig. 2 for further detailed information) The endurance performance of n-type conductance in Fig. 2d exhibits robustness even after 10^4 cycles and a high on/off ratio of $>10^7$. (See Extended Data Fig. 3 for endurance measurement of p-type conductance). The switching speed of the memory device was also assessed by varying pulse length, as shown in Extended Data Fig. 4. Even at a short pulse length of 1 ms, high on/off ratios for both n- and p-type memory states were maintained.

The R-FGFET provides a higher degree of freedom in circuit functions as a fundamental building block for logic computing due to its reconfigurable switching operations through programming pulses. Using a single gate terminal, the R-FGFET can change the memory state by applying programming voltage ($V_{BG, PROG}$) and perform logic operations by applying a $V_{BG} < V_{BG, PROG}$. In this work, the operational V_{BG} range is limited to ± 5 V, not to disturb the programmed memory state. Figure 3a shows transport behavior

obtained by sweeping ± 5 V at different memory states, which were metallic ($V_{BG, PROG}$ = -60 V), n-type semiconductor (n-type, $V_{BG, PROG}$ = -45 V), p-type semiconducting (p-type, $V_{BG, PROG}$ = 45 V), and insulating states ($V_{BG, PROG}$ = 30 V). The trapped charges can change not only the threshold voltage (V_{th}) of the given type FET, but also the type itself of the ambipolar WSe_2 channel, as shown in the device schematics of Fig. 3a. Furthermore, R-FGFETs possess the capability to finely shift the V_{th} of the given type FET by finely controlling the $V_{BG, PROG}$. (See Extended Data Fig. 5) The output (I_{DS}-V_{DS}) of Fig. 3b and c, measured at reading V_{BG} of 0 V for various programmed states, exhibit a linear relation, indicating the formation of Ohmic-like contacts at the source and drain terminals. The output curves of programmed n- and p-type semiconducting states are also linear within the switching voltage range. (See Extended Data Fig. 6) The conductance states of WSe_2 were reconfigured by applying the programming gate voltages (upper graph), and the corresponding currents at ± 5 V were measured (bottom graph) in Fig. 3d to verify the dynamic switching performance of the WSe_2 R-FGFETs. The distinct switching characteristics of the WSe_2 R-FGFET align well with four programming states with high stability and reproducibility of multiple operations.

A programmable inverter (INV) was constructed by connecting two WSe_2 R-FGFETs in series to demonstrate the potential of WSe_2 R-FGFETs as a functional building component in integrated circuits. Figure 4 shows circuit diagrams and corresponding input-output voltage relationship (V_{IN} - V_{OUT}) and truth tables for multi-functional logic operations, including FALSE (Fig. 4a), A (Fig. 4b), NOT A (Fig. 4c), and TRUE (Fig. 4d), within a single INV operation, using the programmed states of each device. The high and low signal voltages represent the logical '1' and '0', respectively. The ambipolar characteristics of WSe_2 allow for reconfiguring the given device to p- and n-type FETs, facilitating the construction of a complementary INV. In the complementary circuit composed of the p- and n-type WSe_2 R-FGFETs, the V_{IN} - V_{OUT} curve exhibits full swing output at various supply voltages, achieving higher voltage gain and lower power consumption compared to an INV composed of a n-type R-FGFET and a resistor. (Extended Data Fig. 7 and Fig. S4) To improve the computing accuracy and operating stability of the circuit, aligning the input and output signals within the INV is essential for logic cascading[30]. Figure 4e exhibits the alignment of input and output signals achieved in the programmable INV by modulating the $V_{BG, PROG}$ of n-type R-FGFET ($V_{PROG, n-type}$) for a given $V_{BG, PROG}$ of the p-type R-FGFET. As the $V_{PROG, n-type}$ is increased from − 45 V to -37.5 V, the V_{th} of the voltage output curve shifted toward the positive value of V_{IN} without noticeable degradation of voltage gain, as shown in Fig. 4e. This result indicates the capability of the R-FGFET to precisely modulate the V_{th}. (See Extended Data Fig. 5)

A reconfigurable CU consisting of the R-FGFETs was constructed to execute all 16 Boolean logic operations. Figure 5a illustrates the reconfigurable CU composed of five WSe_2 R-FGFETs, four designated as pull-down networks and one as a depletion-mode transistor in a fixed n-type state. Figure 5b shows that the proposed reconfigurable CU can function as AND, OR, and IMP gates by reconfiguring four input states. Since the two R-FGFETs in the CU do not incorporate in logic operation, the CU reconfigured with three R-FGFETs is termed as three transistor (3T)-logic gates. Similarly, Fig. 5c shows the 5T-logic gates

that integrate all four R-FGFETs to operate as XOR and XNOR gates. The other logic functions are illustrated in Fig. S5, demonstrating all two-input Boolean logic operations in the single CU with the same circuit structure and bias condition.

A behavioral SPICE simulation model of the R-FGFET was constructed based on its transfer and output characteristics under various $V_{BG, PROG}$ conditions to validate the feasibility of the proposed logic operations. (See Supplementary Notes 1, 2, Fig. S6, and S7 for details of the model) Two voltage inputs of A and B (V_A and V_B) are applied to the gate of each R-FGFET. Figure 5d shows the output of the logic gates represented as buffered output node voltage (V_{OUT}). The AND, OR, IMP, XOR, and XNOR logic operations were simulated based on input combinations using reconfigurable CU of 3T- and 5T-logic gates. (See Fig. S8 for all other cases of two-input Boolean functions and Fig. S9 for the effect of parasitic resistances) Fig. 5e benchmarks the number of reconfigurable logic gates and the required number of elemental devices for 2D material-based reconfigurable logic circuits from the literature[15–17,19,20,31,32]. The WSe_2 R-FGFET proposed in this work for a single CU resides at the preferred top-left corner, indicating the superior area efficiency and flexibility of the current reconfigurable CU in two-input logic operations. (See the Extended Table 1 and Supplementary Notes 3 for further detailed information)

Since combinations of logic gates (operations) construct arithmetic operations, various programmable arithmetic operations can be executed by combining the CUs composed of five R-FGFETs. Figure 6a represents the implementation of a 1-bit FA using three CUs. Each CU has one output terminal representing the outcomes of the intermediate sum (S_{int}, equivalent to the sum of half-adder), sum (S), and carry-out (C_{out}) of the 1-bit FA derived from three inputs, A, B, and C_{in}. Each CU is configured to the corresponding 2-input Boolean logic, and the outcome of the 1-bit FA can be expressed through the following logic expressions: $\mathrm{S_{int}=A\ XOR\ B}$, $\mathrm{S=C_{in}\ XOR\ S_{int}}$, and $\mathrm{C_{out}=(A\ AND\ B)\ OR\ (C_{in}\ AND\ S_{int})}$. The S_{int} is cascaded as input voltage for the next-stage CUs, to obtain S and C_{out}. Using the identical configuration based on three CUs offers the advantage of high adaptability to reconfigure a range of arithmetic logic functions, such as a 1-bit FS and comparator. By simply changing two p-type states to n-type states, the borrow-out (B_{out}) and difference (D) of 1-bit FS, along with an intermediate difference (D_{int}) bit, can be implemented for the 1-bit FS, as depicted in Fig. 6b. Figure 6c shows how the comparator is constructed. The CU1 is reconfigured to XNOR gate, utilizing the previous intermediate result of CU2 and CU3 to output in cases where two input bits are equal (A = B). CU2 and CU3 correspond to situations where one of the input bits is greater than the other. For instance, when A > B, the logic function of the output node is equal to A NIMP B.

Aligning the input gate voltage range with the output node voltage range is essential to cascade logic gates[16,30]. The voltage decaying problem is involved in the logic operations without this alignment. While the previous studies have performed the cascading through materials engineering or by controlling voltage with dual gates, these approaches are constrained either by the requirement for complicated multiple gates or by being applicable only to unipolar devices[33–37]. The reconfigurable CUs in this work can overcome these limitations by adjusting the operating voltage range, which varies linearly with $V_{BG,}$

$_{PROG}$ in R-FGFETs, as demonstrated in Fig. S9. It is also demonstrated from the linear shift of the operating voltage range of a programmable INV in Fig. 4e. Notably, precise V_{th} adjustment and FET type conversion of the R-FGFETs by modulating the trapped charge in the graphene gate are advantageous. (See Supplementary Note 4 and Fig. S9 for detailed information)

Consequently, the effectiveness of the R-FGFET model for arithmetic logic functions (1-bit FA, 1-bit FS, and 1-bit comparator) is evidenced in Fig. 6d, e, and f, respectively. These CUs have high potential in their area efficiency and reconfigurable functionalities, as highlighted by the comparison of 2D-logic gates-based 1-bit FA and its reconfigurable functionalities in Extended Table 2[15,16,38,39]. Specifically, the area consumption factor of 15 for the R-FGFET, defined as $\mathrm{N_{Gate}} \times \mathrm{N_{Logic\ Device}} + \mathrm{N_{Peripheral\ Device}}$ (where N_{Gate}, $N_{\mathrm{Logic\ Device}}$, and $N_{\mathrm{Peripheral\ Device}}$ are the number of gates in a logic device, the total number of logic devices, and an additional number of peripheral devices, respectively), is smaller than those for previously reported devices, indicating that higher-density implementation of R-FGFETs can be achieved for in-memory computing systems.

In conclusion, this work demonstrates the WSe_2 R-FGFETs based on vdW heterostructure, which can reduce complexity and enhance the integration of in-memory logic processers. Modulating the trapped charges in the R-FGFETs as memory components enables the reconfiguration of all types of electrical conductance and the precise control over threshold voltage shift, yielding multi-functional devices with a single gate terminal. Integrating the FGFETs into a single reconfigurable CU enables to realization of multiple logic and arithmetic functions, including 16 Boolean logic, 1-bit FA, FS, and comparator, demonstrating its suitability for in-memory computing systems. Compared to the previously proposed logic circuits with higher complexity, the reconfigurable CU in this work significantly reduces circuit redundancy and enhances operation functionality. This potential is expected to be beneficial in the fields that require multi-functional operations, such as in-memory computing and field programmable gate arrays[40]. While the additional peripheral circuits are still required to control CUs, the overall circuit overhead is significantly reduced. Furthermore, all 16 Boolean logic operations share the same circuit configuration, which can used as a camouflaged circuit from hardware attack[17,41]. (See Supplementary Note 5 and Fig. S10 ~ S13 for more information)

Methods

Device fabrication and material characterization

All flakes were obtained through mechanical exfoliation from a bulk crystal onto a 285 nm-thick SiO_2/Si substrate. The flakes were characterized using Raman spectroscopy (JASCO) with 532 nm laser excitation under ambient conditions and atomic force microscopy (Park Systems, NX10) to confirm the thickness of all flakes. The pick-up transfer technique was used to fabricate flakes comprising the top WSe_2 channel, hBN tunneling layer, and bottom graphene floating gate. A polydimethylsiloxane (PDMS) stamp coated with a polycarbonate (PC) film was used for the transfer. The stacked heterostructure was

transferred onto the SiO_2/Si substrate by releasing the PC film from the PDMS at 180°C. The PC film was dissolved in chloroform overnight. The source and drain contacts were patterned using e-beam lithography (Raith, Pioneer 2). The metals of Ti (30 nm)/Au (30 nm) were deposited using an e-beam evaporator (Korea Vacuum Tech.) under ultrahigh vacuum conditions of ~ 10^{-7} Torr, followed by a lift-off process. The fabricated devices were annealed at 200°C for 3 h at 10^{-4} Torr to enhance adhesion between the layers and remove polymer residues.

Electrical measurements

A semiconductor parameter analyzer (Keithley, 4200A-SCS) was used in all electrical measurements under ambient conditions. For electrical measurements of the inverters consisting of two WSe_2 R-FGFETs, the pads of the samples were connected using a wire bonder (Kulicke & Soffa, K4523).

Device modeling and circuit simulation

The device model used in this work is based on a conventional ambipolar FET compact model with modifications to include V_{th} shift behavior. Verilog-A model is used to simulate the electrical behavior of FGFET, and SPICE simulation is used to perform analog circuit simulation. More details about the device modeling and circuit simulation are provided in Supplementary Notes 1 and 2.

Declarations

Acknowledgments

This work was supported by the Creative-Pioneering Researchers Program through Seoul National University (SNU), and the National Research Foundation (NRF) of Korea Grant funded by the Korean Government (2021R1A3B2079882, 2021R1A2C3014316, 2017R1A5A1014862 (SRC program: vdWMRC center). K.W. and T.T. acknowledge support from the JSPS KAKENHI (Grant Numbers 20H00354 and 23H02052) and World Premier International Research Center Initiative (WPI), MEXT, Japan. G.H.L. acknowledges the support from the Research Institute of Advanced Materials (RIAM), Institute of Engineering Research (IER), Institute of Applied Physics (IAP), and Inter-University Semiconductor Research Center (ISRC) at the Seoul National University.

Author contributions

J.-C.S., T.P., and G.H.L. conceived and designed the study. J.-C.S. and H.-Y.C carried out device fabrication, characterization of materials, electrical measurements, and data analyses. T.P., D.H.S., and C.S.H. performed the device modeling and circuit simulation. K.W. and T.T. provided the hBN crystals. J.-C.S., T.P., D.H.S. H.-Y.C., Y. J., C.S.H, and G.H.L. wrote the manuscript. All authors discussed the results and contributed to the final manuscript.

Competing interests

The authors declare no competing financial interests.

References

1. Beyond von Neumann. *Nat. Nanotech.* **15,** 507-507 (2020).
2. Sebastian, A. *et al.* Memory devices and applications for in-memory computing. *Nat. Nanotech.* **15,** 529–544 (2020).
3. López, C. Artificial intelligence and advanced materials. *Adv. Mater.* **35**, 202208683 (2023).
4. Ghose, S. *et al*. Processing-in-memory: A workload-driven perspective. *IBM J. Res. Dev.* **63**, 3:1-3:19 (2019).
5. Khoram, S. *et al.* Challenges and opportunities: From near-memory computing to in-memory computing. in *Proceedings of the 2017 ACM on International Symposium on Physical Design* 43–46 (ACM, 2017).
6. Cai, F. *et al.* A fully integrated reprogrammable memristor–CMOS system for efficient multiply–accumulate operations. *Nat. Electron.* **2**, 290–299 (2019).
7. Seok, J. Y. *et al.* A review of three-dimensional resistive switching cross-bar array memories from the integration and materials property points of view. *Adv. Funct. Mater.* **24**, 5316–5339 (2014).
8. Hu, X. *et al.* Overhead Requirements for Stateful Memristor Logic. *IEEE TCAS-I* **66**, 263–273 (2019).
9. Reuben, J. *et al.* Memristive logic: A framework for evaluation and comparison. in *2017 27th International Symposium on Power and Timing Modeling, Optimization and Simulation.* 1–8 (2017)
10. Park, T. *et al.* Reliable domain-specific exclusive logic gates using reconfigurable sequential logic based on antiparallel bipolar memristors. *Adv. Intell. Syst.* **4**, 2100267 (2022).
11. Zhu, J. *et al.* Reconfigurable systems for multi-functional electronics. *npj Flex. Electron.* **1**, 8 (2017).
12. Fei, W *et al.* Emerging reconfigurable electronic devices based on two-dimensional materials: A review. *InfoMat* **4**,e12355 (2022).
13. Mikolajick, T. *et al.* Reconfigurable field effect transistors: A technology enablers perspective. *Solid State Electron.* **194**, 108381 (2022).
14. Mikolajick, T. *et al.* The RFET—a reconfigurable nanowire transistor and its application to novel electronic circuits and systems. *Semicond. Sci. Technol.* **32**, 043001 (2017).
15. Resta, G. V. *et al.* Doping-free complementary logic gates enabled by two-dimensional polarity-controllable transistors. *ACS Nano.* **12**, 7039-7047 (2018).
16. Pan, C. *et al.* Reconfigurable logic and neuromorphic circuits based on electrically tunable two-dimensional homojunctions. *Nat. Electron.* **3**, 383-390 (2020).
17. Wu, P. *et al.* Two-dimensional transistors with reconfigurable polarities for secure circuits. *Nat. Electron.* **4**, 45-53 (2021).

18. Huang, X. *et al.* An ultrafast bipolar flash memory for self-activated in-memory computing. *Nat. Nanotechnol.* **18**, 486-492 (2023).
19. Sun, X. *et al.* Reconfigurable logic-in-memory architectures based on a two-dimensional van der Waals heterostructure device. *Nat. Electron.* **5**, 752-760 (2022).
20. Migliato Marega, G. *et al.* Logic-in-memory based on an atomically thin semiconductor. *Nature* **587**, 72-77 (2020).
21. Rabaey, J. M. *Digital integrated circuits a design perspective*. (1999).
22. Wang, Z. *et al.* The ambipolar transport behavior of WSe_2 transistors and its analogue circuits. *NPG Asia Mater.* **10**, 703-712 (2018).
23. Resta, G. V. *et al.* Polarity control in WSe_2 double-gate transistors. *Sci. Rep.* **6**, 29448 (2016).
24. Shin, J. C. *et al.* Electrically confined electroluminescence of neutral excitons in WSe_2 light-emitting transistors. *Adv. Mater.* 202310498 (2024).
25. Dean, C. R. *et al.* Boron nitride substrates for high-quality graphene electronics. *Nat. Nanotechnol.* **5**, 722-726 (2010).
26. Cui, X. *et al.* Multi-terminal transport measurements of MoS_2 using a van der Waals heterostructure device platform. *Nat. Nanotechnol.* **10**, 534-540 (2015).
27. Ahmad, M. H. *et al.* Graphene as charge storage layer in floating gate flash memory with highk tunnel barrier engineering in *2018 IEEE Student Conference on Research and Development* 1-5 (2018).
28. Choi, M. S. *et al.* Controlled charge trapping by molybdenum disulphide and graphene in ultrathin heterostructured memory devices. *Nat. Commun.* **4**, 1624 (2013).
29. Zomer, P. J. *et al.* Fast pick up technique for high quality heterostructures of bilayer graphene and hexagonal boron nitride. *Appl. Phys. Lett.* **105**, 013101 (2014).
30. Li, X. *et al.* Cascaded logic gates based on high-performance ambipolar dual-gate WSe_2 thin film transistors. *ACS Nano* **17**, 12798-12808 (2023)
31. Chen, H. *et al.* Logic gates based on neuristors made from two-dimensional materials. *Nat. Electron.* **4**, 399-404 (2021).
32. Zeng, S. *et al.* An application-specific image processing array based on WSe_2 transistors with electrically switchable logic functions. *Nat. Commun.* **13**, 56 (2022).
33. Wang, H. *et al.* Integrated circuits based on bilayer MoS_2 transistors. *Nano Lett.* **12**, 4674–4680 (2012).
34. Wang, X. *et al.* Pass-transistor logic circuits based on wafer-scale 2D semiconductors. *Adv. Mater.* **34**, 2202472 (2022).
35. Yi, J. *et al.* Double-gate MoS_2 field-effect transistors with full-range tunable threshold voltage for multi-functional logic circuits. *Adv. Mater.* **33**, 2101036 (2021).
36. Liao, F. *et al.* MoS_2 dual-gate transistors with electrostatically doped contacts. *Nano Res.* **12**, 2515–2519 (2019).

37. Lee, G. H. *et al.* Highly stable, dual-gated MoS_2 transistors encapsulated by hexagonal boron nitride with gate-controllable contact, resistance, and threshold voltage. *ACS Nano* **9**, 7019–7026 (2015).
38. Liu, C. *et al.* Small footprint transistor architecture for photoswitching logic and in situ memory. *Nat. Nanotechnol.* **14**, 662-667 (2019).
39. Yadav, A. K. *et al.* Low power high speed 1-bit full adder circuit design at 45nm CMOS technology in *2017 International Conference on Recent Innovations in Signal processing and Embedded Systems* 427-432 (IEEE, 2017).
40. Kuon, I. *et al.* FPGA architecture: survey and challenges. *Found. Trends Electron. Des. Autom.* **2**, 135-253 (2008).
41. Wali, A. *et al.* Hardware and information security primitives based on 2D materials and devices. *Adv. Mater.* **35**, 2205365 (2023).

Figures

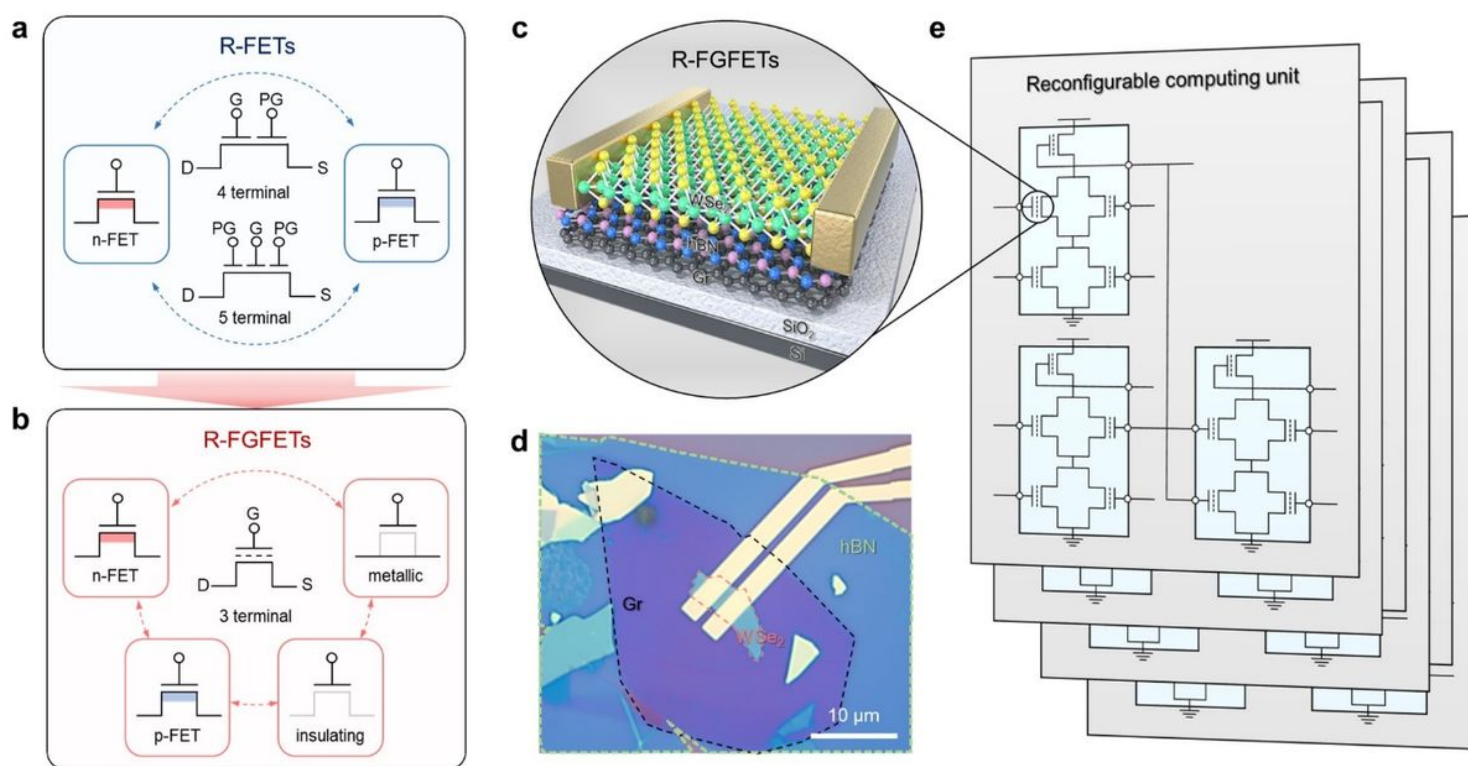


Figure 1

WSe_2 R-FGFET for highly integrated in-memory computing. a, b, Schematics of traditional R-FETs (**a**) and the proposed R-FGFET (**b**). The R-FGFET offers more operational functions using a single gate terminal compared to conventional R-FETs with four or five terminals. **c, d,** Schematic diagram (**c**) and optical microscopy image (**d**) of R-FGFET, a key component of the reconfigurable CU. **e,** Reconfigurable CUs

composed of WSe_2 R-FGFETs to perform multiple functions, including arithmetic and logical operation, within the same configuration.

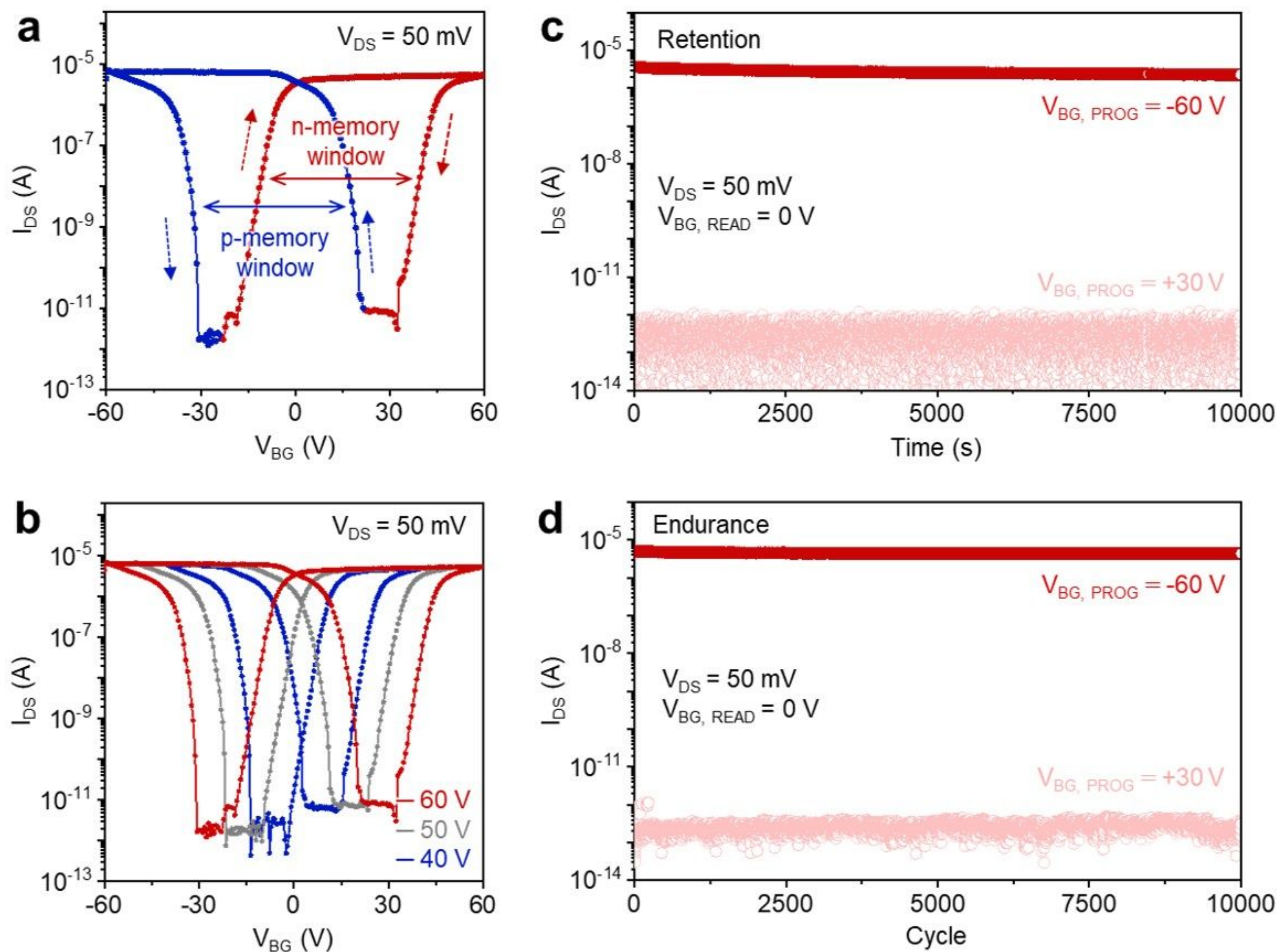


Figure 2

Ambipolar nonvolatile memory characteristics of WSe_2 R-FGFET. a, Transfer curve (I_{DS}-V_{BG}) of the WSe_2 R-FGFET at a fixed voltage of V_{DS} = 50 mV. The transfer curve exhibits the ambipolar memory characteristic with large hysteresis. **b,** Transfer curve (I_{DS}-V_{BG}) of the WSe_2 R-FGFET with various sweep ranges. As the sweep range of V_{BG} increases, both n- and p-memory windows expand. **c,** Retention performance for n-type transport on the time dependence of drain current for high conductance state (dark red circle) and low conductance state (light red circle). **d,** Cycle endurance performance of n-type transport with the high conductance state (dark red circle) and low conductance state (dark light circle). The WSe_2 R-FGFET has long retention times and high endurance in n-type memory performance

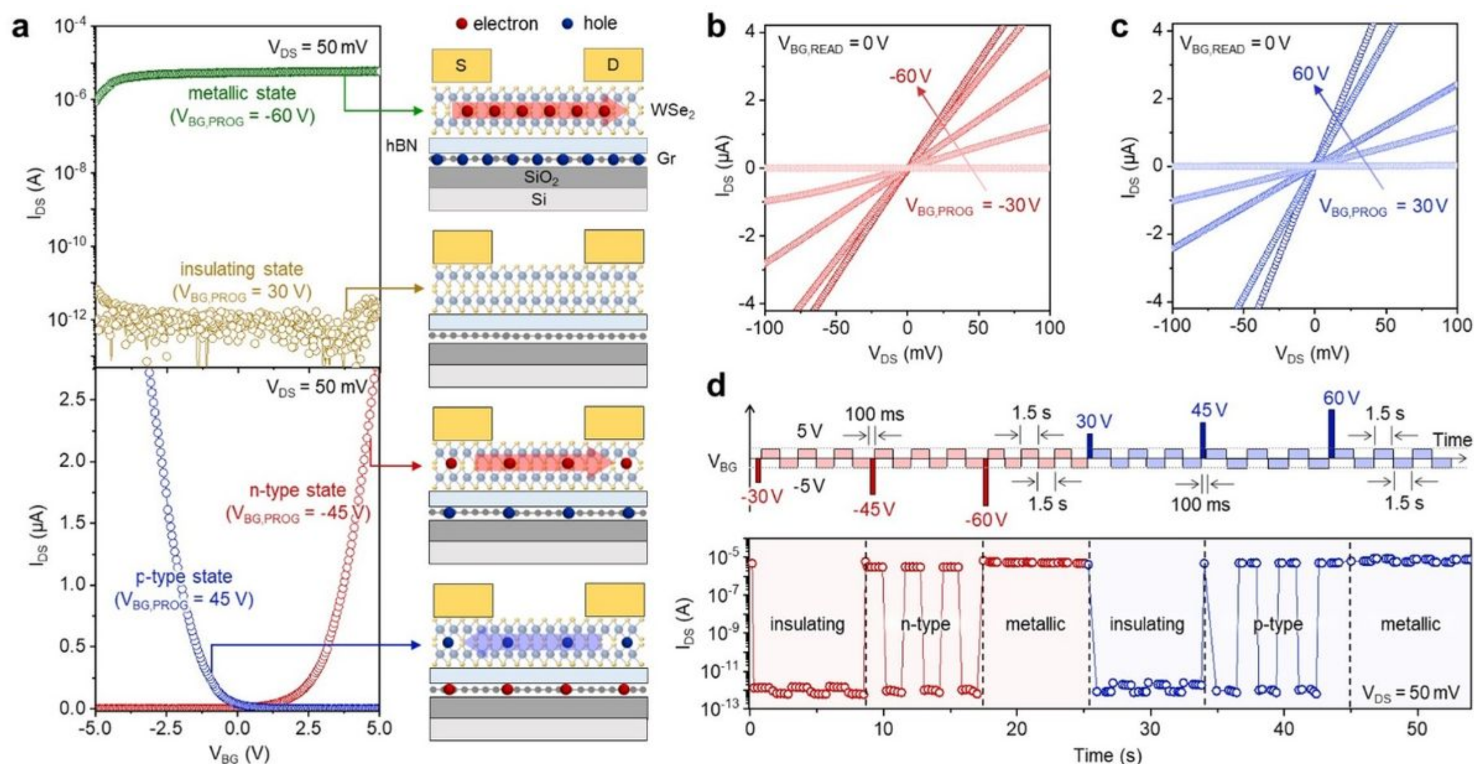
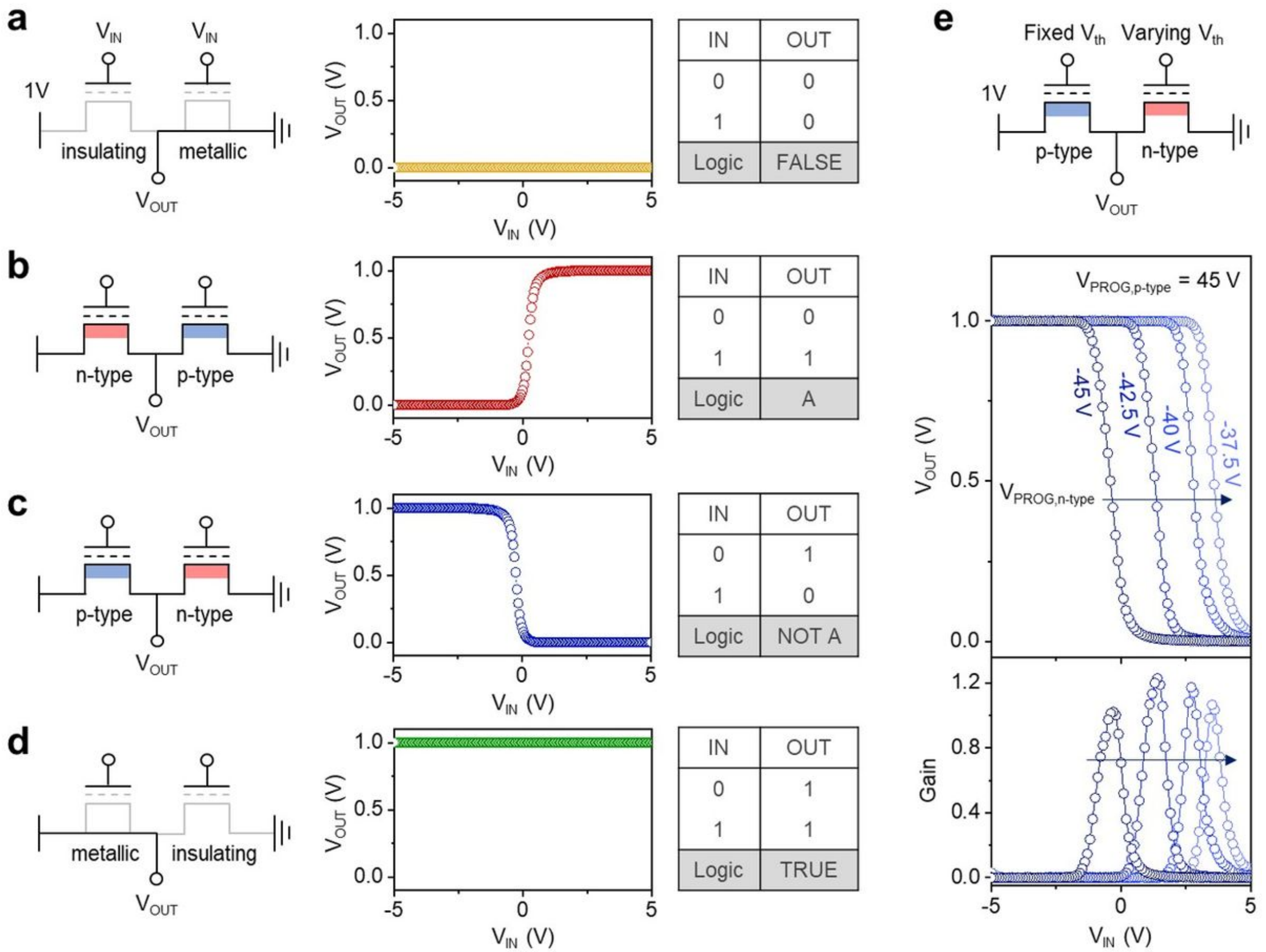


Figure 3

Reconfigurable electrical switching characteristics of WSe_2 R-FGFET. a, Reconfigurable transfer curve (I_{DS}-V_{BG}) and the corresponding schematic diagrams of the working mechanism of the WSe_2 R-FGFET under different programming conditions using $V_{BG, PROG.}$ The transfer curve exhibits reconfigurable operations, including metallic, insulating, n-type semiconductor (n-type), and p-type semiconductor (p-type) states, which are determined by the type and density of carriers trapped in graphene as the floating gate. **b, c,** Output curves (I_{DS}-V_{DS}) of the WSe_2 R-FGFET measured at fixed $V_{BG, READ}$ = 0 V, for various programming conditions. **d,** Dynamic switching performance of the reconfigurable operations as a function of programming pulse.



IN	OUT
0	0
1	0
Logic	FALSE

IN	OUT
0	0
1	1
Logic	A

IN	OUT
0	1
1	0
Logic	NOT A

IN	OUT
0	1
1	1
Logic	TRUE

Figure 4

Programmable inverter based on WSe_2 R-FGFETs. a-d, Schematic of circuit diagrams, voltage transfer curves, and truth tables for different programming states of the programmable inverter (INV). By configuring each reconfigurable FGFET into distinct states, the INV enables reprogrammable logic operations such as FALSE (a), A (b), NOT A (c), and TRUE (d). **e,** Voltage transfer curve and voltage gain of the complementary inverter at various programming voltage of n-type state. The programmable inverter offers a threshold voltage shift of the voltage transfer curve using electrical modulation to align the operating voltage

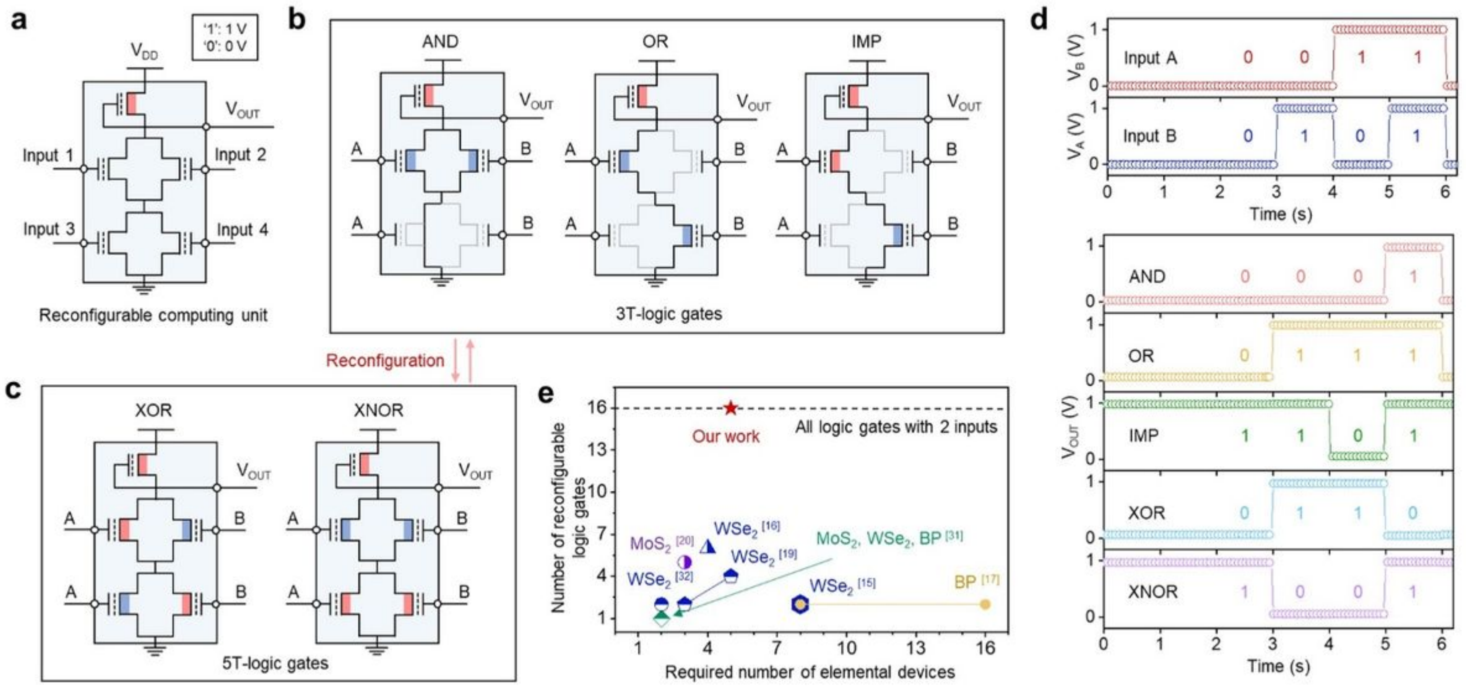


Figure 5

Reconfigurable logic gate with four-mode WSe_2 R-FGFET. a, Circuit diagram of proposed reconfigurable CU. **b,** 3T-logic gate structure and reconfiguration with proposed FGFET devices **c,** 5T-logic gate structure and reconfiguration with proposed FGFET devices. **d,** Circuit simulation results of input and output in voltage form. **e,** Benchmark plot showing the number of devices in 2-input circuits and the reconfigurable logic numbers for our WSe_2 R-FGFET, compared with previously reported reconfigurable devices.

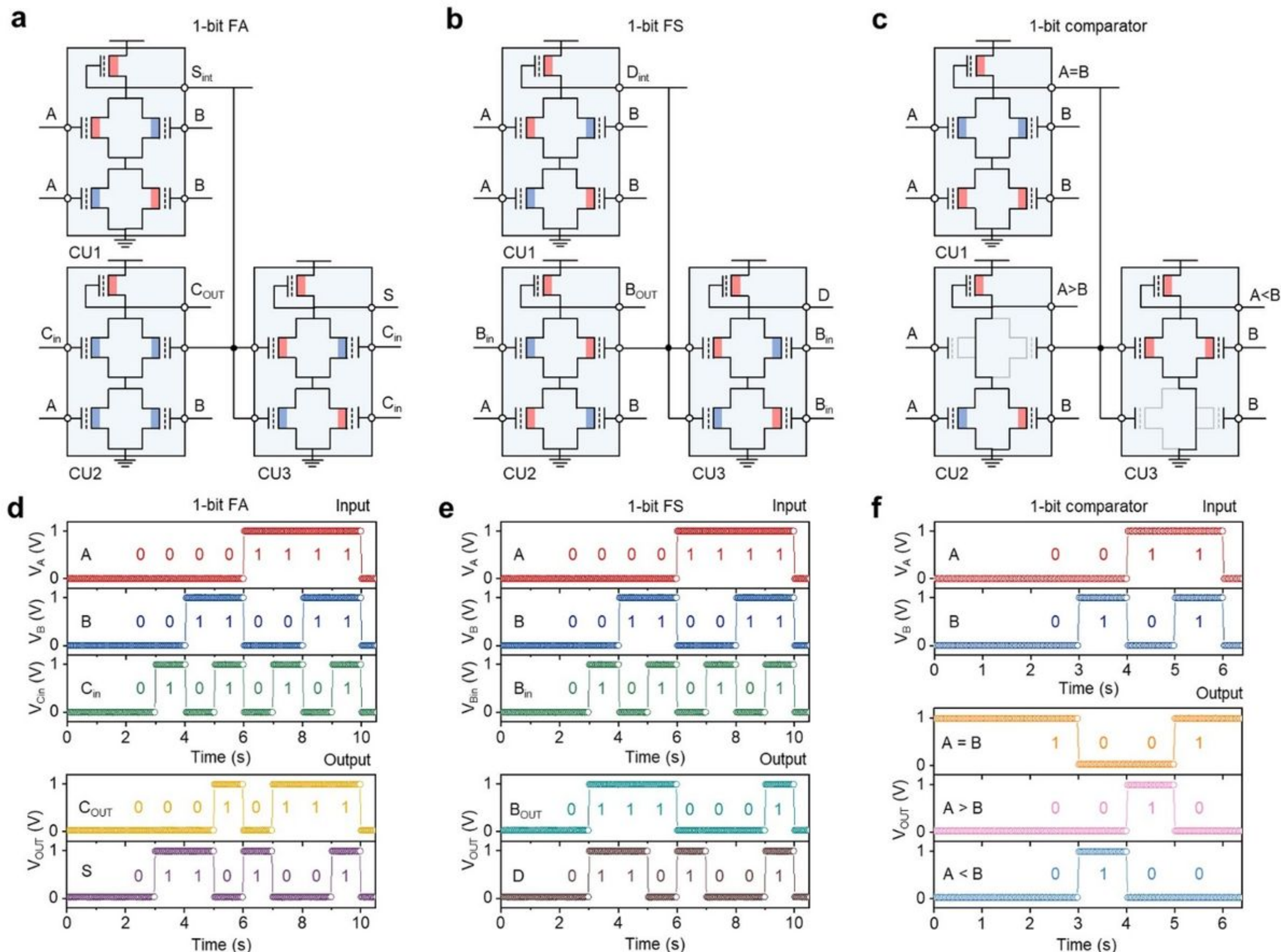


Figure 6

Reconfigurable CUs for arithmetic operation. a-c, Schematics of three combined configurations to demonstrate (**a**) 1-bit full adder (FA), (**b**) 1-bit full subtractor (FS), and (**c**) 1-bit comparator. **d-f,** Circuit simulation results of each operation: (**d**) 1-bit FA, (**e**) 1-bit FS, (**f**) 1-bit comparator.

Supplementary Files

This is a list of supplementary files associated with this preprint. Click to download.

- SI.docx
- ExtendeddataFiguresandTables.docx