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Atomic-scale ferroic HfO_2-ZrO_2 superlattice gate stack for advanced transistors

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With the scaling of lateral dimensions in advanced transistors, an increased gate capacitance is desirable both to retain the control of the gate electrode over the channel and to reduce the operating voltage[1]. This led to the adoption of high-κ dielectric HfO_2 in the gate stack in 2008[2], which remains as the material of choice to date. Here, we report HfO_2-ZrO_2 superlattice heterostructures as a gate stack, stabilized with mixed ferroelectric-antiferroelectric order, directly integrated onto Si transistors and scaled down to $\sim$ 20 Å, the same gate oxide thickness required for high performance transistors. The overall EOT (equivalent oxide thickness) in metal-oxide-semiconductor capacitors is equivalent to $\sim$ 6.5 Å effective SiO_2 thickness, which is, counterintuitively, even smaller than the interfacial SiO_2 thickness (8.0-8.5 Å) itself. Such a low effective oxide thickness and the resulting large capacitance cannot be achieved in conventional HfO_2-based high-κ dielectric gate stacks without scavenging the interfacial SiO_2, which has adverse effects on the electron transport and gate leakage current[3]. Accordingly, our gate stacks, which do not require such scavenging, provide substantially lower leakage current and no mobility degradation. Therefore, our work demonstrates that HfO_2-ZrO_2 multilayers with competing ferroelectric-antiferroelectric order, stabilized in the 2 nm thickness regime, provides a new path towards advanced gate oxide stacks in electronic devices beyond the conventional HfO_2-based high-κ dielectrics.

With the two-dimensional scaling of silicon field-effect transistors reaching fundamental limits[1], new functional improvements to transistors[4], as well as novel computing paradigms and vertical device integration at the architecture-level[5], are currently under intense study[1,4,6]. Gate oxides play a critical role in this endeavor, as it's a common performance booster for all devices, including silicon[2], new channel materials with potential for higher performance[7,8], and even materials suitable for three-dimensional integrated transistors[9,10]. Indeed, the gate oxide transition from SiO_2 to high-κ dielectric (DE) is considered a paradigm shift in computing technology. In this context, ferroelectric oxides offer new functionalities[11] considered promising for energy-efficient electronics[4,9]. The advent of atomic layer deposition (ALD) grown ferroelectric doped-HfO_2[12] has overcome much of the material compatibility issues that plague traditional perovskite-based ferroelectric materials[2]. In addition, considering ferroic order persists down to a thickness of 1 nm in this system[13–15] allows for integration of these oxides in the most aggressively-scaled devices in which the state-of-the-art high-κ oxide thickness is less than 2 nm.

In an advanced silicon transistor, the gate oxide is a combination of two distinct layers. The first is an interfacial SiO_2 formed with a self-limiting process, resulting in $\sim$ 8.0-8.5 Å thickness[16]. The next is the high-κ (HK) dielectric HfO_2 layer that is typically $\sim$ 2 nm in thickness. Higher capacitance of this series combination is desirable to suppress short channel effects. The capacitance is conventionally represented by effective oxide thickness (EOT), EOT = $t_{SiO_2} + t_{HK}/(\epsilon_{HK}/\epsilon_{SiO_2})$, where lower EOT represents higher capacitance. Therefore, the EOT minimum value is limited by the interfacial SiO_2 thickness. Indeed, even integrating HfO_2 as the high-κ layer, the EOT is typically $\sim$ 9 Å. To go below this value[17], the semiconductor industry has implemented sophisticated scavenging techniques[16,18] to reduce the SiO_2 thickness after the full gate stack is formed. Although this technique is very effective in scaling EOT, the thinner SiO_2 results in undesirable leakage[19] and mobility degradation[2,16,20,21].

In this work, we present an ultrathin HfO_2-ZrO_2 superlattice gate stack that exploits mixed ferroelectric-antiferroelectric (FE-AFE) order (Fig. 1a,b). Our films demonstrate mixed ferroic order down to 2 nm thickness – the same thickness of high-κ oxide used in advanced transis-

tors. Moreover, when integrated with silicon, it shows an overall EOT of <6.5 Å, despite the fact that both transmission electron microscopy (TEM) and electrical characterization reveal 8.0-8.5 Å interfacial SiO_2 thickness, as is typically expected. The larger capacitance than its constituent layers is a signature of the charge boost stemming from the negative capacitance effect, possible in materials with ferroic order[11]. The EOT shows a clear dependence on the specific sequence and layering, underlying atomic-level control of the gate oxide behavior. The fact that sub-8 Å EOT is achieved without any interfacial SiO_2 scavenging results in substantially lower leakage current for the same EOT compared to benchmarks established by major semiconductor industries[3]. In addition, no mobility degradation is observed as EOT is scaled with these HfO_2-ZrO_2 ferroic gate stacks. Furthermore, large ON current ($>$ 1mA/μm) obtained in L_G = 90 nm transistors indicate that there is no adverse effect on the carrier velocity. Therefore, ultrathin HfO_2-ZrO_2 multilayers exploiting ferroic order provide a new pathway toward energy-efficient gate stacks for advanced transistors.

Thin films of HfO_2-ZrO_2 are grown using ALD in which the nanolaminate periodicity is dictated by the sequence of Hf:Zr (4:12) ALD cycles before the Hf-Zr superstructure is repeated various times (Figure 1c, Methods). After top metal deposition, the entire gate stack undergoes a low-temperature post-metal anneal (200 C, 60s, N_2) which does not interfere with the HfO_2-ZrO_2 multilayer structure, as various characterization techniques – synchrotron x-ray reflectivity (XRR), layer-resolved electron energy loss spectroscopy (EELS) and angle-resolved X-ray photoelectric spectroscopy (XPS) – confirm the expected Hf 4 Å - Zr 12 Å periodicity (Extended Data Fig. 1). The underlying mixed ferroic order in these HfO_2-ZrO_2 heterostructure is established by high-resolution transmission electron microscopy (TEM) (Fig. 1d, Extended Data Fig. 2e,f) and in-plane grazing incidence diffraction (Fig. 1e and Extended Data Fig. 2a,b). Both techniques indicate the presence of the tetragonal ($P4_2/nmc$, T-) and orthorhombic ($Pca2_1$, O-) phase, which correspond to antiferroelctric and ferroelectric order in fluorite-structure films, respectively. Synchrotron X-ray spectroscopy and optical spectroscopy further confirm the presence of inversion symmetry breaking in the 2 nm HfO_2-ZrO_2-HfO_2 heterostructure (Extended Data Fig. 2c,d).

Mixed-ferroic atomic-scale HfO_2-ZrO_2 multilayers were designed considering FE-AFE order can tune the free energy landscape in a similar manner to the FE-DE model systems originally studied for negative capacitance stabilization[11,22] (Fig. 1a). From the free energy landscape picture within a Landau formalism (Methods), the competition between the negative curvature (i.e. negative capacitance) of the FE and the positive curvature (i.e. positive capacitance) of the AFE can flatten the overall energy landscape, thereby substantially increasing the system's susceptibility. To confirm the higher susceptibility in the mixed AFE-FE system directly, we have performed capacitance-voltage (*C-V*) hysteresis loops in metal-insulator-metal (MIM) capacitor structures on thicker films with the same superlattice periodicity (Fig. 2a). Besides features indicative of mixed FE-AFE order, the total capacitance for the superlattice is larger than both conventional AFE ZrO_2 and FE Zr:HfO_2 of the same thickness (Fig. 2a), demonstrating enhanced susceptibility. To quantify the permittivity, capacitance measurements were performed across the superlattice thickness series. These measurements yield an extracted permittivity of ~ 52 (Fig. 2b, Methods), which is larger than both FE orthorhombic Zr:HfO_2 and AFE tetragonal ZrO_2 values[23].

To further understand the ferroic evolution in these HfO_2-ZrO_2 superlattices, we performed low temperature measurements where enhanced FE phase stabilization is expected. Indeed, temperature-dependent *C-V* loops for thicker HfO_2-ZrO_2 multilayers demonstrate an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room temperature (~ 240 K, Fig. 2c), consistent with temperature-dependent X-ray spectroscopy indicating transition from mixed tetragonal-orthorhombic phase to predominately orthorhombic structure at similar temperatures (Extended Data Fig. 3). The capacitance decrease upon cooling as the system moves away from the highly-susceptible mixed ferroic phase is consistent with previous work on negative capacitance in FE-DE systems[22] which establishes the energy landscape link between enhanced capacitance and susceptibility near phase transitions. Notably, the intertwined FE-AFE phases within the superlattice and resulting enhancement in susceptibility from the competition of FE and AFE phases is conceptually similar to negative stiffness composites of ferroelastics within a metal matrix[24,25], i.e. the mechanical analog to negative capacitance.

Next, the superlattices were grown on Si substrates in metal-oxide-semiconductor (MOS) capacitor structures. A self-limiting chemical oxide SiO_2 was grown first, resulting in $\sim$ 8.0-8.5 Å thickness[3], following the standard practice in advanced Si devices (Methods). Next, a 20-cycle thick multilayer was grown with ALD following the same stacking as before i.e. Hf:Zr:Hf 4:12:4. Accumulation *C-V* curves of the superlattice stack results in significantly larger capacitance in comparison to other conventional stacks – DE HfO_2, AFE ZrO_2, FE Zr:HfO_2 – of the same 20 Å thickness (Fig. 2d). Furthermore, the Hf:Zr:Hf 4:12:4 trilayer demonstrates enhanced capacitance compared to a bilayer (Hf:Zr 8:12) and solid solution (Hf:Zr $[2:3]_4$) of the same thickness and Hf:Zr composition (Fig. 2e). Notably, the composition in our films is close to where several previous reports have postulated a possible morphotropic phase boundary (MPB) in thicker HfO_2-ZrO_2 solid solution films[26–30]. In our ultrathin HfO_2-ZrO_2 multilayers, the negative free energy curvature of the FE O-phase compensates the positive curvature of the AFE T-phase (Fig. 1a), leading to a flattened energy landscape. Indeed, energy landscape flattening is the thermodynamic origin of the MPB in the canonical perovskite ferroelectrics[31,32], in which multiple crystal symmetries are nearly degenerate across a composition phase boundary[33]. However, a critical distinction is that here, the overall energy landscape flattening, and corresponding increase in capacitance, is determined by the stacking of the atomic-scale HfO_2-ZrO_2 layers, and not the volume fraction of the constituent elements[34]. For example, compared to HfO_2-ZrO_2 solid solutions across a range of typically-reported Zr-rich "MPB"-like compositions[26–30], the HfO_2-ZrO_2 multilayer demonstrates larger capacitance (Extended Data Fig. 4). This indicates the enhanced capacitance in HfO_2-ZrO_2 films is not simply driven by doping[23,35], but can instead be tuned by the configuration of the multilayer structure (Extended Data Fig. 4, 5). In the ultrathin regime, surface energies become a more dominant consideration for determining polymorphic phase stability[36,37]; accordingly, the importance of stacking is amplified. Overall, these capacitor studies suggest that the exact stacking sequence plays a crucial role in stabilizing the fluorite-structure FE-AFE phase competition that leads to enhanced capacitance, akin to previous reports in perovskite-based FE-DE superlattices[38–42].

To quantify the observed capacitance, we have performed EOT simulations of MOS capac-

itors using the industry standard model Synopsys simulation platform (Methods). The Hf:Zr:Hf 4:12:4 trilayer stacks vary between 6.5-7.0 Å EOT (Fig. 2f), consistent over many measured capacitors. Notably, this EOT is smaller than the expected thickness of the interfacial SiO_2 layer (8.0-8.5 Å), as mentioned above. To investigate further, we performed high-resolution TEM of our gate stacks (Extended Data Fig. 6), which illustrates the SiO_2 thickness is indeed $\sim$8.5 Å. To supplement this physical characterization, we next implemented electrical characterization of the interfacial layer via standard inverse capacitance vs thickness analysis of conventional dielectric HfO_2 and Al_2O_3 thickness series grown on the same SiO_2 (Methods, Extended Data Fig. 6). All thermal processing is kept exactly the same as the superlattice gate stack. The extracted HfO_2 and Al_2O_3 permittivity – 19 and 9, respectively – is consistent with the typical dielectric phases of these two materials. Therefore, one can reliably extract the SiO_2 layer thickness, yielding 8 Å (Extended Data Fig. 6), consistent with the HR-TEM results and similar to previously studies established by the semiconductor industry[3]. Moreover, the consistent interlayer thickness extracted from both material systems indicates that neither Hf nor Al encroaches into the interfacial SiO_2 which would reduce its thickness and/or increase its permittivity. This is consistent with the fact all our stacks are processed at much lower temperature as compared to that needed for silicate formation[43]. So considering the interfacial layer thickness as 8 Å, the Hf:Zr:Hf 4:12:4 gate stack demonstrates an overall EOT 1.0-1.5 Å lower than the constituent SiO_2 thickness. In other words, capacitance enhancement is observed in this 20 Å mixed ferroic gate oxide integrated on Si. Therefore, the mixed FE-AFE order not only improves the permittivity of the multilayer stack itself, but also couples to the SiO_2 in MOS capacitor structures, yielding improved overall capacitance.

The practical implication of this capacitance enhancement can be clearly seen in Fig. 3a, which shows leakage current vs EOT behavior. The leakage current is measured at V_G - V_{fb} = -1 V, where V_{fb} is the flatband voltage of the semiconductor. All other data points on this plot are taken from reported industrial gate stacks[3]. The leakage current for the Hf:Zr:Hf 4:12:4 stack is substantially lower at the same EOT. Note that below 9 Å, the other gate stacks need sophisticated scavenging techniques to reduce the thickness of the interfacial SiO_2[3]. On the other hand, we can reach $\sim$ 6.5 Å without any scavenging. This leads to the fact that the leakage current for our

stacks is lower (Fig. 3a). Notably, the scavenging the interfacial SiO_2 leads to a loss of mobility due to increase in remote phonon scattering. As it has been shown[3,16], the mobility drops off with a slope of $\sim$ 20 cm^2/V-s per every Å of scavenged SiO_2. To test how mobility is affected by the superlattice gate stack, we fabricated long channel bulk transistors with two different repeats of the superlattice, together with another sample that has thick (60 Å) HfO_2 as the gate stack (Methods). To extract mobility, a careful fitting of the measured *C-V* from the transistor structures is performed. In addition, series resistance is modeled from the data and de-embedded to reveal the intrinsic behavior. Next, the mobility is extracted using the peak transconductance method (Methods, Extended Data Fig. 8). It is found that the mobility remains essentially the same for all three stacks despite the difference in materials and EOT (from 2 nm EOT for HfO_2 down to sub-8 Å for the superlattice gate stack). First, this shows that there is no fundamental change in electron transport due to the use of the superlattice gate stack compared to standard HfO_2. In addition, it shows that there is no penalty in mobility even below an EOT of 9 Å where conventional gate stacks show a degradation due to the need for scavenging (Fig. 3b). Because the absolute value of mobility depends on the specific processing technique, mobility numbers have been normalized in Fig. 3b. This clearly shows the flat mobility-EOT behavior for the superlattice gate stack compared to the falling of trend for conventional gate stacks due to scavenging in the low EOT range.

To examine how the capacitance enhancement behaves at high frequency, radio frequency (RF) measurements were performed on the same long channel (L_G = 1 μm) devices (Methods, Extracted Data Fig. 9). This allows one to extract device parameters up to $\sim$ 800 MHz for our devices (close to the cut-off frequency). Of particular interest is the transconductance (g_m) which is proportional to the product of capacitance and electron velocity (mobility). From Y-parameter measurements one can find AC transconductance as $Re(Y_{21}) = g_m + af^2$, where f is the frequency (Methods). This yields an AC transconductance as a function of applied gate voltage (V_G). This dependence is plotted together with DC transconductance ($\partial I_D/\partial V_G$ from DC I_D-V_G) (Fig. 3c). We find that DC and AC transconductance are similar with AC transconductance roughly 15% larger at the peak value. We hypothesize that this slightly large AC transconductance results from the fact that certain interface traps, which affect the DC behavior, cannot respond at frequencies

larger than 100 MHz, leading to better gate control. More importantly, these results show that the capacitance enhancement is not limited to the low frequency regime[44–46].

Finally, to test the ON current capability, a L_G = 90 nm device was fabricated on a SOI transistor with 18 nm SOI thickness and the superlattice gate stack. The transfer and output characteristic of a typical transistor are shown in Fig. 3d,e. Note that the threshold voltage of this device is 0.55 V which is consistent with the workfunction of W used as the gate metal. Because of this, the transistors have been driven up to 1.6 V gate voltage so that an overdrive voltage (V_{ov} = V_G - V_T) of $\sim$1 V can be applied. It is found that at a drain voltage (V_D) and V_{ov} of 1 V, the drain current exceeds 1 mA/μm. In addition, as shown in Fig. 3f, the measured extrinsic transconductance is $\sim$1.1 mS/μm which gives an intrinsic transconductance of $\sim$1.75 mS/μm (Methods, Extended Data Fig. 10). These values of ON current and transconductance are substantially larger than a conventional 90 nm transistor and is a result of the large capacitance provided by the superlattice gate stack and the fact that the low EOT resulting from the stack does not adversely affect the electron transport.

With the superlattice gate stack demonstrated in integrated Si devices, we now come back to the capacitance enhancement observed in this gate stack. We have already discussed how the mixed FE-AFE order facilitates a flatter energy landscape where the negative curvature of the FE phase is compensated by the positive curvature of the AFE phase (Fig. 1a). Notably when the mixed ferroic oxide is grown on an SiO_2 interlayer, it can lead to similar compensation again. As we have seen from thicker FE-AFE superlattice MIM capacitors, some hysteresis still remains, which manifests at large voltages, indicative of a negative curvature regime still persisting in the superlattices. The interfacial DE SiO_2 can flatten out that energy landscape even further, thus leading to enhanced capacitance. This is similar to the negative capacitance and resultant capacitance enhancement observed in FE-DE series combinations[22]. To supplement the *C-V* evidence of capacitance enhancement (Fig. 2f), pulsed electrical measurements of the superlattice gate stack MOS capacitors – which can quantify the amount of stored charge as a function of voltage[47] (Methods) – demonstrate larger stored charge than if just interfacial SiO_2 was sitting on top of Si, providing further

evidence of negative capacitance[47] in the gate stack (Extended Data Fig. 10). Note that previous studies have shown that negative capacitance stabilization is favored under states of high susceptibility[39,40,48]. Here, the competing ferroic order in HfO_2-ZrO_2 multilayers substantially increases its susceptibility and is thus expected to facilitate negative capacitance behavior when placed on top of the interfacial SiO_2.

Capacitance enhancement has been demonstrated in single-crystalline, perovskite-structure ferroelectric-dielectric superlattices by many groups[38–41]. This work demonstrates that the same enhancement is possible in HfO_2-ZrO_2 fluorite-structure superlattices exhibiting mixed ferroelectric-antiferroelectric order in films as thin as just $\sim$ 2 nm. The ability to control ferroic order in such ultrathin films is of critical importance for advanced electronic devices considering previous studies have shown that negative capacitance can be stabilized under states of high susceptibility[39,40]. Furthermore, this work establishes the critical role of atomic-layer stacking – as opposed to conventional doping techniques[23,35] – in controlling the ferroic phase space and permittivity of fluorite-structure oxides down to ultrathin limits, leveraging its unique size effects[13–15,49] and rich antiferroelectric-ferroelectric polymorphs[36,50]. When this mixed phase HfO_2-ZrO_2 multilayer is integrated on Si, the gate stack exhibits a capacitance enhancement, lowering the EOT below the thickness of SiO_2 itself, which would not be possible with a conventional dielectric. Notably, the lowest EOT achieved (6.5 Å) for the gate stack and interfacial SiO_2 together is lower than that used in the most advanced Si transistors today. Therefore, this work demonstrates that harnessing atomic-scale layering in ultrathin HfO_2-ZrO_2 ferroic gate oxides presents a promising materials design platform for future Si transistors beyond conventional high-κ dielectrics[3] which have enabled the semiconductor industry over the past two decades.

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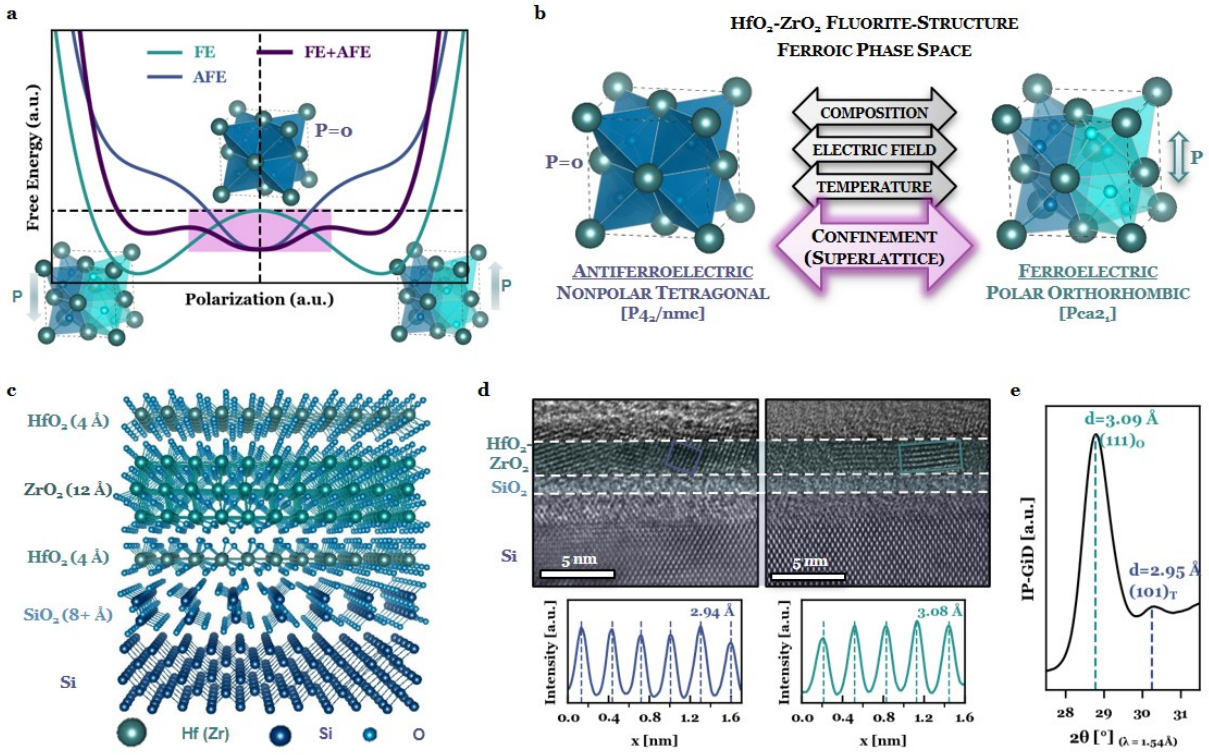

Fig. 1. Atomic-scale design of negative capacitance in ultrathin HfO_2-ZrO_2. **(a)** Phenomenological model of negative capacitance (NC) in a mixed ferroic system. Landau free energy landscapes for a FE, AFE, and mixed FE-AFE system (Methods). Mixed FE-AFE phase competition should suppress polarization[48] and enhance electric susceptibility[22,40] via proximity to a phase boundary, and flattens the energy landscape, desirable traits for NC stabilization. The stable energy minimum of the composite free energy landscape, corresponding to the negative curvature (NC) regime of the ferroelectric energy landscape, is highlighted. **(b)** Engineering ferroic phase competition in the HfO_2-ZrO_2 fluorite-structure system. Beyond the conventionally-studied tuning parameters – composition, electric field, temperature[23,35] – here we introduce dimensional confinement via superlattice layering to tailor ferroic phase competition at the atomic-scale. **(c)** Schematic of the HfO_2-ZrO_2 fluorite-structure multilayer on Si; the heterostructures maintain distinct layers (i.e. not solid solution alloys) based on EELS, XRR, and depth-resolved XPS (Extended Data Fig. 1). The role of the layering on the underlying ferroic order and capacitance is studied by electrical

measurements as a function of HfO_2-ZrO_2 stacking structure and annealing temperature (Extended Data Fig. 4 and 5, respectively). **(d)** HR-TEM image of the atomic-scale HfO_2-ZrO_2-HfO_2 trilayer (top) and extracted d-lattice spacings (bottom) corresponding to the fluorite-structure AFE tetragonal ($P4_2/nmc$, red) and FE orthorhombic ($Pca2_1$, blue) phases, respectively. The layer delineations are approximate, as the HfO_2-ZrO_2 and SiO_2 interlayer thicknesses are more rigorously determined by XRR and TEM analysis (Extended Data Fig. 1 and 6, respectively). Note imaging the crystallinity of the HfO_2-ZrO_2 layers requires mistilt with respect to the Si lattice (Methods). **(e)** Synchrotron IP-GiD demonstrating the presence of both the AFE T-phase $(101)_t$ and FE O-phase $(111)_o$ reflections whose d-lattice spacings are consistent with those extracted from TEM. Detailed indexing to higher-order reflections for structural identification of the ferroic phases is provided by wide-angle synchrotron diffraction (Extended Data Fig. 2a). Further evidence of inversion symmetry breaking is provided by second harmonic generation and synchrotron linear dichroism (Extended Data Fig. 2c,d). Additionally, the evolution between these two ferroic phases are also studied as a function of temperature (Extended Data Fig. 3).

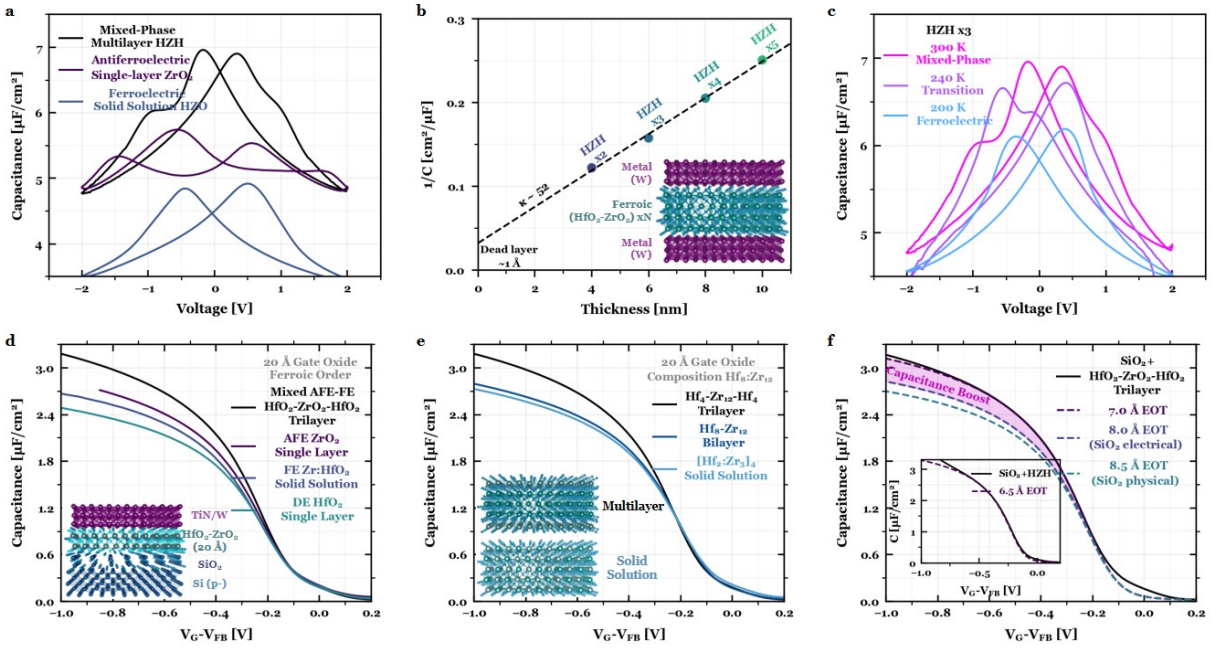

Fig. 2. Enhanced capacitance in ultrathin HfO_2-ZrO_2 mixed-ferroic heterostructures. **(a)** MIM *C-V* hysteresis loops for a mixed FE-AFE HfO_2-ZrO_2 multilayer demonstrating higher capacitance compared against its AFE (ZrO_2) and FE (Zr:HfO_2) counterparts of the same thickness. **(b)** Inverse capacitance versus thickness of the MIM HfO_2-ZrO_2 multilayers up to 5 superlattice repeats (10 nm), with an extracted permittivity of 52 (Methods), extremely large for HfO_2-based oxides. **(c)** MIM *C-V* hysteresis loops for HfO_2-ZrO_2 multilayers of the same periodicity demonstrating an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room temperature. The proximity to the temperature-dependent phase transition (Extended Data Fig. 3) suggests the HfO_2-ZrO_2 heterostructures lies near its maximum electric susceptibility position, ideal for negative capacitance stabilization[40,48]. **(d)** MOS accumulation *C-V* of HfO_2-ZrO_2-HfO_2 trilayer compared to AFE ZrO_2, FE Zr:HfO_2, and DE HfO_2, all of the same thickness (20 Å), indicating mixed-ferroic behavior is optimal for enhancing capacitance rather than purely FE or AFE behavior. **(e)** Accumulation *C-V* of the HfO_2-ZrO_2-HfO_2 trilayer compared to bilayer and solid solutions films of the same thickness (ALD cycles) and composition (Hf:Zr cycles). Inset: Schematic of multilayer (Hf and Zr cations vertically separated) versus solid solution (Hf and Zr cations inter-

mixed). These results suggest the capacitance enhancement in multilayer films is not simply driven by Hf:Zr composition[23,35], but instead the atomic-scale stacking (Extended Data Fig. 4, 5). **(f)** Accumulation *C*-*V* curves for a 2 nm HfO_2-ZrO_2-HfO_2 trilayer grown on sub-nm SiO_2 fit to effective oxide thickness (EOT) simulations (Methods). Inset: Externally verified MOS accumulation *C*-*V* of the same trilayer stack (Methods), demonstrating 6.5 Å EOT. The 2 nm trilayer on top of SiO_2 demonstrates lower EOT than the thickness of SiO_2 interlayer alone, carefully extracted via physical (8.5 Å) and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence of capacitance enhancement. Furthermore, these 2 nm ferroic gate stacks demonstrate amplified charge from pulsed *I*-*V* measurements relative to the SiO_2 interlayer (Extended Data Fig. 10). Notably, this 2 nm HfO_2-ZrO_2 multilayer on sub-nm SiO_2 provides the most scaled demonstration of charge and capacitance enhancement at the capacitor-level (Extended Data Fig. 10).

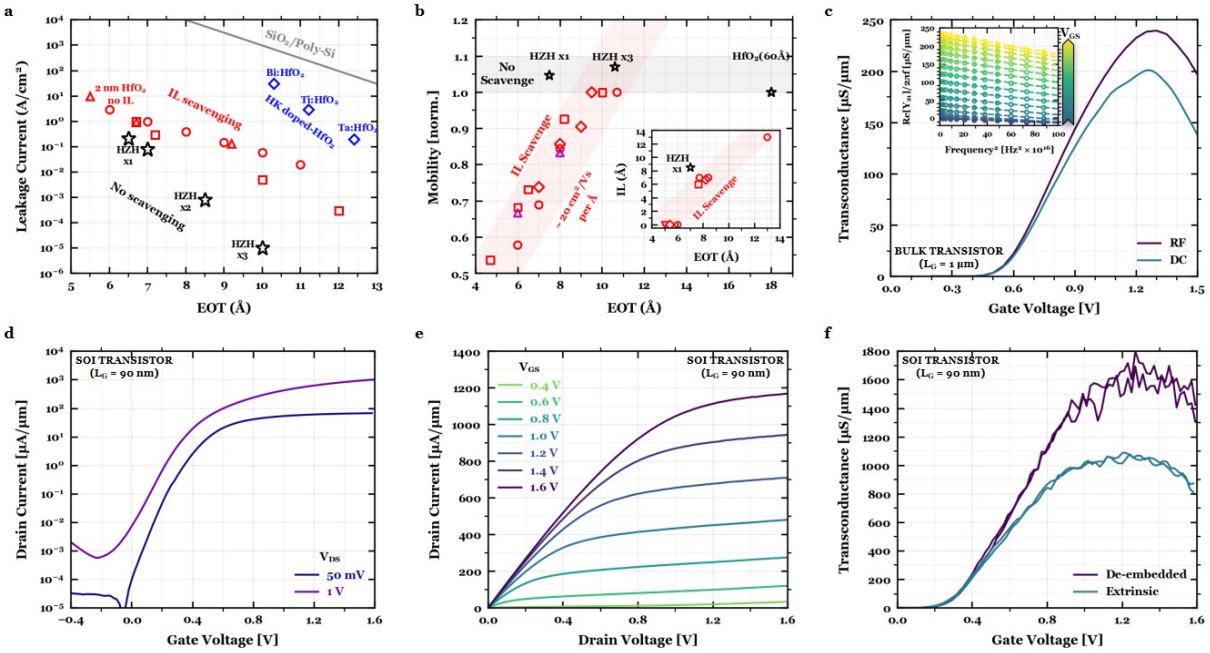

Fig. 3. Device performance benefits utilizing ultrathin mixed-ferroic HfO_2-ZrO_2 gate stacks. **(a)** Leakage-effective oxide thickness (J_G-EOT) scaling of the multilayer gate stacks (black) benchmarked against reported HKMG literature[3], including interlayer-scavenged 2 nm HfO_2 (red), high-κ doped HfO_2 (blue), and SiO_2/poly-Si (gray). The leakage is the lowest reported for a 6.5-7.0 Å EOT MOS capacitor on silicon[3], due to the EOT reduction without requiring interlayer SiO_2 thickness reduction. **(b)** Normalized mobility versus EOT scaling of the multilayer gate stacks (black) benchmarked against reported HKMG literature[3], including interlayer-scavenged 2 nm HfO_2 (red) and hybrid silicate-scavenged interlayer (magenta). For EOT scaling in conventional HKMG systems, the SiO_2 interlayer has to be reduced to lower EOT, which leads to degraded mobility[3]. In this case, enhanced capacitance in HfO_2-ZrO_2 multilayers achieves scaled EOT without having to thin the SiO_2 interlayer; therefore, mobility is not degraded. Inset: SiO_2 interlayer thickness versus EOT scaling comparing the 7.0 Å EOT HfO_2-ZrO_2-HfO_2 trilayer against notable HKMG literature which employ interlayer scavenging to reduce EOT[3]. This scatter plot highlights the underlying reason for the enhanced leakage-EOT and mobility-EOT behavior in the ultrathin trilayer gate stacks: low EOT without reduced SiO_2 interlayer thickness. **(c)** Transconductance (g_m) versus

gate voltage (V_G) for long-channel bulk transistors (L_G = 1 μm) obtained from both DC (derivative of I_D-V_G) and RF (Re[Y_{21}]) measurements (Methods) at V_{DS} = 1 V. Inset: De-embedded $Re[Y_{21}]$ (open circles) as a function of squared frequency at different DC V_{GS} bias points extrapolated to the zero frequency limit (dotted lines) to extract the RF g_m (Extended Data Fig. 8). The high-frequency measurements help suppress defect contributions which would otherwise dampen the intrinsic g_m. **(d, e, f)** DC *I-V* transfer characteristics (I_D-V_G, d), DC output characteristics (I_D-V_D, e), and DC transconductance (g_m-V_G, f) for short-channel (L_G = 90 nm) SOI transistors. Notably, the maximum on-current and g_m at V_{DS} = 1 V exceeds 1 mA/μm and 1 mS/μm. DC mobility and transconductance values are carefully extracted after de-embedding the series resistance from double-swept *I-V* measurements (Extended Data Fig. 7 and 9, respectively).

Methods

Gate stack

Gate oxide Thin films of HfO_2-ZrO_2 were grown by atomic layer deposition (ALD) in a Fiji Ultratech/Cambridge Nanotech tool (U.C. Berkeley) at 270°C in which tetrakis (ethylmethylamino) hafnium and tetrakis (ethylmethylamino) zirconium precursors are heated to 75°C and water vapor is used as the oxidant. For metal-ferroelectric-insulator-semiconductor (MFIS) capacitor structures, sub-nm chemically-grown SiO_2 on lightly-doped Si (10^{15} cm^{-3}) was prepared by the standard clean (SC-1) solution (5:1:1 H_2O:H_2O_2:NH_4OH at 80°C for 10 minutes) after the Si wafer was cleaned in Piranha (120°C for 10 minutes) to remove organics and HF (50:1 H_2O:HF at room temperature for 30 s) to remove any native oxide. Subsequently, HfO_2-ZrO_2 multilayers are deposited at 270°C by ALD. After ALD deposition, post-deposition annealing (PDA) was performed at 175°C (20 min, forming gas N_2/H_2 background) to help cure the SiO_2-oxide interface. For confirmation and reproducibility, HfO_2-ZrO_2 multilayers of the same ALD cycling were also deposited at MIT Lincoln Laboratory (MIT LL); after ALD deposition, PDA was performed at 250°C (1 min, N_2 background).

Gate metal For UC Berkeley capacitors, the first layer of the gate metal, TiN, is deposited by ALD (250°C, 20 cycles, 15 Å) in N_2 and H_2 plasma. Subsequently, W is deposited by sputtering (room temperature, 60 nm). For MIT LL capacitors, the gate metal, TiN, is deposited by PVD (room temperature).

Annealing The entire gate stack undergoes a low-temperature post-metal anneal (200 C, 1 min, N_2) to cure interface defects. This low temperature does not interfere with the HfO_2-ZrO_2 multilayer structure, as confirmed by various characterization techniques (Extended Data Fig. 1), and maintains the mixed ferroic behavior, as high-temperature annealing would induce purely ferroelectric behavior (Extended Data Fig. 5). X-ray diffraction and TEM confirm the

presence of crystalline ultrathin films despite the low deposition temperature, afforded by the low crystallization temperature of ZrO_2 [51]. In fact, non-post-annealed ALD-grown ZrO_2 has previously demonstrated crystallization into the ferroelectric orthorhombic phase on Si [52].

Device fabrication

MOS and MIM capacitors, Bare Structures For MOS capacitor structures, after gate stack deposition, top electrodes are defined by photolithography and dry etching. For bare structures (structural studies), the top metal is removed by chemical etching to expose the gate oxide surface. For metal-insulator-metal (MIM) capacitors, W is deposited by sputtering (room temperature, 30 nm) on a lightly-doped Si substrate as the bottom metal electrode. After ferroic film deposition by ALD, 60 nm of W is deposited by sputtering. The top electrodes are then again defined by photolithography and dry etching.

Bulk transistors The n-type bulk transistors were fabricated by a non-self-aligned gate-last process on bulk silicon wafers (10^{17} cm^{-3}) with local oxidation of silicon (LOCOS) as device isolation technique. First, a 10 nm of SiO_2 thermal oxide and a 30 nm of low-pressure chemical vapor deposition (LPCVD) Si_3N_4 were grown on the Si substrates. After the active region was defined by photolithography and Si_3N_4/SiO_2 etching, dry oxidation was performed to form the LOCOS isolation. Next, the source/drain regions were defined by photolithography and ion implantation with an ion dose of 3×10^{15} ions/cm^2. The dopants were then activated by a rapid thermal anneal (RTA) at 900°C for 7 min in N_2 ambient. The gate stacks with the sub-nm chemically-grown SiO_2, 2 nm HfO_2-ZrO_2 heterostructure, and 100 nm of sputtered W gate were then deposited. After the gate fingers (from 500 nm to 50 μm) were patterned by photolithography and etched by inductively-coupled plasma (ICP) metal etching, the 400 nm thick interlayer dielectric (ILD) SiO_2 was deposited using plasma-enhanced CVD (PECVD). Last, after the contact hole opening, the Ti/TiN contact metal was deposited by sputtering, defined by photolithography, and then etched by ICP metal etching.

Short-channel SOI Transistors The n-type short-channel transistors were fabricated by a non-self-aligned gate-last process on SOI substrates with a gate length (L_G) down to 90 nm. First, the device layer was thinned down to 20 nm and the active regions were defined by photolithography with expose regions etched slightly into the buried oxide. The hydrogen silsequioxane (HSQ) negative resist were written by e-beam lithography as a hard mask for the ion implantation with a dose of 5×10^{15} ions/cm^2. The dopant activation was conducted in an RTA at 900°C for 15 seconds in N_2 ambient. The gate stacks with the sub-nm chemically-grown SiO_2, 2 nm HfO_2-ZrO_2 heterostructure, 1.5 nm of PEALD TiN, and 100 nm of sputtered W were sequentially deposited. The gate region (250 nm) was then patterned by photolithography. Like the back-end process for the bulk transistors, a 400 nm of ILD and a sputtered Ti/TiN contact metal were deposited and defined by photolithography and ICP etching.

Microscopy

Transmission electron microscopy Electron microscopy was performed at the National Center for Electron Microscopy (NCEM) facility of the Molecular Foundry at Lawrence Berkeley National Laboratory (LBNL). The high-resolution bright field TEM images of HfO_2-ZrO_2 thin films were performed by FEI ThemIS 60-300 microscope with image aberration corrector operated at 300 kV (Fig. 1d, Extended Data Fig. 2e,f). To prepare cross-sectional TEM samples of HfO_2-ZrO_2 thin films, mechanical polishing was employed by using an Allied High Tech Multiprep at a 0.5° wedge to thin down the total thickness of samples down to 10 μm. Later, Ar ion milling of the Gatan Precision Ion Milling System was utilized to make an electron-transparent sample, starting from 4 keV down to 200 eV as final cleaning energy. For high-resolution imaging, in order to capture the crystallinity of the HfO_2-ZrO_2 layers, the zone axis alignment required varying degrees of mistilt with respect to the Si lattice, explaining the slightly obscured Si atomic columns (Fig. 1d, Extended Data Fig. 2e,f).

The local interplanar d-spacing in the ultrathin HfO_2-ZrO_2 films (Extended Data Fig. 2e,f) was measured by DigitalMicrograph software using its line profile plus integration width analy-

sis. For the 2 nm HfO_2-ZrO_2-HfO_2 multilayer film, the extracted interplanar lattice spacings were averaged over multiple lattice periodicities and confirmed across various local regions of the film (Extended Data Fig. 2e,f). The SiO_2 interlayer thickness from low-magnification wide field-of-view (FoV) imaging was determined by the same method (Extended Data Fig. 6a). In particular, the intensity line scan from the wide FoV image (Extended Data Foig. 6a) is obtained from averaging across the entire FoV specified by the teal-colored box ($\sim$ 150 nm). Next, the inflection points of the intensity peak were used as the criteria to set the boundaries of the SiO_2 interlayer (Extended Data Fig. 6a). This methodology was also utilized to determine the boundaries of the HfO_2-ZrO_2 layers from the EELS spectrum (Extended Data Fig. 1c). Regarding the wide FoV cross-sectional TEM (Extended Data Fig. 6a), both the low atomic weight and lack of crystallinity of the SiO_2 layer contribute to its weak scattering (bright color), which aids in the visual delineation of the layer boundaries and the thickness extraction from the corresponding averaged intensity line scan.

Optical microscopy Second harmonic generation (SHG) measurements (Extended Data Fig. 2d) were performed with a Ti:sapphire femtosecond laser (Tsunami, Spectra Physics, $\lambda \sim 800$ nm, frequency $\sim$ 80 MHz). The linearly polarized femtosecond laser beam was focused through 50X objective lens (NA $\sim$ 0.42) which results in a focal spot size of 2 μm. The generated SHG signal was collected through the same objective lens and separated from the fundamental beam by the harmonic separator. After passing through the optical bandpass filter, the SHG signals were registered to the photon multiplier tube (PMT) without a polarizer. The fundamental beam was mechanically chopped, and the signal collected by the PMT was filtered by a lock-in amplifier to reduce the background noise. For SHG spatial mapping, a two-axis piezo stage was utilized and the coordinate was synchronized with the PMT signal. The SHG intensity was obtained by averaging the mapping signals across a 100 μm $\times$ 100 μm sample area.

X-ray characterization

X-ray reflectivity Synchrotron X-ray reflectivity (XRR) – performed at Sector 33-BM-C beamline of the Advanced Photon Source, Argonne National Laboratory and at Beamline 2-1 of the Stanford Synchrotron Radiation Lightsource, SLAC National Accelerator Laboratory – confirmed the thickness of HfO_2-ZrO_2 heterostructures (Extended Data Fig. 1b). The overall thickness of the HfO_2-ZrO_2 heterostructures is consistent with the growth rate ($\sim$ 1 Å/cycle) of ALD-grown Zr:HfO_2 as demonstrated in our previous work[13]. Furthermore, the presence of irregularly spaced fringes in the thicker HfO_2-ZrO_2 heterostructures suggests the presence of well-separated HfO_2-ZrO_2 layers, i.e. not a solid solution. This is confirmed by XRR fitting (Extended Data Fig. 1b) performed with the python package GenX[53] which considers factors such as density, roughness, and thickness.

Grazing incidence diffraction: in-plane Synchrotron in-plane grazing-incidence diffraction (GID) (Fig. 1e and Extended Data Fig. 2a) was performed at Sector 33-ID-D beamline of the Advanced Photon Source, Argonne National Laboratory. A Pilatus-II 100K Area Detector mounted on the del-arm was used to collect diffraction signal with a grazing incidence geometry. The region-of-interest on the detector was set such that the ring-like signal was fully integrated. In-plane GID was collected by sweeping the in-plane angle ν (8-50°) with a fixed out-of-plane grazing angle δ (δ = 0.9°); the corrected Bragg angle (2θ) over which the data is plotted and indexed is determined from the relationship $\cos 2\theta = \cos\nu \cdot \cos\delta$ set by the geometry of the diffractometer. The X-ray source was fixed at 16 keV (λ = 0.775 Å). In-plane diffraction yields more diffraction peaks with better defined width, likely due to the preferred orientation and disc-shape domains in the film. Therefore, in-plane GID enables clear indexing to the ferroelectric orthorhombic ($Pca2_1$) and antiferroelectric tetragonal ($P4_2/nmc$) fluorite structure in the ultrathin HfO_2-ZrO_2 films, as the presence of many reflections from the in-plane GID spectra (Fig. 1e, Extended Data Fig. 2a) allow for clear distinction from other nonpolar fluorite-structure polymorphs. Such diffraction spectra would be otherwise prohibited in typical out-of-plane geometry due to the lack of vertical diffraction planes and the large linewidth inherent to ultrathin films.

Two-dimensional diffraction Two-dimensional reciprocal space maps (Extended Data Fig. 2b) were measured at Beamline 11-3 of the Stanford Synchrotron Radiation Lightsource, SLAC National Accelerator Laboratory. Rayonix MX225 CCD area detector collected diffraction flux in gazing incidence (< 0.20°) geometry; the X-ray source (50 microns vertical x 150 microns horizontal beam size) was fixed at 12.7 keV. The sample-detector work distance was set to 80 mm to enable detection of a wide region of reciprocal space (Q-range 0.2 to 5 Å^{-1}) at the expense of reciprocal space resolution, set by the pixel size. The two-dimensional diffraction scans – in which a wide portion of the entire reciprocal space was collected simultaneously, rather than at discrete regions in Q_x-Q_y space – were averaged over data collection time and for repeated scans. These measurement features, in tandem with the high X-ray flux afforded by the synchrotron source, enabled sufficient diffraction signal detection and contrast in films just two nanometers in thickness. Data analysis was performed Nika, an Igor Pro package for correction, calibration and reduction of two-dimensional areal maps into one-dimensional data[54]. Two-dimensional reciprocal space maps on bare HfO_2-ZrO_2 heterostructures confirm the presence of crystalline ultrathin films despite the low deposition temperature, afforded by the low crystallization temperature of ZrO_2 on Si[51].

Ferroic phase identification from diffraction For fluorite-structure thin films, the main phases to consider are the dielectric monoclinic ($P2_1/c$), antiferroelectric tetragonal ($P4_2/nmc$), and ferroelectric orthorhombic ($Pca2_1$) phases. Various diffraction reflections from the wide-angle IP-GiD spectra enable indexing to the orthorhombic $Pca2_1$ phase. Lattice parameters (a, b, c) – determined via Bragg's law from the d_{200} family of reflections – are self-consistently checked against the (111) lattice spacing $\frac{1}{d_{111}^2} = \frac{1}{a^2} + \frac{1}{b^2} + \frac{1}{c^2}$ as well as other higher-order reflections present in the in-plane diffraction spectra (Extended Data Fig. 2a). For example, the lattice parameters extracted from the {200} peaks were a = 5.36 Å, b = 5.23 Å, and c = 5.47 Å. This corresponds to a d_{211} lattice spacing of 2.209 Å, which agrees well with the lattice spacing (2.205 Å) obtained from Bragg's law based on the peak position (Extended Data Fig. 2a)

The monoclinic phase was ruled out due to a lack of two {111} peaks in the diffraction spectra and the $(111)_o$ and $(101)_t$ reflections being significantly offset from its expected peak position

in the monoclinic phase. With regards to the indexing of tetragonal $(101)-t$ peak (Extended Data Fig. 2a), it is always reported that the tetragonal $(101)_t$ reflection has a smaller d-spacing[55] in thicker HfO_2-based films[28], and is therefore expected to be present at a higher angle compared to the orthorhombic $(111)_0$ reflection, which is the case in the indexed diffraction spectra (Extended Data Fig. 2a) based on the self-consistent indexing methodology outlined above provides.

In terms of extracting the phase fraction of the tetragonal and orthorhombic phases, while Rietveld refinement has been applied to grazing incidence x-ray diffraction of thick (10 nm) Zr:HfO_2[56] to determine the orthorhombic phase fraction, that methodology cannot be applied in the ultrathin regime, as the films are highly oriented, as opposed to fully polycrystalline (Extended Data Fig. 2b), which is a requirement to apply Rietveld refinement.

X-ray absorption spectroscopy Hard and soft synchrotron X-ray spectroscopy (Extended Data Fig. 2c) was measured at beamline 4-ID-D of the Advanced Photon Source, Argonne National Laboratory and Beamline 4.0.2. of the Advanced Light Source, Lawrence Berkeley National Laboratory, respectively. Spectroscopy measurements were taken at the oxygen K-edge (520-550 eV), zirconium $M_{3,2}$-edge (325-355 eV), hafnium M_3-edge (2090-2150 eV), and zirconium $L_{3,2}$-edge (2200-2350 eV). X-rays were incident at 20° off grazing. XAS (XLD) was obtained from the average (difference) of horizontal and vertical linearly polarized X-rays. To eliminate systematic artifacts in the signal that drift with time, spectra measured at ALS were captured with the order of polarization rotation reversed (e.g., horizontal, vertical, vertical, and horizontal) in successive scans, in which an elliptically polarizing undulator tuned the polarization and photon energy of the synchrotron X-ray source[57]. Spectra measured at ALS were recorded under total electron yield (TEY) mode[57] from room temperature down to 100 K. Spectra measured at APS were recorded under various modes: total electron yield (TEY), fluorescence yield (FY), and reflectivity (REF).

Ferroic phase identification from spectroscopy X-ray spectroscopy provides various signatures to distinguish the competing ferroelectric orthorhombic ($Pca2_1$) and antiferroelectric tetrag-

onal ($P4_2/nmc$) phase. Simulated XAS spectra at the oxygen K-edge (Extended Data Fig. 3d) for ZrO_2 in the various fluorite-structure polymorphs (orthorhombic $Pca2_1$ and tetragonal $P4_2/nmc$) were computed through the Materials Project[58] open-source database for XAS spectrum[59]. The T-phase ($P4_2/nmc$) nonpolar distortion (D_{4h}, 4-fold prismatic symmetry) from regular tetrahedral (T_d, full tetrahedral symmetry) fluorite-structure symmetry does not split the degenerate e-bands ($d_{x^2-y^2}$, $d_{3z^2-r^2}$), as confirmed by experiment[60] and the aforementioned XAS simulations[13]. Meanwhile, the O-phase ($Pca2_1$) polar rhombic pyramidal distortion (C_{2v}, 2-fold pyramidal symmetry) does split the e-manifold based on crystal field symmetry, providing a spectroscopic means to distinguish the T- and O-phases. The additional spectroscopic feature present between the main e- and t_2- absorption features due to orthorhombic symmetry-lowering distortion is illustrated by its crystal field diagram (Extended Data Fig. 3b). This provides a spectroscopic fingerprint for phase identification beyond diffraction which can often be ambiguous due to the nearly identical T- and O-phase lattice parameters. For the 2 nm HfO_2-ZrO_2-HfO_2 trilayer, the experimental O K-edge XAS spectra demonstrates tetrahedral and rhombic splitting features closely matching the polar O-phase ($Pca2_1$) emerge slightly below room temperature, indicative of the mixed tetragonal-orthorhombic to orthorhombic phase transition upon cooling. This temperature-dependent tetragonal-orthorhombic structural evolution is expected for fluorite-structure thin films[61] and is consistent with temperature-dependent capacitance measurements (Extended Data Fig. 3f). Further XAS phase identification details are provided in previous work on ultrathin Zr:HfO_2 films[13].

X-ray photoelectron spectroscopy Angle-resolved photoelectron spectroscopy (ARPES) was performed using a Phi Versaprobe III at the Stanford Nano Shared Facilities (Extended Data Fig. 1d). A monochromated aluminum source was used to give a photon energy of 1486.6 eV. Data was fit and analyzed using CasaXPS. Angle-dependent XPS at various incident grazing angles enabled depth-resolved composition analysis to help confirm the HfO_2-ZrO_2 multilayer structure.

Dielectric measurements

Metal-oxide-semiconductor (MOS) capacitance Capacitance-voltage (*C-V*) measurements were performed using a commercial Semiconductor Device Analyzer (Agilent B1500) with a multi-frequency capacitance measuring unit (MFCMU). 19 micron W tips (d.c.P-HTR 154-001, FormFactor) made electrical contact within a commercial probe station (Cascade Microtech); voltage was applied to the W top electrode and the lightly-doped Si bottom electrode was grounded. To eliminate contributions from series and parasitic resistances, frequency-dependent *C-V* measurements were performed. In particular, *C-V* data was analyzed at two frequencies (100-500 kHz regime) to allow for the extraction of accurate frequency-independent *C-V* via a three-element circuit model consisting of the capacitor and the parasitic series and parallel resistors[62]. The frequency-independent capacitance is given by

$$C = \frac{f_1^2 C_1(1+D_1^2) - f_2^2 C_2(1+D_2^2)}{f_1^2 - f_2^2} \tag{1}$$

where C_i and D_i refer to the measured capacitance in parallel mode (C_p-R_p) and dissipation values at frequency f_i. The dissipation factor is given by $D = -\cot\theta$, where θ is the phase. In order to maximize the accuracy of this method, it is important the the dissipation factors are small ($\ll 1$) at the frequencies chosen; therefore, high frequencies were selected.

Permittivity extraction The permittivity of Al_2O_3 and HfO_2 dielectric layers was extracted from thickness-dependent MOS *C-V* measurements on lightly-doped p substrates (Extended Data Fig. 6). In the accumulation region of the MOS *C-V* measurements, the MOS capacitor can be modeled as three capacitors (Al_2O_3 or HfO_2 dielectric layer, SiO_2 interlayer, and Si space charge layer) in series using the following equation,

$$\frac{1}{C} = \frac{1}{\epsilon_0 \epsilon_{H\kappa}} t_{H\kappa} + \frac{1}{\epsilon_0 \epsilon_{SiO_2}} \left[t_{SiO_2}^{phys} + t_{\mathrm{CL}} \frac{\epsilon_{SiO_2}}{\epsilon_{Si}} \right], \tag{2}$$

where $t_{H\kappa}$ is the thickness of the high-κ (Al_2O_3 or HfO_2) layer, $t_{SiO_2}^{phys}$ is the physical SiO_2 thickness, and t_{CL} is the charge layer thickness in silicon. The physical SiO_2 thickness is constant across all of the thickness series (Al_2O_3 and HfO_2 single layers). Additionally, the capacitance values were extracted at various values of fixed charge (Q = 0 to -3 μC/cm^2) which ensures that the charge-layer thickness is constant across all thicknesses and in the accumulation region. Therefore, from

Equation 2, the inverse capacitance at a fixed charge as a function of film thickness should result in a line and the permittivity can be extracted from the slope. This yielded extracted permittivities of 9 and 19 for the Al_2O_3 and HfO_2 thickness series, respectively, as expected for these systems. Note that for the HfO_2 thickness series, thicknesses of 6 nm and higher were used to ensure HfO_2 stabilizes in the dielectric monoclinic phase ($\kappa \sim 18$)[36].

Similarly, the permittivity of the HfO_2-ZrO_2 heterostructures was extracted from thickness-dependent MIM *C-V* measurements (Fig. 2b). The inverse capacitance is a linear function of the film thickness, and the permittivity can be extracted from the slope.

Electrical interlayer thickness extraction The thickness of the SiO_2 interlayer was determined not only by TEM (Extended Data Fig. 6a), but also electrically via *C-V* measurements of both dielectric HfO_2 and Al_2O_3 thickness series on SiO_2-buffered Si (Extended Data Fig. 6f). From Equation 2, the inverse capacitance at a fixed charge as a function of dielectric thickness should result in a line and the capacitance-equivalent thickness (CET) of the SiO_2 interlayer and Si charge layer can be extracted from the y-intercept. By extracting the CET at different charge values, the *Q-V* relation of the SiO_2 interlayer and Si charge layer can be calculated through the following equation

$$V - V_{fb} = \int_0^Q \frac{t_{SiO_2}^{phys} + t_{\mathrm{CL}} \frac{\epsilon_{SiO_2}}{\epsilon_{Si}}}{\epsilon_0 \epsilon_{SiO_2}} \, dQ, \tag{3}$$

where V_{fb} is the flatband voltage (Extended Data Fig. 6b,d). To confirm this methodology, another method for determining the *Q-V* relation of the SiO_2 interlayer and Si charge layer was extracted from the *Q-V* relations of both the dielectric HfO_2 and Al_2O_3 thickness series. At a fixed charge, the corresponding voltage values of each thickness were fit to a line and the y-intercept corresponds to the voltage value for the SiO_2 interlayer and Si charge layer *Q-V* relation (Extended Data Fig. 6c,e). As expected, both methods lead to the same extracted *Q-V* relation (Extended Data Fig. 6c,e), corresponding to 8 Å EOT (Extended Data Fig. 6f) – close to the SiO_2 physical thickness of 8.5 Å obtained via TEM (Extended Data Fig. 6a) – based on simulated TCAD *Q-V* relations of different SiO_2 thicknesses on lightly-doped Si.

Hysteretic *C-V* measurements Capacitance-voltage (*C-V*) measurements on MIM capacitors were performed using a commercial Semiconductor Device Analyzer (Agilent B1500) with a multi-frequency capacitance measuring unit. 19 micron W tips (d.c.P-HTR 154-001, FormFactor) made electrical contact within a commercial probe station (Cascade Microtech); voltage was applied to the W top electrode and the W bottom electrode was grounded.

Electrical characterization

Bechmarking to HKMG literature In Figure 3a, the leakage-effective oxide thickness (J_G-EOT) scaling of negative capacitance multilayer gate stack benchmarked against reported HKMG literature includes references taken from interlayer-scavenged 2 nm HfO_2 [16,18,63] (red), high-κ doped HfO_2 [18] (blue), and SiO_2/poly-Si [3] (gray). In Figure 3b, the normalized mobility versus EOT scaling of the negative capacitance multilayer gate stack benchmarked against reported HKMG literature includes references taken from interlayer-scavenged 2 nm HfO_2 [16,18,64] (red) and hybrid silicate-scavenged interlayer [16] (magenta). In the Figure 3b inset, the SiO_2 interlayer thickness versus EOT scaling scatter plot considers the 7.0 Å EOT HfO_2-ZrO_2-HfO_2 trilayer to HKMG references which employ interlayer scavenging to reduce EOT [16,18,63,65].

Transistor transfer and output characteristics Transistor I_d-V_g and I_d-V_d characterization of short-channel and long-channel transistors were performed using a commercial Semiconductor Device Analyzer (Agilent B1500). 19 micron W tips (d.c.P-HTR 154-001, FormFactor) made electrical contact within a commercial probe station (Cascade Microtech); voltage was applied to the gate and drain contacts, while the source and Si substrate were grounded.

Mobility extraction The low-field transistor mobility is calculated based on the channel resistance (R_{ch}) and inversion sheet charge density (Q_{inv}), which are extracted respectively from transfer characteristics ($I_D - V_{GS}$) and from the gate-to-channel capacitance-voltage ($C_{gc} - V_{GS}$) measurements. Given the the device aspect ratio of channel length (L) and channel width (W), we

have

$$R_{ch}(V_{GS}) = \frac{L}{W} \times \frac{1}{\mu_{eff}(V_{GS})Q_{inv}(V_{GS})} \tag{4}$$

Firstly, the channel resistance is extracted at 50 mV drain-to-source bias (V_{DS}) by subtracting the parasitic resistance (R_p) from the measured drain-to-source resistance (R_{DS}).

$$R_{DS}(V_{GS}) = \frac{V_{DS}}{I_D(V_{GS})} = R_{ch}(V_{GS}) + R_p \tag{5}$$

where R_p is ascribed to the resistance of the source and the drain contacts and the n+ extension regions that are extrinsic to the channel region. When the overdrive voltage ($V_{ov} = V_{GS} - V_t$, where V_t is the threshold voltage) is sufficiently large, R_{ch} is known to be inversely proportional to V_{ov} according to 4. Therefore, R_p can be extracted using a linear extrapolation of the $R_{DS} - 1/V_{ov}$ relationship (Extended Data Fig. 7e), which is derived from the $I_D - V_{GS}$ from which the threshold voltage (V_t) can be characterized with the max-g_m method. Secondly, the $C_{gc} - V_{GS}$ of a large (W=L=50μm) device (Extended Data Fig. 7a) is integrated and normalized to the channel area (A=2500μm^2) to estimate the inversion charge.

$$Q_{inv}(V_{GS}) \approx \int_{-\infty}^{V_{GS}} \frac{C_{gc}(v_{gs})}{A} dv_{gs} \tag{6}$$

The large device dimensions minimizes the parasitic capacitance contribution to ensure C_{gc} is representative of the inversion electron responses. Finally, we combine the above characterizations to obtain the effective mobility using Equation 4 (Extended Data Fig. 7f).

Transconductance extraction The measured transconductance ($g_m = \partial I_D / \partial V_{GS}$) and the output conductance ($g_{ds} = \partial I_D / \partial V_{DS}$) are affected by the series resistance on the source (R_S) and the drain sides (R_D), as they reduce the voltage drops on the channel region,

$$V_{GSi} = V_{GS} - I_D R_S \tag{7}$$

$$V_{DSi} = V_{DS} - I_D(R_S + R_D) \tag{8}$$

where V_{GSi} and V_{DSi} are the gate-to-source and the drain-to-source voltages intrinsic to the channel, respectively. $R_S \approx R_D \approx R_p/2$ because the transistor is symmetric.

R_p can be extracted from the $R_{DS} - 1/V_{ov}$ relationships as discussed in the "Mobility Extraction" Methods section (Extended Data Fig. 9b). Besides, devices with different gate length (L_g) series are fabricated on the Silicon-On-Insulator (SOI) wafer, which enables another extraction method with $R_{SD} - L_g$ relations. At low V_D and a given V_{ov}, Q_{inv} and μ_{eff} are unchanged across different L_g if short-channel effect is not significant, making R_{ch} proportional to the channel length. Such condition is confirmed by the consistency of V_t across measured L_g (Extended Data Fig. 9a). Therefore, the L_g offset as well as the R_p can be found at the intersect of the linear relations of the $R_{SD} - L_g$ with different V_{ov} (Extended Data Fig. 9c). The two R_p extraction methods yield consistent results.

The following equation is solved to extract the intrinsic $g_{mi} = \partial I_D/\partial V_{GSi}$ and $g_{dsi} = \partial I_D/\partial V_{DSi}$ without the degradation due to R_S and R_D.

$$\begin{pmatrix} 1 - g_m R_S & -g_m(R_S + R_D) \\ -g_{ds} R_S & 1 - g_{ds}(R_S + R_D) \end{pmatrix} \begin{pmatrix} g_{mi} \\ g_{dsi} \end{pmatrix} = \begin{pmatrix} g_m \\ g_{ds} \end{pmatrix} \tag{9}$$

where g_m and g_{ds} are measured, and $R_S \approx R_D \approx R_p/2$ from the above discussed characterizations. Using this methodology, the intrinsic g_{mi} and intrinsic g_{dsi} are extracted (Fig. 3f, Extended Data Fig. 9d,e).

RF measurements Scattering-parameters (S parameters) for L_G = 1 μm bulk transistors (henceforth referred to as the device under test, DUT) at various DC biases as well as open and short structures (Extended Data Fig. 8a) are measured using a Keysight E8361C Network Analyzer in conjunction with a Keysight 4155C Semiconductor Parameter Analyzer. The devices were measured using low contact resistance Infinity Series probes. To calibrate the measurement setup, a line-reflect-reflect-match (LRRM) calibration was performed with a Cascade Microtech Impedance Standard. Following calibration, S-parameters were measured for each of the DUT, open, and short structures. These measured S-parameters were converted to admittance parameters (Y-parameters), Y_{DUT}, Y_{open}, and Y_{short}. In order to remove the effects of parasitic shunt parasitic pad capacitance and series pad resistance and inductance of the DUT, the following de-embedding process was followed. First, to decouple the effect of shunt parasitic capacitances, the

Y parameters of the open structure (Y_{open}) are subtracted from the Y parameters of the DUT and short structure, and then are converted to impedance parameters (Z parameters):

$$Z_1 = (Y_{DUT} - Y_{open})^{-1} \tag{10}$$

$$Z_2 = (Y_{short} - Y_{open})^{-1} \tag{11}$$

Next, to decouple the effect of series pad resistance and inductance of DUT, Z_2 is subtracted from Z_1 and the resulting difference is converted back to admittance parameters, Y_{corr}:

$$Y_{corr} = (Z_1 - Z_2)^{-1} \tag{12}$$

Y_{corr} represents the de-embedded admittance parameters of the DUT. This de-embedding procedure is schematically represented in Extended Data Fig. 8a.

To extract the total gate capacitance (C_{gg}) and transconductance (g_m) from the de-embedded admittance parameters, a small-signal model of the transistor was assumed (Extended Data Fig. 8b). Under this small-signal model, the Y-parameters can be written in terms model parameters and frequency (assuming $R_s = R_d = 0$, $C_{gg} = C_{gs} + C_{gd}$, and $4\pi^2 C_{gg}^2 R_g^2 f^2 \ll 1$)

$$Y_{11} = 4\pi^2 C_{gg}^2 R_g f^2 + 2\pi f C_{gg} j \tag{13}$$

$$Y_{12} = -4\pi^2 C_{gd} C_{gg} R_g f^2 - 2\pi f C_{gd} j \tag{14}$$

$$Y_{21} = g_m - 4\pi^2 C_{gd} C_{gg} R_g f^2 + 2\pi f (C_{gd} + g_m R_g C_{gg}) j \tag{15}$$

$$Y_{22} = g_{ds} + 4\pi^2 C_{gd} R_g (C_{gd} + C_{gg} g_m R_g) f^2 + 2\pi f (C_{ds} + C_{gd} + C_{gd} g_m R_g) j. \tag{16}$$

The transconductance (g_m) can therefore be extracted at a fixed DC bias via the following relation (Fig. 3c, Extended Data Fig. 9c).

$$g_m = \mathrm{Re}(Y_{21})\Big|_{f^2=0} \tag{17}$$

Charge boost measurements Pulsed charge-voltage measurements (Extended Data Fig. 10) were conducted on p- Si/SiO_2/HfO_2-ZrO_2 (2 nm)/TiN/W capacitor structures to extract the energy landscape of the ferroic HfO_2-ZrO_2 heterostructure, following the measurement scheme

detailed in previous works[47,66–68]. The capacitor structures were connected to an Agilent 81150A Pulse Function Arbitrary Noise Generator and the current and voltage was measured through an InfiniiVision DSOX3024A oscilloscope with a 50 Ω and 1 MΩ input impedance, respectively. Short voltage pulses (500 ns) with increasing amplitudes were applied to the capacitor (Extended Data Fig. 10c). From the integration of the measured discharging current, a charge vs voltage relationship was extracted (Extended Data Fig. 10d). The voltage was calculated by $\max(V - IR)$, where V is the applied voltage pulse, I is the measured current, and R is a combination of the oscilloscope resistance (50 Ω) and parasitic resistances associated with the setup and lightly-doped substrate (220 Ω). Fast voltage pulses were applied in order to minimize charge injection into the ferroelectric-dielectric interface, which could mask the observation of the negative capacitance regime[47,67]. Additionally, short voltage pulses help prevent electrical breakdown of the SiO_2 layer. In order to determine the *P*-E_F relation of the 2 nm HfO_2-ZrO_2 heterostructure, the electric field across the ferroic HfO_2-ZrO_2 heterostructure was calculated by subtracting the voltage across the series capacitance of the SiO_2 interlayer and Si charge layer (V_D) at a fixed charge value,

$$E = \frac{1}{t}\left(V - V_D\right), \tag{18}$$

where t is the thickness of the HfO_2-ZrO_2 heterostructure. The *Q*-*V* relation of the series capacitance of the SiO_2 interlayer and Si charge layer was determined via thickness-dependent *C*-*V* measurements of Al_2O_3 and HfO_2 (Extended Data Fig. 6, Methods, Electrical interlayer thickness extraction), which corresponded to 8 Å SiO_2 on lightly-doped Si. The charge boost due to negative capacitance was calculated by integrating the difference between the *Q*-*V* relations of the 2 nm HfO_2-ZrO_2 heterostructure and the series combination of the SiO_2 interlayer and the Si charge layer (Extended Data Fig. 10e).

Modeling

Landau phenomenology of antiferroelectric-ferroelectric system The qualitative energy landscape for a mixed ferroelectric-antiferroelectric material (Fig. 1a) was calculated by assuming a series combination of antiferroelectric and ferroelectric layers connected to a voltage

source V_s. The energy landscape potentials were calculated via the Landau-Ginzburg-Devonshire (LGD) formalism (without strain coupling)[69–71]:

$$U_{FE} = (\alpha_{FE}P^2 + \beta_{FE}P^4 + \gamma_{FE}P^6 - E_{FE}P)t_{FE} \tag{19}$$

$$\begin{aligned} U_{AFE} = (&\alpha_{AFE}(P_a^2 + P_b^2) + \delta_{AFE}P_aP_b + \beta_{AFE}(P_a^4 + P_b^4) \\ &+ \gamma_{AFE}(P_a^6 + P_b^6) - E_{AFE}(P_a + P_b))t_{AFE} \end{aligned} \tag{20}$$

For the antiferroelectric layer, the energy landscape assumes two sublattices (P_a, P_b) with spontaneous, antiparallel dipoles. In order to express the AFE energy landscape in terms of total polarization, a change of variables was performed ($P = P_a + P_b$, $A = P_a - P_b$). The antiferroelectric profile therefore becomes,

$$\begin{aligned} U_{AFE} = t_{AFE}(&\frac{1}{2}\alpha_{AFE,p}P^2 + \frac{1}{2}\alpha_{AFE,n}A^2 + \frac{\beta_{AFE}}{8}(P^4 + 6A^2P^2 + A^4) \\ &+ \frac{\gamma_{AFE}}{32}(P^6 + A^6 + 15P^2A^2(A^2 + P^2)) - E_{AFE}P). \end{aligned} \tag{21}$$

The system is also constrained by electrical boundary conditions at the antiferroelectric/ferroelectric interface ($\epsilon_0 E_{AFE} + P_{AFE} = \epsilon_0 E_{FE} + P_{FE}$) and that the voltage across both layers must sum up to V_g ($V_g = E_{FE}t_{FE} + E_{AFE}t_{AFE}$). With these constraints, the combined energy profile is given by:

$$\begin{aligned} U_{AFE+FE} = t_{AFE}(&\frac{1}{2}\alpha_{AFE,p}P_{AFE}^2 + \frac{1}{2}\alpha_{AFE,n}A_{AFE}^2 + \frac{\beta_{AFE}}{8}(P_{AFE}^4 + 6A_{AFE}^2P_{AFE}^2 + A_{AFE}^4) \\ &+ \frac{\gamma_{AFE}}{32}(P_{AFE}^6 + A_{AFE}^6 + 15P_{AFE}^2A_{AFE}^2(A_{AFE}^2 + P_{AFE}^2))) \\ &+ (\alpha_{FE}P_{FE}^2 + \beta_{FE}P_{FE}^4 + \gamma_{FE}P_{FE}^6)t_{FE} - V_g\frac{P_{FE}t_{FE} + P_{AFE}t_{AFE}}{t_{FE} + t_{AFE}} \\ &+ \frac{t_{AFE}t_{FE}(P_{AFE} - P_{FE})^2}{\epsilon_0(t_{FE} + t_{AFE})} \end{aligned} \tag{22}$$

In order to further simplify this expression, we note that the last term represents the electrostatic energy arising from polarization mismatch at the AFE-FE interface. In general, such mismatch is quite costly, resulting in nearly uniform polarization across all layers. Therefore, we apply the approximation ($P_{AFE} = P_{FE} = P$), which sets the last term to 0. Furthermore, in order to express U as just a function of P, we can generate another constraint by noting that in equilibrium,

$\nabla U_A = 0$, resulting in the constraint,

$$0 = A^2 \left(\frac{\beta_{AFE}}{2} + \frac{\gamma_{AFE}}{32}(6A^2 + 60P^2) \right) = -\alpha_{AFE_n} - \frac{3}{2}\beta_{AFE}P^2 - \frac{15}{16}\gamma_{AFE}P^4 \qquad (23)$$

This constraint allows for the determination of A for any value of P, which allows us to determine U as a function of P (Fig. 1a).

Technology computer-aided design simulations The measured *C-V* curves are calibrated to Sentuarus Technology computer-aided design simulations (TCAD) device simulator which solves the electrostatics, electron and hole transports, and the quantum confinement effect self-consistently[72]. MOS capacitors with $1 \times 10^{15} cm^{-3}$ p-type substrate doping and L = 50 μm planar MOSFET swith $2 \times 10^{17} cm^{-3}$ p-type substrate doping are simulated with finite-element method. The equivalent oxide thickness (EOT) and the metal work function (ϕ_m) are the only two parameters that are fit to the MOS capacitor measurement results, yet the slope of the accumulation capacitance can be successfully captured by the model (Fig. 2f, Extended Data Fig. 6). Similarly, both components (gate-to-channel and gate-to-body) of the MOSFET split *C-V* are captured by the TCAD model with appropriate EOT, ϕ_m, and an Si/SiO_2 interface state density of $2 \times 10^{12} cm^{-2} eV^{-1}$ (Extended Data Fig. 7a).

Atomic-scale HfO_2-ZrO_2 mixed-ferroic heterostructure

Thickness limits and atomic-scale heterostructures Recent perspectives on HfO_2-based ferroelectricity for device applications[9,73–76] posed the technological challenges stemming from thickness limit concerns of HfO_2-based ferroelectricity, and thereby, negative capacitance. The use of short-period superlattices i.e. nanolaminates is common in the high-κ field to enhance permittivity[77–81]; in particular, rutile-structure TiO_2 is often paired with fluorite-structure HfO_2 and/or ZrO_2 in DRAM capacitors[82]. Recently, fluorite-structure nanolaminates were employed to tune the ferroelectric behavior of HfO_2-ZrO_2 films[83–85]. However, all of these works have studied nanolaminates with thick periodicity, going as thin as 10 ALD cycles ($\sim$ 1.1 nm) per superlattice sub-layer[83]. In this work, we scale down to a much thinner thickness limit while still maintaining

physical separation of the individual layers (Extended Data Fig. 1). The reasoning behind using a short-period superlattice structure to scale down the ferroic behavior of HfO_2-ZrO_2 rather than simply thinning down a solid solution stems from the notorious thickness-dependent ferroelectric behavior in Zr:HfO_2 at fixed composition[35, 61,86]. Here, the use of nanolaminated structures can help provide thickness-independent scaling of ferroic order, as has been previously demonstrated to overcome the upper thickness limit of HfO_2-based ferroelectricity[85]. The persistence of high capacitance for these 2 nm films is notable considering other high-κ dielectric systems suffer from significant permittivity degradation in the thin film (sub-10 nm) regime, particularly TiO_2- and $SrTiO_3$-based oxides[82,87]. Sustaining the mixed ferroic order underlying negative capacitance to the 2 nm regime is extremely relevant for advanced technology nodes[88] which budget only $\sim$ 2 nm for the oxide layer.

Iso-structural polycrystalline multilayer Previous attempts to heterostructure ferroelectric Zr:HfO_2 with dielectric Al_2O_3[47, 67,68] failed to demonstrate capacitance enhancement, which was attributed to the fixed charges at the ferroelectric-dielectric interface. These charges can screen the ferroelectric polarization, pushing the stable point of the energy well to one the minimum points, and thereby preventing stabilization of negative capacitance regime via depolarization fields from the dielectric. Here, the use of iso-structural HfO_2-ZrO_2 to serve as both the nonpolar (antiferroelectric) and polar (ferroelectric) layers, and leveraging the high (low) onset crystallization temperature of HfO_2 (ZrO_2) on Si[51], enables interfaces with diminished defects, allowing for the polar layer to experience the depolarization fields and stabilize in the "forbidden" NC regime. Regarding the polycrystalline nature of the ultrathin multilayers, it has been experimentally[39] and theoretically[89] established that negative capacitance can be stabilized in the presence of ferroelectric domains, as recently reviewed[75].

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Author contributions S.S.C. and S.S. designed the research. S.S.C. performed design, synthesis and optimization of the superlattice oxide heterostructure and its ferroic characterization. C.-H.H. and N.S. performed capacitor fabrication. C.-H.H. helped with optimization of annealing treatments. S.S.C and N.S. performed capacitor measurements and analysis. L.-C.W. fabricated the transistors and performed DC characterization. S.-L.H. performed TEM. S.S.C. and S.-L.H. performed TEM analysis. Y.H.L. performed all simulations include EOT estimation, series resistance determination and mobility and transconductance analysis. M.S.J., J.G. and W.L. contributed to RF electrical measurements and analysis. D.W.K. initiated the gate oxide synthesis. D.W.K. and J.B. developed the initial processes for transistor fabrication. M.M., R.R., C.S., D.P., G.P., M.C., B.T. contributed to capacitor fabrication and characterization at MIT LL. Y.R. performed second harmonic generation. S.V. performed X-ray photoelectron spectroscopy. S.S.C. and C.-H.H. performed synchrotron soft X-ray spectroscopy at ALS. S.S.C., V.A.S., J.W.F. performed synchrotron X-ray spectroscopy at APS. S.S.C., C.-H.H., V.A.S., Z.Z. performed synchrotron in-plane diffraction at APS. S.S.C. and N.S. performed synchrotron X-ray reflectivity and 2D diffraction at SSRL. N.S. performed Landau modeling. S.S.C. and S.S. co-wrote the manuscript. S.S. supervised the research. All authors contributed to discussions and manuscript preparations.

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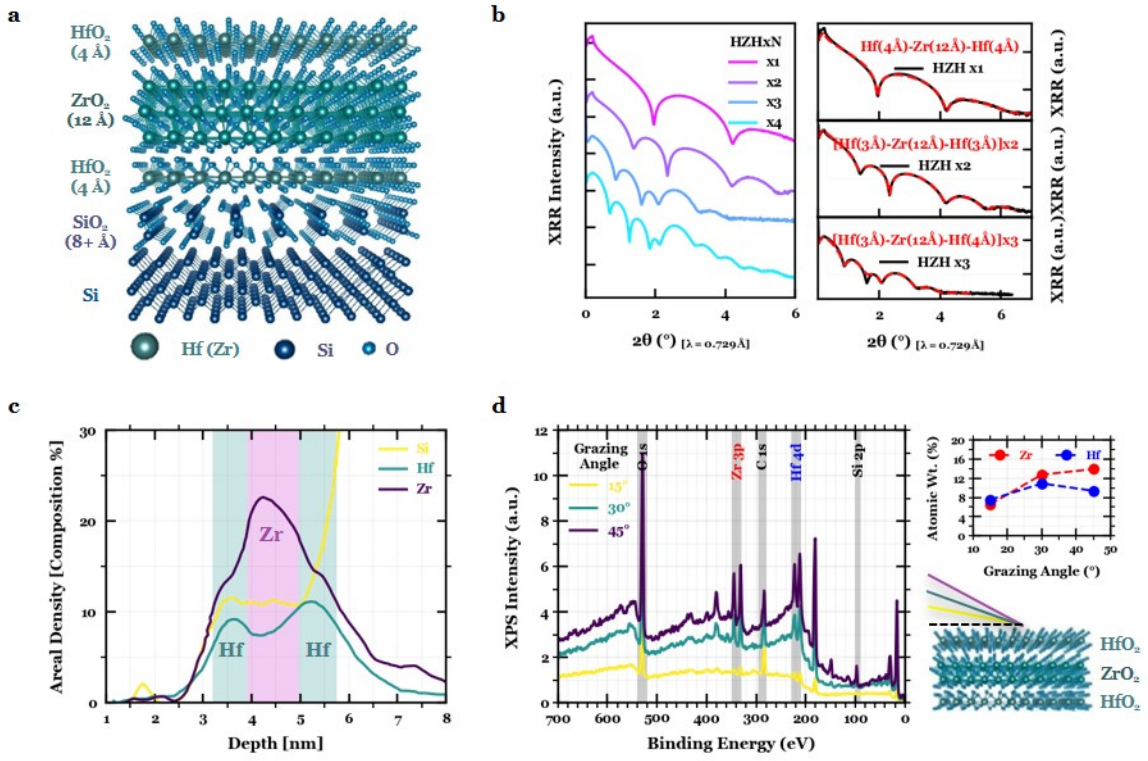
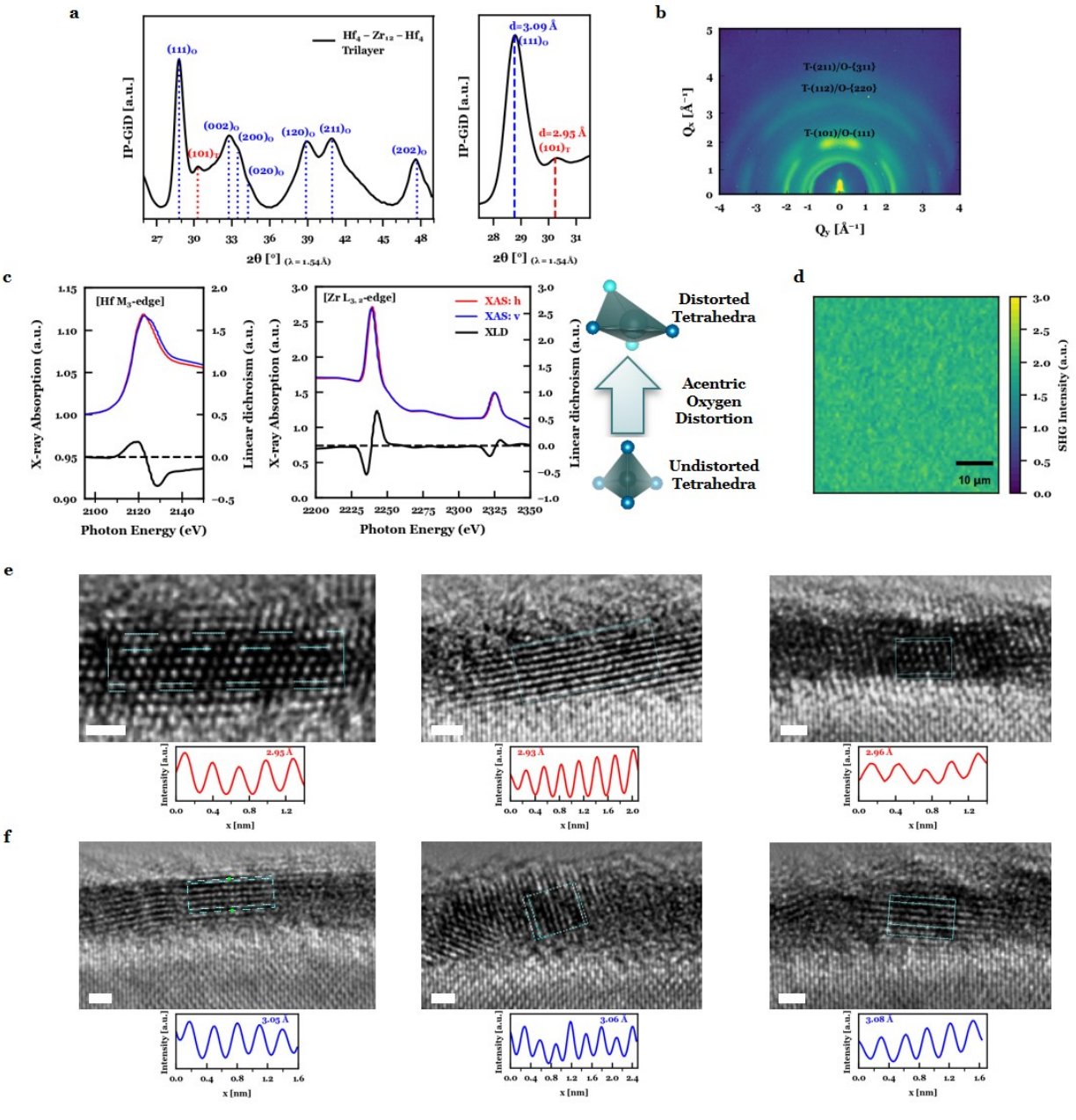
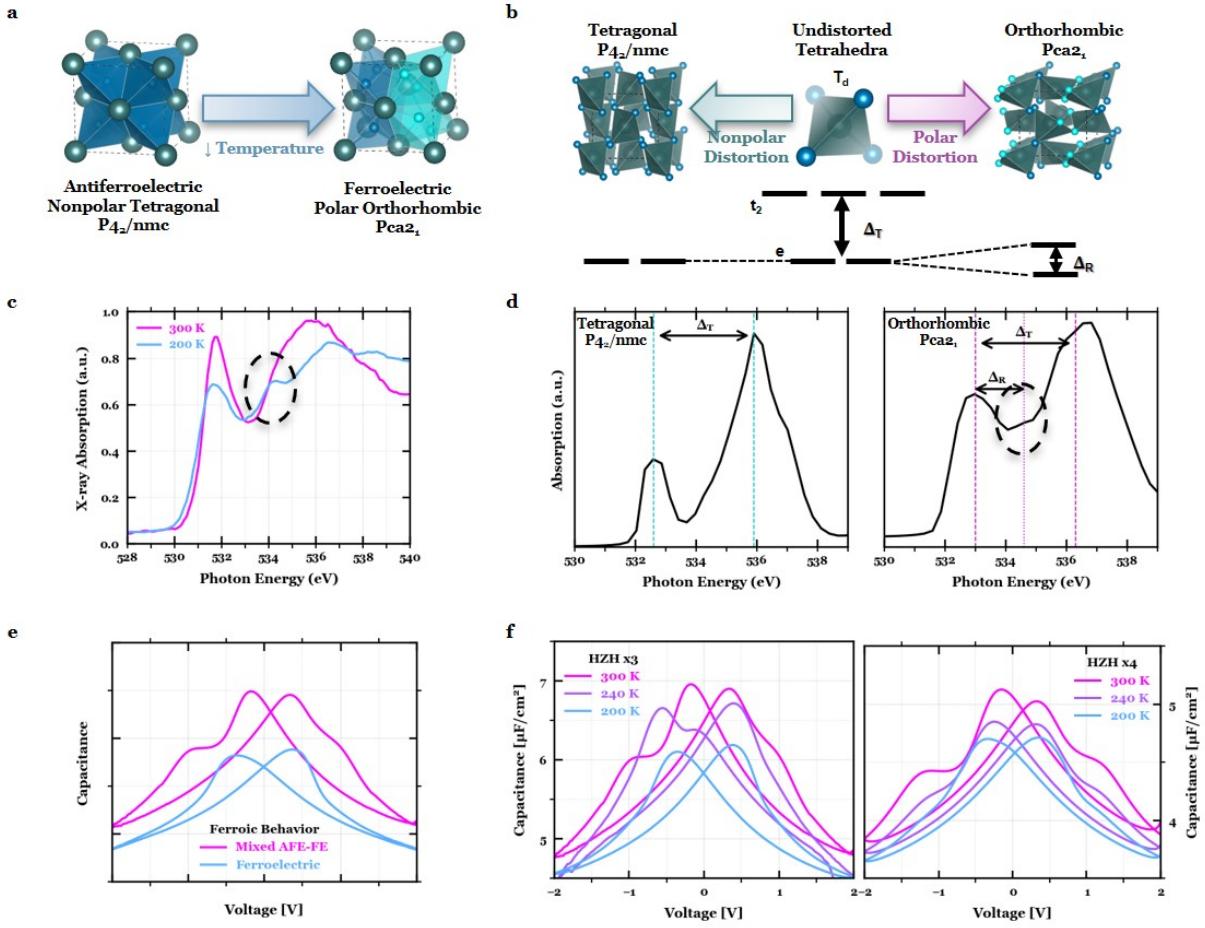


Extended Data Fig. 1. Atomic-scale multilayer structure. **(a)** Schematic of the HfO_2-ZrO_2 multilayer structure on SiO_2-buffered Si. **(b)** Synchrotron x-ray reflectivity (XRR) of thicker HfO_2-ZrO_2 heterostructures (left) repeated with the same periodicity as the thinner trilayer structure; XRR fitting (right) demonstrates the presence of well-separated HfO_2-ZrO_2 layers, i.e. not a solid-solution, for three different multilayer repeats of fixed periodicity, all approximately following the expected 4 Å - 12 Å - 4 Å HfO_2-ZrO_2-HfO_2 structure. **(c)** Layer-resolved electron energy loss spectroscopy (EELS) of the 2 nm HfO_2-ZrO_2-HfO_2 trilayer, demonstrating clear separation of HfO_2-ZrO_2 layers. The exact layer thicknesses are extracted from XRR, which spans a wider sample footprint, rather than the local EELS measurement in which the apparent width increase can be due to beam spreading and local thickness variation. **(d)** Angle-resolved X-ray photoelectric spectroscopy (XPS) of the 2 nm HfO_2-ZrO_2-HfO_2 trilayer (left) and the extracted atomic composition (right). The presence of increasing Zr-content as the grazing angle increases is expected from the multilayer structure in which Zr-content increases after the surface Hf-rich layer.



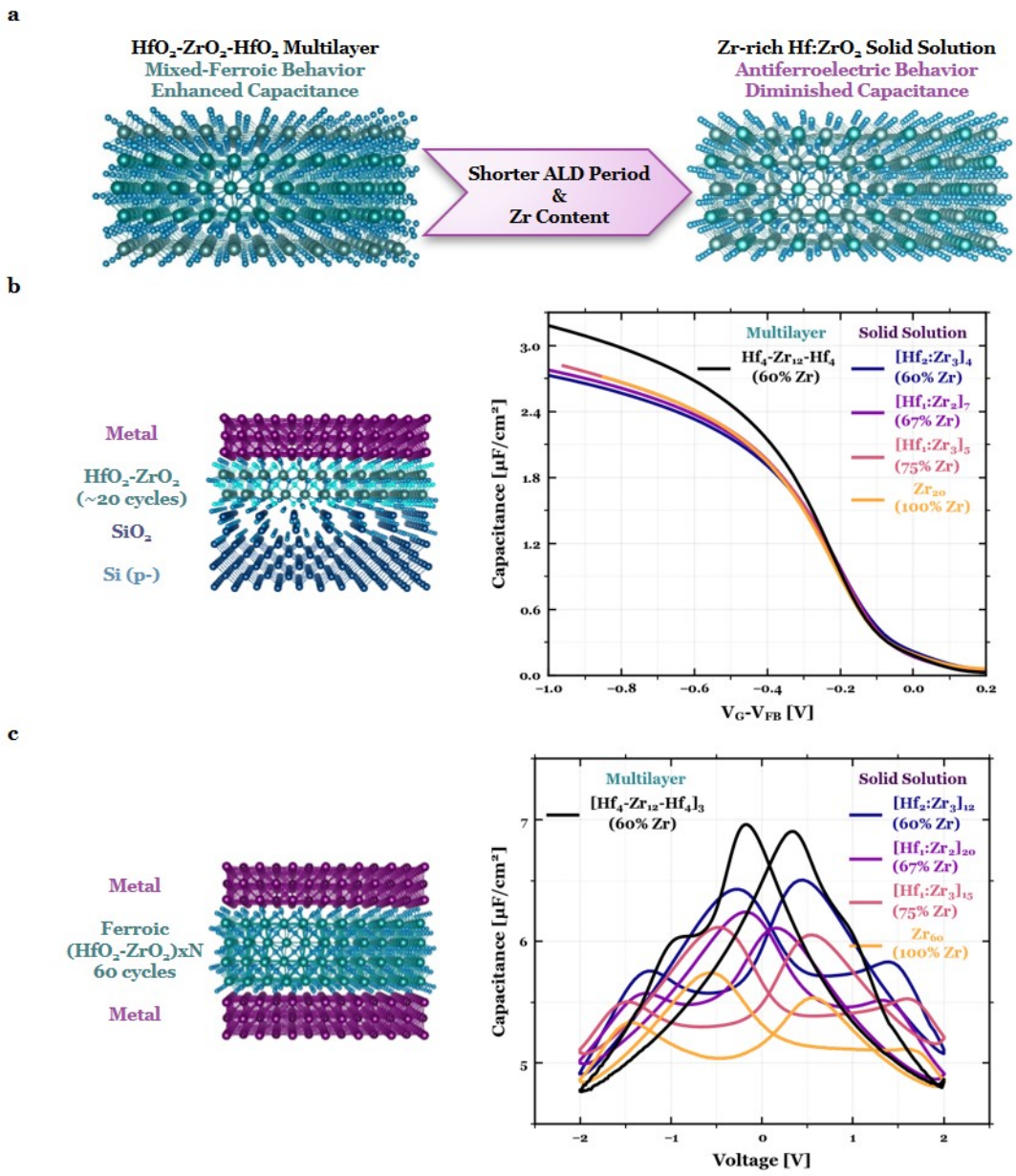
Extended Data Fig. 2. Ferroic phase insights from structural characterization. **(a)** (left) In-plane synchrotron grazing-incidence diffraction (IP-GID) of a bare 2 nm HfO_2-ZrO_2-HfO_2 trilayer indexed to the tetragonal $P4_2/nmc$ and orthorhombic $Pca2_1$ phases and (right) zoom-in of the spectrum about the orthorhombic $(111)_o$ and tetragonal $(101)_t$ reflections, confirming the co-

existing structural polymorphs in the 2 nm film. These two peaks were differentiated via self-consistent indexing of the entire spectrum, in which interplanar lattice spacings – determined from the $\{200\}_o$ family of reflections – closely match the d-spacings for all other reflections – $(111)_o$, $(120)_o$, $(211)_o$, $(202)_o$ – determined by Bragg's law (Methods). **(b)** Two-dimensional reciprocal space map of the bare 2 nm HfO_2-ZrO_2-HfO_2 trilayer, indexed by integrating the diffraction spectrum. The lack of fully polycrystalline rings illustrates that the 2 nm HfO_2-ZrO_2-HfO_2 trilayer is highly-oriented, consistent with TEM imaging. **(c)** Synchrotron spectroscopy (XAS) of the bare 2 nm HfO_2-ZrO_2-HfO_2 trilayer at the (left) Hf M_3- and (center) Zr $L_{3,2}$-edges: (right) the presence of linear dichroism (orbital polarization) provides further evidence of symmetry-breaking in these oriented thin films. **(d)** Second harmonic generation (SHG) mapped across the bare 2 nm HfO_2-ZrO_2-HfO_2 trilayer; the presence of SHG intensity confirms broken inversion symmetry in these ultrathin ferroic films. **(e, f)** Additional cross-sectional TEM providing complementary evidence of the (e) tetragonal $P4_2/nmc$ and (f) orthorhombic $Pca2_1$ phases, in which the extracted $(101)_t$ lattice spacing ($\sim$ 2.95 Å) and $(111)_o$ lattice spacing ($\sim$ 3.08 Å) extracted from IP-GID are consistent with the average lattice spacings extracted from the periodicity of the TEM-imaged planes. The white scale bars in all of the TEM images represent 1 nm.



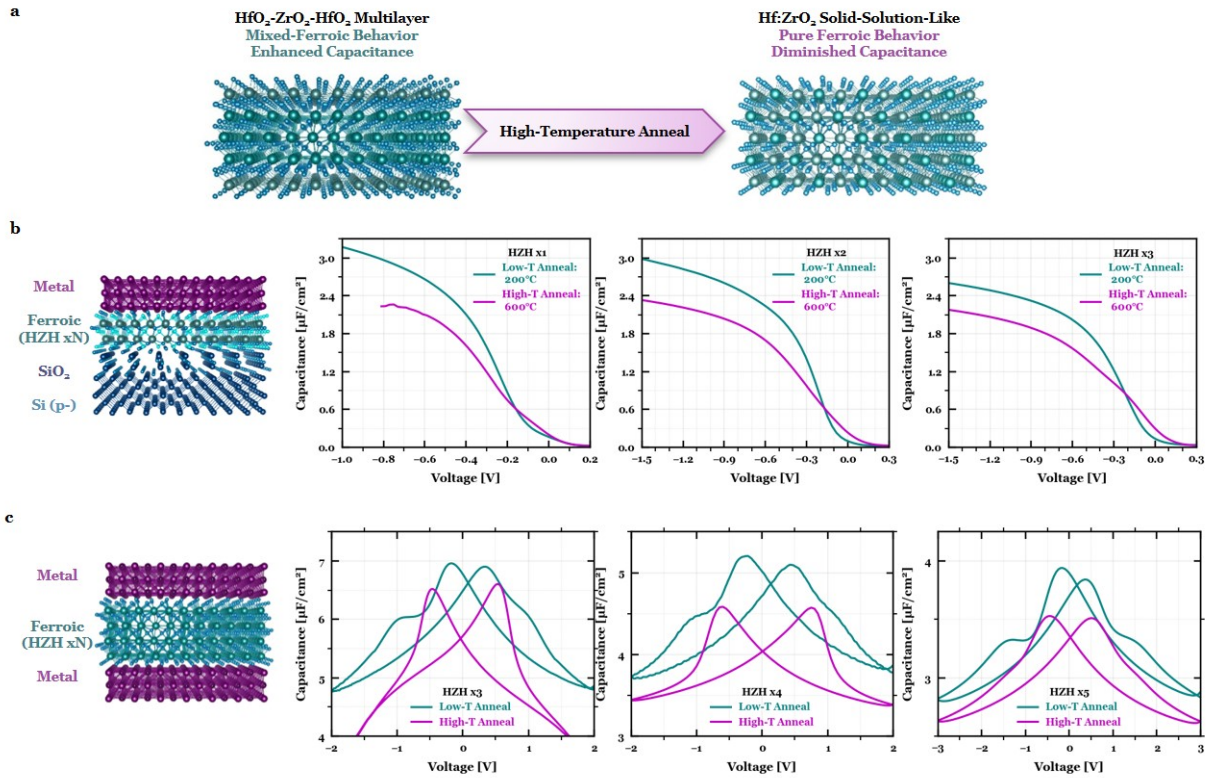
Extended Data Fig. 3. Ferroic phase insights: proximity to temperature-dependent phase transition. **(a)** Schematic of temperature-dependent antiferroelectric-ferroelectric phase evolution in fluorite-structure oxides. At lower temperatures, the higher symmetry tetragonal phase is expected to transition to the lower symmetry orthorhombic phase. **(b)** Schematic crystal field splitting diagram for fluorite-structure polymorphs; symmetry-induced e-splitting provides a spectroscopic signature for the polar O-phase (Methods). **(c)** Temperature-dependent XAS at the oxygen K-edge for a 2 nm HfO_2-ZrO_2-HfO_2 bare film demonstrating clearer spectroscopic signatures of the ferroelectric O-phase emerge slightly below room temperature. **(d)** Simulated oxygen K-edge XAS spectra (Materials Project) for the respective O- and T-phases. XAS provides spectroscopic signatures to distinguish between the O- and T- phases (difficult to resolve from GI-XRD). **(e)**

Prototypical *C*-*V* behavior for mixed antiferroelectric-ferroelectric (shoulder-like features in addition to the characteristic butterfly-like shape) and ferroelectric films (just butterfly-like) in MIM capacitor structures. **(f)** Temperature-dependent *C*-*V* for thicker HfO_2-ZrO_2 multilayers of the same periodicity (in MIM capacitor structure) demonstrating an evolution from mixed-ferroic to ferroelectric-like hysteresis upon cooling slightly below room temperature. Thinner HfO_2-ZrO_2 multilayers films suffer from leakage-limitations, preventing such hysteretic *C*-*V* measurements. The thicker HfO_2-ZrO_2 multilayers of the same periodicity – annealed at the same low-temperature condition to maintain the multilayer structure – demonstrate a similar mixed ferroic to ferroelectric phase transition slightly below room temperature as the thinner 2 nm multilayer (c).

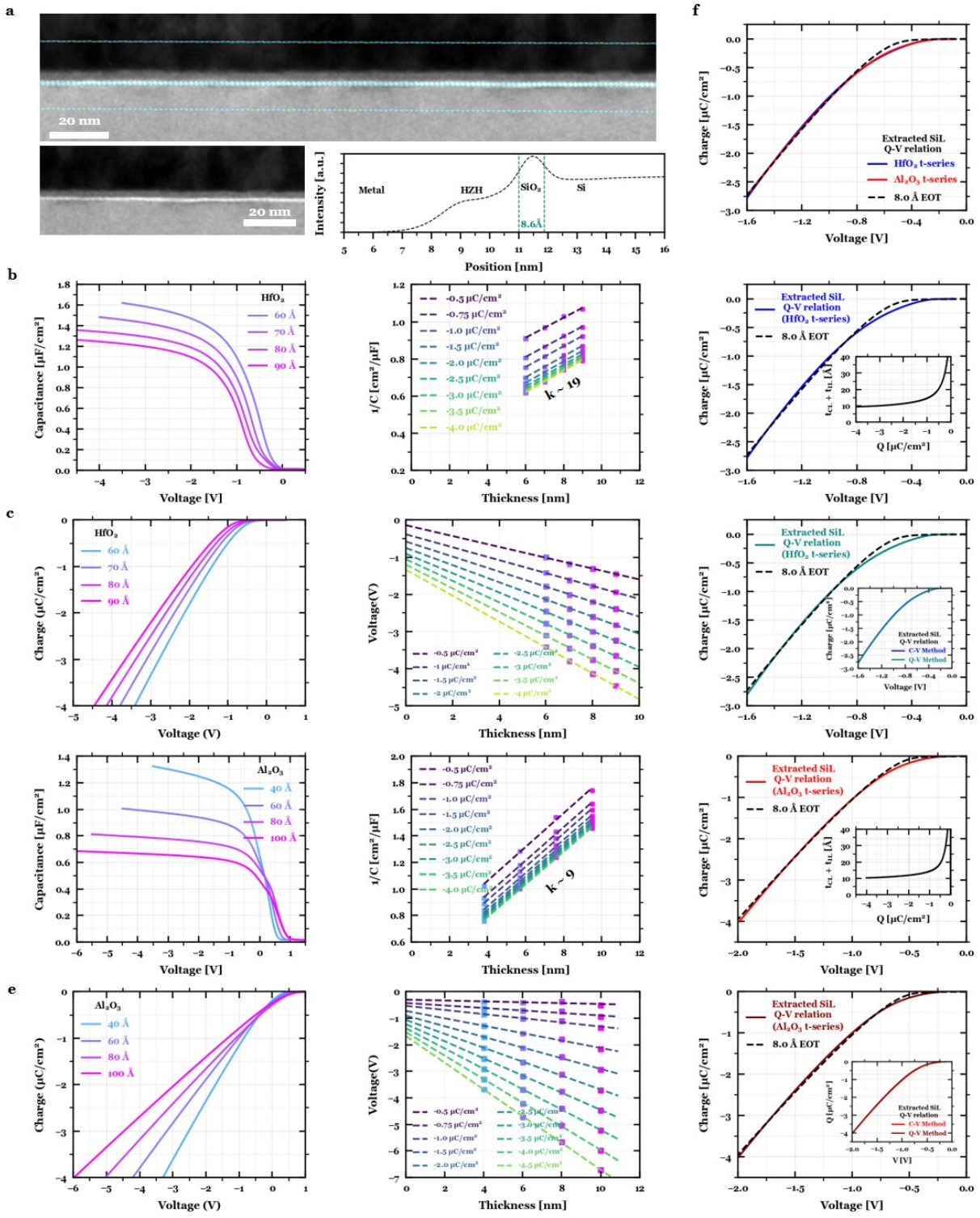


Extended Data Fig. 4. Solid solutions versus superlattice structure: Role of ALD period and Zr-content. **(a)** Schematic of HfO_2-ZrO_2 multilayer and Zr-rich Hf:ZrO_2 solid solution films. With shorter ALD periods, the mixed FE-AFE multilayer structure transitions towards a Hf:ZrO_2 solid-solution with AFE-like behavior. In the solid solution state, the loss of the mixed ferroic order yields diminished capacitance due to the lack of mixed-ferroic-induced capacitance enhancement

(Fig. 1a). **(b)** MOS accumulation *C-V* of the HfO_2-ZrO_2-HfO_2 trilayer (60% Zr) compared to solid solutions films of the same thickness (2 nm) and composition (60% Zr), as well as solid solutions films of the same thickness and higher Zr-composition (67%-100% Zr). **(c)** MIM *C-V* hysteresis loops of the HfO_2-ZrO_2 superlattice (60% Zr) compared to solid solutions films of the same thickness (6 nm) and composition (60% Zr), as well as solid solutions films of the same thickness and higher Zr-composition (67%-100% Zr). Hf:ZrO_2 solid solution films with higher Zr content (60%-75%) is around the range attributed to the "MPB" in thicker Hf:ZrO_2 alloys[26–30,90]. These results indicate the capacitance enhancement in multilayer films is not simply driven by Zr-content[23,35,61,86], but instead the atomic-scale stacking, as the solid solution films with sub-atomic superlattice period do not demonstrate the same mixed ferroic behavior and enhanced capacitance as the superlattices.

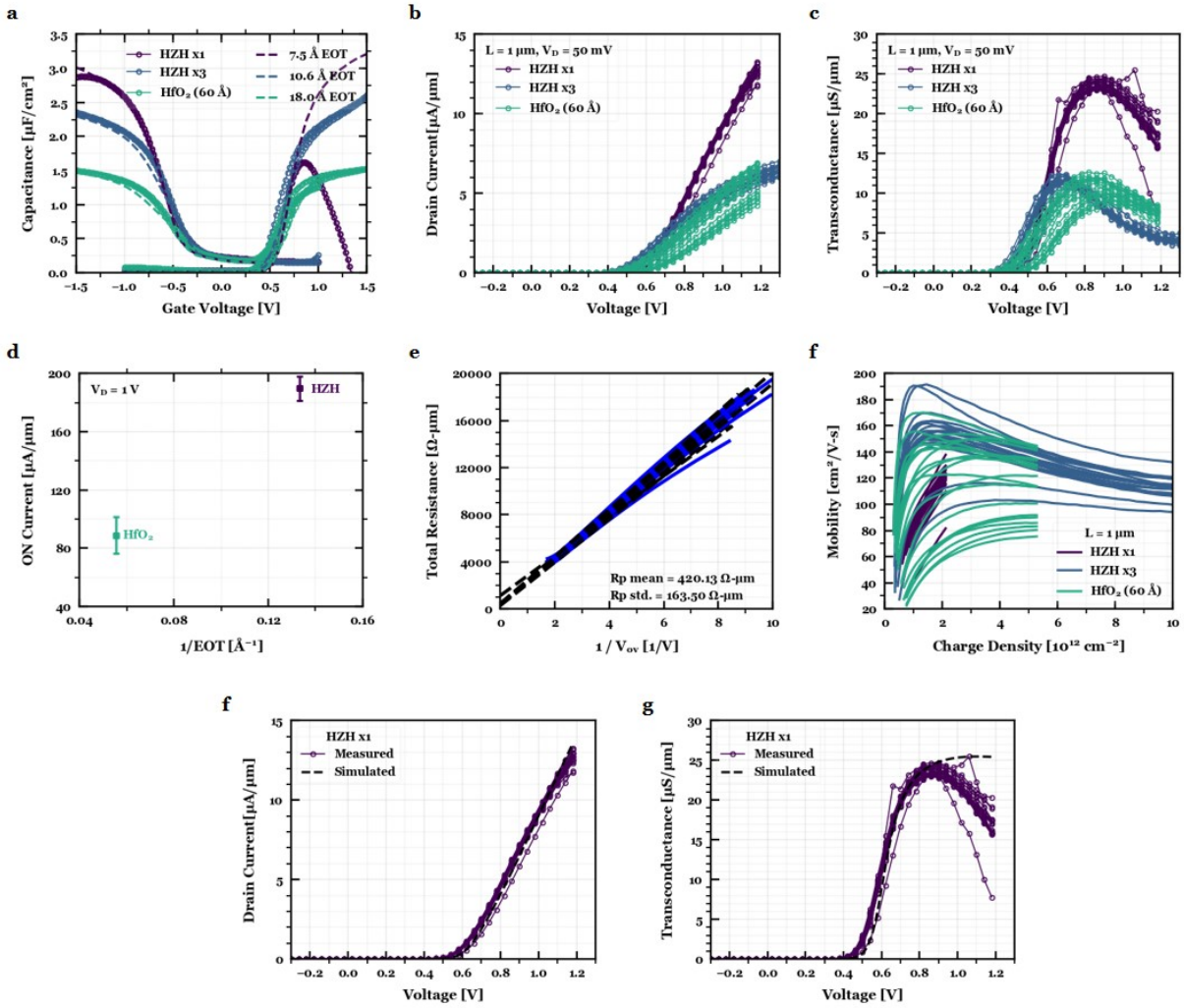


Extended Data Fig. 5. Solid solutions versus superlattice structure: Role of annealing temperature. **(a)** Schematic of HfO_2-ZrO_2 multilayer and Hf:ZrO_2 solid solution films. Under a high-temperature anneal, the multilayer structure transitions towards a Hf:ZrO_2 solid-solution-like structure demonstrating more FE-like behavior. The solid solution state yields diminished capacitance due to the lack of both the higher-permittivity AFE phase and the mixed-ferroic-induced capacitance enhancement (Fig. 1a). **(b)** Comparison of MOS capacitor accumulation *C-V* characteristics in HfO_2-ZrO_2 multilayers, where the superstructure was repeated (left) 1, (center) 2, or (right) 3 times, under both low- and high-temperature anneals. **(c)** Comparison of mixed-ferroic behavior in low-temperature treated MIM HfO_2-ZrO_2 multilayers versus FE behavior in in the same multilayers annealed at high temperatures, where the superstructure was repeated (left) 3, (center) 4, or (right) 5 times. In all instances, the high-temperature anneal (> 500°C) results in diminished accumulation capacitance compared to the low-temperature anneals, as the multilayered mixed-ferroic films presumably transition to more FE-like solid-solution alloys.


a
20 nm
20 nm
Intensity [a.u.]
Metal
HZH
SiO2
Si
8.6Å
Position [nm]
f
Charge [μC/cm²]
Voltage [V]
Extracted SiL
Q-V relation
HfO2 t-series
Al2O3 t-series
8.0 Å EOT
b
Capacitance [μF/cm²]
HfO2
60 Å
70 Å
80 Å
90 Å
Voltage [V]
1/C [cm²/μF]
-0.5 μC/cm²
-0.75 μC/cm²
-1.0 μC/cm²
-1.5 μC/cm²
-2.0 μC/cm²
-2.5 μC/cm²
-3.0 μC/cm²
-3.5 μC/cm²
-4.0 μC/cm²
k ~ 19
Thickness [nm]
Extracted SiL
Q-V relation
(HfO2 t-series)
8.0 Å EOT
tCL + tIL [Å]
Q [μC/cm²]
c
Charge (μC/cm²)
Voltage (V)
Voltage(V)
-0.5 μC/cm²
-1 μC/cm²
-1.5 μC/cm²
-2 μC/cm²
-2.5 μC/cm²
-3 μC/cm²
-3.5 μC/cm²
-4 μC/cm²
Thickness [nm]
Extracted SiL
Q-V relation
(HfO2 t-series)
8.0 Å EOT
C-V Method
Q-V Method
Al2O3
40 Å
60 Å
80 Å
100 Å
k ~ 9
Extracted SiL
Q-V relation
(Al2O3 t-series)
8.0 Å EOT
e
Extracted SiL
Q-V relation
(Al2O3 t-series)
8.0 Å EOT
V [V]

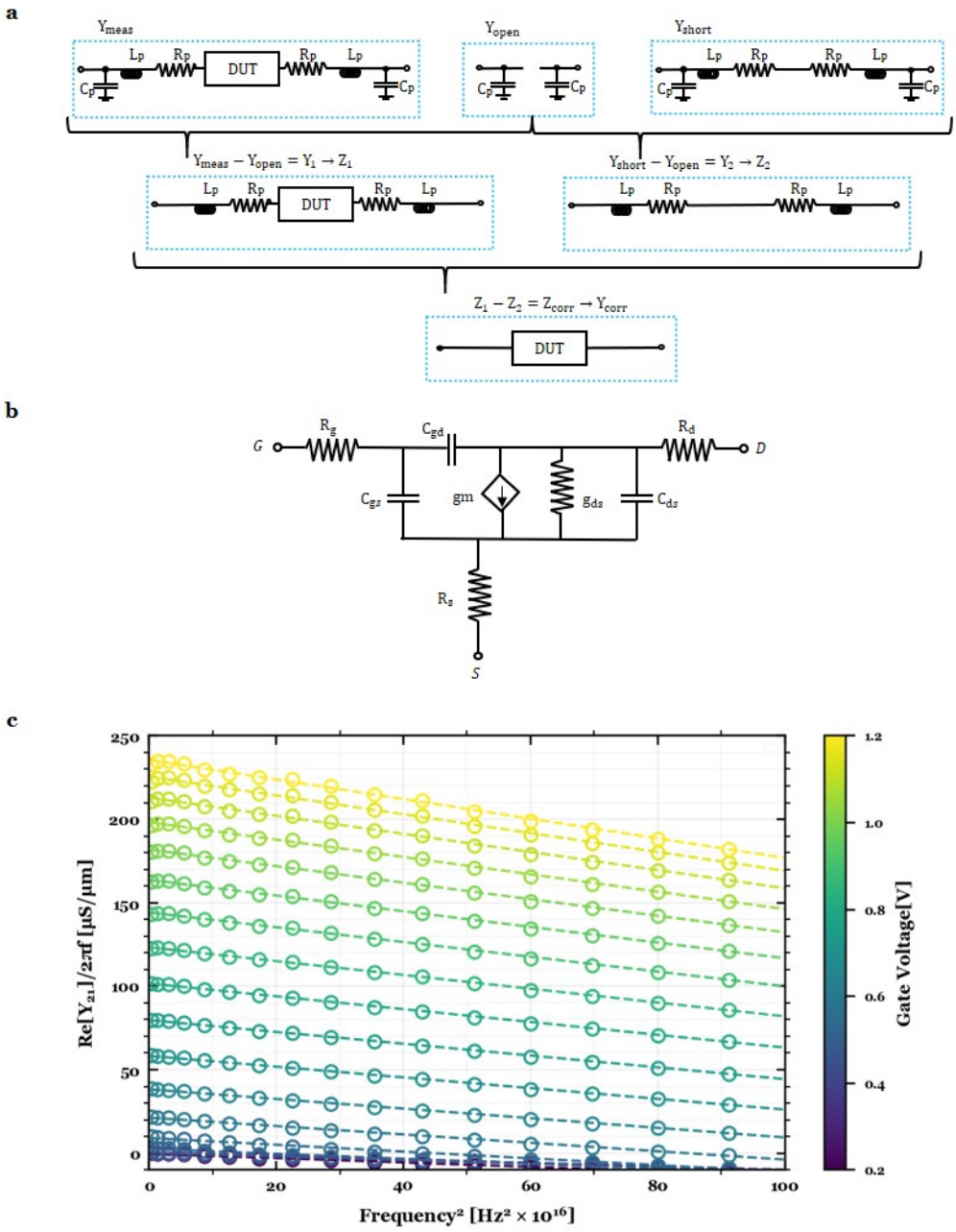
1089

Extended Data Fig. 6. SiO_2 interlayer thickness. **(a)** Wide field-of-view cross-sectional TEM images of the HfO_2-ZrO_2 multilayer structure and its corresponding intensity line scan (bottom right) averaged across the entire field-of-view (FoV) of the top cross-sectional image ($\sim$ 150 nm), specified by the teal-colored box. Note the vertical teal-colored lines in the intensity line scan correspond to the inner teal-colored box in the wide-FoV image, which delineate the SiO_2 interlayer boundaries. The bottom cross-sectional TEM image is provided to highlight the thin SiO_2 interlayer (white region) without obfuscation by the teal-colored box. A physical SiO_2 thickness of 8.6 Å is extracted from analysis of the averaged intensity line scan of the wide FoV TEM (Methods). **(b), (d)** *C-V* measurements of HfO_2 (b) and Al_2O_3 (d) thickness series in MOS capacitor structures (left), extracted inverse capacitance versus thickness at various values of charge (center), and extracted *Q-V* relation Si charge layer and SiO_2 interlayer (SiL) (right), which fits to TCAD simulations for 8.0 Å SiO_2. The SiL *Q-V* relation was found by integrating the extracted capacitance equivalent thickness of SiL versus charge (right, inset). This electrical interlayer thickness (8.0 Å) is slightly less the physical thickness determined by TEM (8.6 Å). As a sanity check, the extracted permittivity from this methodology for HfO_2 and Al_2O_3 corresponds to 18 and 9, respectively, as is expected (Methods, Permittivity Extraction). **(c), (e)** *Q-V* curves of HfO_2 (c) and Al_2O_3 (e) thickness series obtained from integrating MOS *C-V* measurements (left), extracted voltage vs thickness at various values of charge (center), and extracted *Q-V* relation of SiL (right). The SiL *Q-V* relation is consistent with the *Q-V* relation extracted from the *C-V* data (inset). **(f)** Consistency in the SiL *Q-V* relation extracted from the *C-V* data from both the HfO_2 and Al_2O_3 thickness series, which both fit to an SiO_2 interlayer thickness of 8.0 Å.



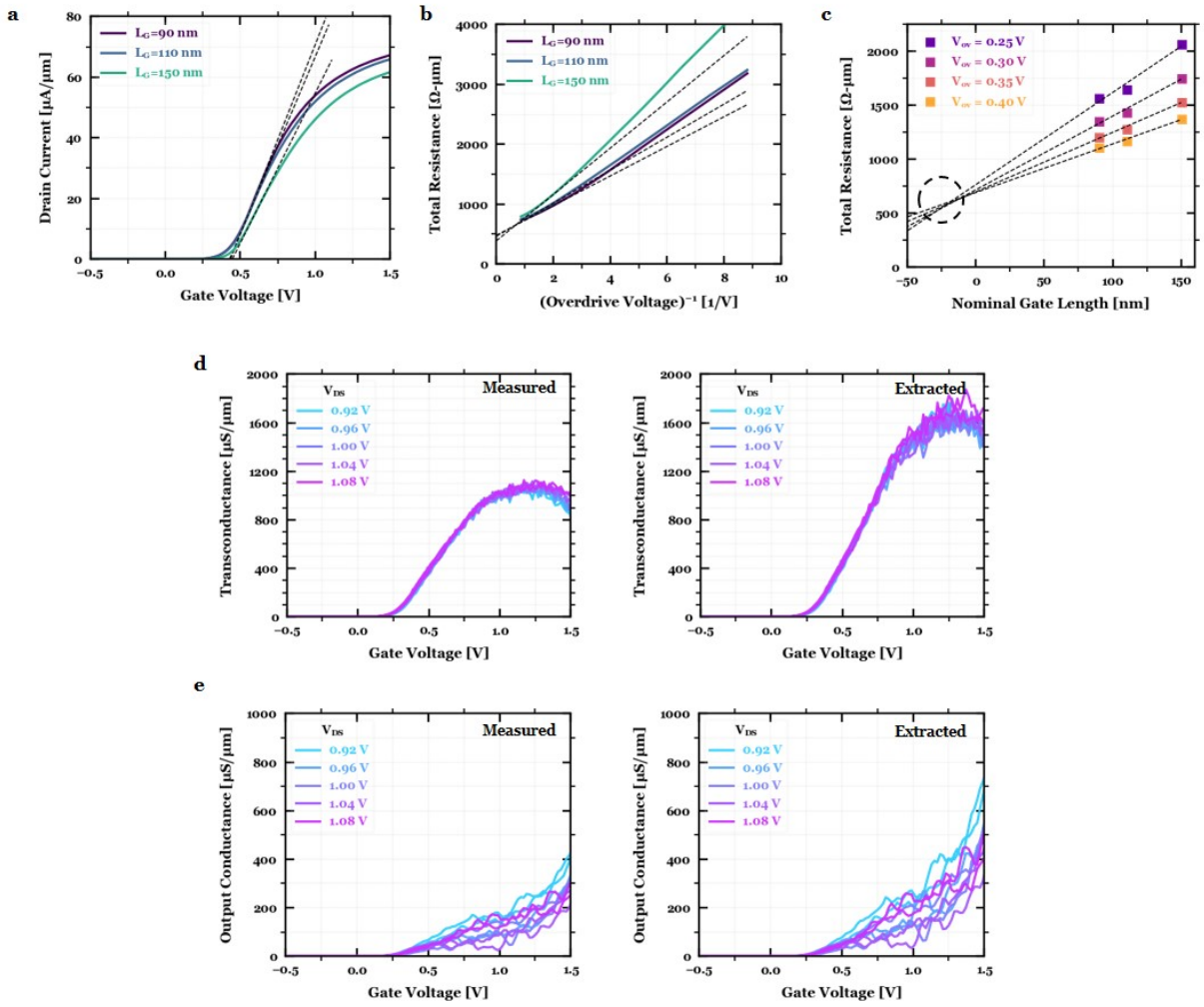
Extended Data Fig. 7. Mobility extraction. **(a)** Split *C-V* curves obtained for multilayer HfO_2-ZrO_2 gate stacks (repeated 1 and 3 times i.e. HZHx1 and HZHx3) and 60 Å HfO_2 dielectric control (Hf-60) from L_G = 50 μm bulk transistors at 10 kHz. These *C-V* curves were fit to EOT simulations of 7.5 Å, 10.6 Å, and 18 Å for HZHx1, HZHx3, and Hf-60, respectively. From the off-state accumulation *C-V*, a doping level of $N_a = 2 \times 10^{17}$ cm^{-3} was extracted and from the slope of the inversion *C-V*, the interface trap density was found to be $D_{it} = 3 \times 10^{12}$ eV^{-1} cm^{-2}. **(b, c)** I_D-V_G (b) and g_m-V_G (c) transfer characteristics for L_G = 1μm bulk transistors at V_{DS} = 50 mV for multiple devices per sample. **(d)** ON current-capacitance (plotted as I_{ON}-1/EOT) comparison

of the HZH multilayer gate stack versus the HfO_2 dielectric control for L_G = 0.5 μm devices. Here, the ON-current is defined as I_D at V_D = 1 V with an overdrive voltage V_{ov} = 0.5 V. The error bars represent 1 standard deviation of the ON-current measured from 20 different devices. As expected, the ON current increases as the inverse-EOT (proportional to the gate capacitance) increases. **(e)** Series resistance extraction from $1/V_{ov}$ method for $V_{ov} = V_{gs} - V_t$ = 0.3 V to 0.5 V for L_G = 1 μm devices. The threshold voltage was extracted from the maximum g_m method. **(f)** Extracted mobility as a function of inversion sheet charge density. The effective mobility was taken to be the average maximum mobility across multiple L_G = 1 μm devices. **(g, h)** Transfer I_D-V_G (g) and g_m (h) data fit to a constant mobility model based on the extracted effectively mobility in (f). A summary of the EOT-mobility trend from the various samples is provided in Figure 3b.



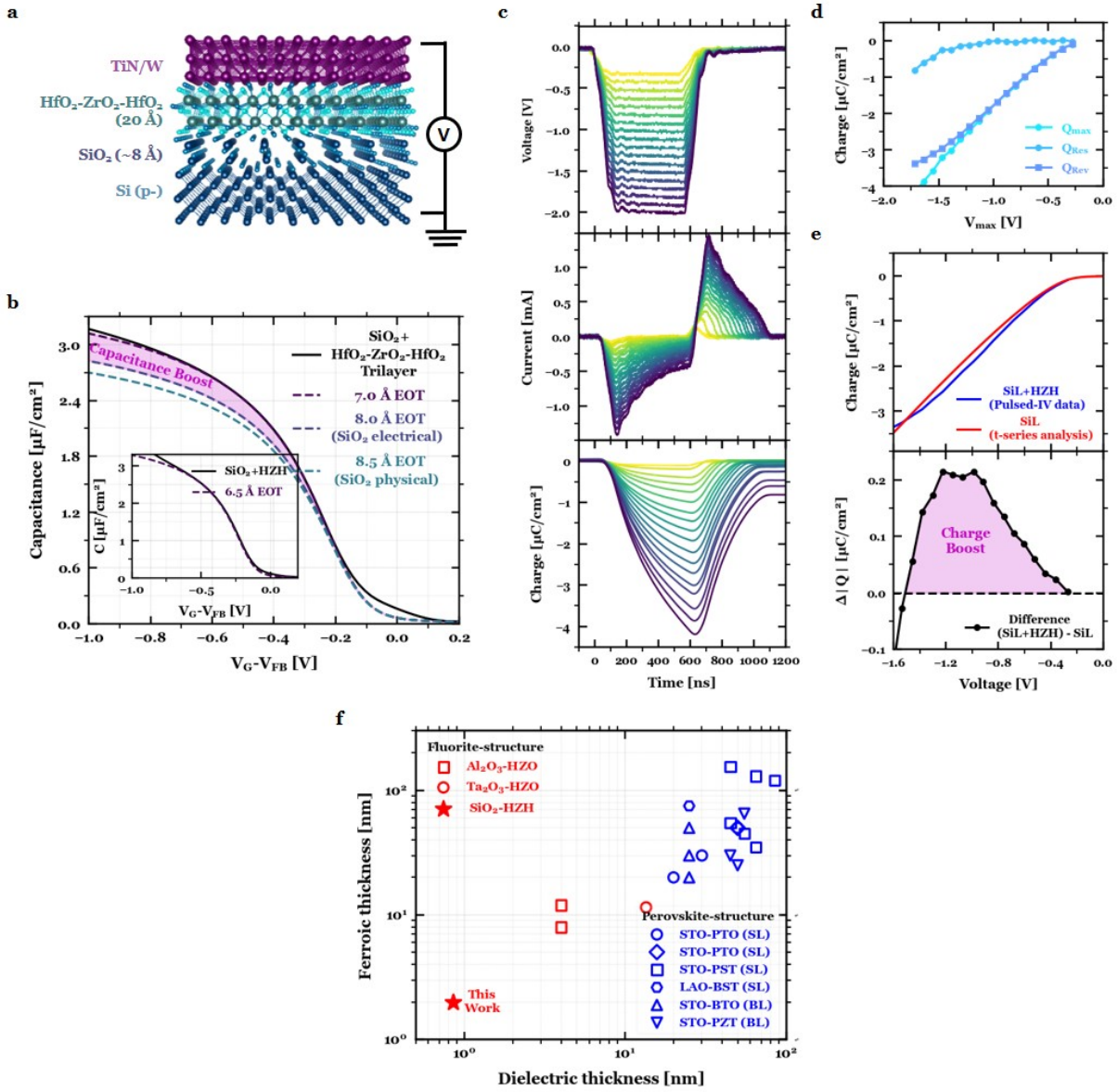
Extended Data Fig. 8. RF device characterization. **(a)** De-embedding procedure for extracting corrected admittance parameters (Y_{corr}) by decoupling parasitic shunt capacitance and series resistance and inductance by measuring scattering parameters for the device under test (DUT) as well as open and short structures. More details can be found in the Methods. **(b)** Small-signal model for

transistor used to extract transconductance (g_m) and total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$)). **(c)** De-embedded $\frac{Re[Y_{21}]}{2\pi f}$ (open circles) as a function of squared frequency at different DC V_{GS} bias points extrapolated to the zero frequency limit (dotted lines) to extract the RF g_m. All data shown was extracted from bulk transistors (L_G = 1 μm) integrating the 2 nm HfO_2-ZrO_2-HfO_2 ferroic gate stack.



Extended Data Fig. 9. Transconductance extraction. **(a)** Threshold voltage extraction by linear extrapolation for various channel lengths. All channel lengths give nearly constant V_T ($\sim$ 0.42 V), satisfying the assumption for the line resistance method. **(b)** Source/drain series resistance extracted using the $1/V_{ov}$ method (Methods). By performing a linear interpolation of the total resistance for V_{ov} = 0.5-0.6 V, the extracted series resistance is $\sim$ 500 Ω-μm. **(c)** Source/drain series resistance extracted using the line resistance method (Methods). The trend is considered down to L_G = 90 nm, which intersects at $\sim$ 500-600 Ω-μm – consistent with the $1/V_{ov}$ method– with an L_G offset of $\sim$ 50 nm. **(d), (e)** Measured (left) and extracted (right) transconductance (d)

and output conductance (e) versus V_G for V_{DS} = 0.9-1.1 V, assuming R_s = R_d = 250 Ω-μm for L_G = 90 nm. The de-embedding of intrinsic g_m and g_{ds} from extrinsic G_m and G_{ds} is described in the Methods. All data shown was measured on SOI short-channel transistors integrating the 2 nm HfO_2-ZrO_2-HfO_2 ferroic gate stack.



Extended Data Fig. 10. Capacitance and charge enhancement. **(a)** MOS schematic of the 20 Å HfO_2-ZrO_2-HfO_2 mixed ferroic trilayer sample on lightly-doped Si (10^{15} cm^{-3}) considered for the following accumulation *C-V* and pulsed *I-V* measurements. **(b)** Accumulation *C-V* curves for the 2 nm HfO_2-ZrO_2-HfO_2 trilayer grown on sub-nm SiO_2 fit to effective oxide thickness (EOT) simulations (Methods). Inset: Externally verified MOS accumulation *C-V* of the same trilayer stack (Methods), demonstrating 6.5 Å EOT. The 2 nm trilayer on top of SiO_2 demonstrates

lower EOT than the thickness of SiO_2 interlayer alone, carefully extracted via physical (8.5 Å) and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence of capacitance enhancement. **(c)** The applied voltage pulse (top), the measured current response (center) and the integrated charge (bottom) as a function of time for 2 nm HfO_2-ZrO_2-HfO_2 trilayer in MOS capacitors. **(d)** The maximum charge Q_{max}, the residual charge Q_{res}, and their difference, Q_{rev}, derived from the charge vs time curve for each of the voltage pulses (Methods). **(e)** The reversible charge of the MOS layer (top) compared against the extracted charge of the Si charge layer plus SiO_2 interlayer (SiL) derived electrically (Extended Data Fig. 5f). The charge boost (bottom) present in the total MOS structure (SiL plus HZH capacitors) compared to just the SiL is a signature of negative capacitance, as previously demonstrated in metal-ferroelectric-insulator-metal (MFIM) structures[47,67]. **(f)** Scatter plot of reported ferroelectric-dielectric systems demonstrating negative capacitance at the capacitor level via capacitance (*C-V* measurements) or charge (pulsed *I-V* measurements) enhancement. The plot considers fluorite-structure bilayers[47,67] (red), perovskite-structure bilayers[22,91] (blue, BL), and perovskite-structure superlattices[38–41] (blue, SL). This work employing sub-nm SiO_2 interlayer and 2 nm HfO_2-ZrO_2 multilayer on silicon (black, star) provides the most scaled demonstration of negative capacitance, as supported by enhanced capacitance from *C-V* measurements (b) and amplified charge from pulsed *I-V* measurements (e) relative to the SiO_2 dielectric interlayer.

Figures

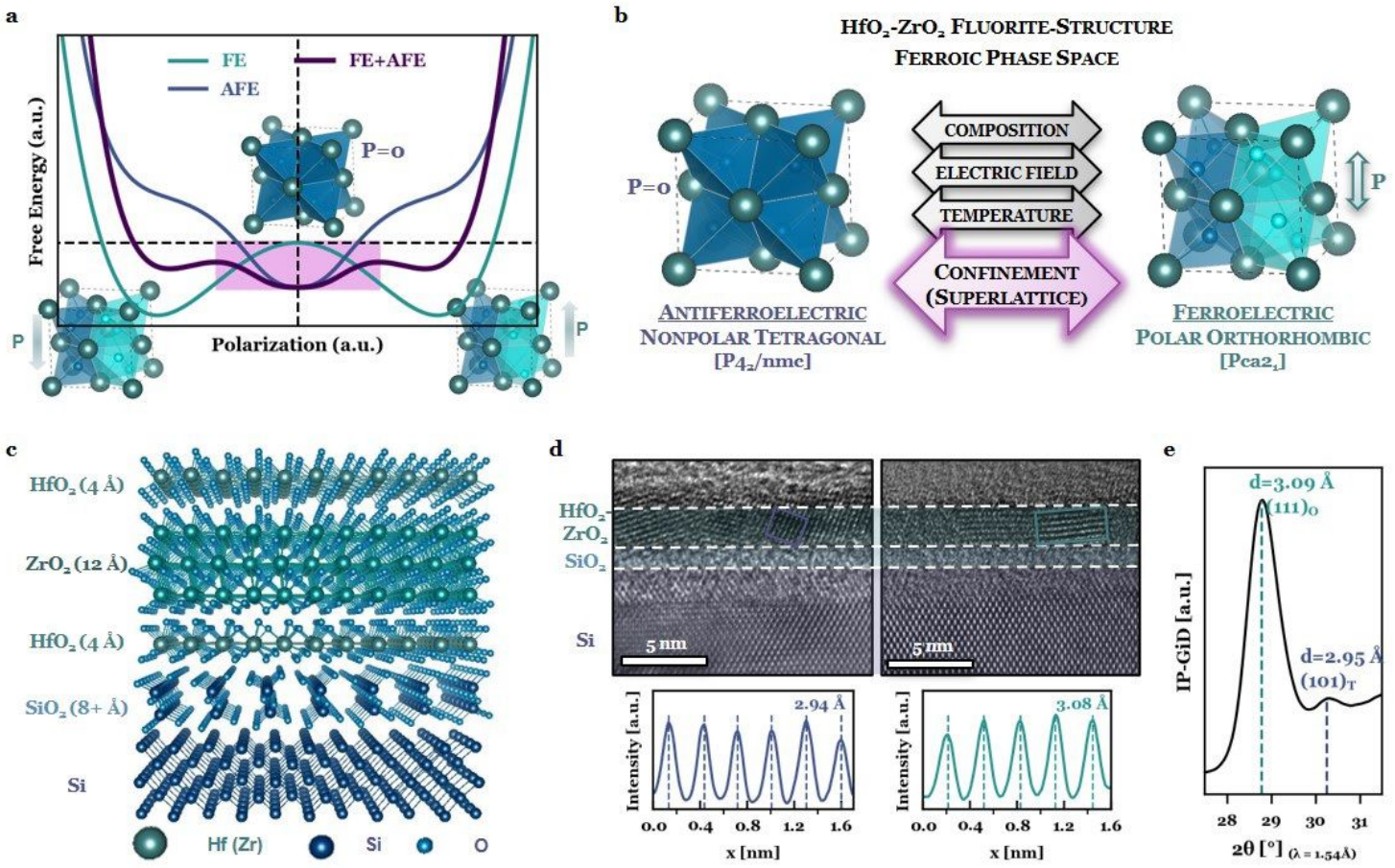


Figure 1

Atomic-scale design of negative capacitance in ultrathin HfO2-ZrO2. (a) Phenomeno logical model of negative capacitance (NC) in a mixed ferroic system. Landau free energy land scapes for a FE, AFE, and mixed FE-AFE system (Methods). Mixed FE-AFE phase competition should suppress polarization48 and enhance electric susceptibility22,40 via proximity to a phase4 boundary, and flattens the energy landscape, desirable traits for NC stabilization. The stable energy minimum of the composite free energy landscape, corresponding to the negative curvature (NC) regime of the ferroelectric energy landscape, is highlighted. (b) Engineering ferroic phase competition in the HfO2-ZrO2 fluorite-structure system. Beyond the conventionally-studied tuning parameters – composition, electric field, temperature23,35 – here we introduce dimensional confine ment via superlattice layering to tailor ferroic phase competition at the atomic-scale. (c) Schematic of the HfO2-ZrO2 fluorite-structure multilayer on Si; the heterostructures maintain distinct layers (i.e. not solid solution alloys) based on EELS, XRR, and depth-resolved XPS (Extended Data Fig. 1). The role of the layering on the underlying ferroic order and capacitance is studied by electrical measurements as a function of HfO2-ZrO2 stacking structure and annealing temperature (Extended Data Fig. 4 and 5, respectively). (d) HR-TEMimage of the atomic-scale HfO2-ZrO2-HfO2 trilayer (top) and extracted d-lattice spacings (bottom) corresponding to the fluorite-structure AFE

tetrago nal (P42/nmc, red) and FE orthorhombic (Pca21, blue) phases, respectively. The layer delineations are approximate, as the HfO2-ZrO2 and SiO2 interlayer thicknesses are more rigorously deter mined by XRR and TEM analysis (Extended Data Fig. 1 and 6, respectively). Note imaging the crystallinity of the HfO2-ZrO2 layers requires mistilt with respect to the Si lattice (Methods). (e) Synchrotron IP-GiD demonstrating the presence of both the AFE T-phase (101)t and FE O-phase (111)o reflections whose d-lattice spacings are consistent with those extracted from TEM. Detailed indexing to higher-order reflections for structural identification of the ferroic phases is provided by wide-angle synchrotron diffraction (Extended Data Fig. 2a). Further evidence of inversion symmetry breaking is provided by second harmonic generation and synchrotron linear dichroism (Extended Data Fig. 2c,d). Additionally, the evolution between these two ferroic phases are also studied as a function of temperature (Extended Data Fig. 3).

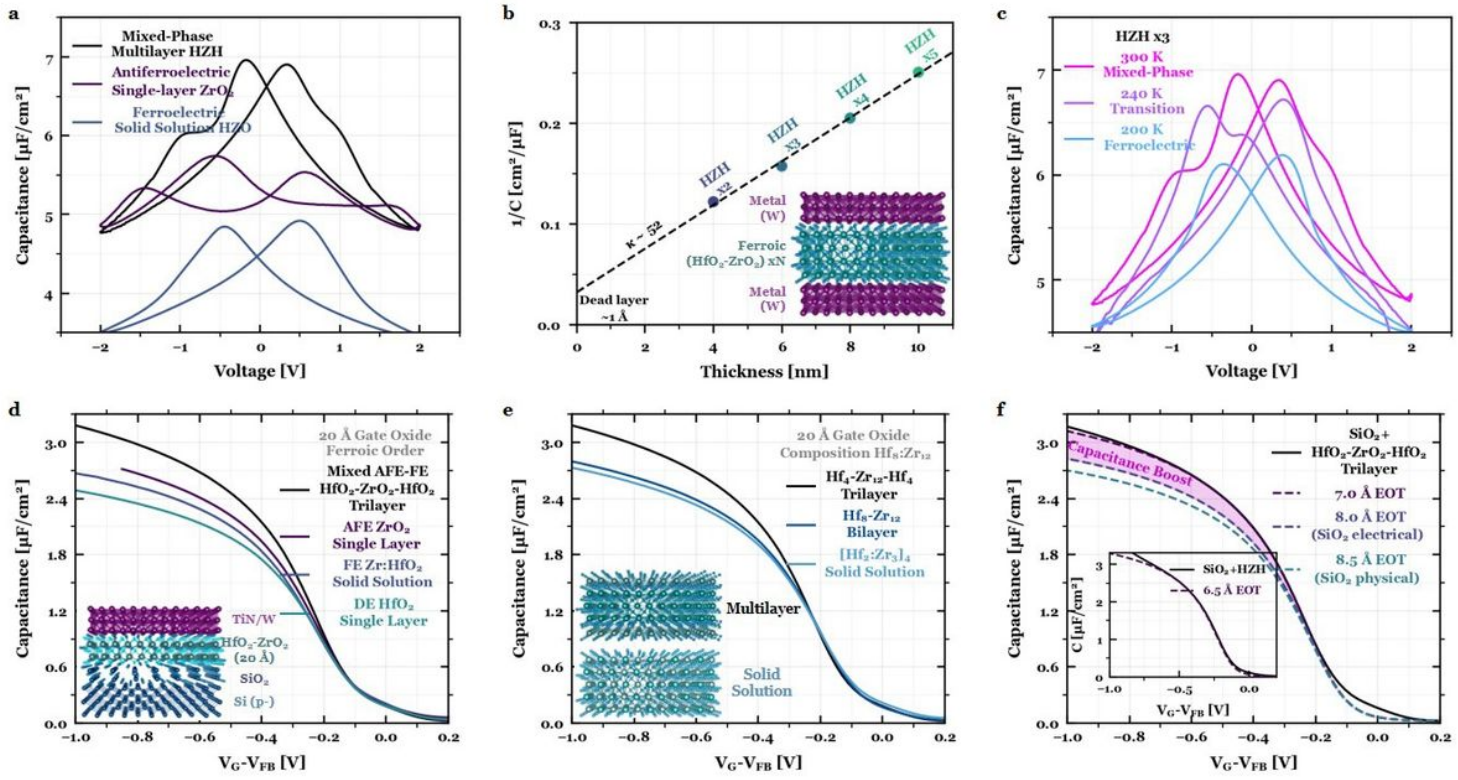


Figure 2

Enhanced capacitance in ultrathin HfO2-ZrO2 mixed-ferroic heterostructures. (a) MIM C-V hysteresis loops for a mixed FE-AFE HfO2-ZrO2 multilayer demonstrating higher ca pacitance compared against its AFE (ZrO2) and FE (Zr:HfO2) counterparts of the same thickness. (b) Inverse capacitance versus thickness of the MIM HfO2-ZrO2 multilayers up to 5 superlattice repeats (10 nm), with an extracted permittivity of 52 (Methods), extremely large for HfO2-based oxides. (c) MIM C-V hysteresis loops for HfO2-ZrO2 multilayers of the same periodicity demon strating an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room temperature. The proximity to the temperature-dependent phase transition (Extended Data Fig. 3) suggests the HfO2-ZrO2 heterostructures lies near its maximum electric susceptibility position, ideal for negative capacitance stabilization40,48. (d) MOS accumulation

C-V of HfO2-ZrO2-HfO2 trilayer compared to AFE ZrO2, FE Zr:HfO2, and DE HfO2, all of the same thickness (20 Å), indicating mixed-ferroic behavior is optimal for enhancing capacitance rather than purely FE or AFE behavior. (e) Accumulation C-V of the HfO2-ZrO2-HfO2 trilayer compared to bilayer and solid solutions films of the same thickness (ALD cycles) and composition (Hf:Zr cycles). Inset: Schematic of multilayer (Hf and Zr cations vertically separated) versus solid solution (Hf and Zr cations inter-mixed). These results suggest the capacitance enhancement in multilayer films is not simply driven by Hf:Zr composition23,35, but instead the atomic-scale stacking (Extended Data Fig. 4, 5). (f) Accumulation C-V curves for a 2 nm HfO2-ZrO2-HfO2 trilayer grown on sub-nm SiO2 fit to effective oxide thickness (EOT) simulations (Methods). Inset: Externally verified MOS accumulation C V of the same trilayer stack (Methods), demonstrating 6.5 Å EOT. The 2 nm trilayer on top of SiO2 demonstrates lower EOT than the thickness of SiO2 interlayer alone, carefully extracted via physical (8.5 Å) and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence of capacitance enhancement. Furthermore, these 2 nm ferroic gate stacks demonstrate amplified charge from pulsed I-V measurements relative to the SiO2 interlayer (Extended Data Fig. 10). Notably, this 2 nm HfO2-ZrO2 multilayer on sub-nm SiO2 provides the most scaled demonstration of charge and capacitance enhancement at the capacitor-level (Extended Data Fig. 10).

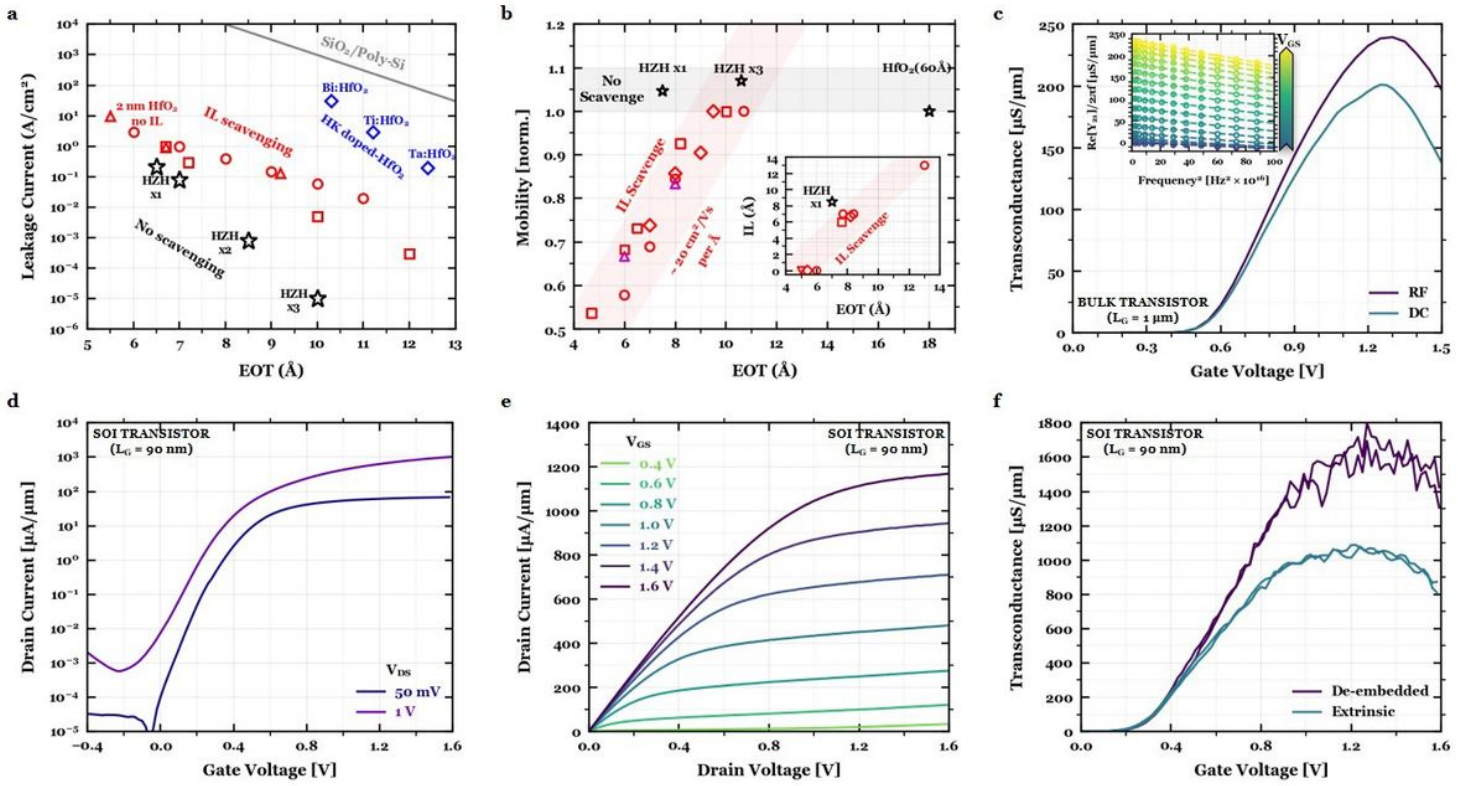


Figure 3

Device performance benefits utilizing ultrathin mixed-ferroic HfO2-ZrO2 gate stacks. (a) Leakage-effective oxide thickness (JG-EOT) scaling of the multilayer gate stacks (black) bench marked against reported HKMG literature3, including interlayer-scavenged 2 nm HfO2 (red), high-doped HfO2 (blue), and SiO2/poly-Si (gray). The leakage is the lowest reported for a 6.5-7.0 Å EOTMOS capacitor on silicon3, due

to the EOT reduction without requiring interlayer SiO2 thickness reduction. (b) Normalized mobility versus EOT scaling of the multilayer gate stacks (black) benchmarked against reported HKMG literature3, including interlayer-scavenged 2 nm HfO2 (red) and hybrid silicate-scavenged interlayer (magenta). For EOT scaling in conventional HKMG systems, the SiO2 interlayer has to be reduced to lower EOT, which leads to degraded mobility3. In this case, enhanced capacitance in HfO2-ZrO2 multilayers achieves scaled EOT without having to thin the SiO2 interlayer; therefore, mobility is not degraded. Inset: SiO2 interlayer thickness versus EOT scaling comparing the 7.0 Å EOT HfO2-ZrO2-HfO2 trilayer against notable HKMG literature which employ interlayer scavenging to reduce EOT3. This scatter plot highlights the underlying reason for the enhanced leakage-EOT and mobility-EOT behavior in the ultrathin trilayer gate stacks: low EOT without reduced SiO2 interlayer thickness. (c) Transconductance (gm) versus gate voltage (VG) 450 for long-channel bulk transistors (LG = 1 m) obtained from both DC (derivative of ID-VG) and RF (Re[Y21]) measurements (Methods) at VDS = 1 V. Inset: De-embedded Re[Y21] (open circles) as a function of squared frequency at different DC VGS bias points extrapolated tothe zero frequency limit (dotted lines) to extract the RF gm (Extended Data Fig. 8). The high frequency measurements help suppress defect contributions which would otherwise dampen the intrinsic gm. (d, e, f) DC I-V transfer characteristics (ID-VG, d), DC output characteristics (ID-VD, e), and DC transconductance (gm-VG, f) for short-channel (LG = 90 nm) SOI transistors. Notably, the maximum on-current and gm at VDS = 1 V exceeds 1 mA/m and 1 mS/m. DC mobility and transconductance values are carefully extracted after de-embedding the series resistance from double-swept I-V measurements (Extended Data Fig. 7 and 9, respectively).