# A wrap-gate CNT-MOSFET based SRAM bit-cell with asymmetrical ground gating and built-in read-assist schemes for limited-energy environments application

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**Research Article**

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# *A wrap-gate CNT-MOSFET based SRAM bit-cell with asymmetrical ground gating and built-in read-assist schemes for limited-energy environments application*

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## Abstract

Today, designing low-power single-bit SRAM structures with the ability to operate regularly at low supply voltages and with high immunity against standard radiation particles impact is challenging for designers. In the present article, a novel design of a low-power radiation-hardened single-ended SRAM bit-cell (UPRHSE) based on gate-diffusion input (GDI) method using gate-all-around carbon nano-tube (CNT) MOSFETs (GAA CNT-MOSFETs) along with dual-chirality/multiple-diameter technique for CNTs with an asymmetric virtual ground gating and built-in read-assist schemes with inherent single-node event upset (SEU) preventive and self-correction capabilities and a high degree of robustness against multiple-node event upsets (MEUs) in the presence of more consumption area storage has been proposed. In order to investigate single/double upset injection circuit model using the structure of the T-connected pseudo resistors (TPRs) has been proposed. Also, based on the analytical-compact model, an equation for calculating the data-retention voltage ($V_{DR}$) metric for the suggested bit-cell structure and an algorithm for facile estimate of $V_{DR}$ for other bit-cell architectures is presented. The results of extensive Monte-Carlo (MC) simulations to evaluate the proposed bit-cell indicate larger noise margins, acceptable yield, less sensitivity to process, voltage and temperature (PVT) variations, higher critical charge and consequence more robustness to soft errors with high reliability of data storage in standby mode in the presence of voltage conditions lower than the nominal power supply, and better results in other comprehensive figure of merits (FoMs) criteria compared to nanotechnology-based state-of-the-art radiation-hardened (rad-hard) bit-cell circuits with the same number of transistors in the 16 nm technology node. So, the proposed UPRHSE design can be a reasonable choice for applications that demands high stability, impact resistance to radiation particles and extremely low power in a radiation abundant environment with limited-energy sources. Finally, in order to use the suggested UPRHSE bit-cell in a real application with secure data transfer approach, the suggested structure is employed for storing. The results show the better performance of UPRHSE in terms of other comprehensive FoMs based on PSNR and MSSIM metric to evaluate the appropriate accuracy in pixel-by-pixel image compared to other well-known counterpart designs.

***Keywords***: Gate-all-around (GAA) carbon nano-tube (CNT) FET · Gate-diffusion input (GDI) method · single-bit line · Soft error immunity · Process, voltage and temperature (PVT) variation · High yield · Data-retention voltage ($V_{DR}$) · Image processing

## 1. Introduction

Today, with the increasing implementation of applications based on global positioning system (GPS) on a variety of digital systems in the presence of radiation effects through the earth's atmosphere, high-performance and low power on-chip memory for these types of systems with reliability unchanged in data-bit storage and low susceptible to the radiation effects is required. In designing memory structures based on emerging technologies in the presence of high scaling problem, the possibility of soft errors increases drastically, especially multiple-node event upsets (MEU), due to sensitive nodes with smaller parasitic capacitors being at a smaller area and also circuits with lower supply voltage [1]. So far, various topologies have been suggested to hardening the structure of SRAM cells to event upset mitigation to improve their radiation immunity, which can be added to some passive elements such as P-type MOSFET/N-type MOSFET-based resistances and capacitors to the internal structure of cross-inverters or the addition of cross-connection inverters parallel to each of the feedback loop inverters to enhance the resistance and overall critical charge of a typical SRAM bit-cell structure with 6 transistors and other special design with the approach of reinforces the local charge in sensitive nodes to reduce bit flips [2,3]. In recent research, memory circuits have been proposed with the approach of application in environments with limited-energy resources in the direction of optimal performance against the basis of process, voltage and temperature (PVT) variations and radiation hardened under low power consumption conditions [4-6]. Single-port (SP) or single bit-line (BL) scheme based static random-access memory (SRAM) structures are one of the most basic blocks in the design of circuit structures with special applications and approaching the low power and area consumption and complexity in the field of nanotechnology [7]. Single-ended (SE) SRAM topologies with simultaneous single-line data sharing for both read and write operations reduce the BL charge per operation about 50% compared to conventional dual or differential-port (DP), as a result the probability of bit-line charging (due to the large capacitance of bit-line) in memory will be reduced by about 38%, assuming a DP design for writing operations and a SE scheme for the read operation [8]. The gate-all-around (GAA) or gate-wrap-around (GWA) carbon nano-tube (CNT) metal oxide semiconductor field-effect transistors (CNT-MOSFETs) are one of the most efficient types of CNT-MOSFETs with wrap-around or cylindrical gate geometry structure. These

transistors provide the controllability of the gate through a *high-k* dielectric material over the CNT channel and consequently lower short-channel effects (SCE) such as their drain-induced barrier lowering (DIBL), $V_{th}$ *roll-off*, sub-threshold swing (SS) factor and hot-carrier effect to the supply voltage, are and appropriate candidate for designing high-performance ultra-scaled circuit's architecture [9]. Also, the gate-diffusion input (GDI) method is a logic design methodology for reducing power consumption, propagation delay under PVT corners, enhanced hazard tolerance and maintaining low area complexity in digital combinatorial circuits [10]. Until now, CNT-MOSFET technology-based modified GDI (m-GDI) has been used in designing energy-efficient circuits [11]. In the present paper, GAA CNT-MOSFET-based GDI method (GAA CNT-GDI) with no bulk terminal and all body effects compared with its common CNT-MOSFET-based design counterpart [10], with high compatible and immunity against misaligned/mis-positioned challenges of CNT transistors technology in fabrication phase is introduced for memory bit-cell array design. A novel structure of ultra-low power radiation-hardened (rad-hard) asymmetric SE 11T-SRAM bit-cell (UPRHSE) with inherent single-node event upset (SEU) prevention and also self-correction capabilities based on GAA CNT-GDI technique with the approach of improving performance and more strength in the presence of PVT variations, appropriate performance in data storage at data-retention voltage ($V_{DR}$) conditions as an electrical parameter has been proposed and evaluated with other counterpart designs in the same number of transistors at 16 nm node. The proposed rad-hard cell-bit structure has the unique features as mentioned below compared to its other counterparts:

*(a) Utilizing the proposed asymmetric write-assist circuit based on functions of GAA CNT-GDI in a lower complexity with maximum voltage swing, for special improvement in write-ability.*

*(b) Using built-in read-assist scheme in a positive feedback mode to reduce consumption and creation of redundant storage nodes to reduce the vulnerability caused by radiation particles impact.*

*(c) Application of single BL (like SE) design with GDI technique in the presence of GAA CNT-MOSFET technology in order to save power consumption compared to other counterpart designs, significantly.*

*(d) Designing a memory array based on write/read blocks in a proposed bit-interleaving structure to increase the specific correlation in the cell structure for receive, store, and send data-bits.*

*(f) Storing images in the form of two-layer quick response (2LQR) code in a desirable quality based on the accurate conversion of pixel values of the image to its voltage equivalent using the proposed algorithmic mechanism.*

In today's life, QR codes are a special type of optical 2D matrix barcode designed to store bit information, efficiently which can be easily decoded physically due to the fast readability and increased storage capacity. QR codes with good radiation tolerance, peak signal-to-noise ratio (PSNR) are used in a variety of multimedia applications such as personal identification, accessing websites, digital downloading by intelligent systems, data transfer security and sending information to social networks [12,13]. Figure 1 demonstrates a sample system of using and reading a two-layer QR code [14] related to weather studies that includes three components, atmosphere as a target environment, satellite in the rotating axis low earth orbit (LEO) with an altitude of approximately one-third of the earth's radius equipped with SRAM block to store QR code of information, which indicates the web server host on the territorial station. Since satellite application systems based on sending information in the form of QR code require memory with high stability/performance, in high capacity to store data including image and text message in the nano process, so at a real-application level, the two-layer QR-based image processing application is used to store pixel-by-pixel image data in two separate layers in the memory array in separate even and odd columns based on the to the suggested algorithm. The rest of this paper is organized as follows: section 2 includes the brief overview of the GAA MOSFET-like CNT-MOSFET device and its basic concepts. Section 3 represents the proposed GAA CNT-MOSFET technology process-based basic GDI cell and proposed UPRHSE bit-cell and working mechanism detail, respectively. Investigation of proposed single event transient (SET) injection circuit model and evaluation of SEU and MEU and also data retention voltage metric for the suggested bit-cell structure in subsections 4 and section 5 are provided, respectively. The comprehensive simulation results and figure of merits (FoMs) comparisons for different bit-cells architectures are given in subsections 6.

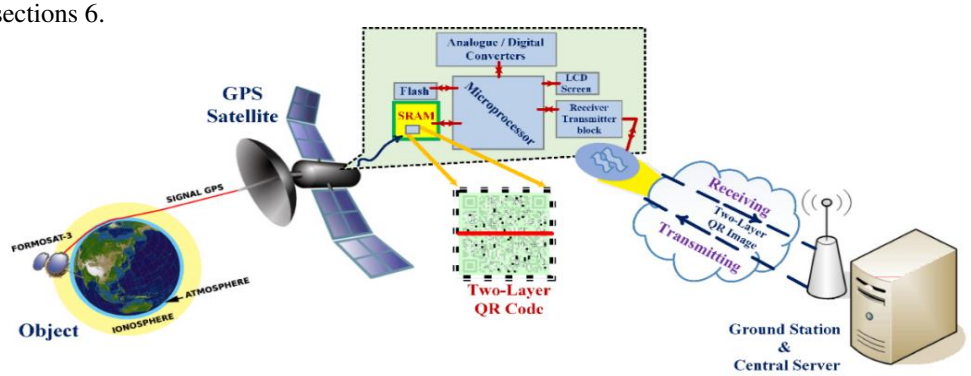



**Fig**. **1** Overview of the system for sending information based on two-layer QR code by GPS satellites for weather studies applications.

In the following, image processing based on two-layer QR code and satellite system applications and results comparison for other counterpart bit-cells are given in subsection 7 and finally, the paper is concluded in section 8.

## 2. The wrap-gate carbon nano-tube (CNT)-MOSFET structure

The GAA or wrap-gate MOSFET-like CNTFET (CNT-MOSFET) is one of the most efficient types of CNT-MOSFETs which provides the conditions for scaling the technology up to 10 nm and beyond due to o extraordinary electrostatic characteristics [15], where Fig. 2 shows the GAA CNT-MOSFET device structure. These features prevent the increment of the gate leakage current and the parasitic RC (which CNTs in the drain/source extension regions for N-type and P-type are heavily doped/undoped respectively and separated from silicon body by a thick dielectric material to overcome the body effect), hence the bulk terminal can be ignored with their planar counterparts and have attracted extensive attention of nano-electronics scientists as excellent platform for the nano-scale integrated circuits (ICs) and digital applications [16,17]. Single-wall CNT (SWCNT) structure with only one cylinder and wrapping vector (known as the chirality vector integer pair (*n, m*)) can be utilized either as zero-bandgap metals (when *n-m* is unequal with a multiple of 3k, (k ∈ Z, is an integer number)) or semiconductors with finite bandgap (the chirality (*n, m=0*) corresponds to a CNT with semiconducting properties). The physical gate width ($W_{gate}$) of a GAA CNT-MOSFET device can be approximated by Eq. (1) [16,17]:

$$W_{gate} \text{ (including overhangs)} = S\times(N_{CNT}-1) + d_{CNT} + W_{ov} \approx \text{Max}\,(W_{ov}, N_{CNT}\times S) \quad (1)$$

Which $N_{CNT}$ is the number of parallel CNTs under the channel, $S$ is the inter-tubes pitch, $d_{CNT}$ is the CNT diameter and $W_{ov}$ is the overhang width of the gate from the edge of the CNT array (typically 2 *Lambda* (λ) and 16 nm in this study). The $W_{gate}$ (including the overhangs) of a minimum sized CNT-MOSFET with only one nanotube in the channel ($N_{CNT}$ =1) is $d_{CNT}$ + 2×Wov = 32.84 nm. The CNT diameter ($d_{CNT}$) can be determined by the chirality or wrapping vector (n,m) of the CNT as given by Eq. (2) [16]:

$$d_{CNT}(nm) = \frac{a\sqrt{n^2+n.m+m^2}}{\pi} \approx 0.07828 \times \sqrt{n^2+n.m+m^2} \quad (2)$$

Where a is the distance between the centers of two adjacent nanotubes (i.e. lattice constant, $\sqrt{3}a_0 \approx 2.45A°$), $a_0$ is the carbon–carbon distance in the CNT structure (≈ 0.142 nm). Threshold voltage ($V_{th}$) of an N-type GAA CNT-MOSFET (GAA N-CNT-MOSFET) according to Eq. (3) with estimating $V_{th0}$ based on the half-band gap of CNT and changing the diameter of the CNTs or the flat-band voltage of the transistor can be appraised [9,16,17]:

$$qV_{th} \approx E_{gap} + \text{offset} \rightarrow V_{th} \approx E_{gap}/2q + \Delta V_{th0} + V_{fb} - \delta.V_{dsi} \approx \frac{E_{gap}}{2q} \approx \frac{0.5773aE_{\pi}}{qd_{CNT}} \approx \frac{0.4312}{d_{CNT}(nm)} \quad (3)$$

Where $E_{\pi}$ = 3.033 eVolt from the Hückel tight-binding model, $\delta$ is DIBL coefficient in CNT, $V_{fb}$ is the CNT flat-band voltage, $\Delta V_{th0}$ ($V_{th}$ roll-off) is the threshold voltage without DIBL effect and $V_{dsi}$ is the internal drain to the source voltage. The total effective gate capacitor ($C_{gate}$) for CNTFET devices with surrounding-gate structure based on three effects of parasitic effects including a) gate to gate or gate to drain/source ($C_{gtg}$), b) gate to channel ($C_{gc}$) and c) outer fringing ($C_{of}$) capacitances, with assuming only single CNT channel and therefore ignoring the screening effects (capacitor without screening effect ($C_{inf}$)) as equations (4)-(6) is expressed [18]:

$$C_{gtg} = \frac{3k_2\varepsilon_0 H_g}{L_{sd}} + \alpha_{gtg}.\frac{\pi k_2\varepsilon_0}{ln(\frac{2\pi(L_{sd}+L_g)}{2L_g+\tau_{bk}(H_g+h+r)})} \quad (4)$$

$$C_{gc.inf} = \frac{2\pi k_1\varepsilon_0}{cosh^{-1}\left(\frac{2h}{d_{CNT}}\right)+\frac{1}{3}\underbrace{\left(\frac{k_1-k_2}{k_1+k_2}\right)}_{\lambda_1}.\ln\left(\frac{2h+2d_{CNT}}{3d_{CNT}}\right)} \quad (5)$$

$$C_{of.inf} = \frac{\alpha_{of}}{3}.\frac{2\pi k_2\varepsilon_0 L_{sd}}{cosh^{-1}(\frac{2\sqrt{h^2+(0.28L_{sd})^2}}{d_{CNT}})} \quad (6)$$

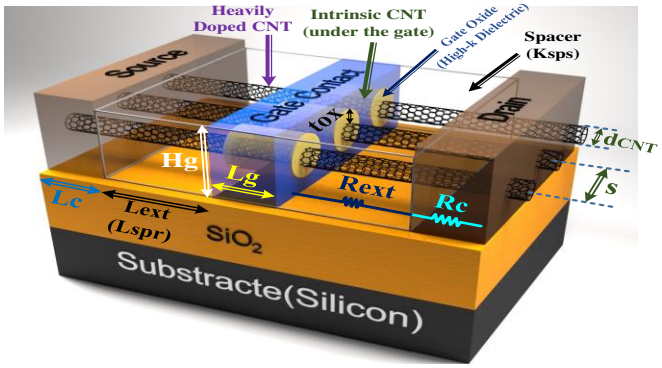



**Fig. 2** Three-dimensional (3-D) cross-sectional view of GAA CNT-MOSFET device structure.

Where $L_{sd}$ is the length between adjacent contacts, $H_g$ and $L_g$ are the height and length of the gate contact, $d_{CNT}$ and r are the diameter and radius of the CNT and $t_{ox}$ is the thickness of the dielectric layer, respectively. Also, $k_1$ and $k_2$ are the dielectric constants of the dielectric and the substrate, $\tau_{bk}$ is the factor for the effects of back plates on the $C_{gtg}$ fringe capacitance, $\alpha_{of}$ and $\alpha_{gtg}$ are fitting parameters for incorporating the screening effect of adjacent contacts, respectively and $h=r+t_{ox}$ is the height of the gate above the channel.

## 3. The proposed low-power rad-hard SE 11-T SRAM bit-cell (UPRHSE) and behavioral mechanism

Figure 3 shows the proposed GAA CNT-MOSFET technology-based GDI (GAA CNT-GDI) cell and also its 2-D/3-D chip layout, which instead of conventional Si-MOSFETs in binary basic GDI cell [10] in pull-up and pull-down network transistors from positive-type GAA CNT-MOSFET (GAA P-CNT-MOSFET) and negative-type GAA CNT-MOSFET (GAA N-CNT-MOSFET) are used, respectively. This cell is 2×1 multiplexer and contains three diffusion-terminals: G (common diffusion-terminal, i.e. the select (control) signal, which connects to gate pair of network transistors), P (the outer diffusion-node of the GAA P-CNT-MOSFET transistor), N (the outer diffusion node of the GAA N-CNT-MOSFET transistor) and the out-node (the common of both network transistors). Table 1 shows simple examples of changes in the P, N, and G terminal inputs for the configuration of the GAA CNT-GDI cell to achieve different *Boolean* functions in the output node. In cases, reduce hardware costs and power consumption in designs are important together, the basic GDI-based OR, AND, $F_1$, $F_2$ structures with no need of full swing/high drive current illustrated in Table 1, can be used. Nevertheless, if voltage restoring/driving large capacitor (high fan-out) are required, the NOR, NAND, $F_1$, and $F_2$ structures from the basic GAA CNT-GDI method-based cell structure with reverse cell (NOT gate) must be used, where their output node connect in a cascade form with GAA CNT-GDI cell based-inverter cell for guarantees sufficient drive of the cascaded arbitrarily cells and work reliably increase for any cascade circuit, where these architectures are illustrated in Table 1. Due to the fact that in the inverter cell structures the misaligned/mis-positioned CNTs do not occur [19], and because they are a special case of the GAA CNT-GDI cell, the fundamental logic functions implemented through the proposed cell structure will be very immune against to the challenge of misaligned/mis-positioned CNTs in the manufacturing phase.

The transistor/gate level schematics of proposed GAA CNT-MOSFET-based radiation-hardened (rad-hard) SE 11T-SRAM bit-cell (UPRHSE) structure by three control signal inputs show in Fig. 4. The proposed asymmetrical bit-cell has $q$ main sensitive node and pair nodes, $qb$ master or $q$ complement ($qb_m$) and also $qb$ slave ($qb_s$) (with the same logical state) as indicated in the Fig. 4, where are responsible to maintain the stored data-bit correctly in the cell structure. It should be noted that row-word line (RWL) terminal is controlled row-by-row, where column-word line (CWL) and its complement ($\overline{CWL}$) and also virtual floating ground (VirGND) terminals are controlled column-by-column. The following is a detailed description of the bit-cell structure:

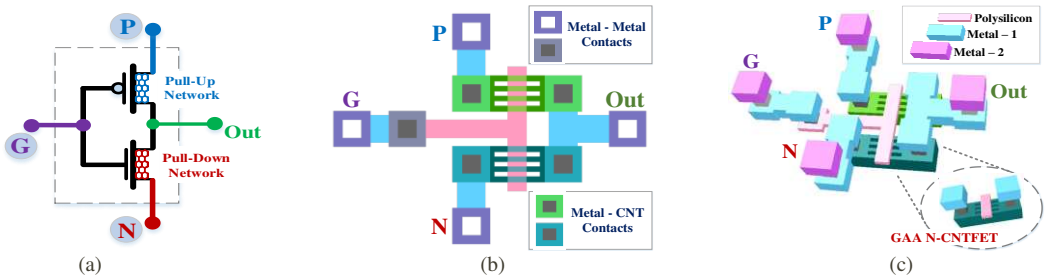



**Fig. 3** (a) Binary GAA CNT-GDI cell structure, (b) 2-D and (c) 3-D layout area view.

**Table 1** Different logic functions implemented with one/two GAA CNT-GDI cell for various configurations of inputs.

| no Full Swing output/reduce hardware and power consumption (Basis Functions) | | | | | High Drive Current and Capability of Voltage Restoring (Specific-appropriate Functions) | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Input diffusion-terminals | | | Description | | Input diffusion-terminals | | | Description | |
| P | G | N | Output | Functions | P | G | N | Output (Cascaded with NOT gate) | Functions |
| B | A | C | $(\bar{A}.B)+(A.C)$ | ***MUX*** | B | A | C | $(\bar{A}.\bar{B}+A.\bar{C})'$ | ***MUX*** |
| B | A | '1' | A + B | ***OR*** | $\bar{B}$ | A | '0' | $(\bar{A}.\bar{B})'$ | ***OR*** |
| '0' | A | B | A . B | ***AND*** | '1' | A | $\bar{B}$ | $(\bar{A}+A.\bar{B})'$ | ***AND*** |
| B | A | '0' | A . B | $F_1$ | '1' | A | B | $(\bar{A}+A.B)'$ | $F_1$ |
| '1' | A | B | A + B | $F_2$ | '0' | A | $\bar{B}$ | $(A.\bar{B})'$ | $F_2$ |

- ***Assume**: 'A' terminal (common-diffusion input), 'B' and 'C' terminals: Input binary variable signals and also '1' and '0' : High and low level logic signals.*

***Left-side inverter in the proposed bit-cell***: According to Fig. 3 (a) and Table 1, by separating the single output node in a standard inverter gate based on GAA CNT-GDI technique into two nodes (nodes *w* and *z*) and placing the transistors in the role of diodes ($PL_2$ and $NL_1$ transistors), between these nodes up to a single $qb_m$ output node, a special inverter gate with higher drive capability can be obtained as part of the data keeper in the proposed bit cell shown in Fig. 4. Also, due to the increase in the number of nodes connected to the $qb_m$ single output (four nodes in each path between nodes *w* or *z* to node $qb_m$) to the inverter gate with a higher node capacitance and less vulnerability to the effects of noise will be obtained. In the structure of this gate, $PL_1$ and $NL_2$ transistors act as pull-up and pull-down networks (PUN and PDN) on the main and $PL_2$ diode transistors (GAA P-CNTFET type) and $NL_1$ (GAA N-CNTFET type) with the approach of eliminating the speed problem of the conventional voltage restorer compared to inverters and achieving voltage with full swing are used for the $qb_m$ output node in the center of the bit-cell. According to Fig. 4, the data transfers in two stages, first the data formed in *w* and *z* nodes according to the data in *q* node and then the activation of one of the diodes according to the data in *w* and *z* nodes. Due to the fact that at the time of output data, the transistors in the PUN and PDN ($PL_1$ and $NL_2$ transistors) are activated with diode transistors in their opposite network ($PL_2$ and $NL_1$ transistors) connected to the same supply terminal, so there is no direct path between $V_{dd}$ and GND and therefore leakage current will be reduced, significantly, compared to conventional inverter structures.

***Right-side inverter in proposed bit cell***: this inverter is as another keeper part of the suggested bit-cell, comprises of two nested multiplexers (Mux.) cell ($PR_1$ and $NR_2$ transistors as external multiplexer (mux.) and $PR_2$ and $NR_1$ transistors as inner mux.) with cross-connected diffusion areas based on GAA CNT-GDI cell in a role of dynamic C-element (two input NAND gate (TAG) or guard-gate) structure, where a radiation tolerant isolation/cut off or delay network (AR transistors as a single event transients (SETs) filter) as internal connecting between either input (i.e. input signal ($qb_m$ node) and its delayed replica ($qb_s$ node) of the Mux. cell is inserted. Eventually, a positive feedback sensing series path ($PR_2$, $NR_1$ transistors) has been connected to output sensitive node of right-side inverter for data-bit retention and read-out mode. Note that due to the transmission through the drain to the source terminal of AR transistors and that GAA N-CNT-MOSFET drive voltage up to $V_{dd}$-$V_{th}$ and GAA P-CNT-MOSFET drive voltage as low as $V_{th}$, so the voltage level at the $qb_s$ secondary data storage node can be switched between $V_{th}$ and $V_{dd}$-$V_{th}$ in the gated inverter on the right-side, and the voltage level at these two nodes will be very close due to the charge sharing effect between them.Once the CWL is changed to low logic level and its complements to an opposing level, the path in the network is disconnected by series connection transistors and the output value of right-side inverter (q node) is retain unchanged. It should be noted that the write signal path to the output of the inverter is controlled by three RWL, CWL and its complement signal inputs, which these dual controls reduce the probability of output hazards (i.e. the design of the block building will be hazard-free).

### *3.1 The proposed 1×1 memory architecture and its peripherals blocks*

The main plot in Fig. 5 shows circuit level implementation of one-row/one-column (1×1) memory array structure using proposed UPRHSE bit-cell with write-assist circuitry controllable using column decoder WL (i.e. CWL signal) and chip enable/select (CE/CS) terminal and write driver and input buffer block (both CNT-GDI GAA cell-based blocks with NOT and $F_1$ functions), sense amplifier (amp.) and output buffer block based on NOT, $F_1$ and $F_2$ functions, and $F_2$ function-based control block, in less complexity structure.

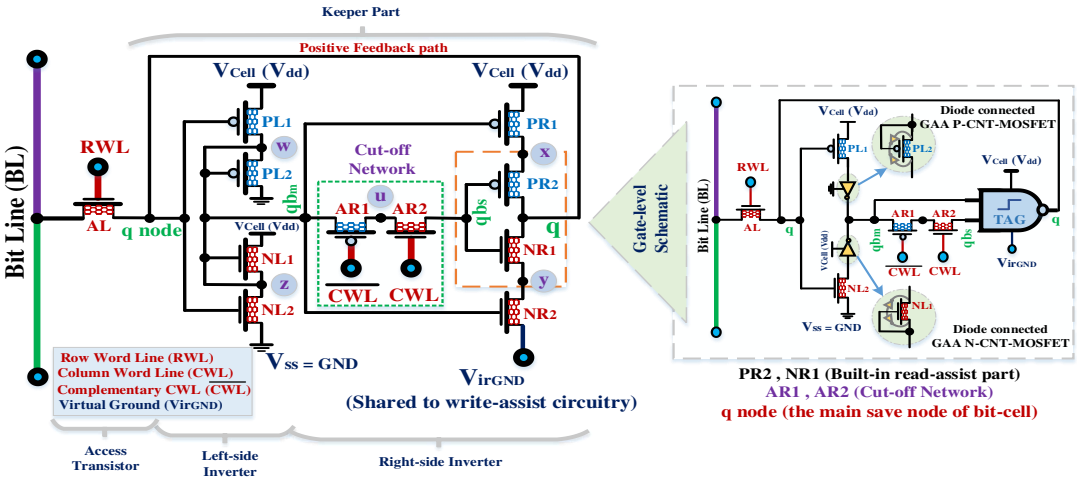



**Fig. 4** The transistor and gate levels structure of the newly proposed UPRHSE bit-cell.

Because the bit of data '1' potentially disturbs the storage process at the q sensitive node due to the write-constraint conditions caused by the same drive current in the pull-up/down network transistors ($PR_1$, $PR_2$, $NR_1$, $NR_2$), therefore, the proposed array is based on the VirGND mechanism using the write-assist circuit in the bit-cell designed to data transfer from BL into bit-cell under column control-based CWL and its complement signals in a half-select technique. The inset plot of Fig. 5, depicts the control signals setting in write, hold and read operation cycles. As shown in Fig. 5, before the write operation cycle, the data-bit line in the write driver and input buffer block ($BL_w$) through $Nw_3$ transistor in the $F_1$ function and the data-bit path in the cell (i.e. BL) through the $Pw_4$ transistor with the activation of chip enable/select (CE/CS), the write-enable (WE) and the pre-charge (Pre) signals by the control block will be pre-charged to a low logical level of '0' and float mode, respectively. In write operation mode, the data-bit is stored in the write driver and input buffer block after passing through an Np transistor for storage from the input/output port, and after passing two NOT gates based on GAA CNT-GDI cell in a full swing voltage from $Pw_3$ and $Pw_4$ transistors will be placed on BL. Simultaneously, the VirGND terminal will go to a high logic level (floating pulse) via the write-assist circuit in the proposed architecture by activating the RWL and CWL terminals using the decoders connected to them and $\overline{CWL}$ by internal write-assist circuit to complete the data-bit write cycle. In the data-bit storage cycle, the two WLs are set to a low logic level through their decoder circuits, and the VirGND and $CWL$ terminals are set to a low and high logical levels respectively, through the write-assist circuit to connect to a fix ground (GND). The AL and cut-off network are turned OFF and the bit-cell is disconnected from the BL and the data-bit in the main q node remains floating and in its previous logical state and the data-bit will be held in other sensitive nodes in the bit-cell through the positive feedback path. Finally, before starting the read cycle, the data-bit line in the sense amp. and output buffer block (BLr) is pre-charged to the logic level '0' by the control block with activated CE, read-enable (RE) and pre-charge (Pre) signals. In read operation mode, the two terminals CWL and VirGND remain at a reasonably low logical level, and only the RWL terminal returns to the high logic level, and the AL transistor will only turn ON again, BL according to the data-bit stored in the main sensitive node, the bit-cell will be charged or discharged. The data-bit enters the sense amp. and output buffer block through the $PS_4$ transistor and finally after passing through the GAA CNT-GDI cells with $F_1$, $F_2$ and NOT functions in a full swing voltage will be received in the common input/output port. According to the cause expressed for fabrication phase and since the inverter gate is a special case of GAA CNT-GDI cell with the probability of misaligned/mis-positioned problem of CNTs (short path from output to $V_{dd}$ or GND, i.e. source and drain terminal [19]), so to achieve a memory array circuit design with optimal implementation as well as high drive current and voltage restoring capability structures, body structure design of writing driver/input buffer

and sense amplifier (Amp.)/output buffer blocks in the write/read direct paths of the data-bit into the proposed bit-cell, according to the functions presented in Table 1, was performed using the $F_1$, $F_2$ and NOT functions of the CNT-GDI GAA cell based on multiple-threshold voltage technique (i.e., multi-CNT diameter/chirality design [20]). Also in the proposed memory array structure for the design of the control block, due to no direct path of input data-bit to the memory array through the structure of this block and only the need to generate a control signal for gate of transistors in writing driver/input buffer and sense amplifier (Amp.)/output buffer blocks utilizes the GAA CNT-GDI cell-based functions in no full swing output structures listed in Table 1 with a view to reducing hardware complexity as well as lower power consumption. Figure 6 shows the transient simulation results for the one-row/one-column (1×1) memory array structure based on the proposed bit-cell in Fig. 5 for non-existent state of radiation strike with the memory structure, for the '0' and '1' bit sequences for write/read mechanisms. The waveforms indicate the correct operation of the bit-cell and the authentication of complete success in write/read data-bit (at typical-typical (TT) corner process analysis).

### 3.2 The 4×4 memory mini-array architecture and its peripherals blocks based half-select method for radiation-immunity

In Fig. 7, the four-row/four-column (4×4) memory mini-array structure using the proposed UPRHSE bit-cell with common interconnection on-chip (pin-out) input/output is provided. According to the control voltage generation table presented in inset plot and that each row/column of the memory array has a common control circuit, the overall write/read mode operation of the array structure in a bit-interleaving structure with full and half-selected mechanism in order to reduce the soft errors and the effectiveness of radiation particles impact. To improve the read-stability of data-bit from bit-cells in the suggested memory array (especially when '0' is stored in the main node of the data-bit), a row/column decoder circuit based on the word-line under-drive (WLUD) scheme as read-assist technique includes a P-type pull-up transistor and two N-type pull-down transistors attached to the WLs are used for the strength of the drive in each WL, by reducing the voltage level below the WL pulses of $V_{dd}$ level at the output during the read operation [21].

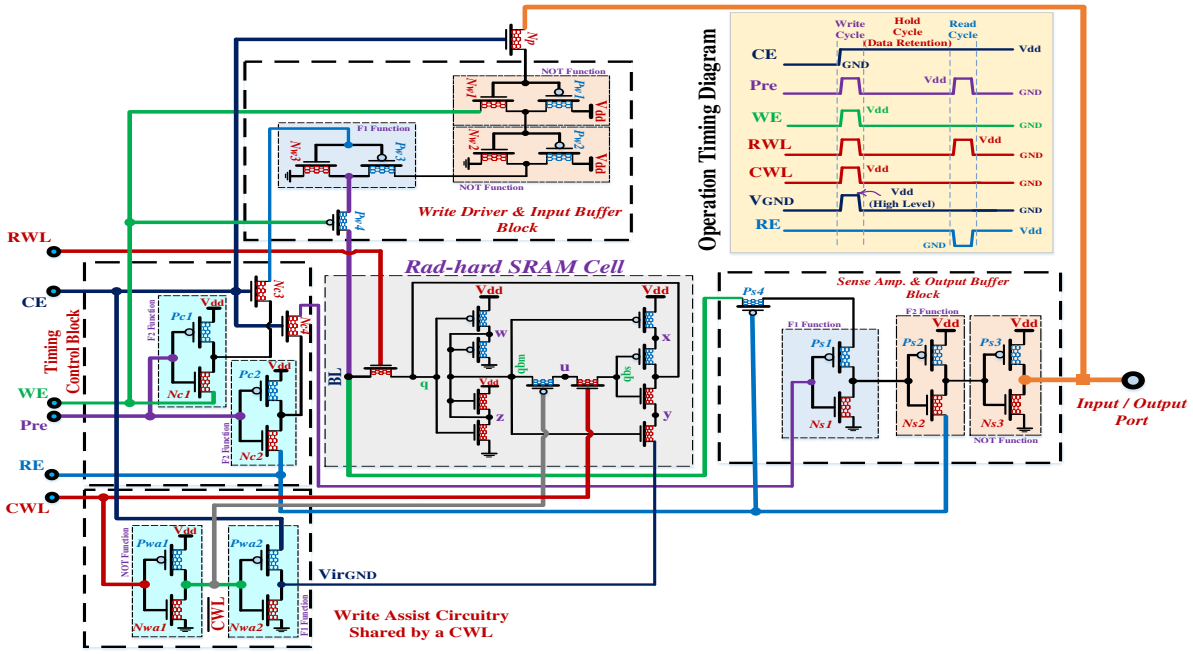



**Fig. 5** Circuit level implementation of one-row/column (1×1) memory array structure using proposed UPRHSE bit-cell and its peripherals blocks.

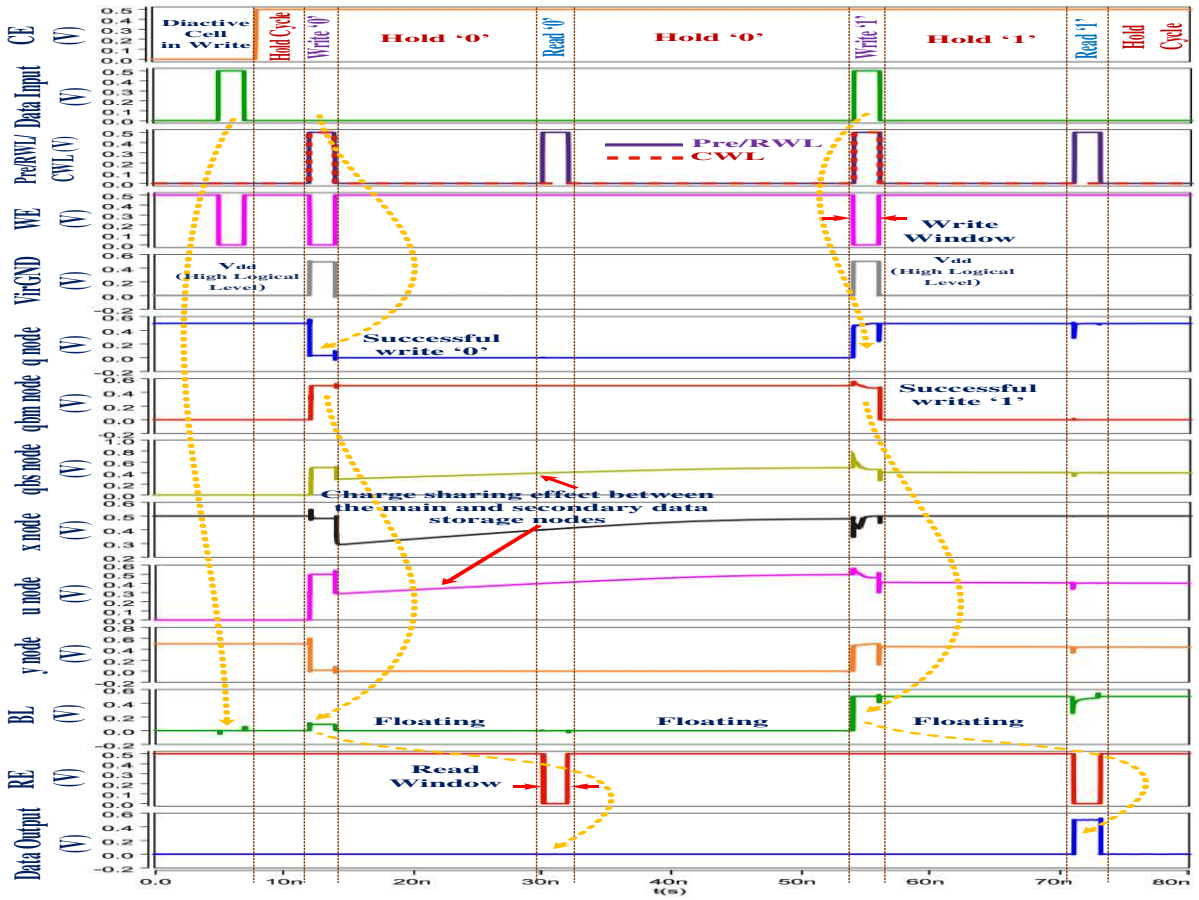



**Fig. 6** Time-domain simulation results of proposed UPRHSE bit-cell with input/output waveforms and control signals for a sequential set: Write/Read '0' and '1'.

## *4. Investigations of SET injection mechanism and error tolerance in the proposed bit-cell structure*

### *4.1 Proposed SET injection circuit model to simulate SEU and MEU in memory structure*

In the present paper, modeling and simulation of circuit-level soft errors using injection of transient pulse voltage to sensitive nodes in the target circuit to investigate the SET voltage pulse propagation and critical charge estimation (minimum charge necessary to cause a SET) has been considered. In Fig. 8, the proposed SET circuits implemented by GAA CNT-MOSFET for injecting the negative and positive SET transient waveforms based on the Ref. design [22] into a structure using the T-connected pseudo resistors (TPRs) with large resistance in *Tera ohm* (TΩ) range [23] as variable resistance switches are shown with a low distortion and linear behavior at larger values. According to Fig. 8, the value of resistance equivalent to TPR can be controlled by adjusting the voltage in the $TR_3$ through the signal amplitude of $V_c$ and in a general case can be expressed by Eq. (7):

$$R_{TPR} = TR_1 + TR_2 + (TR_1 \times TR_2)/TR_3 \tag{7}$$

The voltage pulse equation (V(t)) obtained from the proposed circuit model in H-SPICE can be expressed by Eq. (8):

$$V(t) = \begin{cases} 0; & t < t_{d1} \\ V_{Peak}\left(1 - e^{\frac{-(t-t_{d1})}{\tau_R}}\right); & t_{d1} < t < t_{d2} \\ V_{Peak}\left(e^{\frac{-(t-t_{d2})}{\tau_F}} - e^{\frac{-(t-t_{d1})}{\tau_R}}\right); & t > t_{d2} \end{cases} \tag{8}$$

Where $t_{d1}$ $t_{d2}$ are the onset of the rise and fall of the voltage, respectively, $V_{Peak}$ is the maximum voltage desired and $\tau_R$ and $\tau_F$ are the rise and fall time constants, respectively. The total charge delivered by the pulse, $Q_{Total}$, can be calculated by integrating from V(t) as given in Eq. (9):

$$Q_{Total} = V_{Peak}\left[\tau_R + \tau_F + (t_{d2} - t_{d1}) - \tau_R e^{\frac{-(t_{d2}-t_{d1})}{\tau_R}}\right] \quad (9)$$

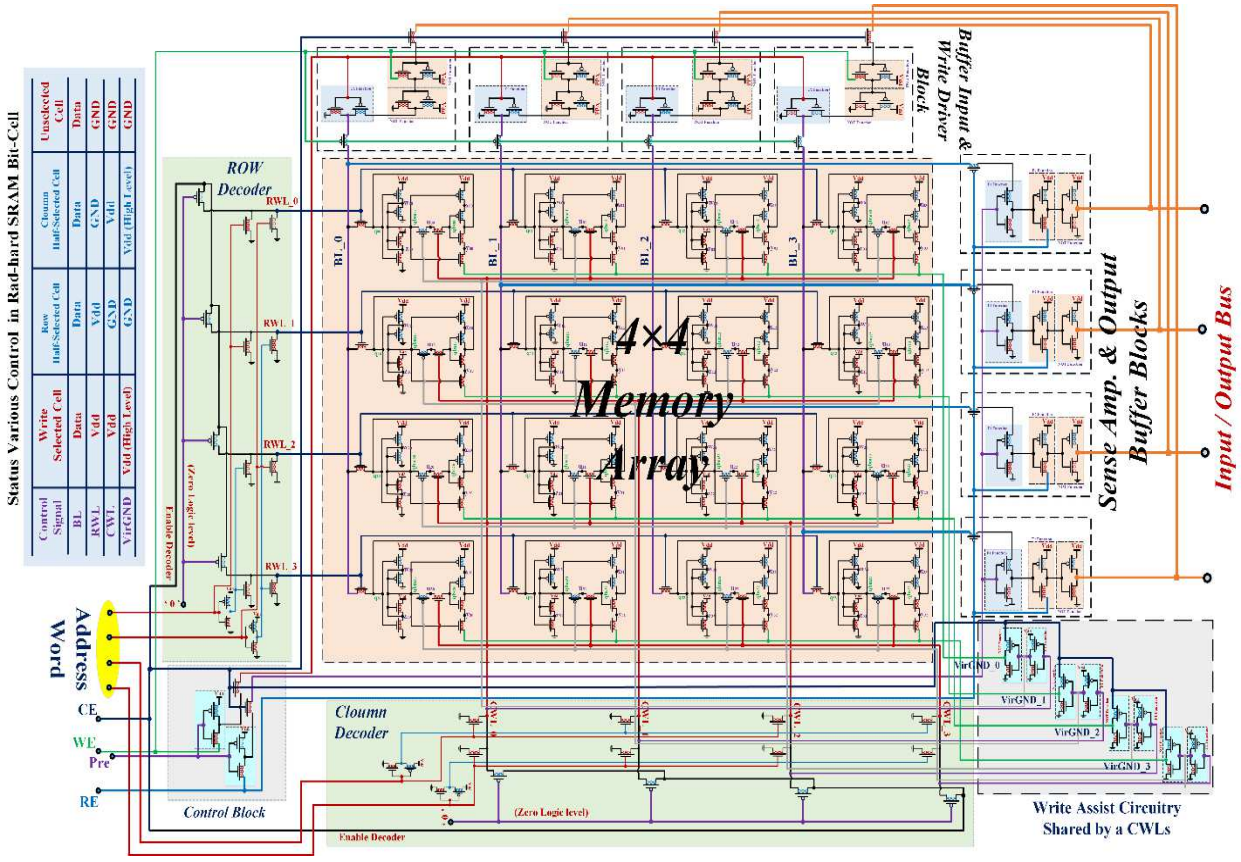



**Fig.7** The transistor level structure of 4×4 memory mini-array using proposed UPRHSE bit-cell and its peripheral blocks with status table of control signals.

Now if the $\tau_R$ parameter is small compared to the difference in time between the rising and falling edges of the double-exponential waveform ($t_{d2}$-$t_{d1}$), the last term inside the bracket is negligible and the calculation of the total charge will be simplified. In the suggested circuit model, in order to reach the amplitude and width of the SET voltage pulse, and to achieve a collected saturation charge, the diameter of the tubes in the GAA CNT-MOSFETs forming the TPR network and the duration of the applied signal ($t_c$) to $TR_3$ transistor must be calibrated, respectively. To simulate MEUs in memory structures, both proposed circuits will be used to inject both negative and positive SET transient waveforms simultaneously.

### 4.2 Evaluation of radiation robustness in the presence of single-node event upset (SEU)

Figure 9 (a) shows the failure mechanism due to the strike of particles inside the proposed SRAM bit-cell with sensitive areas of possible radiation exposure with the ability to change the data all over the structure. For this purpose, a fault injection experiment using H-SPICE simulation based on the suggested circuit of Fig. 8 to the *q* sensitive node in the proposed UPRHSE bit-cell structure has been utilized. In the proposed bit-cell structure, special inverters have been used in order to reduce the effects of radiation based on the separation scheme in the write and read data process, as well as using the cut-off network in the role of switch by creating larger node capacitance. Use of left-side inverter based on write data in a structure with separate and two-stage transistor transfer technique and right-side inverter with two-transistor chain formation as a disconnection network with the aim of preventing the propagation of both '0' → '1' and '1' → '0' due to radiation, where the GAA P-CNT-MOSFET due to its location in an N-well, acts as a potential barrier to prevent less charge propagation beyond the N-well boundaries in an encapsulate role of the GAA N-CNT-MOSFET connected to the $qb_s$ sensitive node. Figure 9 (b) indicates the proposed layout scheme for the UPRHSE cell and 6-transistors of Ref. [17] in which the transistor-transistor distance of both pairs of critical nodes is greater

than the effective range of charge sharing until the radiation particles hit to the node(s), the probability of effects on other adjacent sensitive node(s) is negligible and the substantial difference in amounts between sensitive nodes will be minimized.

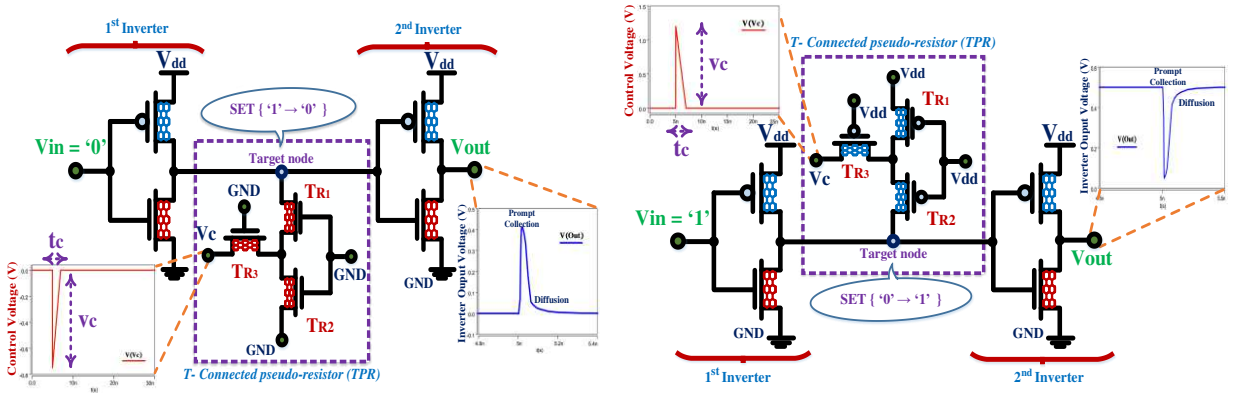



**Fig. 8** Proposed upset injection circuits based on TPRs in the production of transient glitch pulses: (a) Positive (0 → 1), (b) Negative (0 → 1) to extract SEU and MEU parameters in memory cell structures.

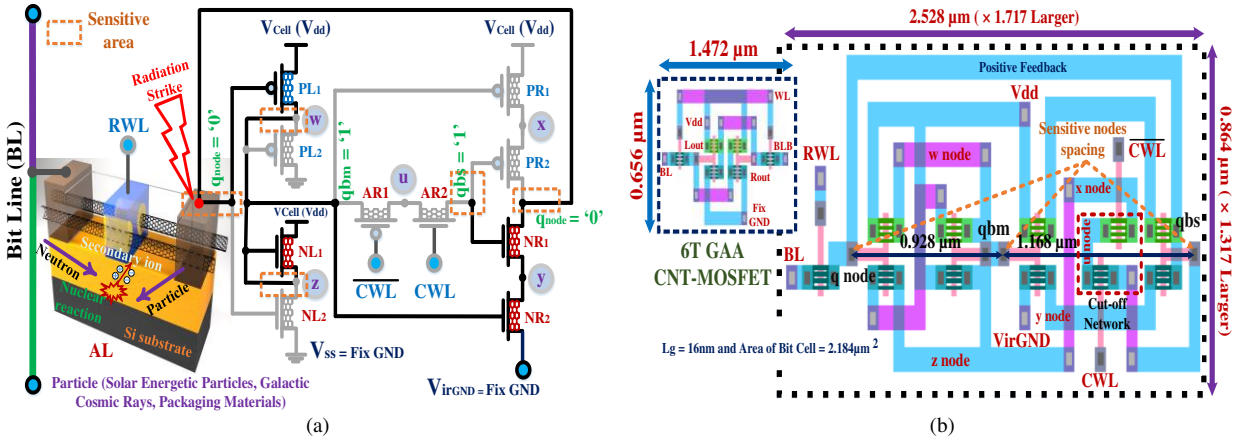



**Fig. 9** (a) The proposed UPRHSE bit cell structure in the presence of SET injection to q node in the '0' logical data retention performance cycle with a display of sensitive areas, (b) The main image of the proposed layout area and the inset image of the 6T GAA CNT-MOSFET layout [17] in 16 nm technology (total area 2.184µm$^2$)

According to Fig. 9 (b), the layout design area for the proposed bit-cell in 16 nm technology is about 2.184 µm$^2$, where the approximate consumption area is 58% µm$^2$ bigger compared to the conventional 6T SRAM bit-cell in the same technology as the GAA CNT-MOSFET.

### 4.3 Reliability assessment in the presence of multiple (double)-node event upset (MEU)

In the memory cell structure if the amount of charge injected into a main node become large enough, it can change the logic state of the main node and the consequence of a single event causing data failure in other nodes, where this amount of failure of a node to a few more nodes are determined by the critical charge in the secondary node and multi-node upset (MEU) scenarios will be formed due to the effects of charge sharing [24]. The maximum total number of node pairs in each circuit with $n$ nodes can be $\frac{n!}{2(n-2)!}$ of the selected combination, the number of effective compounds can also depend on the cell functionality and circuit structure. The process of finding a critical node pair in a memory structure by identifying the main node with the highest sensitivity and lowest critical charge ($Q_{crit}$) as the voltage of the node ($V_{node}$) multiplied by the node capacitor ($C_{node}$) based on the *command .option captab=1* in the H-SPICE simulator starts. Then the main node found with all the combinations between the other nodes will continue with it in order to identify the node pair with the most vulnerability to start the MEU simulation. After detecting the critical node pair, using the circuit-level simulation using the proposed upset injection model of H-SPICE in Fig. 8 is applied by simultaneously injecting a charge on them in order to find the critical charge curve. The point is that the node to which the main portion of the charge is injected is known as the main node, while the node that collects the remaining

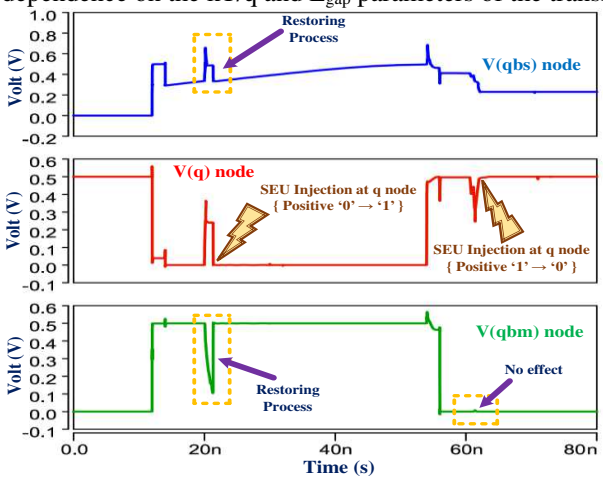
portion of the charge is known as the secondary node in order to evaluate the MEU for a memory structure. Also, by properly calibrating the resistance of the inner cut-off network structure in right-side inverter, it can be ensure that when one of the transistors fails while the cell is in standby mode, the other remains closed, resulting in a rad-hard structure with no penetration of the SEU and MEU to the other end of the disconnected network and data destruction was achieved through the positive feedback path to the main node. Also, by properly calibrating the resistance of the inner cut-off network structure in right-side inverter, it can be ensure that when one of the transistors fails while the cell is in standby mode, the other remains closed, resulting in a rad-hard structure with no penetration of the SEU and MEU to the other end of the disconnected network and data destruction was achieved through the positive feedback path to the main node. Figure 10 shows the simulation results for the SEU and MEU scenario by injecting upset into one and more nodes of the bit-cell in the 3-row and 3-column, in the proposed 4×4 memory mini-array structure of Fig. 7 using H-SPICE model schemes of TF injection to evaluate the ability and tolerance of the bit-cell structure. According to the results in the Fig.10, it can be seen that if the suggested bit-cell has SEU in any sensitive node, it can be restored to its original state without considering the upset polarity, and also has the ability to fully tolerate the MEU regardless of the stored amount of the memory cell, because in the suggested bit-cell structure, there is always one or two unaffected sensitive nodes that can recover the nodes with the flipped data-bit and from failure data completely prevented.

**5. Evaluation of data retention voltage ($V_{DR}$) based on analytical model for the proposed architectural structure**

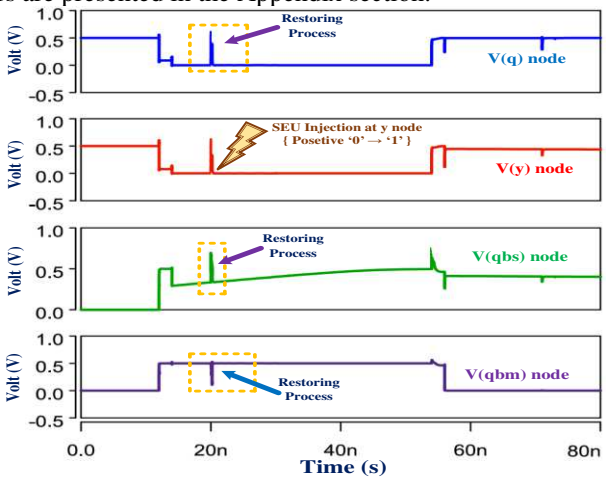
Due to the limited energy resources in natural environments with high-radiation, the design compatibility of bit-cells in a low power consumption condition with the ability to operate regularly with reliable data retention at low supply voltages and impact robustness to radiation particles for designers is challenge. The simplest and easiest approach to reduce and suppress the leakage power in standby (or hold) mode significantly in a memory cell is to reduce the nominal power supply voltage ($V_{dd}$) to the possible critical level before VTC deteriorate of internal inverters, i.e. data-retention voltage ($V_{DR}$), indicated that at higher values one bit of data will be reliably maintenance [25]. In this section, an approximate formula of the $V_{DR}$ parameter for the proposed bit-cell using the analytical model in the Ref. [26] is presented in order to investigate the effective parameters and analyze the stability of the bit-cell when $V_{dd}$ approaches the $V_{DR}$. According to the model, examining the behavior for a cell when operating under $V_{DR}$ conditions, all structure transistors in the sub-threshold voltage (sub-$V_{th}$) region are biased, and therefore, the ability to store SRAM data strongly depends on the conductivity behavior sub-threshold. The $V_{DR}$ formula under the two assumptions that the leakage current from the access transistor is very small and also all leakage currents other than sub-threshold leakage because in GAA CNT-MOSFET technology their effect will be negligible under sub-threshold bias conditions, by solving the VTC equations of cross-coupled inverter for the proposed structure (with the details provided in *Appendix*) will be obtained according to Eq. (10):

$$V_{DR} = V_{DR.intial} + \frac{\frac{4q}{kT}V_q}{H} \tag{10}$$

Where the details of the equation for the $V_{DR,intial}$ (the initial estimated value of $V_{DR)}$ and H parameters and its dependence on the kT/q and $E_{gap}$ parameters of the transistors are presented in the Appendix section.




(a)




(b)

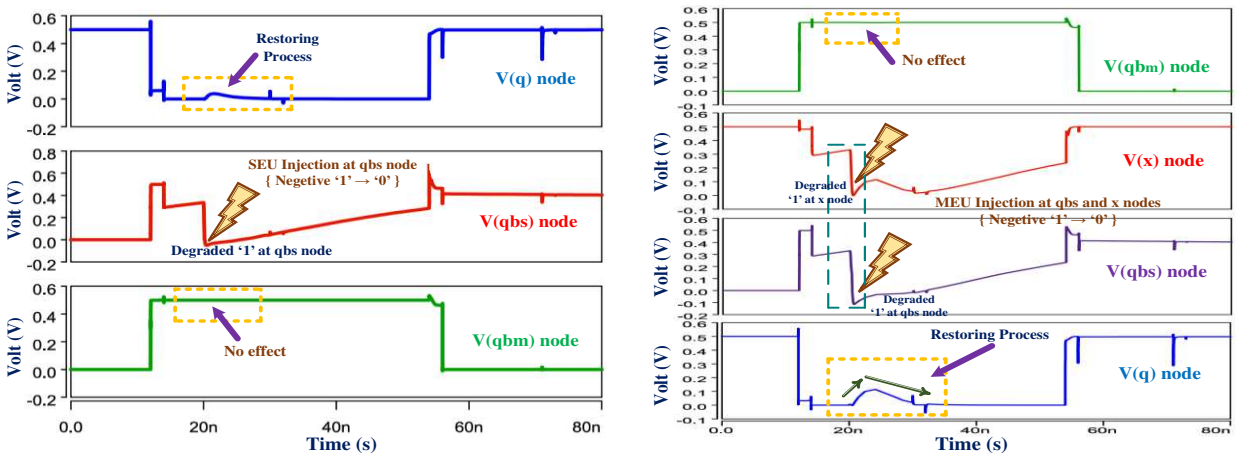



**Fig. 10** Simulated response in the presence of upset injection in single and multiple nodes with a demonstration of self-correction for the proposed bit-cell: (a) *q* node with both positive SEU (0 → 1) and negative SEU (1→0), (b) *y* node with positive SEU (0 → 1), (c) *q* node with negative SEU (1→0), (d) *x* and $qb_s$ nodes with negative MEU (1→0).

Furthermore, with $V_{DR}$ obtained, the minimum leakage current and cell total power of proposed cell in standby mode and sub-$V_{th}$ conditions are assumed that the data is in the main storage node '1' and that BL is pre-charged to a GND level. By placing the sub-threshold current equation of the CNT-MOSFETs (Eq. (A.1) in the Appendix section) they can be calculated with Eqs. (11) and (12), respectively:

$$I_{leak} = I_{PR1} + I_{PL1} + I_{NL1} \tag{11}$$

$$I_{leak} = \frac{KT}{qR_Q}\left[\left(\exp\frac{2q\left(V_{DR}-Vq_{bm}\right)-E_{gPR1}}{2KT} - \exp\frac{2q\left(V_{DR}-Vq_{bm}\right)-2aq\left(V_{DR}-V_x\right)-E_{gPR1}}{2KT}\right) + \left(\exp\frac{2q\left(V_{DR}-Vq\right)-E_{gPL1}}{2KT} - \exp\frac{2q\left(V_{DR}-Vq\right)-2aq\left(V_{DR}-Vq_{bm}\right)-E_{gPL1}}{2KT}\right) + \left(\exp\frac{-E_{gNL1}}{2KT} - \exp\frac{-2aq\left(V_{DR}-Vq_{bm}\right)-E_{gNL1}}{2KT}\right)\right] \times V_{DR}$$

$$P_{leak} = I_{leak} \times V_{DR} \tag{12}$$

One of the direct methods to determine $V_{DR}$ as the minimum standby voltage for memory array structures is to perform simulations using the desired parameter despite of high time-consuming to find the accurate value of $V_{DR}$ distribution Monte-Carlo (MC) based on a large number of samples until a desired failure probability level. Since obtaining the exact failure point of a rare event using MC simulation can be very time-consuming [27], so in this section a method for facile estimation of the $V_{DR}$ parameter is suggested. Figure 11 chart of suggested algorithm for shows the evaluation and estimation of $V_{DR}$ using thermal voltage (*KT*=26 mVolt). First, algorithm for estimating the $V_{DR}$ of a bit-cell, assuming the selection of an approximate range of minimum and maximum changes for the cell supply voltage ($V_{cell}$) (in the present paper, a range $V_{ddmin}$=0 Volt and $V_{ddmax}$ = 0.5 Volt, respectively) as well as the step of determining the average voltage between two points ($V_{ddmid}$) starts as the base value. Then, considering the temperature (T) and one of corner conditions (SS, SF, TT, FS, FF) considered in the evaluation in the H-SPICE netlist, with initial guess that the $V_{DR}$ value is in the lower $V_{ddmid}$ range, the difference (Δ) between the two points (i.e. Δ =$V_{ddmid}$-$V_{dmin}$) is replaced by $V_{cell}$. After examining the value of the hold-static noise margin (HSNM) curve by butterfly curve, if the noise margin in the curve is around 26 mVolt as the amount of failure tolerance due to thermal noise (since HSNM is less than the thermal voltage (KT = 26 mVolt) at 300 Kelvin, it can be due to changes in the bit-cell data content due to noise thermal [28]), $V_{ddmid}$ is considered as $V_{DR}$, otherwise $V_{DR}$ is limited below the value of $V_{ddmid}$ and the difference value of $V_{ddmid}$ is updated with an arbitrary coefficient of the amount of thermal voltage and until the condition is update and replaces $V_{cell}$ in the H-SPICE netlist. The HSNM test is repeated until the difference reaches about 26 mVolt, and if no $V_{DR}$ is found, the $V_{ddmid}$ and $V_{ddmax}$ difference evaluation range will continue in a similar stepwise process until the approximate $V_{DR}$ value is reached. Note that in this process, the repetition limit is $V_{ddmax}$ and if $V_{DR}$ is not achieved again in this interval, the value of $V_{ddmax}$ will be considered as the value of $V_{DR}$ and the process of the algorithm will end. Then, by updating the T values and corner conditions, the algorithm process will be repeated from the beginning for the circuit netlist.

## 6. Main challenges: Simulation results, comparative analysis and discussion

### 6.1 Setup for simulation

In this paper, MATLAB and *synopsys* HSPICE tools with computational time-efficient compact SPICE semi-empirical VS CNT-MOSFET and quasi-ballistic *Stanford* (S)-CNT-MOSFET models for the GAA CNT-MOSFET device [29], and PTM model for high-performance silicon (Si)-based MOSFET nano-device [30] incorporating *high-k/metal* gate and stress effect at the same physical gate length ($L_g$ = 16nm feature size) are used. Also, simulation conditions at a nominal power supply (0.5 Volt) and room temperature (25°C) are adjusted. The characteristics of the input structure parameters related to the designs based on other GAA CNT-MOSFET and Si-MOSFET devices and can be defined by the user with the range of values used for them and brief descriptions are listed in Table 2. It is worthwhile to mention that all well-known counterpart heterogeneous and asymmetrical bit-cells designs [31, 32] and Ref. [33] (typical CNTFET technology-based redesigned and optimized) with the same number of transistors compared in this paper have been redesigned in 16 nm technology to achieve a fair and realistic evaluation between them and the proposed design. In this section, according to the Ref. [34], since there is a 99% probability that over 80% of all possible component values that can occur correctly for a circuit in a function will be obtained by 30 iterations, so static and transient and *Monte-Carlo* (MC) analysis in the present paper, for more accurate results, the number of iterations is estimated to be 300 iterations (10 times more than the usual assumption) and also variations under various processes such as $d_{CNT}$ in the range of 1 to 2 nm and $V_{dd}$ with ± 20% Volt compared to its original values in the presence of *Gaussian distribution* with +/-10% variations at the at +/- 3 *sigma* (σ) failure probability level or standard deviation (Std. Dev.) are considered.

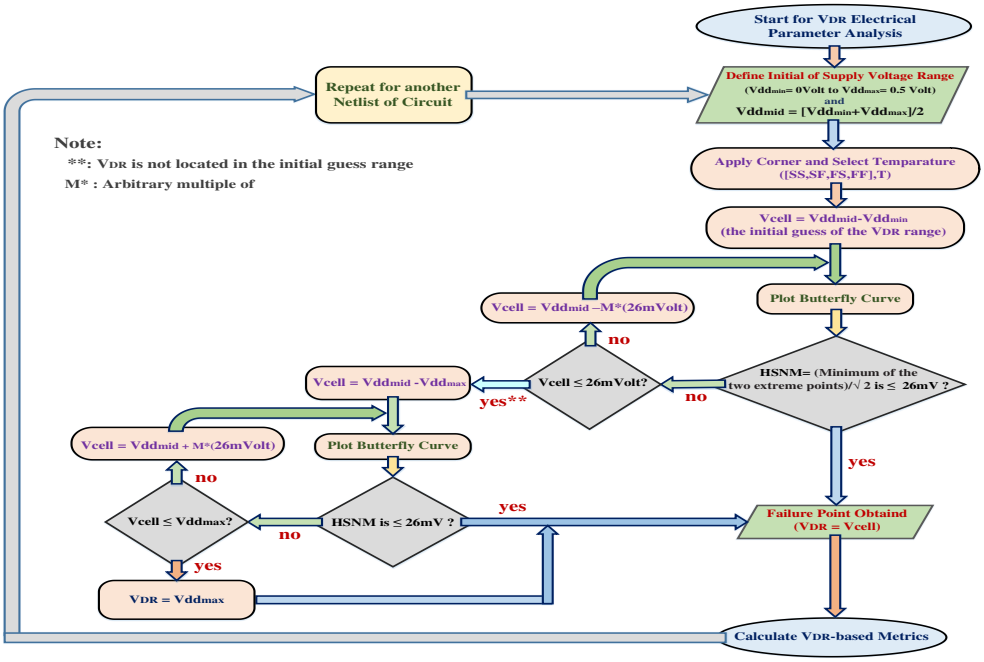
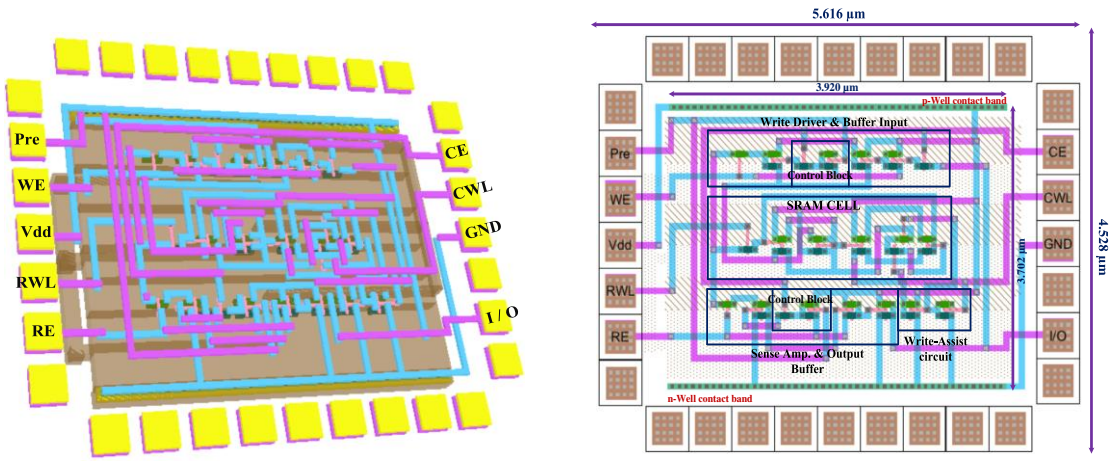



**Fig. 11** The proposed general block diagram for facile evaluation and estimation of the $V_{DR}$ parameter.




(a) (b)

**Fig.12** physical layout views of 1×1 memory array structure: (a) 3-D, and (b) 2-D, based on the proposed UPRHSE bit-cell placed in a ring pad.

**Table 2** The important SPICE process parameters of the GAA CNT-MOSFET and Si-MOSFET devices for simulations.

| Technology | Variable Parameters | Brief Description | Values |
|---|---|---|---|
| GAA CNT-MOSFET | $L_c$ | *Source / Drain Contact Length* | 16 nm |
| | $d_{CNT}$ | *CNT Diameter* | ~ |
| | $Vfb_{n,p}$ | *Flat Band Voltage* | +/- 0.015V |
| | $S$ | *CNT-to-CNT Center Space (Sublithographic Pitch)* | 4 nm |
| | $L_{spr}$ | *Source/Drain Spacer Region* | 3 nm |
| | $K_{sub}$ & $k_{spa}$ , $k_{CNT}$ | *Substrate & Drain/Source Spacer , Nanotube Dielectric Constant* | 3.9 , 1 |
| | $T_{ox}$ | *Gate Oxide Thickness* | 4 nm |
| | $H_g$ | *Gate Height* | 20 nm |
| Si-MOSFET | $Wn,Wp$ | *N-type, P-type transistor widths* | 16 nm , 48nm |
| | $Vth_0$ $n,p$ | *Threshold voltage (N-type , P-Type MOS devices)* | 0.47965 V , -0.43121 V |
| | $Tox$ | *Gate Oxide Thickness* | 0.95 nm |

- Physical gate length ($L_g$) = 16nm, Nominal power supply = 0.5Volt, and room Temperature = 25 ºC for different technologies. ~ :Variable parameter (Various in design)

## 6.2 The layout chip area estimation of proposed SRAM bit-cell

Figures 12 and 13 depict the 2-D and 3-D chip layouts view for two memory arrays based on proposed UPRHSE bit-cell in the standard cell form using the *CAD electric-VLSI Design* tool with the *mocmos-cn* technology library [35], where the minimum feature size i.e. half of the physical gate length (λ)-based rules (2λ) in a 16 nm feature size for achieving the optimum power consumption is considered. In order to estimate the area of the two samples of the memory array, the occupied area in terms of λ × λ is shown in Figures. As shown in Figures 13 and 14, the physical chip layout size of the one-row/one-column (1×1) and four-row/four-column (4×4) memories is about 25 µm$^2$ and 144 µm$^2$, respectively. Considering the use of design method with bit-interleaved architecture and also the use of GAA CNT-GDI method in order to eliminate the complexity of peripheral blocks in the memory array, it is observed that the size of the proposed memory arrays based on the proposed bit-cell has a low occupation level.

### *6.3 Read-stability and write-ability static noise margins (SNMs) analyzes for other SRAM bit-cells*

Read-stability and write-ability margins for bit-cells due to the progressive increase in intra-die variability and cell voltage scaling ($V_{cell}$) have been a major concern in nano-regime technologies for designers. Static noise margins (SNMs) in different write, hole (retention) an read cycles can be used as metric for evaluating the ability/stability of bit-cells in different operational modes based on the margin of change in values of BL, WLs and VirGND terminals. The results of MC analysis of read-static noise margin (RSNM), hold (standby)-static noise margin (HSNM) and write-static noise margin (WSNM) parameters with setup measurement schematics to evaluate the parameters presented in main and insert plots in Fig. 14 for the proposed SE bit-cell, in the presence of a scope variation of 1 nm to 2 nm for $d_{CNT}$ and $V_{dd}$ under +/- 20% variation range of the nominal voltage ($V_{dd}$ = 0.5 Volt). Also, the amount of changes (Δ) in the edges and around flipping points in the VTC curves resulting from the impact MC simulation with the curves in a performance mode is shown for a more accurate evaluation for the nominal parameters mentioned in the figures as dotted lines. As demonstrated in Figures 14, the SNM curves in the proposed bit-cell circuit are quite less sensitive in the presence of parametric changes and have very steep transition regions, and appropriate noise margin where and when even the $V_{cell}$ decreases from the nominal value (i.e. half of $V_{dd}$ = 0.25 Volt) can still perform well without disturb in write/retention/read modes. Next, evaluation of the other RSNM, HSNM and WSNM

parameters in the worst-case corner process: fast-fast (FF) = 0.65 Volt / 0 ° C, typical-typical (TT) or nominal-nominal = 0.5 Volt / 25 ° C, slow-slow (SS) = 0.4 Volt / 80 ° C, for other rad-hard bit-cells in different technologies in various structures with the same number of transistors as well as the conventional 6T structure has been performed, the results for these parameters are shown in Fig. 15 (a)-(c).

According to the results presented in the Figure (a)-(c), it can be seen that the suggested bit-cell based on GAA CNT-MOSFET technology regarding the other SNM parameters has the higher values in the different corner conditions than other SRAM architectures, where the proposed rad-hard bit-cell structure demonstrates 1.974×, 1.159× WSNM and HSNM variability in the SS-corner than the TT-corner respectively, and 1.208× RSNM variability at TT-Corner than FF-Corner. Also, Figure 15 (d) - (f) shows the mean (μ) and sigma (σ) related to other SNMs for rad-hard bit-cells in the presence of TT-corner process by MC simulation with a sample of 300 iterations in 16 nm technology node. The lower the value of variability (σ/μ) the higher the robust behavior of circuit against the variations. According to the curves in the figure, except for the bit-cells of Ref. [17] and [32], which are in a much worst position than other bit-cells, the two bit-cells of Ref. [31] and [33] are not very far apart in terms of (σ/μ) ratio and the difference between the proposed bit-cell as the best design and the worst in the WSNM, HSNM and RSNM modes is about 1.9×, 1.88× and 2.41×, respectively. In conclusion, the higher write-ability and also improved write/retention/read variability (σ/μ) make the suggested rad-hard bit-cell robust and a preferred choice than other bit-cell structures.

### *6.4 Evaluation of write/read access times and FoM metrics for other rad-hard bit-cells*

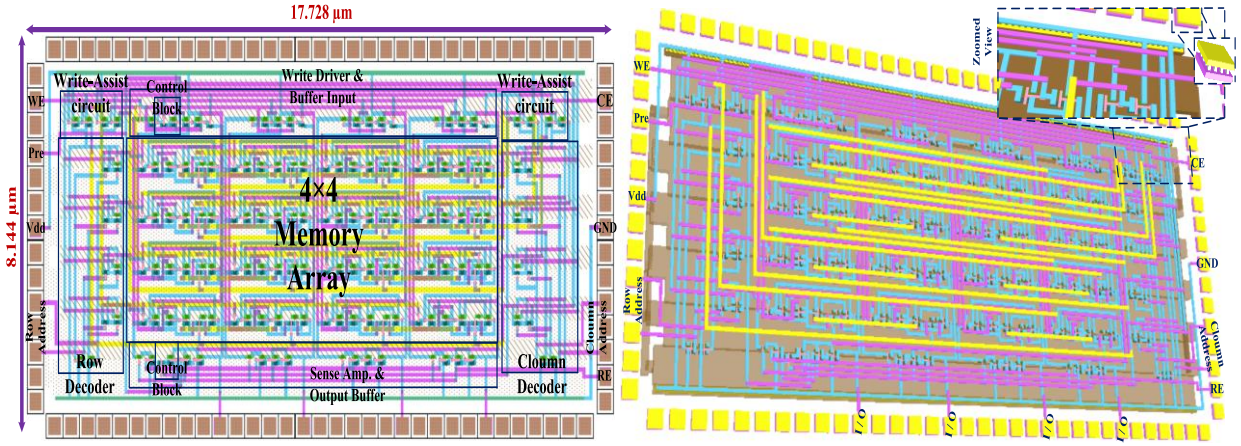
To comprehensively evaluate the performance of SRAM bit-cell structures, two figure of merit (FoM) have been used by considering other important metric based on the fundamental parameters: stability, area, PDP and yield in order to evaluate the overall quality and relative superiority of the structures over each other. According to the tradeoff that exists among the various metrics for evaluating the performance of bit-cells, the comprehensive electrical quality metric (EQM) suggested in Ref. [36] can be used to evaluate the overall quality of a cell, which can be defined as follows:

$$EQM = \frac{Read\ SNM \times Hold\ SNM \times WVM}{R_{AT} \times P_{leak} \times P_{read} \times P_{write} \times Array\_area} \tag{13}$$

Where the RSNM and WVM parameters are the metrics for read-stability and worst-case (narrowest) voltage margin for transferring '0' and '1' into the SRAM bit-cell in mVolt, respectively, HSNM is the hold (retention) SNM of bit-cell in mVolt, $R_{AT}$ is the read access time in nSec., $P_{leak}$ is the average leakage power consumption in pWatt, $P_{write}$ and $P_{read}$ are the average power consumption of the bit-cell during read and write operation in nWatt, respectively. Array_area metric in $\mu m^2$ is the bit-cell chip area normalized to the 6T GAA CNT-MOSFET bit-cell. For a comprehensive evaluation of the stability and leakage power in the structure of SRAM cells, in Ref. [37] a metric consisting of yields, static power and normalized area is introduced as equation (14):

$$YSNA(\sigma/W) = \frac{\frac{\mu}{\sigma}Hold\ SNM \times \frac{\mu}{\sigma}Read\ SNM \times \frac{\mu}{\sigma}Write\ SNM}{P_{Leak} \times Normalized\_Area} \tag{14}$$

Where yield metric by dividing the mean of a parameter by its standard deviation and the target yield is at least six-sigma (6σ) (i.e. failure point ($P_{fail}$)=$10^{-9}$) or larger is required to have a sufficiently stable operation [28]. The write-ability yield ($\frac{\mu}{\sigma}Write\ SNM$), hold stability yield ($\frac{\mu}{\sigma}Hold\ SNM$) and read-stability yield ($\frac{\mu}{\sigma}Read\ SNM$) have been obtained from the normal distribution with 300 iteration samples of MC-HSPICE simulation. A higher magnitude for this comprehensive FoM indicates better performance for a cell structure.



(a) (b)

**Fig. 13** physical layout views of 4×4 memory array structure: (a) 2-D, and (b) 3-D, based on the suggested bit-cell placed in a ring pad.

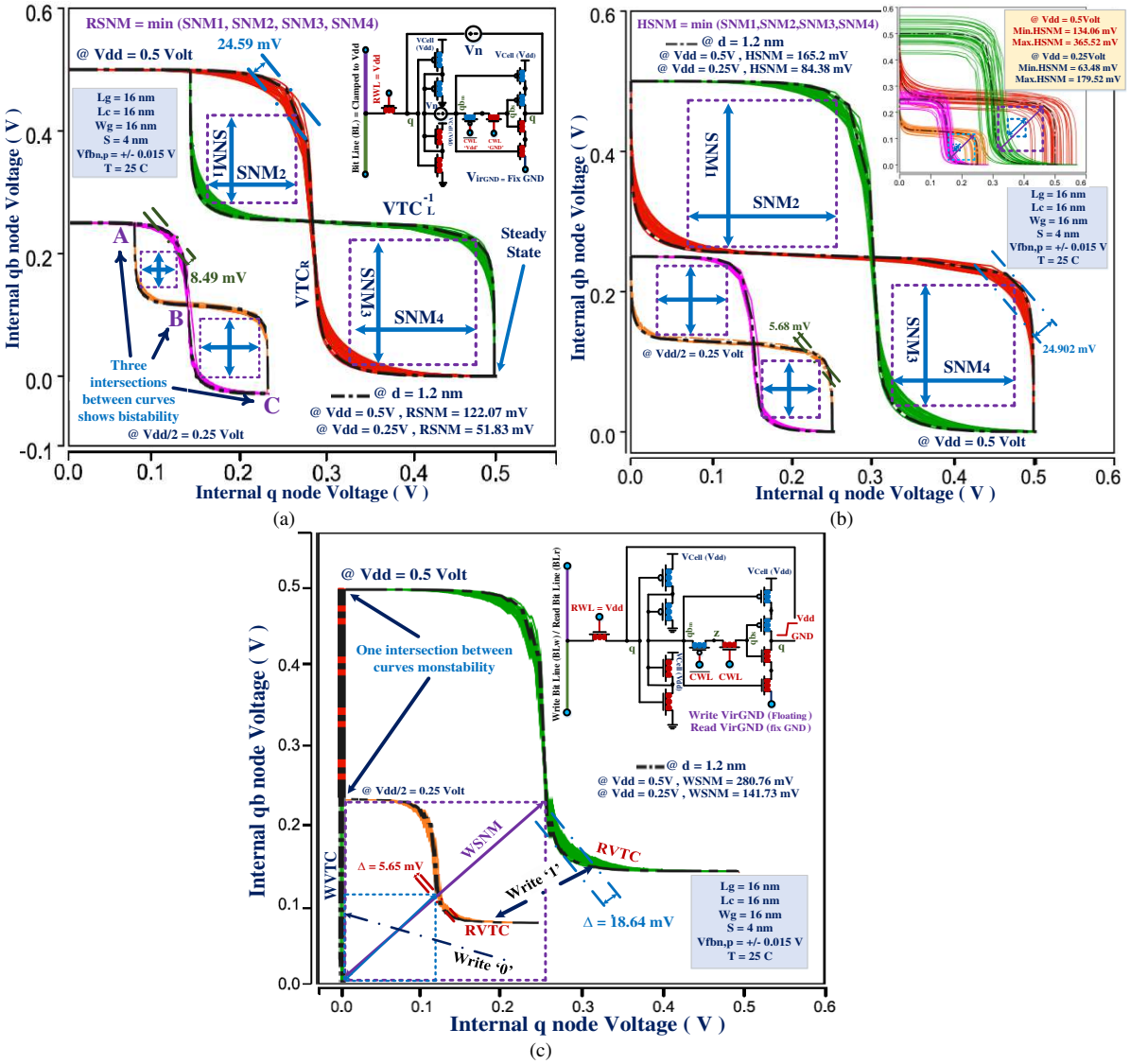



**Fig**. **14** The results of the MC DC analyses for SNMs of proposed bit-cell: (a) Read (restore) SNM eye diagram, (b) Hold (retention) SNM and (c) Write SNM (blend of write-VTC (WVTC) and read-VTC (RVTC) curves).

The EQM and YSNA plots in the presence of supply voltage changes from 0.25 Volt to 0.65 Volt as the main factor in determining the metrics for other bit-cell designs at an ambient temperature (T=25 °C) are evaluated and the results shown in Fig. 16. The performance of other schemes in the plots is improved by lowering the supply voltage, where the proposed cell optimally presents the EQM and YSNA in the test supply voltage range. According to the EQM and YSNA plots, the proposed bit-cell as a sample is about 6.4% and 5.8% higher than the structures based on Si-MOSFET and usual CNTFET technologies node in the Ref.s [31] and [33] at 0.5 Voltage, respectively, where the proposed bit-cell and Ref. [33] with a yield of more than 6-sigma can robust in the design of sub-threshold voltages.

## 6.5 Evaluation of comprehensive parameters for $V_{DR}$-based bit cells

The $V_{DR}$ or the critical $V_{dd}$, represents the minimum operating supply voltage at which a bit-cell can still preserve its bit-data, introduced as an evaluation criterion of SRAM bit-cell in low voltage designs [26-28] to be able to move the designs near or sub-$V_{DR}$ to reduce power consumption. The effectiveness of temperature variations on SRAM stability in terms of $V_{DR}$ process in the presence of other TT, SS, SF, FS, FF corner conditions using the proposed algorithm in Fig. 11 and also based on MC for proposed cell structure and other counterpart bit-cells are evaluated. The spider/web chart of $V_{DR}$ parameter analysis in the presence of different corner conditions are presented in Fig. 17 for

other cells. The six axes/legs of the graph represent the six different corners while the individual thread/line represents value of temperatures.

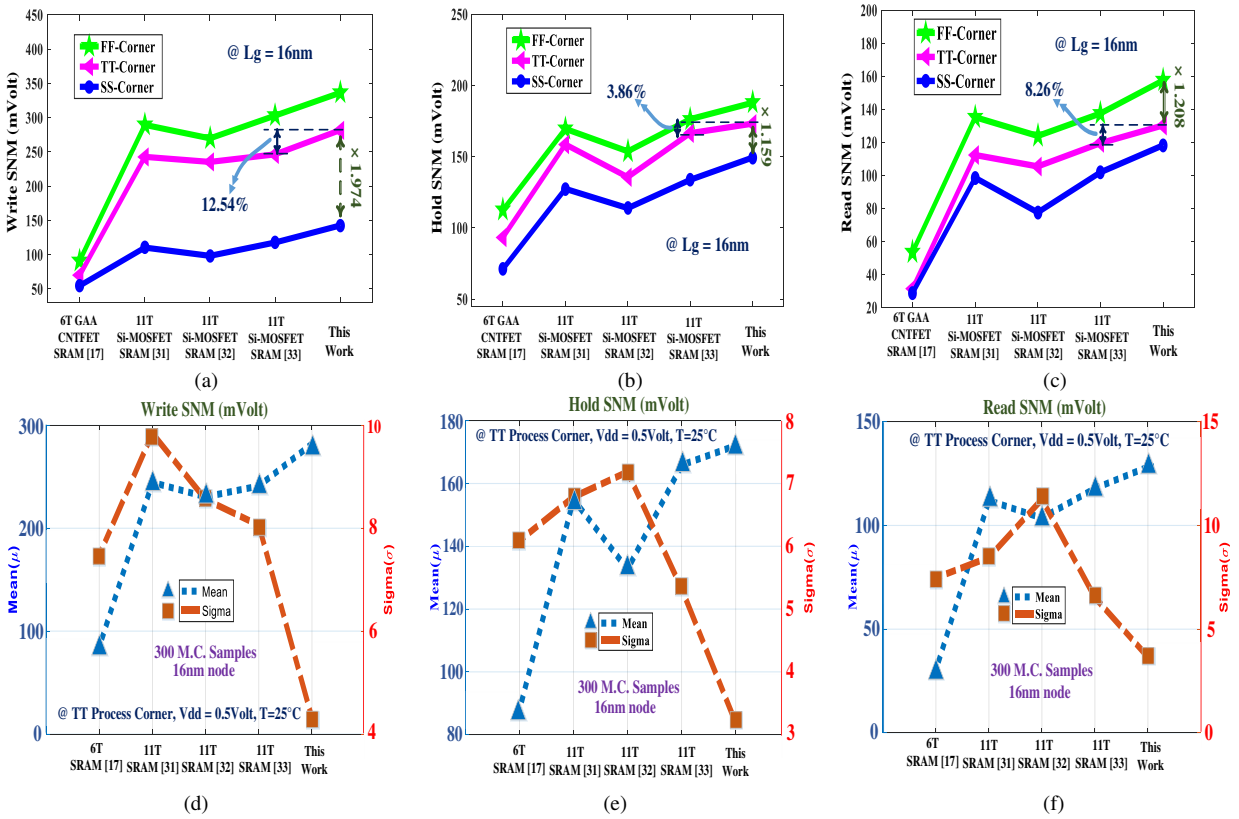



**Fig. 15** Results of the various metrics: (a) WSNM, (b) HSNM and (c) RSNM, (d) mean and sigma (at mVolt) of other SNMs for bit-cells in the presence of different corner processes.

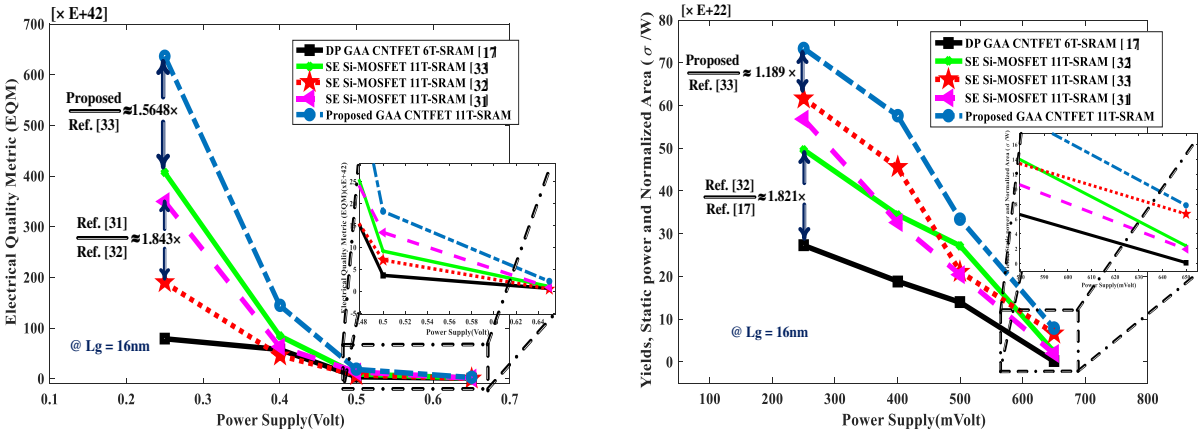



**Fig. 16.** The FoM metrics: (a) EQM and (b) YSNA for other bit-cells simulated under the same conditions.

As the obtained results reveal, it can be concluded that $V_{DR}$ increases with temperature for TT, FF, slow-fast (SF) (0.4 Volt /0°C) and fast-slow (FS) (0.65 Volt / 80 °C) in all structures based on Si-MOSFET technology node, while decreases for the FS and SS corners, where due to the high thermal conductivity (stability) of carbon atoms in CNT-MOSFETs [38], the $V_{DR}$ metric for the suggested bit-cell and 6T CNT-MOSFET are less sensitive to the temperature variation process than other state-of-the art counterpart bit-cells. Finally, the distance of the worst result for VDR in the presence of temperature changes in the TT corner based on the algorithm and MC from the simulation for cell [32] in Fig.17 (b) and the proposed cell is about 3 and 5.5%. This percentage difference indicates the robustness of the algorithm in extracting results close to the more accurate results of the MC simulation process. Due to the large effect

of the reduction in the supply voltage of a bit-cell on its correct performance and in order to show the robustness of a design in the implementation even in the presence of scaling problem, bit-cells can be evaluated based on other important parameters at the $V_{DR}$ operating point. Comprehensive FoM criterion in Ref. [28] by defining the three-variable $V_{ddmin}$ point, in order to evaluate the bit-cell based on the performance of static margins in other cycles in a critical condition (i.e. minimum HSNM and RSNM values equal to 26 mVolt, because the static noise margin falls sub-thermal voltage may be corrupted of data-bit due to thermal noise ($kT$ =26mVolt at T=300 Kelvin) and also WNM with positive values (which the easier data are written into the bit cell)) to express the capability of a bit-cell at a minimum supply voltage ($V_{dd,min}$) from MC simulation , which is defined by Eq. (15):

*Tri-variate* $V_{dd,min}$ = Max. [$V_{dd,min}$ (@RSNM ≥ 26 mVolt), $V_{dd,min}$ (@HSNM ≥ 26 mVolt), $V_{dd,min}$ (@WNM ≥ 0 Volt)] (15)

Smaller values for this FoM indicate greater savings in leakage power and therefore lower overall energy consumption at a higher operating stability for a bit-cell. On the other hand, in modern technologies, by reducing the supply voltage in bit-cells, the correct state of data write performance in an unintelligible margin is very important, and by scaling the supply voltage, the speed of failure in write will increase. Hence, a FoM criterion as the write-error rate (WER) introduced in the Ref. [39] based on transient analysis in MC simulation conditions in a number of iterations, has been used to evaluate the ability to write data in a bit-cell, which as Eq. (16) can be defined:

*WER = [Number of write failures] / [Number of simulations*] (16)

Where in the present paper, the evaluation of this FoM has been done in the presence of the $V_{dd,min}$ for other designs. Table 3 compares the results between the structural topologies and capabilities of each architecture, along with examining the performance of other basic parameters such as power consumption, static margins, and two basic parameter-based FoMs in the presence of a voltage drop limit at the power supply terminal for other bit-cells by providing comparative values for the consumption area parameter relative to the GAA CNT-MOSFET 6T-SRAM cell [17]. According to the attained results, the proposed bit-cell is relatively less in a structure with hardware complexity, where the consumption layout area is lower than other bit-cells compared to 6T SRAM bit-cell and only about 1.4× higher, which will provide the ability to design memory arrays with a higher capacity at a lower consumption layout area. As shown in Table 3, the proposed cell has less power dissipation in $V_{DR}$ conditions than its stat-of-the art counterparts with the same number of transistors due to the unique characteristics of GAA CNT-MOSFET technology. Also, in terms of static margin parameters, it has better performance due to its ability versus further reduction of the supply voltage terminal, where the limiting parameter is RSNM. Therefore, in terms of evaluation parameter, the proposed cell has the lowest value and therefore more energy storage. In this case, the worst result for the counterpart bit-cell based on Si-MOSFET technology in the Ref. [33] is about 321 mVolt, which indicates the weakness of this design in the face of the problem of voltage scaling. The results of MC simulation at a number of 300 iterations in the WER metric extraction indicate the destructive performance in write data-bit in the cell at the lowest value for the proposed bit-cell due to its unique structure and the highest value for the counterpart design in the Ref. [32] based on Si-MOSFET technology. Finally, with an overview of the comparative results of the structural and functional parameters based on $V_{DR}$ conditions for other bit-cells in the Table 3, it can be seen that the proposed bit-cell with very good potential in saving energy for implementation of memory arrays is a promising candidate for use in specific applications in natural environments with limited energy compared to other counterparts suggested in [17, 31-33].

### 6.6 Investigation of parameters based on SEU and MEU along with other FoMs for rad-hard bit-cells

The reliability of rad-hard memory cells is one of the most important concerns in safety-space applications, as they must maintain research data with full accuracy in radiation environments. For this reason, in this part of the paper, some of the parameters for evaluating the reliability and tolerability of SEU and SMU based on limitations in the design of a bit-cell architecture such as leakage power consumption, recovery delay and sensitive area in memory circuits will be evaluated. In this regard, the upset model proposed in section 5.1 is used by injecting transient fault (TF) to all nodes in a structure, to examine and compare other parameters for cells. Table 4 shows the evaluation of other essential parameters regarding the SEU topic for rad-hard bit-cells. It is indicated that the proposed UPRHSE bit-cell in the presence of an operation with a better recovery time of the upset node, in contrast to injecting charge into the drain nodes of OFF state transistor, in maintaining the amount of charge deposited by considering the average values of '0' and '1' holding cases in the nodes with the highest sensitivity and the possibility of logical data flip in the node by one SEU compared to other counterpart cells with the same number of transistors and dimensions of the same technology. Whereas the structure of the bit-cells in the Ref. [17] in comparison with the suggested structure has a $Q_{Cmin}$ (minimum collected charge needed to trigger an upset of the original logic state of a sensitive node) of about 3.4%. For nanoscale technologies, a shorter distance between nodes significantly lead to the diffusion and distribution of charge in the bit-cell design from the hit node to adjacent nodes and the voltage change in the drain/source regions of the transistors. Therefore, evaluating the amount of sensitive area in a cell arrangement can also lead to examining the robustness of a radiation cell design. On the other hand, regarding the soft error robustness of a cell, it is mainly

based on the $Q_{Cmin}$ parameter as well as $P_s$ (probability of SEU effect on the sensitive node of a circuit) and can be defined by Eq. (17) [40]:

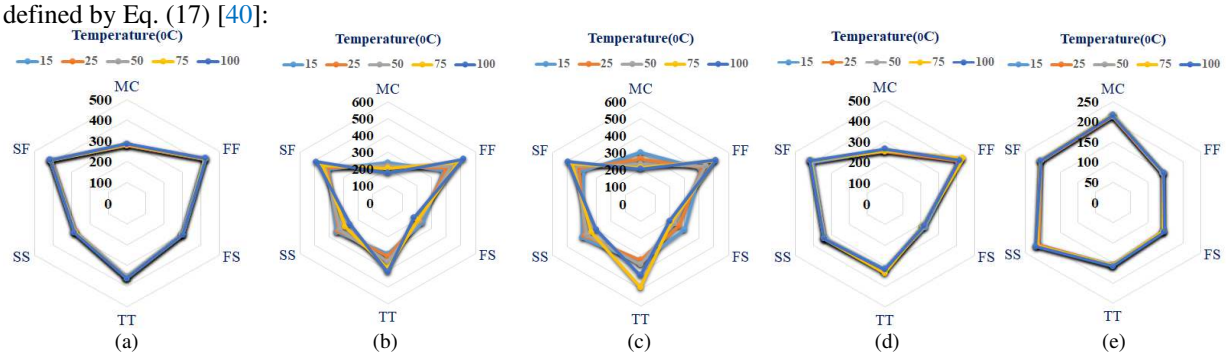



**Fig. 17** Spider/web chart of $V_{DR}$ changes in the presence of different process temperature changes and corner conditions using the proposed algorithm and MC.

$$\textit{Probability sensitive}\ (P_s) = A_{si} / A_{cell\ (total)} \tag{17}$$

Where $A_{Si}$ is the sensitive area for the drain junction of OFF transistor at *i* node on one level of the memory cell and $A_{cell}$ is the total layout area of the cell design, which for the proposed memory cell is the most sensitive area for the other nodes in Fig. 9 (a). The smaller the $P_S$ parameter value, the less the probability a memory cell is to be affected by TF. As shown in Table 4, the proposed bit-cell had the lowest probability of being affected by an SEU, while the 11T bit-cell in Ref. [32] had the highest susceptibility property among other well-known counterpart schemes. The recovery time from peak voltage to 0.5 V level with 1fC (femto-coulomb) deposition on the vulnerable node is measured, which according to the results for this parameter, the proposed cell with a unique structure based on the properties of GAA CN-MOSFET has a much lower value. Although the 6T GAA CNT-MOSFET architecture has the smallest layout cell and sensitivity area among other bit-cells, with a lower $Q_{Cmin}$ parameter, it is still with high probability to be affected by TF. On the other hand, the ratio for the probability of data failure caused by TF for a cellular structure in order to assess the robust of memory cells can be expressed based on Eq. (18) [40]:

$$Failure\ Probability = \frac{Number\ Of\ flips\ (Failure\ number)}{Toltal\ number\ of\ trials} \tag{18}$$

Where the probability of failure in the present paper has been investigated in the presence of MC simulation under iteration of 300 runs for other memory cells, the results are presented in Table 4. Based on the results presented in Table 4, it is confirmed that the proposed memory cell can tolerate the impact of the SEU and recover its condition to its original normal state faster than other cells. The operational supply voltage, critical charge and cell layout area are three important, interdependent and challenging aspects in the design of rad-hard SRAM cells. In Ref. [41], considering these three metrics, a combined criterion as the critical charge to power-delay product ratio (CPDR) with coulomb per joule (C/J) unit is suggested for comprehensive evaluation of rad-hard memory architectures. Since the layout of a cell design is very important in the charge sharing/collection in the node and its sharing, so by adding the area parameter in the CPDR metric, a more comprehensive metric of critical charge to power-delay-area (PDAP) ratio (CPDAR) is introduced, which can be defined as Eq. (19):

$$CPDAR(C/J) = \frac{Sharing\ Critical\ Charge}{PDAP} = \frac{Q_{Crit}}{P \times D \times A(Normalized\ to\ 6T)} \tag{19}$$

The $Q_{crit}$ parameter represents the critical charge, and the two P and D parameters represent the power dissipation and total delay, and A is normalized area to GAA 6T CNT-MOSFET cell, respectively, where for a rad-hard design the CPDR parameter should be as high as possible. Figure 19 shows the CPDR values obtained for other memory cells at different supply voltages. According to Fig. 18, it can be seen that the CPDR parameter for the proposed cell has higher values at different supply voltages, indicating better cell performance in the presence of challenging parameters in rad-hard and safe designs than other designs under the same simulation conditions. In this section, the results of simulating the tolerance of other MEU-based cells by identifying the most vulnerable critical node pairs and applying TF by the upset injection circuits proposed in Fig. 8 will be presented. According to the layout of suggested bit-cell in Fig. 9 (b), although the *q* main node with the lowest charge to $qb_m$ is closer to $qb_s$, but the critical charge of the $qb_m$ node is 7 fC and above the 5 fC at $qb_s$ node and hence $qb_s$ node considered as a secondary node. In order to evaluate the tolerance of each design in the presence of PVT variation in the node pairs, the critical node pairs curve was extracted from each design at a supply voltage of 0.5 Volt as shown in Fig. 18 (b). In the figure, the area under the larger curve is related to the design being stronger than the SMU, and if a charge pair is placed under the curve, the

presence of PVT changes will affect its hardening capability to tolerate a SMU impact. In order to have a quantitative analysis of the reliability of each rad-hard bit-cell, the *A* (3.5fC, 2fC) and *B* (3.5fC, 2fC) points (the first number indicates the charge on the primary node, while the second number indicates the charge on secondary node) in Fig. 18 (b) is due to its close proximity to the cross of the curves, as points for MC simulation in the presence of 300 iteration sample and 5% Gaussian distribution with variation at the ±3-sigma level based on the charge injected into the node using the proposed model in Fig. 8. The results presented in Table 4 confirm the significant reliability of the proposed design in the presence of node pairs with charge distribution, whereas the reliability of the other architectures in charge pair in (*B*) point and design in Ref. [17] in the charge pair of the (*A*) and (*B*) points will be completely fail and the logical values stored in them will be affected. Also, the results of the ratio of the number of tests that the cell withstands multi-node discomfort to the total tests (referred to probability of failure) confirms the SMU at the sample points for the suggested bit-cell in the presence of PVT changes.

## 7. Applications: Image processing

One of the most effective methods in evaluating the effectiveness of digital blocks is their application in real applications such as image processing [42, 43]. With the increasing demand in this field, extensive studies have been done so far and image storage in bit-cells based on different methods such as approximate data storage structure [44,45], bit-data encoding/decoding algorithm [46] and lookup table (LUT) [47]. As a result of these algorithms, the process of store and read the data-bits of an image will be associated with a high probability of the distance between the results obtained in the simulation phase and the hardware implementation phase.

### 7.1 Preliminaries to the structure of two-layer quick response (2LQR) code

Two-level or layer QR (2LQR) codes have been introduced to combine and store two messages in a code structure and so far in a type for specific applications that requires a specialized reader [48] and a more flexible type that requires a standard QR code reader [14]. Two-layer QR codes with the ability to display messages of arbitrary length in two valid and standard QR codes when scanning from two different directions, can be used to encrypt the data transmission in order not to destroy the information stored in the use of systems around the earth such as GPS satellites in the presence of the destructive signal effects of radiation traveling through the atmosphere on the earth's surface is very efficient. This type of code is designed in a special structure consisting of a top and a bottom layer, so that the bottom layer of black and white modules is the same as the module structure in standard single layer QR (1LQR) codes and the top layer consists of a similar number of modules that some modules are transparent. There is space between the two layers in the structure of this type of code, which will allow the formation and decoding of information in two standard one-layer QRs separately in a changing angle in scanning a two-layer QR code [14]. Figure 19 shows the structure of an example of a two-layer QR (2LQR). The bottom layer is designed in a modular structure with N×N dimensions and like the single-layer QR, each white and black module in the bottom layer is representative for 0 and 1, respectively, where the top layer has a module (N+1) × N and with N+1 and N dimensions are in the direction of the *x* and *y* axes, respectively, each of its modules may be white (0), black (1), or transparent (t) (Note that in a standard QR code with version 5 would be N = 37). The structures of the top and bottom layers are aligned and symmetrical along the y-axis, where the two layers are placed along the x-axis with an offset spacing half the width of a module. When viewed from the specific angle along the left side of the two-layer QR, the intended offset between the top and bottom layers will change to exactly 0. Similarly, when viewed at a two-layer QR in a specific direction to the right side, the predicted offset will change to exactly 1 [14].

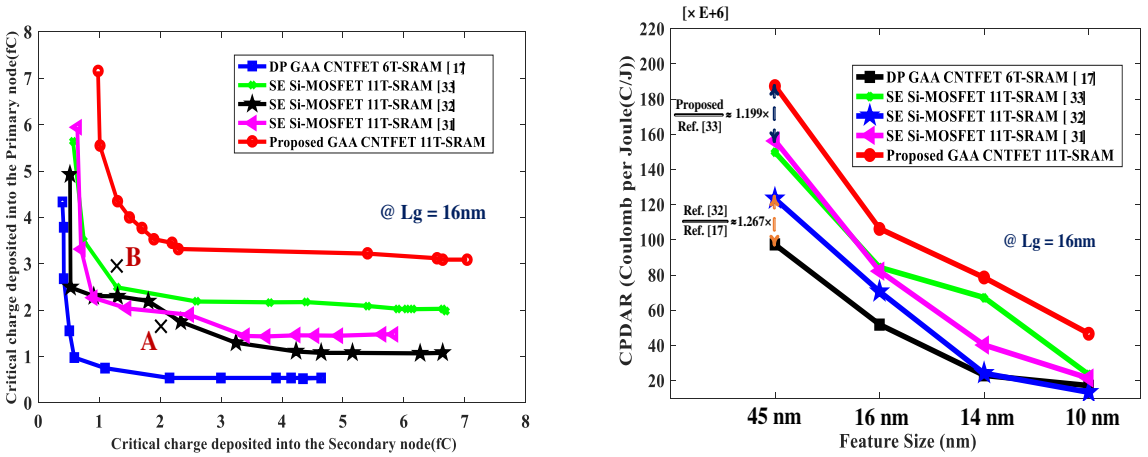
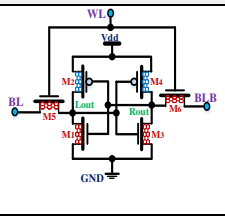
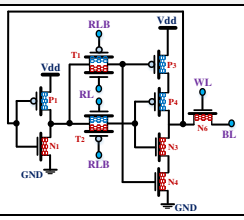
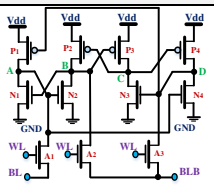
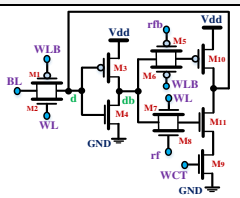
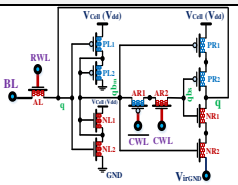



**Fig. 18** (a) Critical charge plot in the MEU scenario, (b) CPDAR values in the SEU scenario for other rad-hard bit cells.

### *7.2 Proposed image processing mechanism based on 2LQR code*

In this part, a mechanism to trial a real application for the suggested UPRHSE cell-based memory array regarding the storage of images with research content by GPS satellites using two-layer QR code in order to send with minimal impact from the effects of radiation passing through the atmosphere on the earth's surface is suggested. Figure 20 shows the general framework of the implementation process mechanism of the proposed algorithm for storing images separately in odd and even columns in the suggested memory array structure with transistors based on GAA CNT-MOSFET libraries.

**Table 3** Evaluate the structure of other bit-cells and compare their basic parameters under $V_{DR}$ operating conditions.

| Feature / Performance Metrics | Rad-hard Bit-cell Topologies (at Lg and Wg = 16 nm, T=25 ºC) | | | | |
|---|---|---|---|---|---|
| | 6T-SRAM [17] | 11T-SRAM [33] | 11T-SRAM [32] | 11T- SRAM [31] | This work (11T-SRAM) |
| Design Technology | *GAA CNT-MOSFET* | CNTFET | *Si-MOSFET* | | *GAA CNT-MOSFET* |
| Bit-cell structure |  |  |  |  |  |
| Writing / Reading path | Diff./ Diff. | SE./ SE. | Diff./ Diff. | SE./ SE. | SE./ SE. |
| Control Signals (CLs) | 2-W/R BL | 1-WWL<br>2-RWL | 3-WWL | 3-WWL<br>2-RWL | 2-WWL<br>1-RWL<br>1- VirGND |
| # No. CLs | One | Three | Three | Five | Four |
| No. of N-Type Transistor in Write/ Read paths | Two/Two | One/One | Two/Two | One/One | One/One |
| Bit-interleaving | No | Yes | No | Yes | Yes |
| Absolute Area ($\mu m^2$) (at Normalized to Ref.[17]) | 1.472 | 2.235 (×1.51) | 2.314 (×1.57) | 3.543 (×2.4) | 2.184 (×1.48) |
| Energy Consumption (ps.aJ) @$V_{ddmin}$ | 0.206 | 1.43 | 2.53 | 1.65 | 0.232 |
| WNM (mV) @ $V_{ddmin}$ | 251.34 | 264.09 | 277.94 | 235.66 | 143.72 |
| HSNM (mV) @ $V_{ddmin}$ | 232.39 | 308.74 | 227.23 | 321.43 | 122.81 |
| RSNM (mV) @ $V_{ddmin}$ | 322.58 | 225.33 | 284.55 | 257.92 | 228.84 |
| Tri-variate @$V_{ddmin}$ | 322.58 (RSNM) | 308.74 (HSNM) | 284.55 (RSNM) | 321.43 (HSNM) | 228.84 (RSNM) |

| | | | | | |
|---|---|---|---|---|---|
| **WER ( at 300 iterations)** | 29 (9.66 % failure) | 37 (12.33% failure) | 77 (25.66 % failure) | 49 (16.33 % failure) | 0 (No failure) |

- **SE.**: Single-Ended, **Diff.**: Differential, **BL**: Bit-line, **WWL**: Write word-line, **RWL**: Read word-line, **VirGND**: Virtual ground floating node.

**Table 4** Comparison of the effectiveness of SEU between the proposed cell and other cells in terms of nominal supply voltage and room temperature.

| Rad-hard Memory Cell | Number of Sensitive Nodes | Number of Sensitive Node Pairs | $Q_{crit}$ (min) (fC) (at q node) | Ps | Recovery Time (ns) (at 1fC) | # of tolerated trials (at A: Q1= 2fC, Q2= 1.8 fC) / (at B: Q1= 1.1 fC, Q2= 3 fC) | Failure Probability |
|---|---|---|---|---|---|---|---|
| **6T-SRAM [17]** | 2 | 4 | 3.4 | 0.02 | 10.22 | 243/300 | 81 % |
| | | | | | | 300/300 | 100 % |
| **11T-SRAM [31]** | 3 | 3 | 5.1 | 0.03 | 15.32 | 300/300 | 100 % |
| | | | | | | 148/300 | 49.3 % |
| **11T-SRAM [32]** | 4 | 6 | 3.7 | 0.11 | 20.44 | 300/300 | 100 % |
| | | | | | | 203/300 | 67.6 % |
| **11T-SRAM [33]** | 3 | 3 | 4.4 | 0.05 | 18.61 | 300/300 | 100 % |
| | | | | | | 182/300 | 60.6 % |
| **This work (11T-SRAM)** | 3 | 3 | 6.7 | 0.04 | 6.33 | 0/300 | 0 % |
| | | | | | | 0/300 | 0 % |

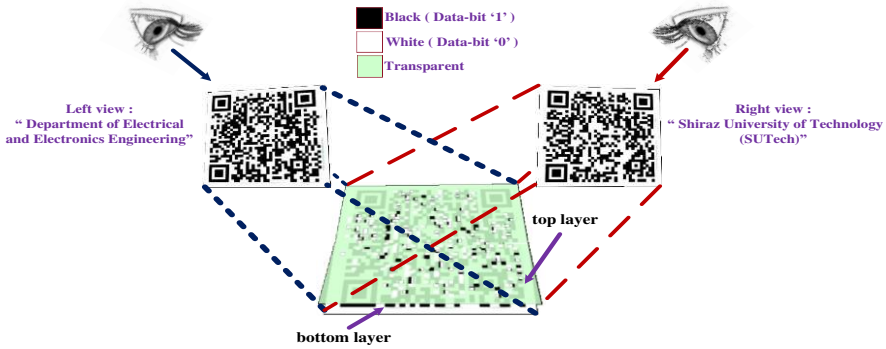



**Fig. 19** A sample of a 2LQR code with appears of a standard 1LQR with data string contents of "*Department of Electrical and Electronics Engineering*" from the left view and appears of a standard 1LQR with different data string contents of "*Shiraz University of Technology (SUTech)*" from the right view.

In order to implement this mechanism, a combination and link is created between the *synopsys* H-SPICE and MATLAB simulators are needed to provide a natural space environment close to the real evaluation for hardware implementation. Note that according to Fig. 20, it is possible to store pixel-by-pixel images directly by equivalent voltage levels for each pixel in a voltage range between GND and cell supply voltage as a new mechanism in engaging the transistor-level which provides a real trial. The steps of the proposed mechanism of Fig. 20 are described below:

- **First level**: This basic level consists of three important main parts. In the first step, the RGB (red-green-blue) background color image with information from a natural environment is received by GPS satellite as input for bit-cell storage in the form of two-layer QR storage, and then images of views left and right extracted in binary model format with the high capability of decoding [49], based on the two-layer QR codes algorithm to binary images in sizes equal to 256×256 (where a binary image according to the color intensity in level values between 0 and 255 (representing dark-black and light-white) are converted to 65536 pixels by functions in MATLAB software. In Fig. 20, in the first level, the standard single-layer QR images of left and right views extracted from the two-layer QR codes algorithm with a histogram diagram based on pixel intensity and pixel value of the image (where the horizontal axis stands for 0 to 255 and the vertical axis pixels) in the presence of selecting the parameter, the usual Q error correction level, i.e. nearly 25%, the ability to recover damaged information and the maximum levels of $L_{max.1}$ and $L_{max.2}$ are shown. In the next step, which is the most important step at this level, in order to convert the pixel data in the binary image into their equivalent values of voltage as input to the circuit in H-SPICE tool, pulse signal generation method based on piece-wise linear (PWL) signals function has been used in H-SPICE software. At the end of the first level of the suggested mechanism, the voltage signal as input based on pixels of left and right QR images will be ready to be applied to BL terminals for single and even row cells in the proposed memory array, respectively, for storage in the array structure.

- **Two level**: At this level, we will now have a reverse execution procedure compared to the first level by simultaneously re-running the two H-SPICE and MATLAB tools and sharing the results with them. The stored voltage signals resulting from the execution of the netlist in the H-SPICE tool environment for sensitive nodes $q$, $qb_m$ and $qb_s$ are printed separately as a matrix with *m-rows* in *one-column* in file with *lis.* suffix as the output of the simulation. Then, by re-linking to MATLAB software, the numerical voltage data for sensitive nodes are returned to a matrix by data proposed by a proposed return function to data with an equivalent number of pixels of the same size (256×256). Finally, the resulting matrix can be displayed as output images stored in each sensitive node by image processing commands in MATLAB software and the evaluation of image quality parameters can be done.

### 7.3 Estimate the quality of stored images and performance evaluation parameters for bit-cells

In order to calculate the peak signal-to-noise ratio (PSNR) metric, which is widely used as the most common parameter in calculating the accuracy and evaluation of performance/quality of image, the mean squared error (MSE) parameter must first be measured based on the pixel difference between the QR code binary image as a reference and the distortion binary image in the presence of radiation noise with shape based on Fig. 8 from the bit cell structure [50]. The relation for the PSNR metric can be expressed by Eq. (20):

$$PSNR\ (Quality) = 20\ log_{10}\left(\frac{MAX_f}{MSE}\right) = 20\ log_{10}\left(\frac{MAX_f}{\frac{1}{m\times n}\sum_{i=0}^{m-1}\sum_{j=0}^{n-1}\underbrace{[I(i.j)-K(i.j)]^2}_{pixel}}\right) \quad (20)$$

Where $m$ and $n$ are image dimensions (with $m \times n$ pixels), I (i, j) and K (i, j) express the pixel values of the noise-free images (original) and the noisy approximation obtained from similar results, respectively. Where the $MAX_f$ parameter indicates the maximum possible pixel value ($2^{2n}$ for the images with n-bit pixels). The mean structural similarity index measure (Mean SSIM) parameter based on the SSIM index is expressed between two windows: $x$ (one window on the distortion-free (reference) image) and $y$ (one window on the distorted image) which includes three components: luminance comparison $l(x, y)$, contrast comparison $c(x, y)$ and structural similarity $s(x, y)$, according to Eq. (21):

$$\text{Mean SSIM}\ (\text{x.y}) = \frac{1}{M}\sum_{j=1}^{M} SSIM(x_j.y_j) = \frac{1}{M}\sum_{j=1}^{M}\frac{(2\mu_x.\mu_y+C_1)(2\sigma_{xy}+C_2)}{(\mu_x{}^2+\mu_y{}^2+C_1)(\sigma_x{}^2+\sigma_y{}^2+C_2)} \quad (23)$$

Where X and Y are the noisy-free (or reference) and distorted images, respectively, the parameters $\mu_X$, $\mu_Y$, $\sigma_X$, $\sigma_Y$, and $\sigma_{XY}$ are the mean, standard deviations, and cross-correlations for the X and Y images, respectively. Also, $C_1$, $C_2$ and $C_3$ values, $K_1 \ll 1$ and $K_2 \ll 1$ are small positive constants, and the L parameter will be the dynamic range of pixel values and typically 255. To provide an realizable sense of the quality of QR code-based binary images stored in the proposed bit-cell, other RGB images to two layer QR code-based binary images contains research information sent from GPS satellites prepared as input for application to the circuit, as well as saved images read with no difference in the structure of the QR code, from the two sensitive nodes in the proposed cell structure along with the presentation of PSNR and MSSIM parameters for them are shown in Table 5 for four test image samples. Note that according to the results of the Table, considering the images of binary QR code as input, it is expected that the output images are also be completely binary with pixel values of '0' and '1'. In other words, the voltage of the storage nodes must be exactly in the values equal to GND and the cell supply voltage, while due to the trial conditions in a real platform, threshold voltage ($V_{th}$) circuit transistors cause voltage levels in a margin of difference between the maximum and minimum voltage values and finally the output images are seen on a slightly gray background. The results of the PSNR parameters in decibels (dBs) and MSSIM presented in the Table 5 for the two test images are the result of the average of these parameters in three consecutive executions per image. For example, according to the Table, the resulting PSNR and MSSIM values the sensitive nodes for the "*weather"* test image were (40.944, 39.865, 40.586) and (0.9970, 0.9954, 0.9969), respectively.

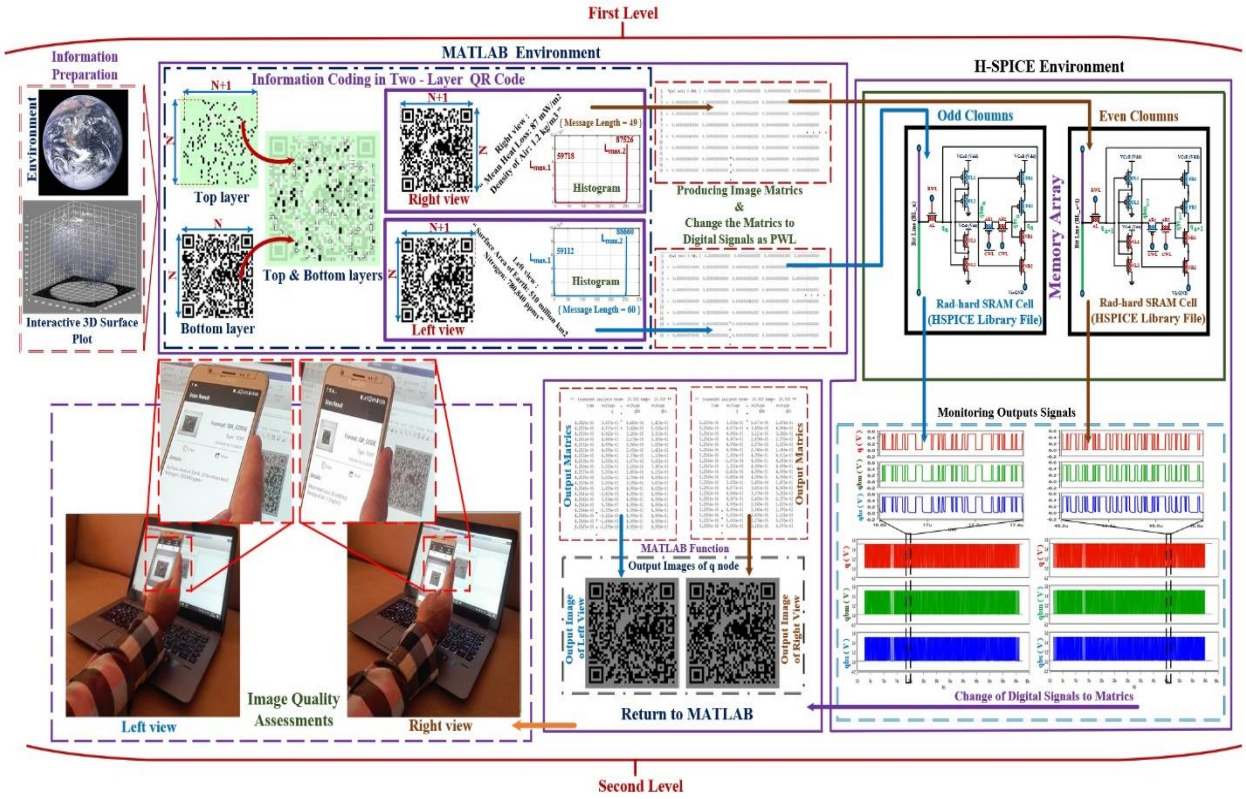
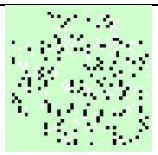
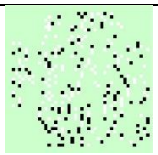



**Fig. 20** Overview of the storage mechanism of a sample of images based on a two-layer QR code using the proposed algorithm with real evaluation of results by a smartphone.

**Table 5** Two examples of two-layer QR code images extracted from the bit-cell structure using the suggested mechanism with PSNR and MSSIM values for each image.

| **Input images** | | | | | | **Output QR code images of sensitive nodes** | |
|---|---|---|---|---|---|---|---|
| **Orginal image / Data Length** | | **Bottom Layer** | **Top Layer** | **Left View/ Hiding Text** | **Right View/ Hiding Text** | **q node of odd cell** | **q node of even cell** |
| *Earth* |  (49,60) |  |  |  Surface Area of Earth: 510 million km2 Nitrogen: 780,840 ppmv |  Mean Heat Loss: 87 mW/m2 Density of Air: 1.2 kg/m3 |  **PSNR= 40.978 MSSIM= 0.9970** |  **PSNR= 42.081 MSSIM= 0.9966** |
| | | | | | | **qb$_S$ node of odd cell** | **qb$_S$ node of even cell** |
| | | | | | |  **PSNR= 41.265 MSSIM= 0.9959** |  **PSNR= 42.343 MSSIM=0.9971** |
| *Weather* |  (66,44) |  |  |  |  Wind Speed: 19 km/h | **q node of odd cell**  | **q node of even cell**  |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | High-level of the Clouds: 3,000 to 7,600m Water Vapor: 2.27 MJ/kg | Temperature Range: ±40 °C | | |
| | | | | | | PSNR= 39.567<br>MSSIM= 0.9937 | PSNR= 41.667<br>MSSIM= 0.9965 |
| | | | | | | $qb_s$ node of odd cell | $qb_s$ node of even cell |
| | | | | | |  |  |
| | | | | | | PSNR= 40.643<br>MSSIM=0.9957 | PSNR= 41.987<br>MSSIM=0.9967 |

According to the results, it can be seen that the proposed bit-cell in terms of quality evaluation parameter as well as the basic parameters in evaluating the energy saving rate is much better compared to its counterpart designs in other technologies. Finally, according to the range of values obtained for the PSNR metric, it is observed that other images in the proposed sensitive cell nodes are around 40 dB, which indicates that the circuit is suitable for use in most applications [51], especially in the presence of natural environmental conditions and can be used in image processing applications to achieve image storage at an acceptable quality level. Figure 21 shows the QR code test images in two left and right views stored in the main sensitive node of proposed bit-cell in the presence of internal noise application of Fig. 8 over an alternating period. The contents of the information stored in each of them can be accessed for an experiment with the help of a QR code image scanner on smartphones and scanning the images in Fig. 21. The results of evaluations in the field of image processing for quality parameter, PSNR, (for image stored in the main sensitive node) and efficiency parameters such as propagation delay, power dissipation and PDP for two QR code-based test images are given in Table 6.

| **Earth** | | **Weather** | |
|---|---|---|---|
| Left-View | Right-View | Left-View | Right-View |
|  |  |  |  |
| Peak-SNR Value = 14.5119<br>SNR Value = 6.0166<br>SSIM Value = 0.2303 | Peak-SNR Value = 14.5015<br>SNR Value = 5.9872<br>SSIM Value = 0.2306 | Peak-SNR Value = 14.5741<br>SNR Value = 6.4473<br>SSIM Value = 0.2511 | Peak-SNR Value = 14.6519<br>SNR Value = 6.5099<br>SSIM Value = 0.2266 |
| (a) | (b) | (c) | (d) |

**Fig.21** The left/right-views QR codes stored in the main sensitive node within the proposed bit-cell structure in the presence of noisy signal.

**Table 6** Evaluation results of other parameters of storage quality and image processing efficiency for other designs in TT-corner conditions.

| **Rad-hard Bit-Cells** | **Design Technology** | **Parameters** | **Input Test Images** | | | |
|---|---|---|---|---|---|---|
| | | | ***Earth*** | | ***Weather*** | |
| | | | Left-View | Right-View | Left-View | Right-View |
| **6T-SRAM [17]** | **GAA CNT-MOSFET** | **PSNR (dB) (at q node)** | 36.21 | 36.69 | 35.83 | 35.40 |
| | | **Delay (ps)** | 5.15 | 5.14 | 5.43 | 4.97 |
| | | **Power (nW)** | 25.98 | 26.05 | 25.39 | 25.76 |
| | | **PDP (aJ)** | 133.797 | 133.897 | 137.86 | 128.02 |
| **11T-SRAM [31]** | **Si-MOSFET** | **PSNR (dB) (at q node)** | 31.23 | 31.43 | 33.42 | 33.54 |
| | | **Delay (ps)** | 11.21 | 11.19 | 10.78 | 11.03 |
| | | **Power (nW)** | 38.62 | 39.72 | 39.11 | 39.44 |
| | | **PDP (aJ)** | 432.93 | 444.46 | 421.60 | 435.02 |
| **11T-SRAM [32]** | | **PSNR (dB) (at q node)** | 34.43 | 34.50 | 34.21 | 34.33 |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | Delay (ps) | 15.03 | 15.10 | 15.59 | 15.12 |
| | | Power (nW) | 62.62 | 62.72 | 60.53 | 60.74 |
| | | PDP (aJ) | 941.17 | 974.07 | 943.66 | 918.38 |
| 11T-SRAM [33] | CNTFET | PSNR (dB) (at q node) | 37.43 | 37.50 | 35.66 | 35.42 |
| | | Delay (ps) | 7.48 | 7.42 | 7.19 | 7.32 |
| | | Power (nW) | 22.38 | 22.11 | 22.69 | 21.94 |
| | | PDP (aJ) | 167.40 | 164.05 | 163.14 | 160.60 |
| This work (11T-SRAM) | GAA CNT-MOSFET | PSNR (dB) (at q node) | 40.978 | 42.081 | 39.567 | 41.667 |
| | | Delay (ps) | 6.29 | 6.07 | 6.18 | 6.21 |
| | | Power (nW) | 17.89 | 17.77 | 17.43 | 17.50 |
| | | PDP (aJ) | 112.52 | 107.86 | 107.71 | 108.67 |

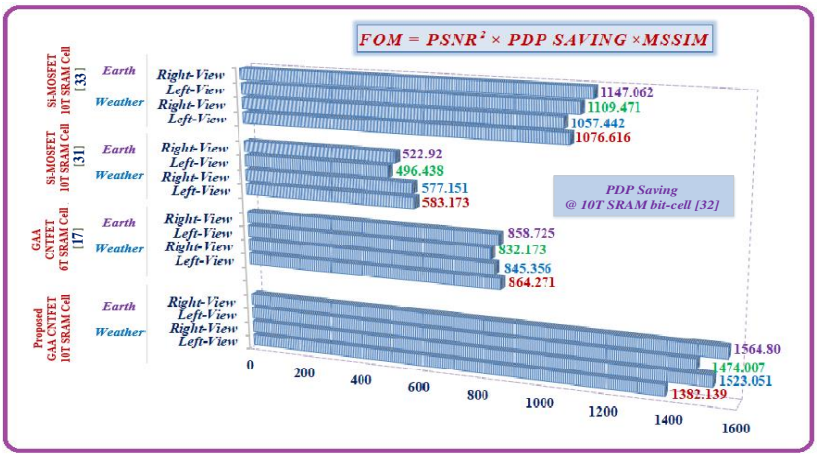



**Fig. 22** Evaluation of the comprehensive FoM parameter for other architectures by normalize PDP parameter relative to the bit-cell based on the Si-MOSFET structure [32].

In papers [42] and [43], two FoM criteria for evaluating the performance and quality of images are presented, which can be achieved by combining common components to a comprehensive FoM parameter with more emphasis on evaluating the quality/performance of a circuit in image storage. Where higher values for this parameter indicate the more capability of a design to implement hardware in the field of image processing. Eq. (22) expresses the FoM relationship based on three parameters:

$$FoM = PSNR^2 \times PDP\ saving \times Mean\ SSIM \quad (22)$$

Where the PDP parameter (in atto-Joule (aJ)) as the average energy consumption, and the propagation delay (in pico-seconds (ps)) × the average power dissipation (in nano-watts (nW)), whereas the ratio of improvement of this parameter for other designs to the proposed design based on Si-MOSFET technology as a reference with the worst PDP has been done. Figure 22 shows the results values for the comprehensive FoM parameter for other bit-cells based on other different technologies. According to the results obtained, it can be seen that among the other cells, the design of 10-transistors based on Si-MOSFET technology in [32] has resulted in a much lower FoM due to its lower image storage quality compared to other state-of-the art designs. The proposed design with the highest FoMs shows a better exchange between accuracy and efficiency and can be used in circuits with other applications such as Bluetooth modules and radio frequency identification (RFID) tags and GPS tracking circuits is based on data storage in the form of two-layer QR code.

## 8. Conclusion

The new design of a low-power rad-hard single-ended SRAM bit-cell (UPRHSE) using outer asymmetrical virtual ground gating and inner read decoupling schemes at a much lower consumption area of about $2\mu m^2$ is provided using the GDI method based on the GAA CNT-MOSFET technology using the dual-chirality/multiple-diameter technique, where the consumption layout area used in implementation 1x1 and 4x4 memory mini-arrays based on the proposed bit-cell and peripheral circuits is about 25 $\mu m^2$ and 144 $\mu m^2$, respectively. In the present article, in order to investigate single/double upset injection circuit model based on the structure of TPRs in the presence of implementation by GAA CNT-MOSFETs with unique electrostatic characteristics has been proposed. Based on the analytical-compact model, an equation for calculating the $V_{DR}$ metric for the proposed bit-cell structure is presented. Also, an algorithm is suggested to facile estimate of the $V_{DR}$ parameter. The error distance of the worst results for $V_{DR}$ metric in the presence

of temperature variations at TT-corner from Monte-Carlo (MC)-HSPICE simulation and suggested algorithm for the robustness and weakest bit-cell structures will be about 3% and 5.5%, respectively.

The simulation results for other bit-cells show that the unique structure of the proposed bit-cell architecture in terms of write/hold/read noise margin parameters shows an advantage of about 12.5%, 3.8% and 8.2% over the best-performing bit- cell for TT-corner condition respectively, whereas in terms of other Figure of Merits (FoMs), such as performance, yield, variability ($\mu/\sigma$) and critical charge show the best results against other counterpart designs. Also, the suggested bit-cell architecture in the presence of other parameters such as: SNMs, propagation delay, power consumption and EDP in based on MC simulation critical $V_{dd}$ has more robustness and higher reliability of data storage in standby mode in the presence of low $V_{dd}$ with more leakage current savings compared to other state-of-the art bit-cells under the same evaluation conditions in 16 nm technology node. The simulation results show that the proposed architecture is robustness in terms of SEU and MEU and demonstrates full immunity to the effects of high-energy particles strikes on data storage nodes while retaining data in most of the time compared to rad-hard SRAM bit-cells. Finally, to implement the proposed scheme in a real application, the suggested memory architecture is used as an example for storing images based on a two-layer QR code that contains content and information extracted by satellite systems. According to the results obtained for the proposed design, other important parameters in evaluating the quality of the stored output images such as PSNR and MSSIM metrics are in the values around 40 dB and 0.99, respectively, and in terms of other comprehensive FoMs based on these metrics, the suggested bit-cell architecture compared to the other counterpart designs has more appropriate results, which indicates that the proposed UPRHSE design can be a reasonable choice for applications that demands high stability, impact resistance to radiation particles and extremely low power in a radiation abundant environment with limited-energy sources.

## ■ Appendix

In this section, the details of calculating the data-retention voltage ($V_{DR}$) electric parameter using the analytical model in the Ref. [26] at a room-temperature standby operation condition, as well as applying the current equation for the sub-threshold region for CNT-MOSFET devices [52] for the suggested UPRHSE bit-cell, according to the VTC curves of the inverters forming HSNM is shown in Fig. 14 (b). Start calculations by considering the sub-threshold operating scheme for the cell and applying the sub-threshold current equation based on the ballistic CNT-MOSFET model assuming standby operation at room temperature (ignoring gate leakage and other leakage mechanisms compared to the threshold current have a minor contribution) will take place. The total current in the sub-threshold region ($I_{sub}$) can be modeled according to Eq. (A.1):

$$I_{sub} \approx \frac{KT}{qR_Q}\left[\left(exp\frac{2qV_{GS}-E_g}{2KT}\right)-\left(exp\frac{2qV_{GS}-2\alpha qV_{DS}-E_g}{2KT}\right)\right] \quad (A.1)$$

Where KT and $E_g$ are the thermal energy and the CNT band gap, q is the unit electron charge and $R_Q$ is the quantum resistance, where $KT/qR_Q \sim 4\mu A$. Also, $V_{GS}$ are the gate voltage relative to the source terminal and $V_{DS}$ are the drain terminal voltage at the source. Note that the parameter α can be selected as a drain optical phonon scattering (DOPS) parameter to effectively change the drain voltage ($V_D$) in a range of $0 < \alpha \leq 1$. In the proposed cell structure, to maintain the data stable, cross-coupled inverters must have loop gain greater than one. When the value of $V_{dd}$ to $V_{DR}$ is scale down in the cell structure, the VTC curves of the internal inverters are degraded to such a level that the loop gain is reduced to one and the HSNM (maximum possible square between the VTC curves of inner inverters) reaches about zero. According to Fig.10 (a) and the symbols, these conditions are expressed by the following Eq. (A.2):

$$\left.\frac{\partial \mathrm{V}q}{\partial V_{qbm}}\right|_{\text{Left inverter}} \times \left.\frac{\partial V_{qm}}{\partial \mathrm{V}q}\right|_{\text{Right inverter}} = 1\,, \text{When } V_{dd} = V_{DR} \quad (A.2)$$

Based on Equation (A.2), the $V_{DR}$ parameter for the proposed bit-cell can be determined by solving the sub-threshold VTC equations of the two internal data-holding inverters, because all transistors are in the weak inversion region when the $V_{dd}$ operates around the $V_{DR}$. Assuming the original state of the stored data is in the cell:

$$\mathrm{V}q \approx 0 \;\&\; \mathrm{V}qb_m \approx V_{dd} \quad (A.3)$$

and that when the bit-cell is in standby mode, the current in each internal inverter is balanced, so according to Fig. 10 (a):

$$I_{PR1} + I_{AL} = I_{NR2} \quad (A.4)$$

and the fact that a single BL is pre-charged while holding on GND level, so the current sub-threshold for the AL transistor is negligible and the equation can be simplified:

$$(I_{PR1} = I_{PR2} = I_{NR1} = I_{NR2}) \rightarrow I_{PR1} = I_{NR2} \quad (A.5)$$

In order to calculate the VTC for the left-side inverter in the suggested structure in the sub-threshold state, by substituting the expression sub-threshold current (A.1) in Eq. (A.5):

$$exp\left(\frac{2qVq_{bm}}{KT}\right)=\frac{\left(1-exp\frac{-aq(V_{dd}-V_x)}{KT}\right)}{\left(1-exp\frac{-aqV_y}{KT}\right)}\times exp\frac{E_{gNR2}-E_{gPR1}}{2KT}\times exp\frac{qV_{dd}}{KT}$$

Now by taking *natural Log* from both sides of the equation will be obtained:

$$Vq_{bm}=\frac{KT}{2q}ln\left[\frac{\left(1-exp\frac{-aq(V_{dd}-V_x)}{KT}\right)}{\left(1-exp\frac{-aqV_y}{KT}\right)}\right]+\left(\frac{E_{gNR2}-E_{gPR1}}{2q}\right)+\frac{V_{dd}}{2} \quad (A.6)$$

Given that all the structure transistors in the memory cell are biased when operating in $V_{DR}$ conditions sub-threshold, so with a general approximation for $V_x$ and $V_y$ in the proposed bit-cell structure as $V_x=\frac{V_{dd}+Vq}{2}$ and $V_y=\frac{Vq}{2}$ will be obtained (where $0Volt\leq V_q\leq V_{dd}$):

$$Vq_{bm}=\frac{KT}{2q}ln\left[\frac{\left(1-exp\frac{-aq(V_{dd}-Vq\ )}{2KT}\right)}{\left(1-exp\frac{-aqVq}{2KT}\right)}\right]+\left(\frac{E_{gNR2}-E_{gPR1}}{2q}\right)+\frac{V_{dd}}{2} \quad (A.7)$$

According to Fig. 10 (a), the following sub-threshold current equation for the right-side inverter in the proposed cell structure would be:

$$I_{PL1}-I_{PL2}+I_{NL1}=I_{NL2} \quad (A.8)$$

Substituting the following sub-threshold current (A.1) in Eq. (A.8) for the right-side inverter will give:

$$\left(exp\frac{-2aqV_{dd}}{2KT}.\left(\exp\frac{2aqVq_{bm}}{2KT}\right)^2\right)+\left(\frac{\left(\exp\frac{-E_{gPL2}}{2KT}+\exp\frac{2qVq-E_{gNL2}}{2KT}\right)}{\left(\exp\frac{-E_{gNL1}}{2KT}+\exp\frac{2q(V_{dd}-Vq)-E_{gPL1}}{2KT}\right)}-1\right)\left(\exp\frac{2aqVq_{bm}}{2KT}\right)\ -\frac{\left(\exp\frac{-E_{gPL2}}{2KT}+\exp\frac{2qVq-E_{gNL2}}{2KT}\right)}{\left(\exp\frac{-E_{gNL1}}{2KT}+\exp\frac{2q(V_{dd}-Vq)-E_{gPL1}}{2KT}\right)}=0$$

Because it is $-\frac{\left(exp\frac{-E_{gPL2}}{2KT}+exp\frac{2qVq-E_{gNL2}}{2KT}\right)}{\left(exp\frac{-E_{gNL1}}{2KT}+exp\frac{2q(V_{dd}-Vq)-E_{gPL1}}{2KT}\right)}\Big/exp\frac{-2aqV_{dd}}{2KT}<0$, certainly this quadratic equation in terms of $\left(exp\frac{2aqVq_{bm}}{2KT}\right)$ has two different roots of the sign that results from the following equation:

$$\Delta=\left(\frac{\left(\exp\frac{-E_{gPL2}}{2KT}+\exp\frac{2qVq-E_{gNL2}}{2KT}\right)}{\left(\exp\frac{-E_{gNL1}}{2KT}+\exp\frac{2q(V_{dd}-Vq)-E_{gPL1}}{2KT}\right)}-1\right)^2-4\left(exp\frac{-2aqVdd}{2KT}\right)\left(-\frac{\left(\exp\frac{-E_{gPL2}}{2KT}+\exp\frac{2qVq-E_{gNL2}}{2KT}\right)}{\left(\exp\frac{-E_{gNL1}}{2KT}+\exp\frac{2q(V_{dd}-Vq)-E_{gPL1}}{2KT}\right)}\right)=$$

$$\left(\frac{\left(\exp\frac{-E_{gPL2}}{2KT}+\exp\frac{2qVq-E_{gNL2}}{2KT}\right)}{\left(\exp\frac{-E_{gNL1}}{2KT}+\exp\frac{2q(V_{dd}-Vq)-E_{gPL1}}{2KT}\right)}-1\right)^2+4\left(exp\frac{-2aV_{dd}}{2KT}\right)\left(\frac{\left(\exp\frac{-E_{gPL2}}{2KT}+\exp\frac{2qVq-E_{gNL2}}{2KT}\right)}{\left(\exp\frac{-E_{gNL1}}{2KT}+\exp\frac{2q(V_{dd}-Vq)-E_{gPL1}}{2KT}\right)}\right)>0$$

$$\left(\exp\frac{2aqVq_{bm}}{2KT}\right)=\left(-\left(\frac{\left(\exp\frac{-E_{gPL2}}{2KT}+\exp\frac{2qVq-E_{gNL2}}{2KT}\right)}{\left(\exp\frac{-E_{gNL1}}{2KT}+\exp\frac{2q(V_{dd}-Vq)-E_{gPL1}}{2KT}\right)}-1\right)\pm(\Delta)^{1/2}\right)\Big/(2\,exp\frac{-2aqV_{dd}}{2KT})$$

By taking the *natural log* from the sides of the above relation, Eq. (A.9) will be obtained:

$$Vq_{bm}=\frac{KT}{aq}ln\left[\left(\left(-\frac{\left(\exp\frac{-E_{gPL2}}{2KT}+\exp\frac{2qVq-E_{gNL2}}{2KT}\right)}{\left(\exp\frac{-E_{gNL1}}{2KT}+\exp\frac{2q(V_{dd}-Vq)-E_{gPL1}}{2KT}\right)}+1\right)+(\Delta)^{1/2}\right)\Big/(2exp\frac{-2aqV_{dd}}{2KT})\right] \quad (A.9)$$

Furthermore, since the nominal supply voltage is 0.5Volt ($V_{dd}$ integer < 1), so the higher order statements of $V_q$ and $V_{dd}$ parameters due to their reduced effectiveness and also the deficiency of need to use a general solution to solve these equations based on need for numerical iterations and estimation of the initial value in order to avoid repetition in the calculation process will be ignored. Now using the *standard expansion Maclaurin's series* $e^{\pm x}=1\pm x+\frac{x^2}{2!}\pm\ldots$ and the placement in Eq. (A.7) for the left-side inverter we will have:

$$Vq_{bm}\approx\frac{KT}{2q}ln\left[\frac{\left(1-\frac{aq(V_{DD}-Vq\ )}{2KT}\right)}{\left(1-\frac{aqVq}{2KT}\right)}\right]+\left(\frac{E_{gNR2}-E_{gPR1}}{2q}\right)+\frac{V_{DD}}{2}\ \approx\ \frac{KT}{2q}ln\left[\frac{4KTaq-(aq)^2V_{dd}}{(2KT)^2-2KTaqV_{dd}+(aq)^2V_{dd}V_q}\right]+\left(\frac{E_{gNR2}-E_{gPR1}}{2q}\right)+\frac{V_{DD}}{2} \quad (A.10)$$

Also using the *standard expansion Maclaurin's series* and the *Bernoulli's inequality* $(1+x)^n\geq(1+nx)$ and placement in Eq. (A.9) for the right-side inverter, we have:

$$Vq_{bm}=\frac{KT}{aq}ln\left[\frac{4KT+KTR^2-4aqV_{dd}R}{4(KT-aqV_{dd})}\right] \quad (A.11)$$

Where the R parameter is defined by:

$$R \triangleq \frac{4KT - \left(E_{gPL2} + E_{gNL2}\right) + 2qVq}{4KT - \left(E_{gPL1} + E_{gNL1}\right) + 2qV_{dd} - 2qVq}$$

Next, each equation (A.10) and (A.11) are derived from the $V_q$ parameter and the resulting results are equated. Finally, by substituting the $V_{DR}$ metric in the final equation, we will have the $V_{dd}$:

$$V_{DR} = V_{DR.intial} - \frac{\frac{4q}{kT}V_q}{H} \tag{A.12}$$

In the equation, $V_{DRintial}$, the initial estimated value of $V_{DR}$ and is equal to:

$$V_{DR,intial} = \frac{2\frac{kT}{q}[8(2-kT) + \left(E_{gPR1} + E_{gNR1} + E_{gPR2} + E_{gNR2}\right)]}{H}$$

Where the H parameter will be equal to:

$$H = -\left[4\frac{kT}{q} - \left(E_{gPR1} + E_{gNR1}\right)\right] \times \left[\left(\frac{4kT}{q} - \left(E_{gPR1} + E_{gNR1}\right)\right) + \frac{aq}{4kT} - \frac{(4kT - \left(E_{gPR1} + E_{gNR1}\right))aq}{4kT}\right] - \left[\frac{4kT}{q}(2-q) + 3aq\left(E_{gPR1} + E_{gNR1} + E_{gPR2} + E_{gNR2}\right) + \frac{4q}{kT}\right]$$

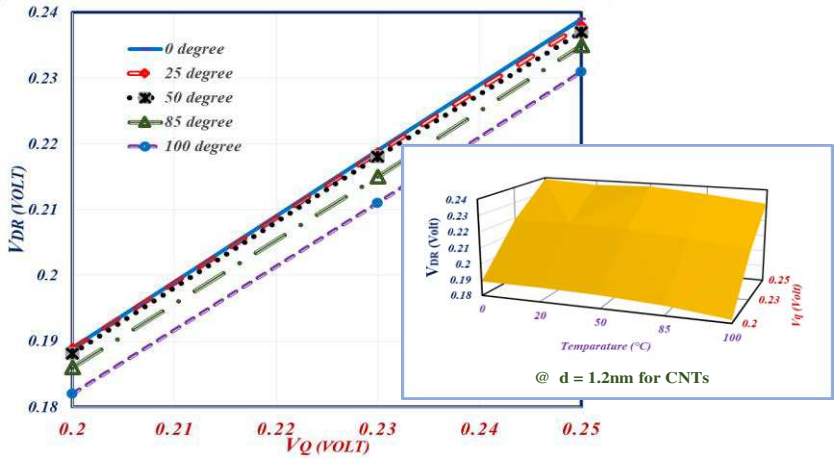



**Fig. (a.1)** Simulation results for the resulting $V_{DR}$ parameter equation for the proposed bit-cell in the presence of various temperature and voltage at the main node.

The H parameter for a temperature of 25°C with the assumption $d_{CNT}$= 1.2nm for other transistors in the suggested structure will be approximately equal to -158.405. The results of the investigation confirming Eq. (A.12) in the presence of other voltages for the main storage node ($V_q$) and different temperatures are presented in Fig. (a.1). According to the results presented in the Figure, it can be seen that the total $V_{DR}$ parameter is not significantly dependent on temperature values due to the high thermal stability of CNT-MOSFETs, where for example the assumption of 0.2Volt for $V_q$ at 25°C, $V_{DRintial}$ and $V_{DR}$ values will be -8.307mVolt and 0.188 Volt, respectively.

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# Figures

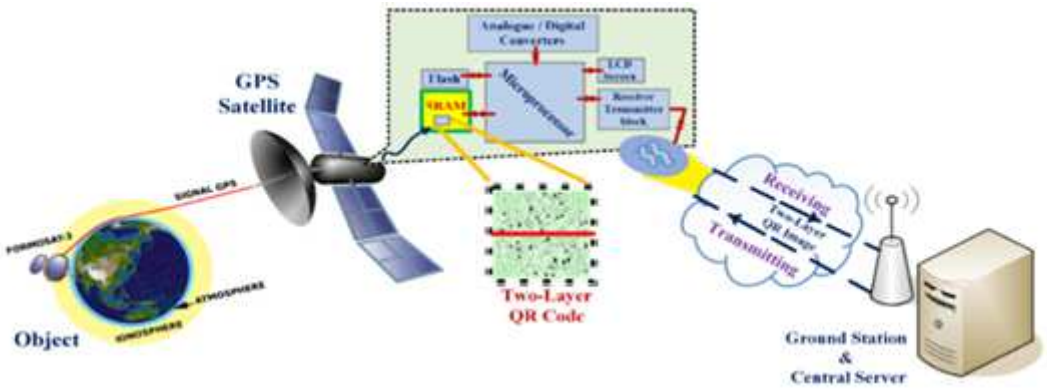



**Figure 1**

Overview of the system for sending information based on two-layer QR code by GPS satellites for weather studies applications.

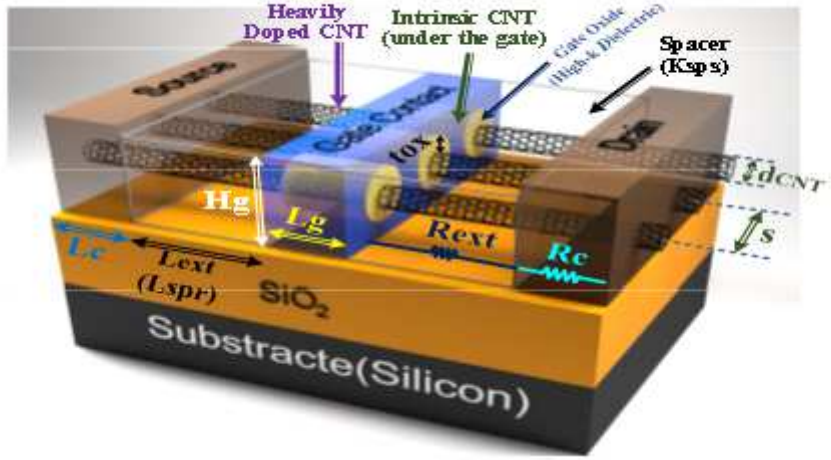



**Figure 2**

Three-dimensional (3-D) cross-sectional view of GAA CNT-MOSFET device structure.

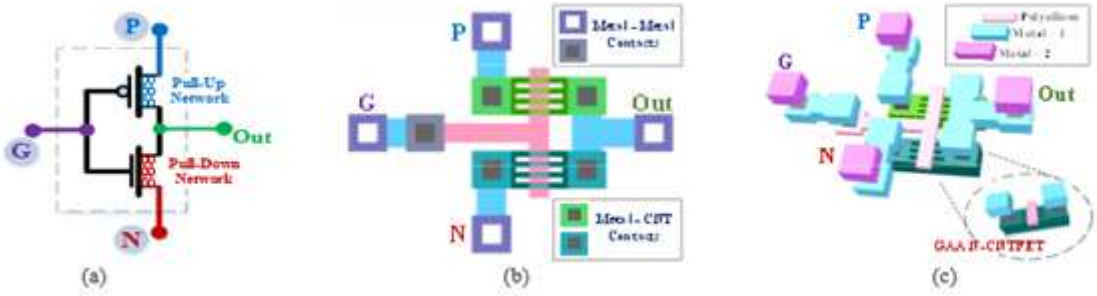



**Figure 3**

(a) Binary GAA CNT-GDI cell structure, (b) 2-D and (c) 3-D layout area view.

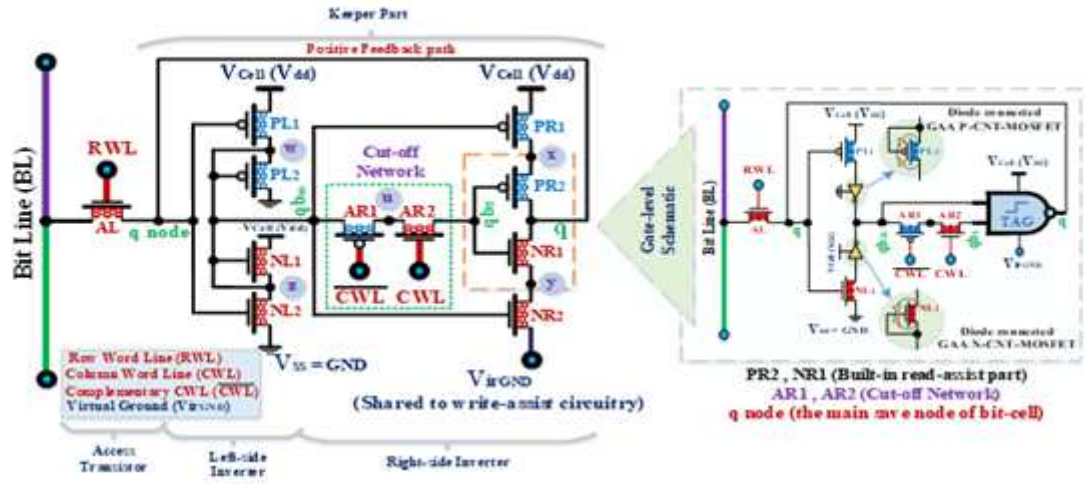



**Figure 4**

The transistor and gate levels structure of the newly proposed UPRHSE bit-cell.

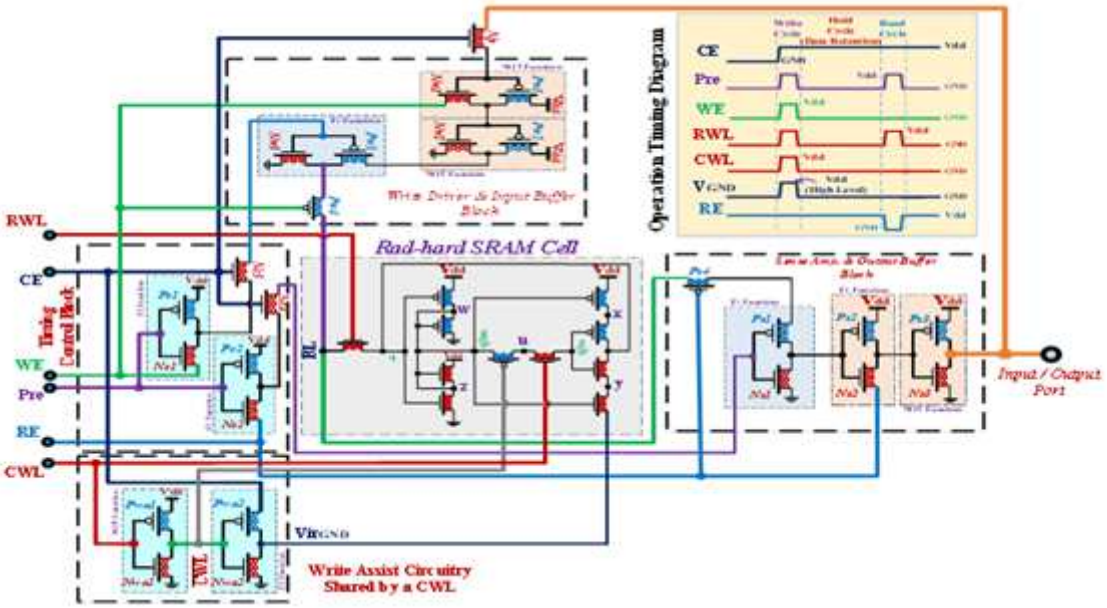



**Figure 5**

Circuit level implementation of one-row/column (1×1) memory array structure using proposed UPRHSE bit-cell and its peripherals blocks.

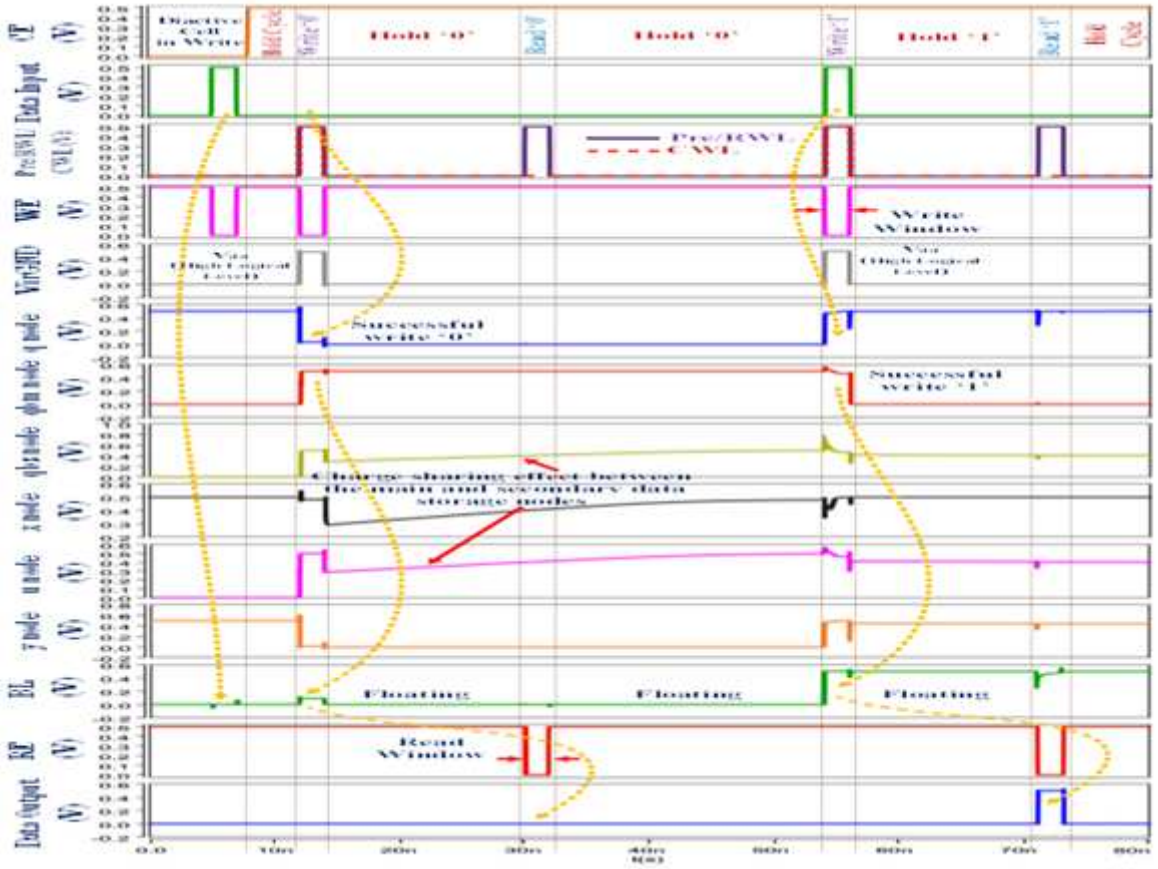
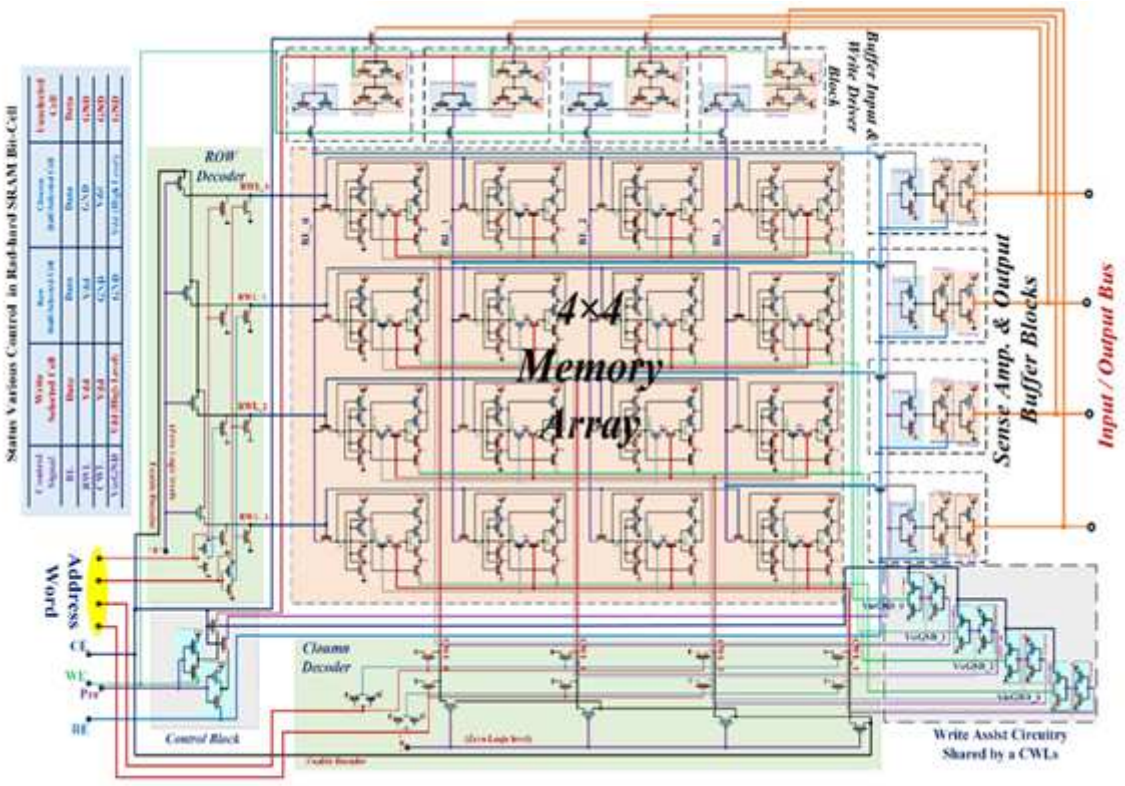


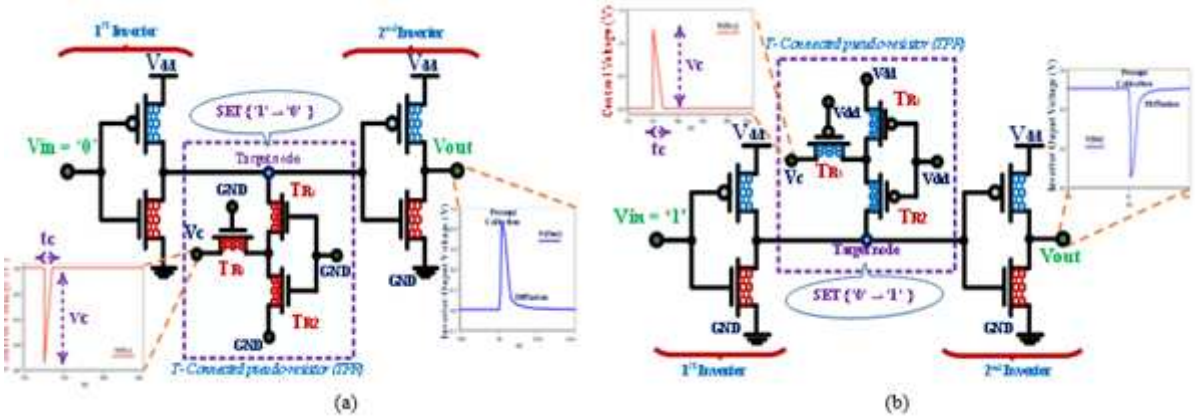

**Figure 6**

Time-domain simulation results of proposed UPRHSE bit-cell with input/output waveforms and control signals for a sequential set: Write/Read ‘0’ and ‘1’.




## Figure 7

The transistor level structure of 4×4 memory mini-array using proposed UPRHSE bit-cell and its peripheral blocks with status table of control signals.




## Figure 8

Proposed upset injection circuits based on TPRs in the production of transient glitch pulses: (a) Positive (0 ⍰ 1), (b) Negative (0 ⍰ 1) to extract SEU and MEU parameters in memory cell structures.

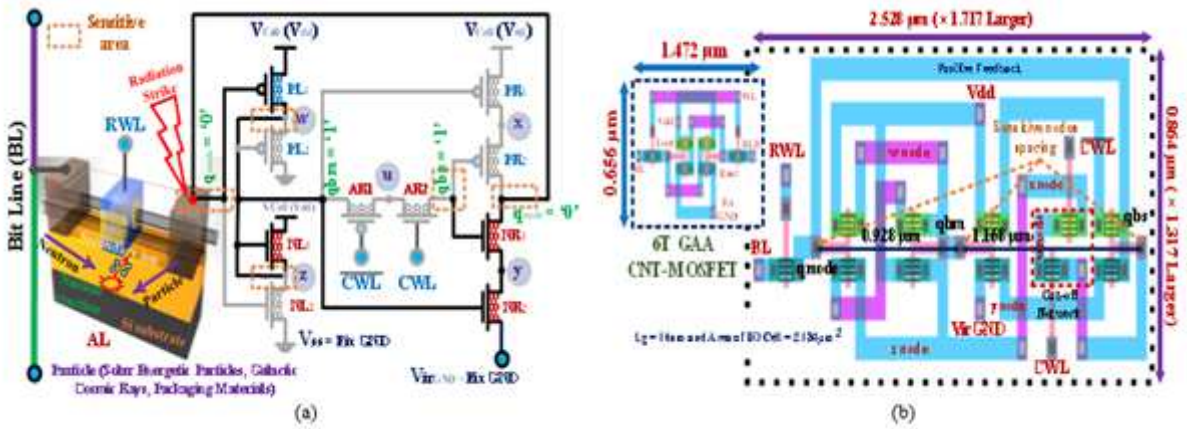



Figure 9

a) The proposed UPRHSE bit cell structure in the presence of SET injection to q node in the '0' logical data retention performance cycle with a display of sensitive areas, (b) The main image of the proposed layout area and the inset image of the 6T GAA CNT-MOSFET layout [17] in 16 nm technology (total area 2.184µm2)

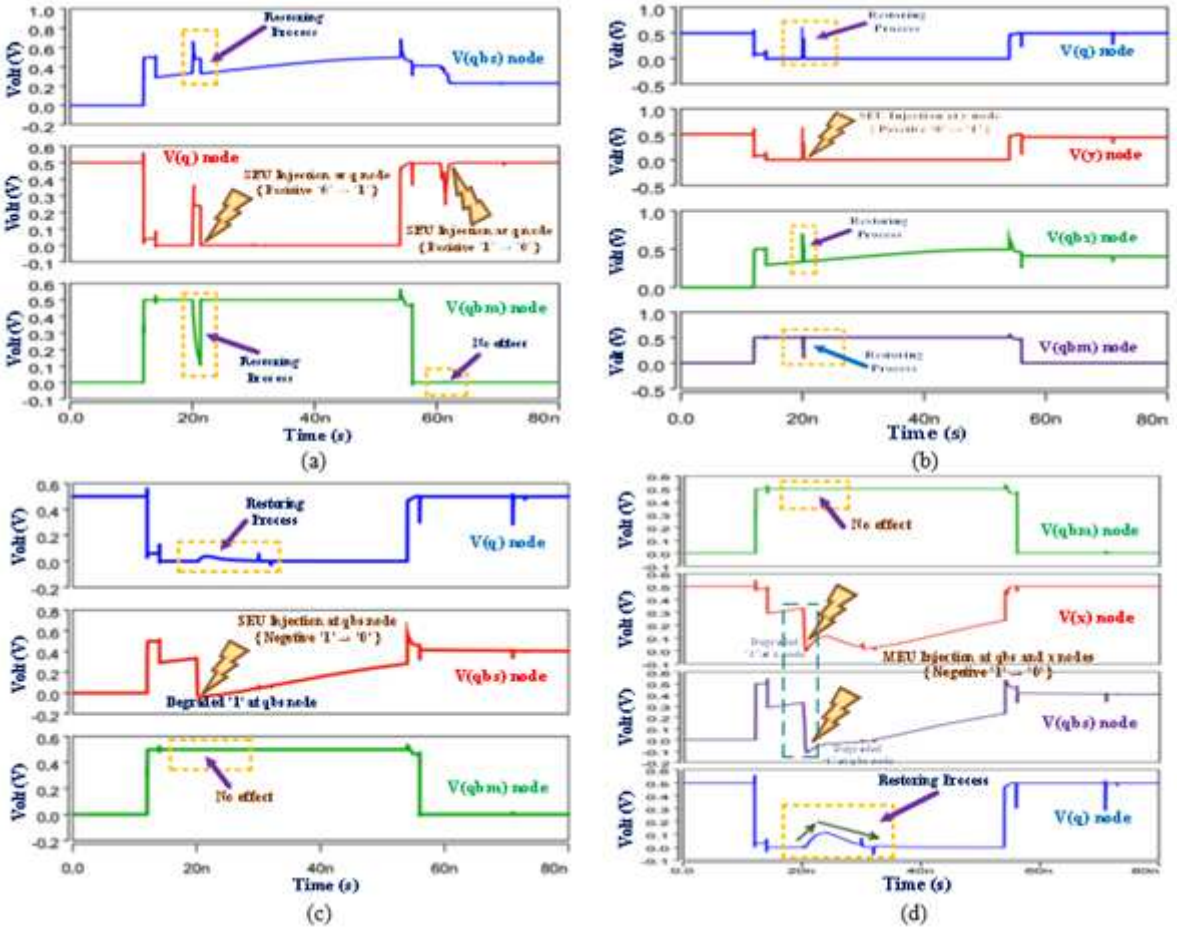
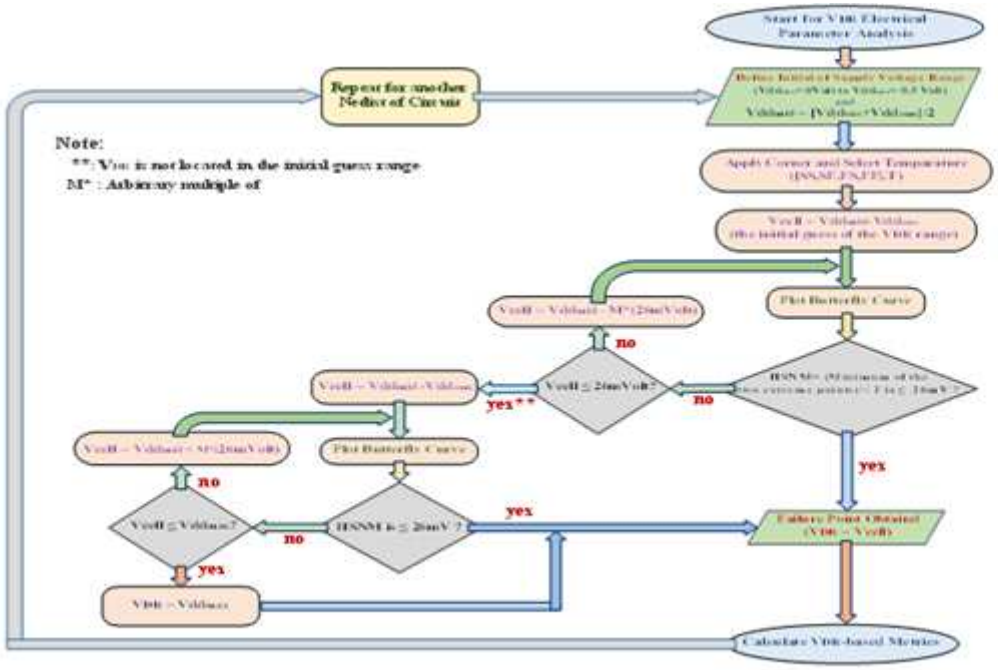


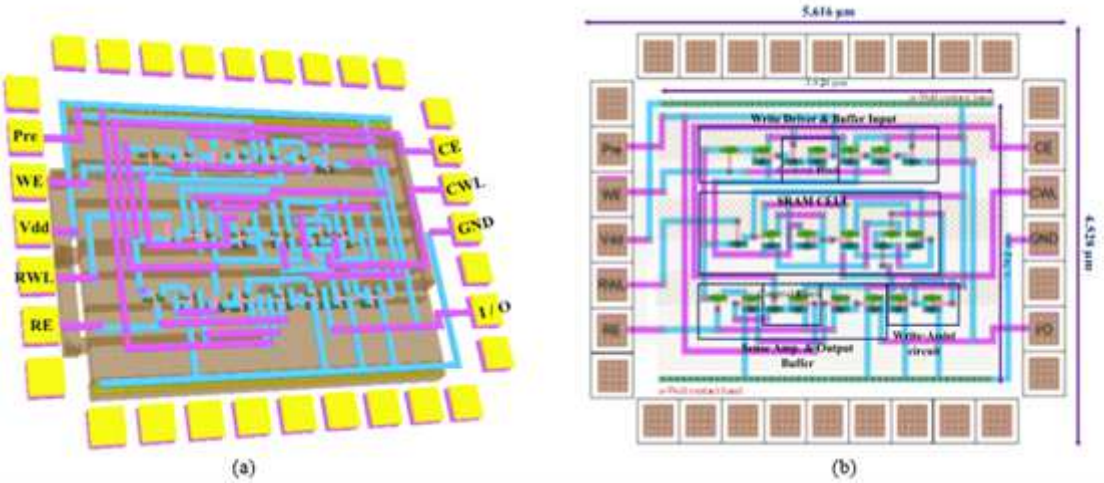

Figure 10

a) The proposed UPRHSE bit cell structure in the presence of SET injection to q node in the ‘0’ logical data retention performance cycle with a display of sensitive areas, (b) The main image of the proposed layout area and the inset image of the 6T GAA CNT-MOSFET layout [17] in 16 nm technology (total area 2.184μm2)



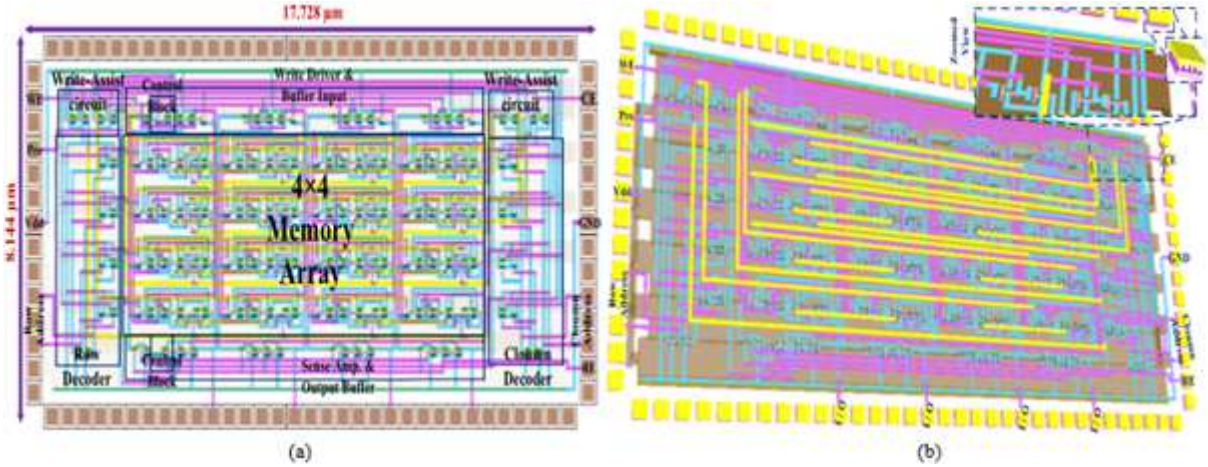

## Figure 11

The proposed general block diagram for facile evaluation and estimation of the VDR parameter.



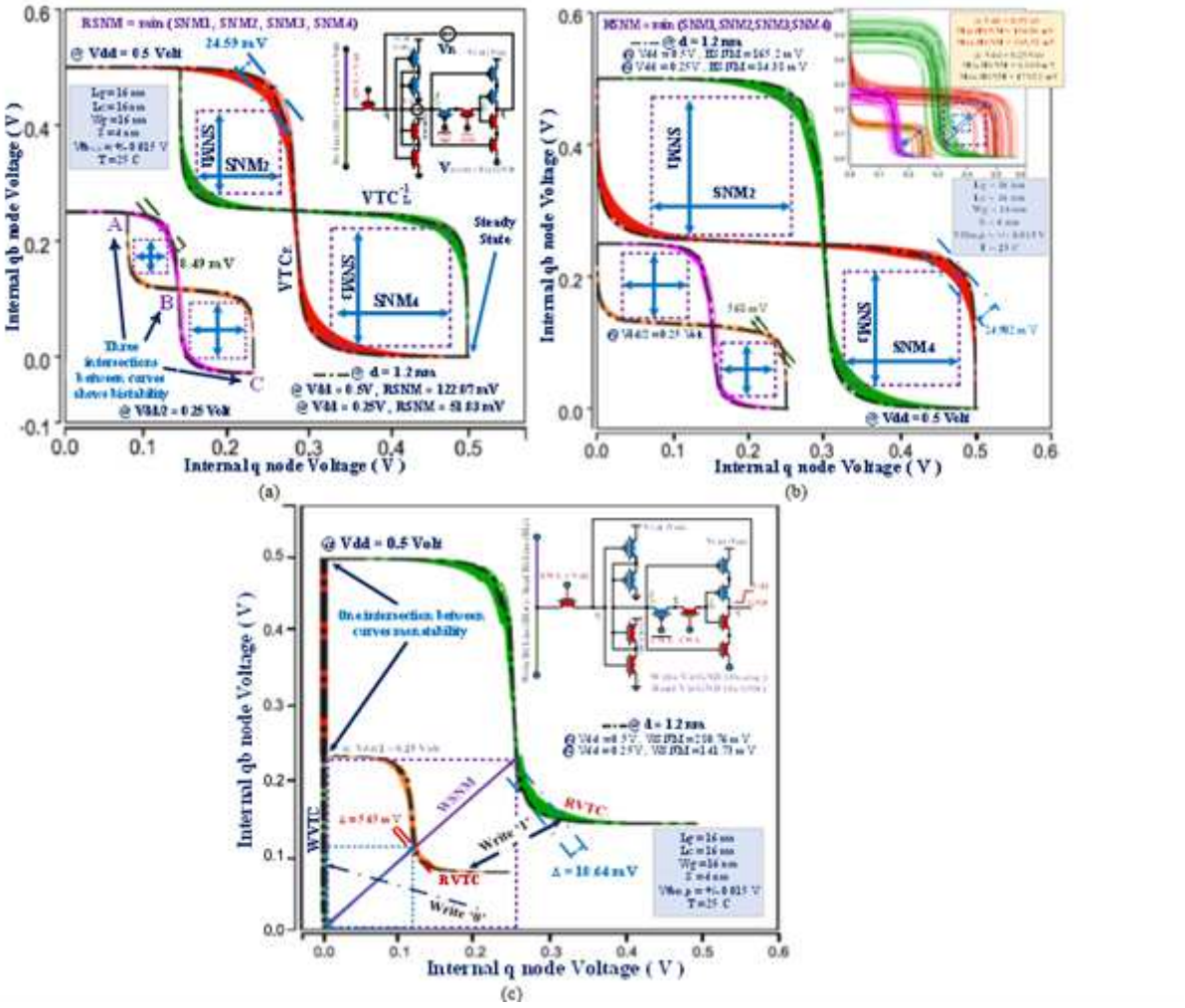

## Figure 12

Physical layout views of 1×1 memory array structure: (a) 3-D, and (b) 2-D, based on the proposed UPRHSE bit-cell placed in a ring pad.



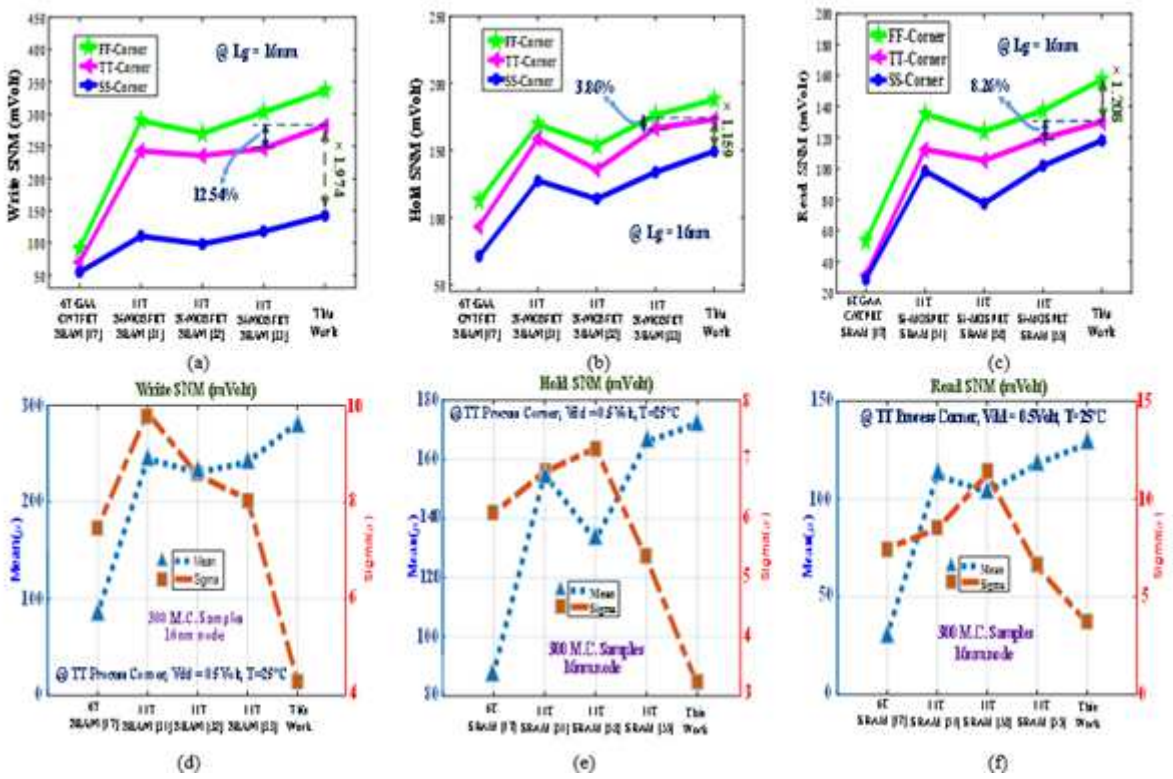

## Figure 13

Physical layout views of 4×4 memory array structure: (a) 2-D, and (b) 3-D, based on the suggested bit-cell placed in a ring pad.



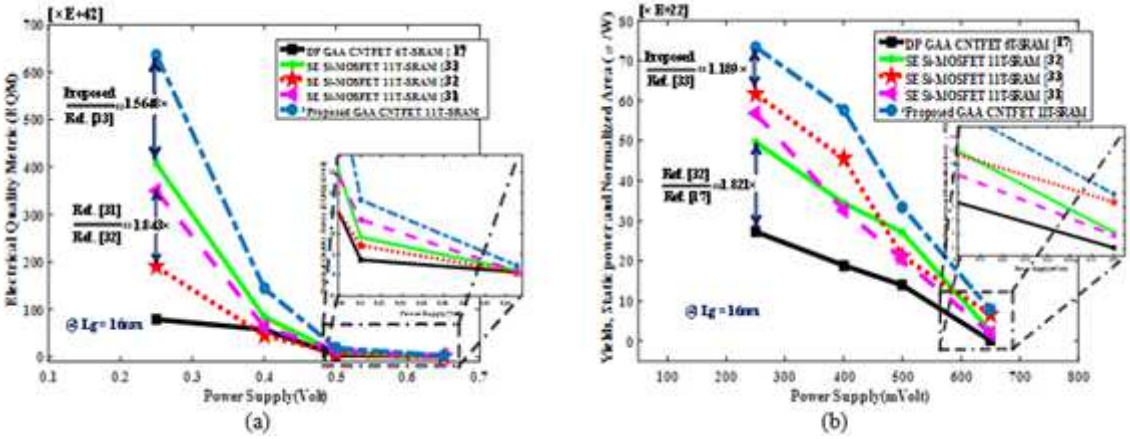

## Figure 14

The results of the MC DC analyses for SNMs of proposed bit-cell: (a) Read (restore) SNM eye diagram, (b) Hold (retention) SNM and (c) Write SNM (blend of write-VTC (WVTC) and read-VTC (RVTC) curves).



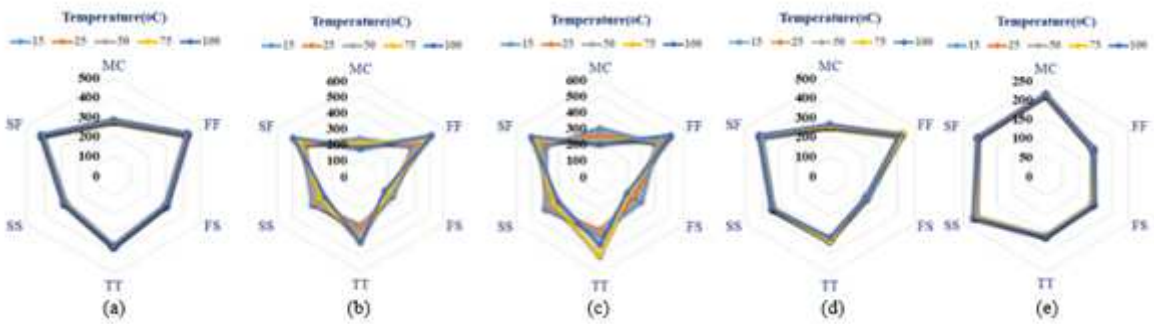

## Figure 15

Results of the various metrics: (a) WSNM, (b) HSNM and (c) RSNM, (d) mean and sigma (at mVolt) of other SNMs for bit-cells in the presence of different corner processes.



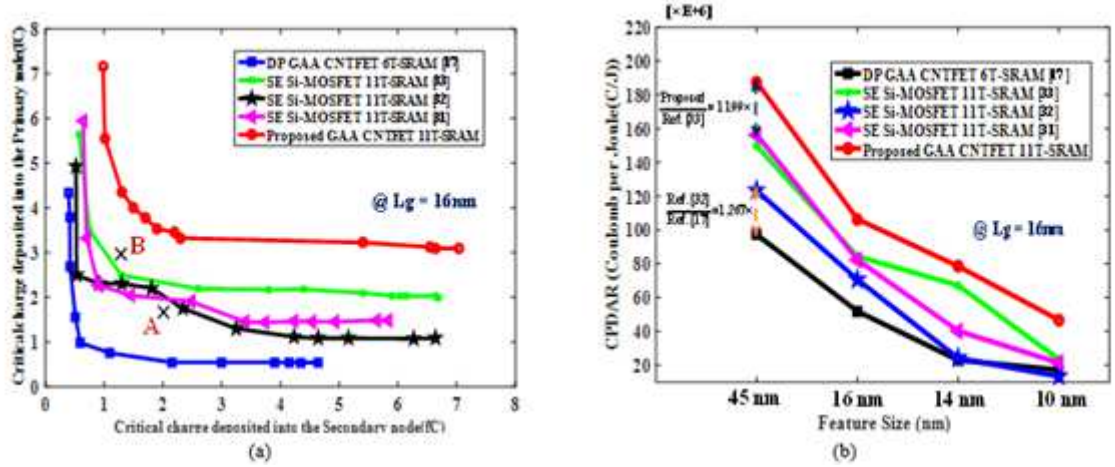

## Figure 16

The FoM metrics: (a) EQM and (b) YSNA for other bit-cells simulated under the same conditions.



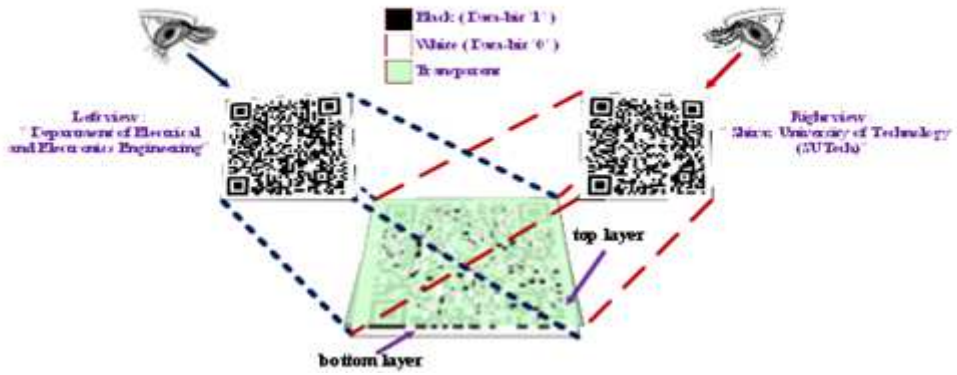

## Figure 17

Spider/web chart of VDR changes in the presence of different process temperature changes and corner conditions using the proposed algorithm and MC.




## Figure 18

(a) Critical charge plot in the MEU scenario, (b) CPDAR values in the SEU scenario for other rad-hard bit cells.




## Figure 19

A sample of a 2LQR code with appears of a standard 1LQR with data string contents of “Department of Electrical and Electronics Engineering” from the left view and appears of a standard 1LQR with different data string contents of “Shiraz University of Technology (SUTech)” from the right view.

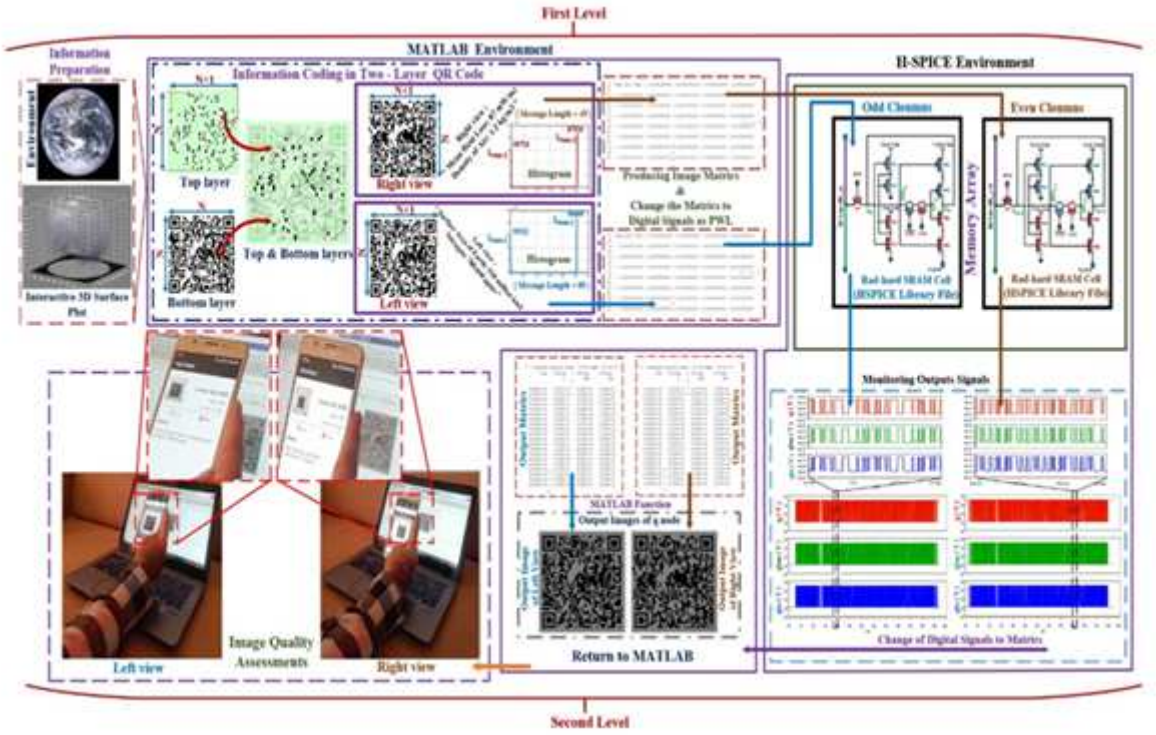



Figure 20

Overview of the storage mechanism of a sample of images based on a two-layer QR code using the proposed algorithm with real evaluation of results by a smartphone.

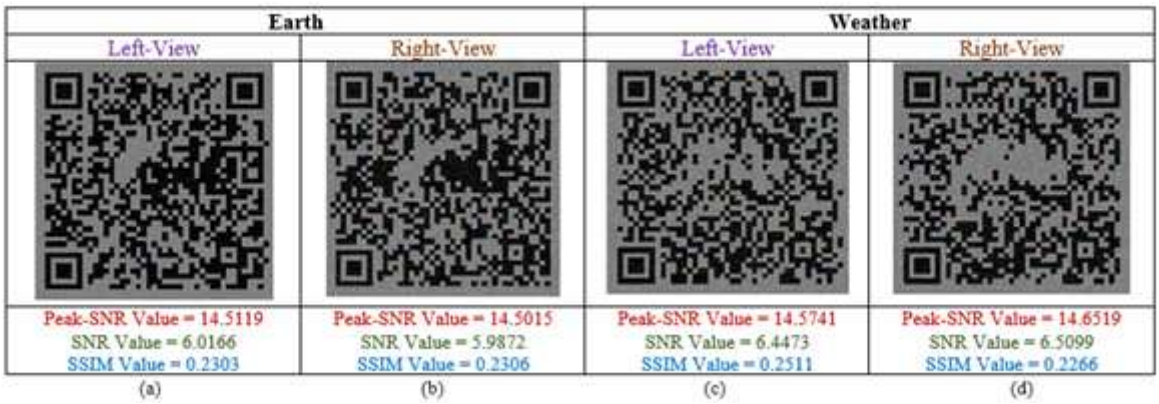
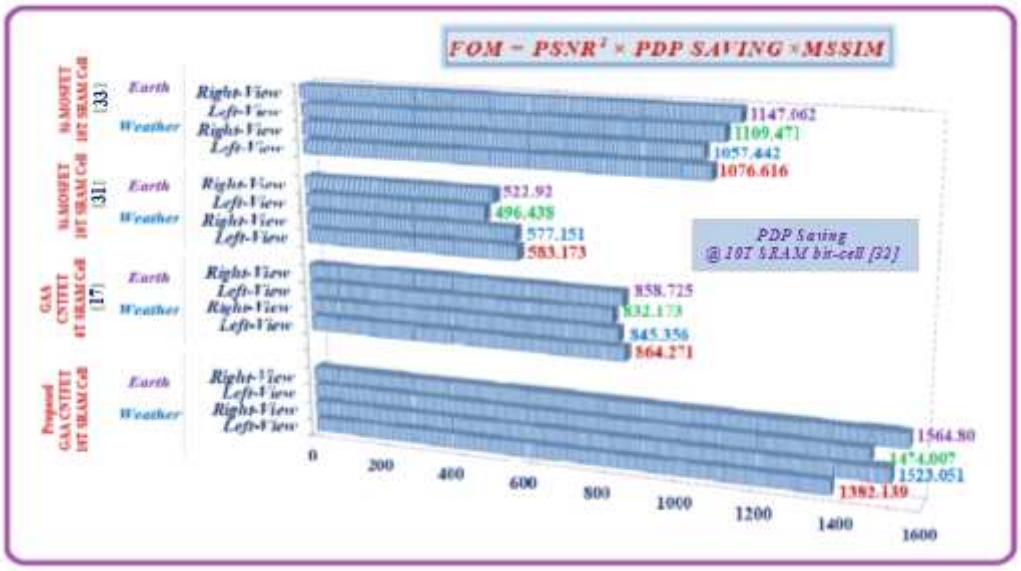



Figure 21

The left/right-views QR codes stored in the main sensitive node within the proposed bit-cell structure in the presence of noisy signal.




## Figure 22

Evaluation of the comprehensive FoM parameter for other architectures by normalize PDP parameter relative to the bit-cell based on the Si-MOSFET structure [32].