Performance Analysis of Vertically Stacked Nanosheet Tunnel Field Effect Transistor with Ideal Subthreshold Swing

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Abstract

In this paper, a novel vertically stacked silicon Nanosheet Tunnel Field Effect Transistor (NS-TFET) device scaled to a gate length of 12nm with Contact poly pitch (CPP) of 48nm is simulated. NS-TFET device is investigated for its electrostatics characteristics using technology computer-aided design (TCAD) simulator. The inter-band tunneling mechanism with a P-I-N layout has been incorporated in the stacked nanosheet devices. The asymmetric design technique for doping has been used for optimum results. NS-TFET provides a low leakage current of order10^{-16} A, an excellent subthreshold swing (SW) of 23mv/decade, and negligible drain induced barrier lowering (DIBL) having a value of 10.5 mv/V. The notable ON to OFF current ratio of the order of 10^{11} has been achieved. The device exhibits a high transconductance of $3.022x10^{-5}$ S at the gate to source voltage of 1V. NS-TFET shows tremendous improvement in short channel effects (SCE) and is a good option for advanced technologies.

Introduction

Nanosheets have emerged as a potential successor to conventional Finfets and stacked nanowires for 7nm technology and beyond [1–3]. Finfets need tall and thin fins, which enhance the fabrication cost and complexity [4] while the surface roughness factor degrades the performance of stacked nanowires [5]. The Nanosheet Field Effect Transistor (NS-FET) exhibits enormous current density due to its increased effective width per footprint [6]. NS-FET has good electrostatics control and hence remains immune to short channel effects [7]. It has been reported that NS-FET shows superior electrostatic performance in comparison to stacked nanowires or Finfets [8]. Thus NS-FET with 3D vertically stacked channels is a promising candidate for future advanced technology applications [6].

At low voltages, the device miniaturization below 50nm leads to immense OFF-state power consumption and elevated subthreshold swing (SW) [9–10]. The SW at CPP of 48nm has been reported as 83mv/decade and 94 mv/decade for nfet and pfet respectively [11].

The thermionic conduction mechanism of NS-FET makes SW temperature-dependent and this temperature constraint makes SW worse.

Vertically stacked Junctionless nanosheets(JL-Ns) show highly improved performance in terms of leakage current and SW [12]. JL-Ns with a different number of channels exhibit high ON current. At channel/oxide interface, JL-Ns provide indemnity for mobility degradation due to scattering of carriers [13]. The major bottleneck associated with JL-Ns is the exhibition of high leakage current while SW becomes non-scalable below 60 mv/decade

Tunnel Field Effect Transistors (TFETS) provide a remedy for high OFF-state current and exhibit steep SW [14–16]. TFETs work on the principle of the BTBT mechanism. In NS-FETS, the BTBT mechanism can be incorporated; thus making it a novel device consisting of vertically stacked nanosheet tunnel field effect transistor (NS-TFET). Inner spacers can be treated as an underlapped region for TFETS. It has been further reported that underlapped source and drain regions assist in reducing ambipolarity [17–18]. The

fabrication process of TFETs varies from that of Mosfets in terms of their source doping. Thus, the fabrication of NS-TFET is comparatively easier to implement with minimal deviation from the NS-FET fabrication process [19–20].

In Sect. 2, we have discussed the calibration characteristics of NS-FET. Section 3 describes the design of a vertically stacked NS-TFET device with three layers. In our proposed work, the design parameters of the NS-TFET device are optimized to achieve good electrostatics. To the best of our knowledge, no tunneling-based Silicon stacked nanosheets with P-I-N configuration have been reported in the literature. Section 4 highlights the performance metrics of NS-TFET. The ultimate aim of NS-TFET is to tune the tunneling barrier at the extended source-channel junction; thereby reducing short channel effects such as low leakage current, minimal DIBL, and superior Subthreshold swing. Section 5 explains the drawn conclusions.

Calibration Characteristics

Vertically stacked Nanosheet transistors exhibit excellent ON-current density due to their increased effective width. The reference model of NS-FET with three layers having CPP of 48nm, the gate length of 12nm, and a sheet thickness of 5nm are simulated on a visual TCAD platform [21]. The inner spacer thickness and the width of NS-FET are kept at 5nm and 50nm respectively. The vertical sheet-to-sheet spacing is 10nm. A combination of high-k dielectric material HFO_2 having thickness 1.28nm and SiO_2having thickness of 0.5nm has been used for effective oxide thickness of 0.7nm. The symmetrical source and drain doping have a value of $3x10^{20}$ cm^{-3}while the channel doping is $1x10^{17}cm^{-3}$. Titanium Nitride material has been selected for gate with gate metal work function of4.7eV. The calibration graph of the simulation result is benchmarked with the experimental data at a drain voltage of 0.65V as shown in Fig. 1.

Device Structure

The dimensions of NS-TFET are in accordance with the reference structure [21]. The proposed NS-TFET device differs from the NS-FET device in terms of the type of doping. The reference structure has n-type symmetrical doping in both source and drain [21] while in NS-TFET; asymmetrical P-I-N configuration has been employed. P-I-N design with BTBT mechanism shows tremendous improvement in short channel effects (SCE). In the BTBT mechanism, the width of the tunneling barrier is modulated on the variation of gate voltage at constant drain voltage. The asymmetric lower drain doping is used to curb ambipolar behavior [22–23]. Work function engineering has been done to achieve desirable results. For simulation of NS-TFET, the work function is chosen to be 5.00eV. Figure 2a represents the 3-D view of NS-TFET. Figure 2b depicts a cross-sectional view of NS-TFET with P-I-N configuration. The geometric parameters, doping concentrations of NS-TFET are listed in Table 1.

Physical models used in Genius code define the behavior of semiconductor devices [22]. These models specify physical parameters like mobility, recombination rate, etc. Drift-Diffusion (DD) model is the

fundamental solver for Poisson's and continuity equations [23] and has been recommended to use for determining the transport of charge carriers and computation of the drain current. The Lombardi model is invoked for carrier mobility in the inversion layer of the NS-TFET device. This mobility model incorporates bulk mobility, mobility due to surface charge, and scattering [24]. Gate tunneling plays a pertinent role in NS-TFET devices. Kane's Model invokes the BTBT mechanism for carrier generation. For 3D simulations; Kane's model provides better convergence results [31]. Shockley-Read-Hall (SRH) model has been considered for carrier recombination mechanism and it stimulates the leakage current that determines Ioff in TFETs [32].

Table 1
The design parameters of vertically stacked NS-TFET

Parameters	Dimension
Gate length (L_g)	12nm
Gate work function of n-NS-TFET	5.0eV
Gate work function of p-NS-TFET	4.23eV
Source Doping *(Na)*	$3x10^{20}$ cm^{-3}
Drain Doping, *(Nd)*	$1x10^{17}$ cm^{-3}
Channel Doping, *(Nch)*	$1x10^{16}$ cm^{-3}
Effective oxide thickness, *(EOT)*	0.7nm
Nanosheet width, *(Ns_W)*	50nm
Nanosheet Thickness, *(Ns_Th)*	5nm

Results And Discussion

Three-dimensional simulations of NS-TFET are done using COGENDA-TCAD software [24]. The physical models such as the DD model, Lombardi mobility model, Kane's BTBT model, and SRH model are evaluated at each mesh node using TCAD software. The performance metrics of vertically stacked NS-TFET device has been discussed in this section.

4.1 Triple nanosheet

Gate all-around devices provide little room for carriers to drift when the transistor is in ON state [25]. The stacking of nanowires increases the effective width and allows the carriers to flow, but the increased device capacitance along with surface roughness decreases the speed of carriers [26]. Stacking thin nanosheets atop one another enhances the effective width and hence provides larger room for carriers to

flow. This further enables the large drive current while maintaining constricted control of the leakage current [25–26].

We have performed the simulations for vertically stacked single, double and triple NS-TFETs at the drain to source voltage (Vds) of 0.65V. The plot of drain current of single nanosheet (Id_1ns), double nanosheet (Id_2ns), and triple nanosheet (Id_3ns) is depicted in Fig. 3. The results show that ON-current increases exponentially in the case of double and triple NS-TFETs as compared to single NS-TFET. The drain current of Id_3ns and Id_2ns is observed to be 2.0168 and 3.03 times higher than Id_1ns respectively. Ion/Ioff ratio in triple-stacked NS-TFET is 9.557 times that of single NS-TFET while with double-stacked NS-TFET, it is observed to be 4.73 times high. Hence, three-layered NS-TFET exhibits superior performance in terms of drive current

4.2 Energy Band Diagram

The NS-TFET exhibits similar behavior to that of n-TFET on the application of constant drain voltage. In NS-TFET, an interband tunneling conduction mechanism has been incorporated. In the OFF state of the p-type extended source of NS-TFET, very few electrons are available at the conduction band of the source for injection into the channel. This results in negligible movement of carriers and hence poor leakage current. With variation in the gate voltage, the energy band of the channel varies relative to the extended source. From Fig. 4, it is evident that at saturation voltage of Vds = 0.65V with positive gate to source voltage (Vgs > 0V), the valence band of the extended source is aligned with the conduction band of the channel. The carriers tunnel through the potential barrier between the valence band of the extended source and the conduction band of the channel. These charge carriers present in channel drift towards the extended drain (ext_d) to produce drain current.

4.3 On Current and OFF current

Figure 5 depicts the transfer characteristics of NS-TFET. In the off state of TFETs with zero gate to source voltage, the movement of charge carriers from the valence band of the extended source region into the channel region is hindered due to large tunneling barrier width. Hence, the leakage current is extremely low. In the off state, linear leakage current(I_Lin) is of the order 10^{-16}A at gate voltage Vgs = 0V with drain voltage Vds = 0.10V. On application of positive gate voltage, bandgap modulation takes place as shown in Fig. 4. With the gradual increase in gate bias, the bands of the channel are lowered; thus enabling more electrons to tunnel from the valence band of the extended source into the conduction band of the channel. The tunneling barrier width is reduced near the extended-source channel region leading to a steep increase in the drain current. At saturation voltage of Vds = 0.65V, leakage current is of order 10^{-14}A. The saturation ON current (I_sat) reported is $1.26x10^{-5}$A at Vds = 0.65V with Vgs = 1.2V. Thus, the Ion/Ioff ratio for three-layered NS-TFET is $1.101x10^{11}$. This high Ion/Ioff ratio is desirable for high-performance nanoscale devices.

Table 2
Figures of merit of NS-TFET

Figures of Merit	Values of n-NS-TFET	Values of p-NS-TFET
Leakage current	$1.0144x10^{-16}A$	$1.16147x10^{-16}A$
Ion/Ioff ratio	$1.101x10^{11}$	$9.378x10^{11}$
Threshold Voltage	0.402V	0.400680V
DIBL	10.5	11.4
Subthreshold swing	23mv/decade	23.786mv/decade

4.4 Sub-threshold swing and DIBL

The main premise of designing NS-TFET as an alternative to NS-FET is due to its refined subthreshold swing. NS-FETs operate on a thermionic injection mechanism and thus have a thermal limit of 60mv/decade [27]. In NS-TFETs, the BTBT conduction mechanism is utilized. NS-TFET offers desired steep SW of 23mv/decade at low Vds = 0.10V with the desired ON-state performance. For this subthreshold regime, the threshold voltage is 0.402 V and negligible Drain induced barrier lowering (DIBL) of 10.5 is found. SW gives a higher Ion/Ioff ratio and thus makes itself apt for faster switching circuitry. Table 2 represents the performance metrics of NS-TFET in terms of threshold voltage, SW, DIBL, etc.

4.5 Ambipolairty

The transfer characteristics of three-layered NS-TFET under different doping concentrations have been represented in Fig. 6. It is evident from the figure that NS-TFET shows its ambipolar behavior when it is subjected to the negative gate to source voltage(Vgs < 0V). The electrons tunnel from the channel to the conduction band of the extended drain and thus results in the current flow of the same polarity and hence behave as p-type. This behavior is not desirable in digital circuitry where tunneling between channel and drain is curbed [28–30]. The best results are observed for the doping concentration of $10^{17}cm^{-3}$. It is evident that with the decrease in the doping concentration of drain, an ambipolar current is reduced up to a considerable amount. The depletion width of the drain side increases due to lower drain doping concentration. As a result, ambipolar current reduces.

4.6 Transconductance(g_m),Transconductance generation efficiency(TGF) and Total Gate Capacitance(C_{gg})

Transconductance (g_m) is a performance metric, which reflects the device efficiency in terms of effective input voltage conversion into output current [31]. It is described by first-order differentiation of drain current with reference to the gate to source voltage [32].

$$g_m = \left.\frac{\partial I_{dd}}{\partial V_{GS}}\right|_{V_{DS}} \quad \text{(A)}$$

where I_{dd} represents current tunneling from the source terminal to the drain end. V_{gs}, V_{ds} represents the gate to source voltage and constant drain voltage respectively.

Transconductance generation efficiency (TGF) is another vital parameter that determines the efficiency of NS-TFET in terms of conversion of the current into transconductance (g_m) and is given by [33].

$$TGF = \frac{g_m}{I_{dd}} \text{V}^{-1} \quad \text{(B)}$$

Figure 7a and 7b represent the variation in transconductance and TGF with respect to the gate-source voltage respectively. It is unambiguously clear that NS-TFET exhibits comparatively higher transconductance due to the hike in tunneling of carriers in the channel. For the selected value of I_{dd}= 10^{-10} A, TGF is found to be $54V^{-1}$.

The plot of the variation of total gate capacitance (C_{gg}) with respect to Vgs is depicted in Fig. 7c. C_{gg} at Vgs = 1V is found to be $1.662x10^{-17}$F.

p-Ns-TFET design:

The vertically stacked NS-TFET with N-I-P configuration has been designed to demonstrate its p-type characteristics. The geometry parameters are kept the same as mentioned in Table 1. Work function engineering has been implemented to match ON and leakage currents. For p-SN-TFET, the work function is kept at 4.23eV. The source has donor impurities with a concentration of $3x10^{20}$ cm^{-3} while the drain has acceptor impurities having a concentration of 10^{17} cm^{-3}. The transfer characteristics of p-SN-TFET at linear voltage Vds= -0.10V and saturation voltage of Vds=-0.65V are simulated using TCAD. The simulation results of both p and n-type at linear and saturation voltage are displayed in Fig. 8. The performance metrics of p-NS-TFET are mentioned in Table 2.

Conclusion

In this paper, vertically stacked NS-TFET with three layers has been modeled and simulated. The short channel effects have reduced tremendously by using the BTBT mechanism with P-I-N configuration. A high Ion/Ioff ratio with a low leakage current has been achieved. The steep subthreshold swing of 23 mv/decade with negligible DIBL makes NS-TFET useful for low power applications. High Transconductance, device efficiency, total capacitance parameters of NS-TFET have been extracted. p-TFET configuration for NS-TFET has also been proposed which makes it apt for faster switching

applications. All these advantages make NS-TFET a viable option for next-generation applications and towards future advancements.

Declarations

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Conflicts of interest/Competing interests the authors have declared that no competing interests exist.

Availability of data and material Not applicable

Code availability Not applicable

Compliance with Ethical Standards This study was ap-proved by the university research ethics committee. All procedures per-formed in this study follow the ethical standards of the institutional and research committee.

Consent for publication Yes

Authors' contributions All authors contributed to the design and simulation. Material preparation, data collection and analysis were performed by Garima Jain, Dr. Ravinder Singh Sawhney, Dr. Ravinder Kumar and Amit Saini. The first draft of the manuscript was written by Garima Jain and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

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Figures

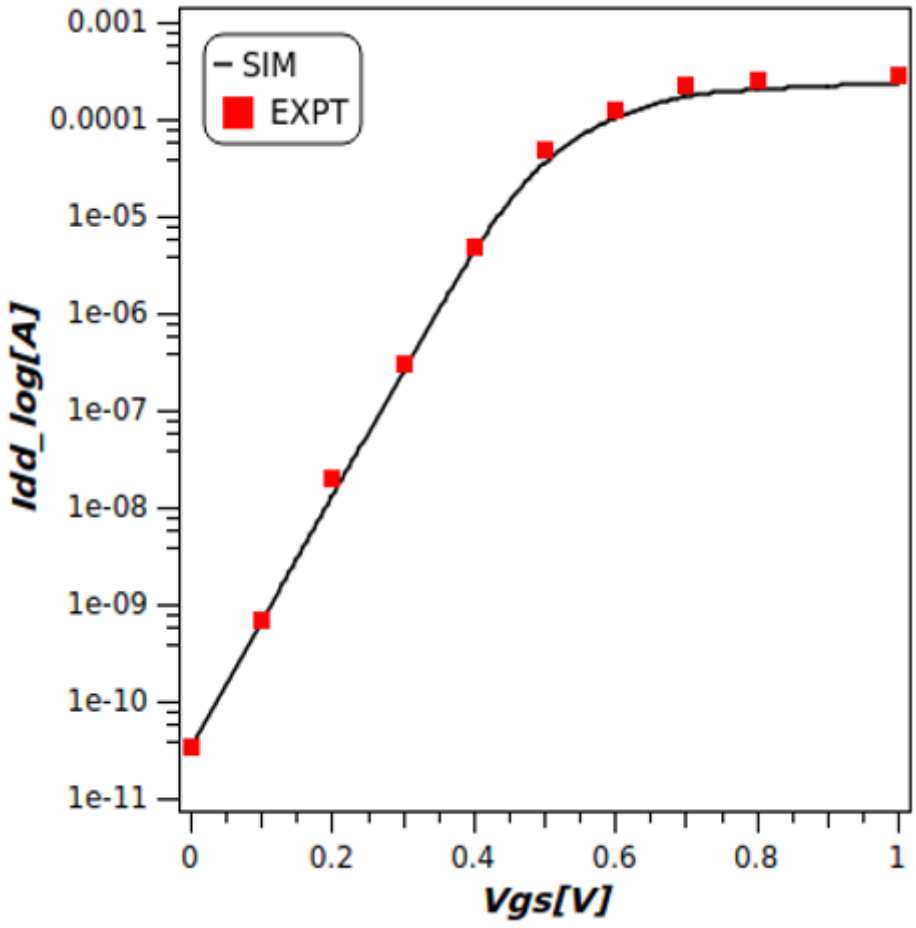


Figure 1

Calibration graph of transfer characteristics of NS-FET [21]

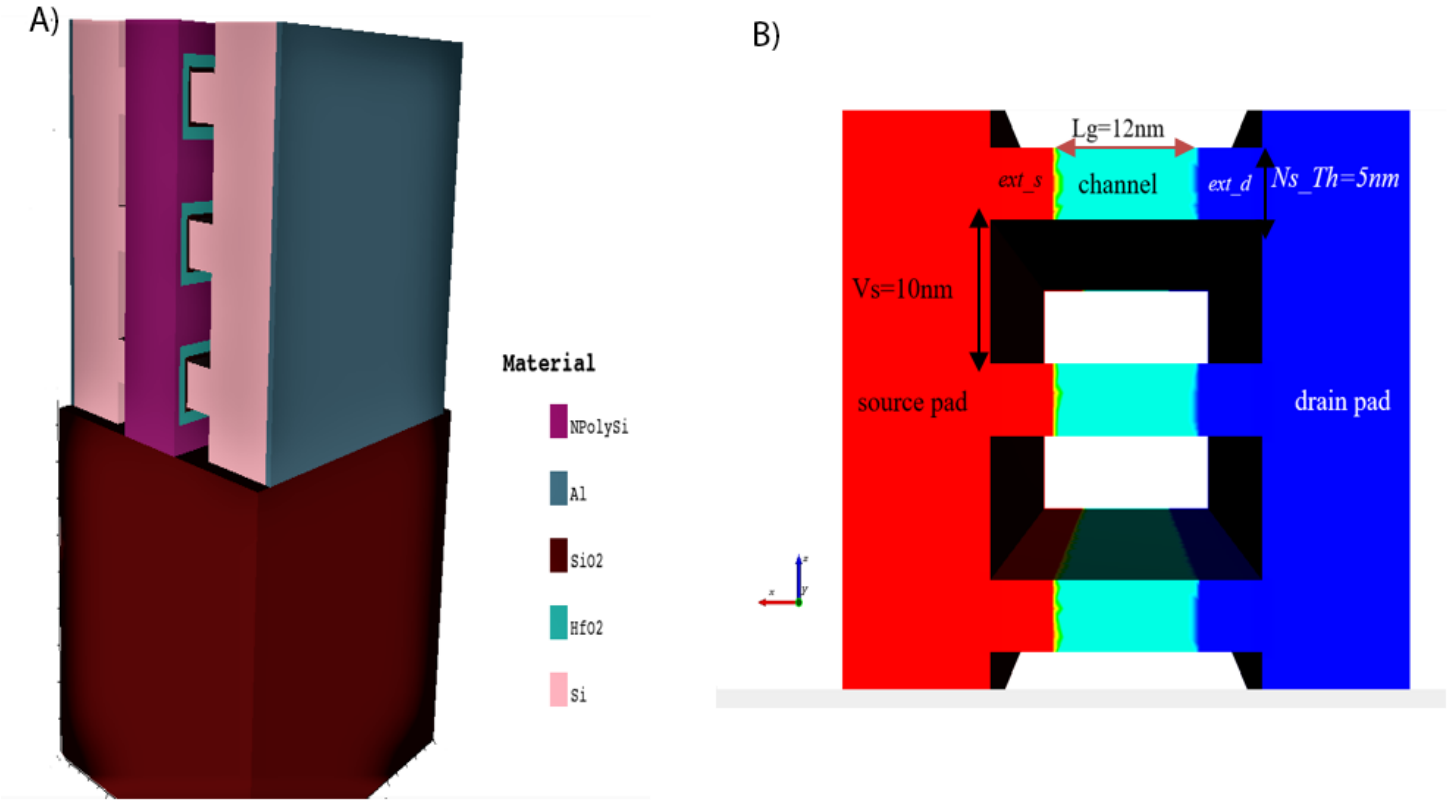


Figure 2

a: 3-D view of NS-TFET. b: Cross-sectional view of P-I-N tunneling NS-TFET

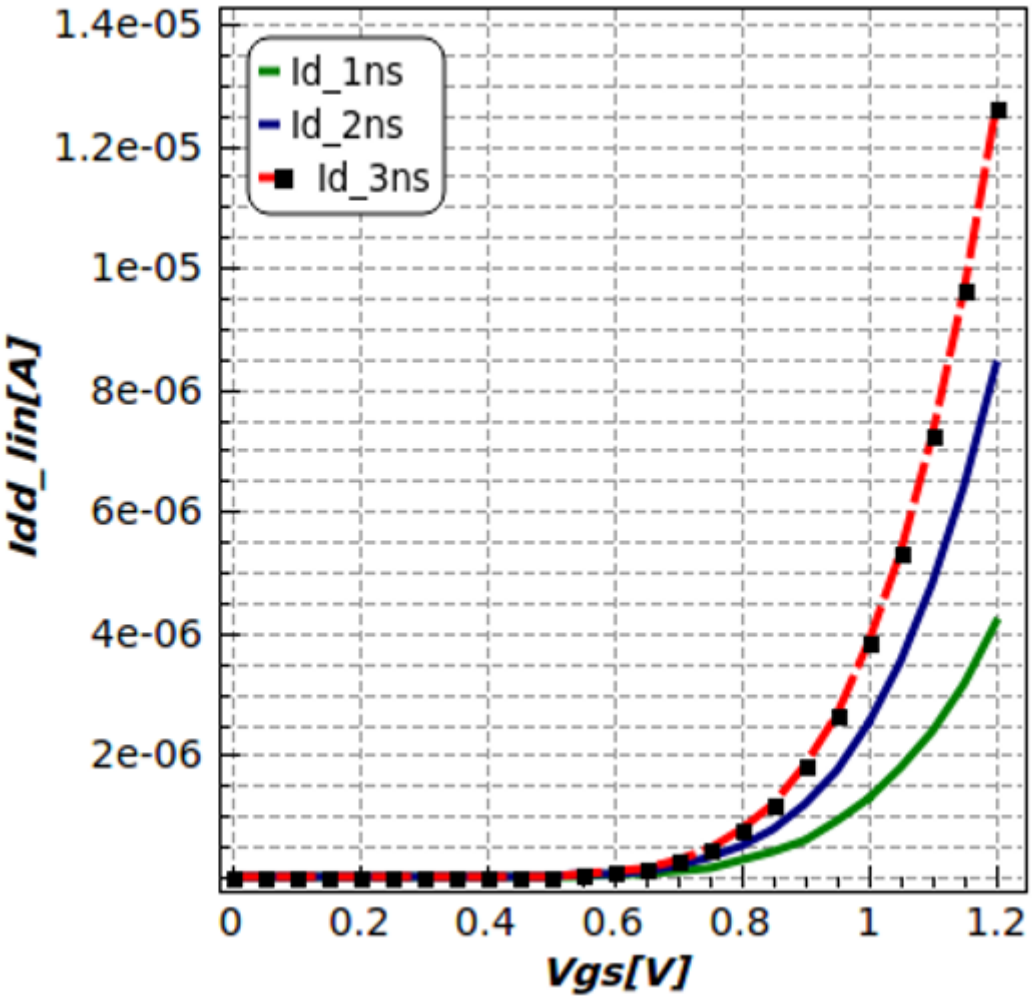


Figure 3

Simulation for single, double, and triple-stacked NS-TFET.

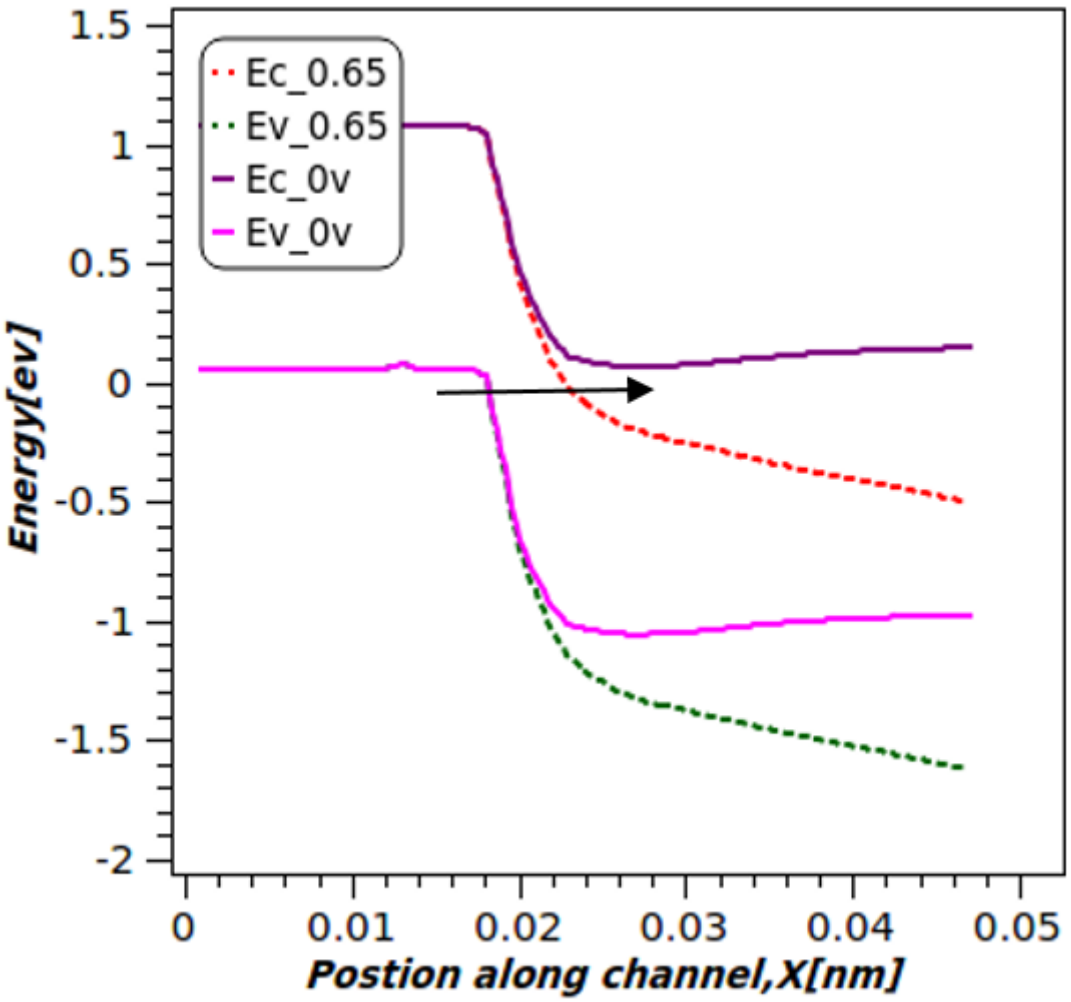


Figure 4

Band diagram of the middle layer of NS-TFET at OFF state (Vgs=0V) and ON state (Vgs>0)

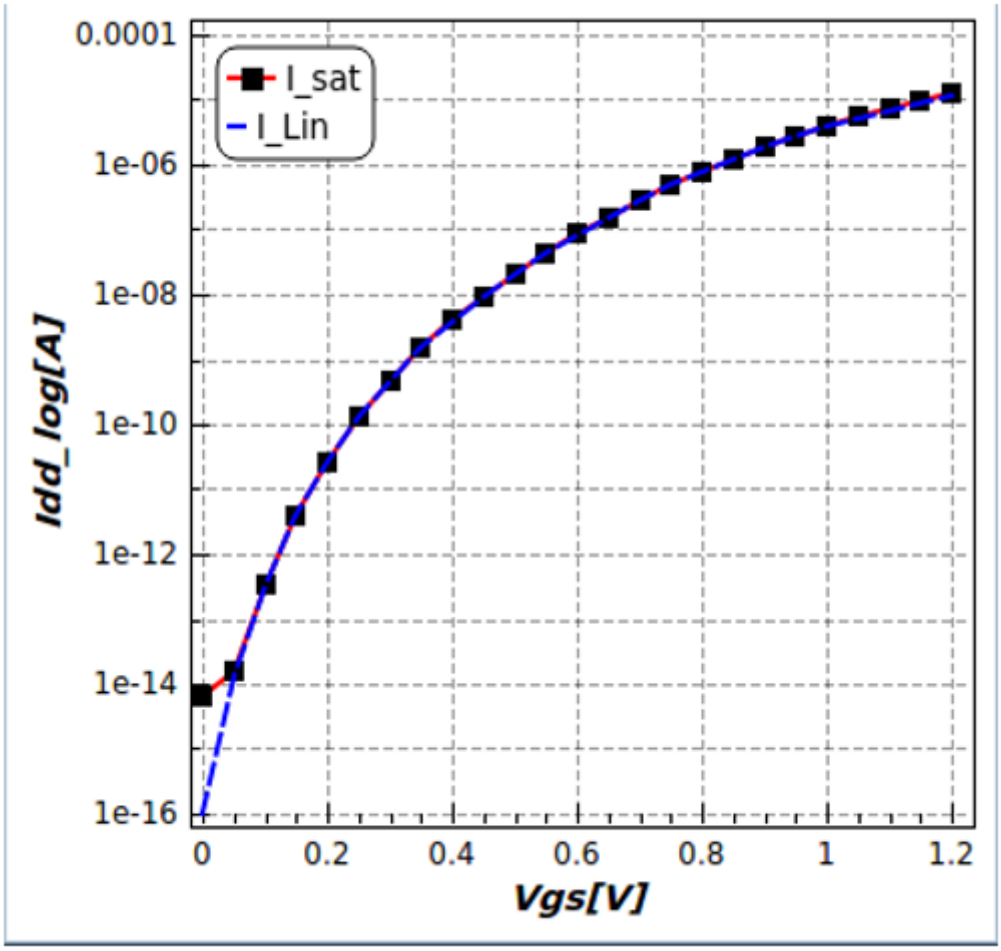


Figure 5

Transfer characteristics plot of NS-TFET at Vds=0.10V and Vds=0.65V

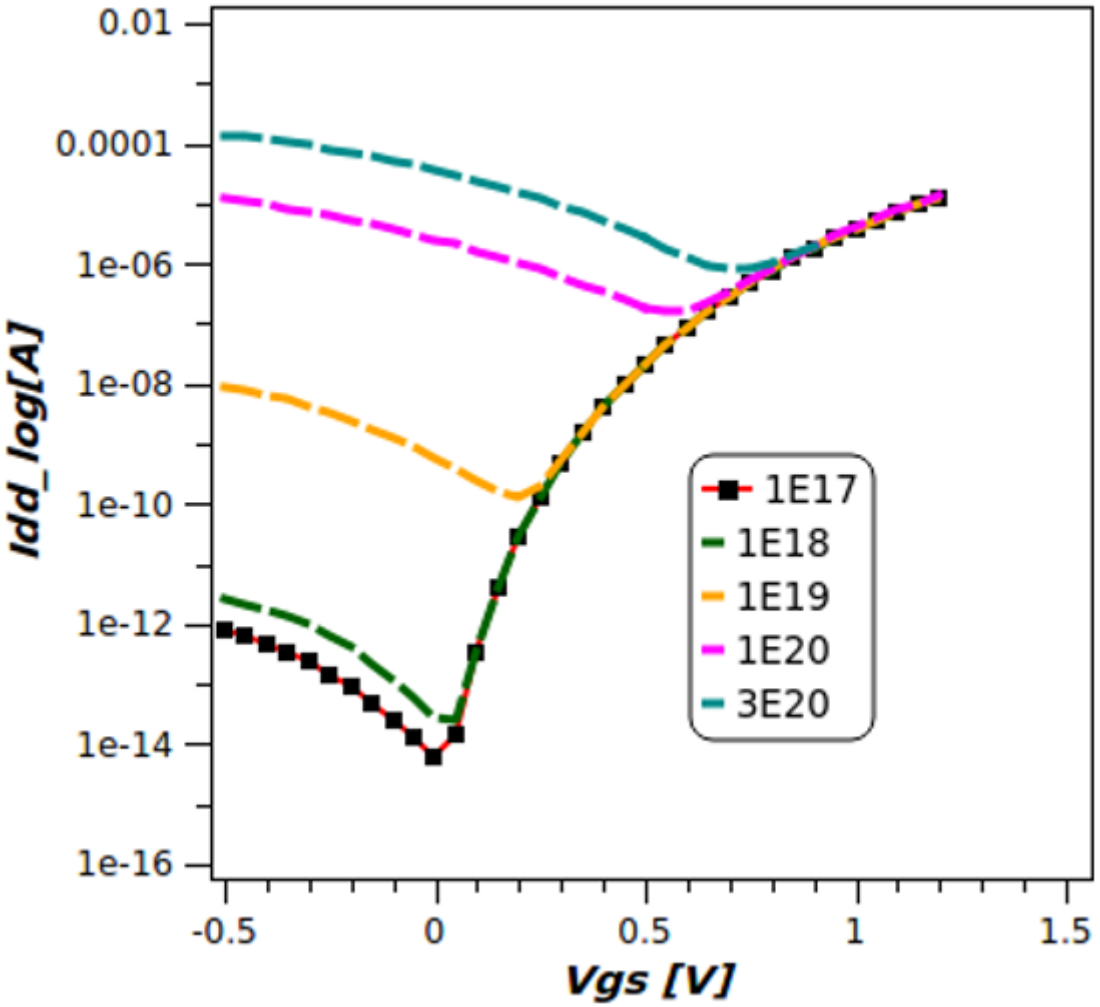
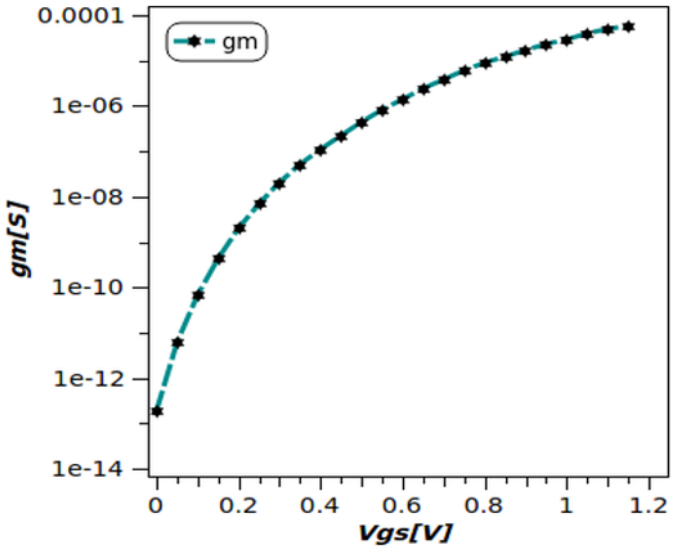
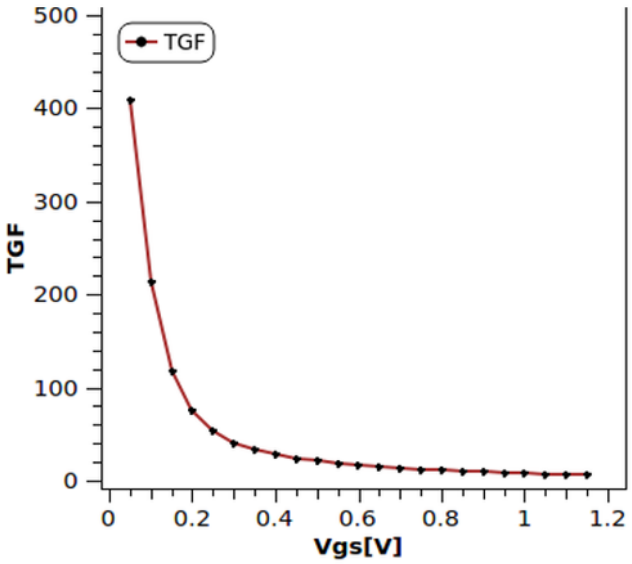


Figure 6

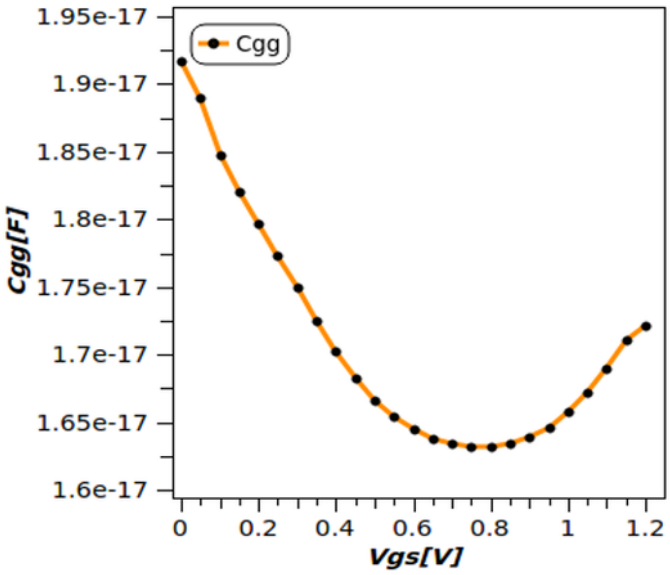
Transfer characteristics curve under different drain doping concentrations.



A)



B)



C)

Figure 7

a: Transconducatnce graph of Ns-TFET device. b: TGF plot of Ns-TFET device. c: Total gate capacitance (Cgg) plot of Ns-TFET device.

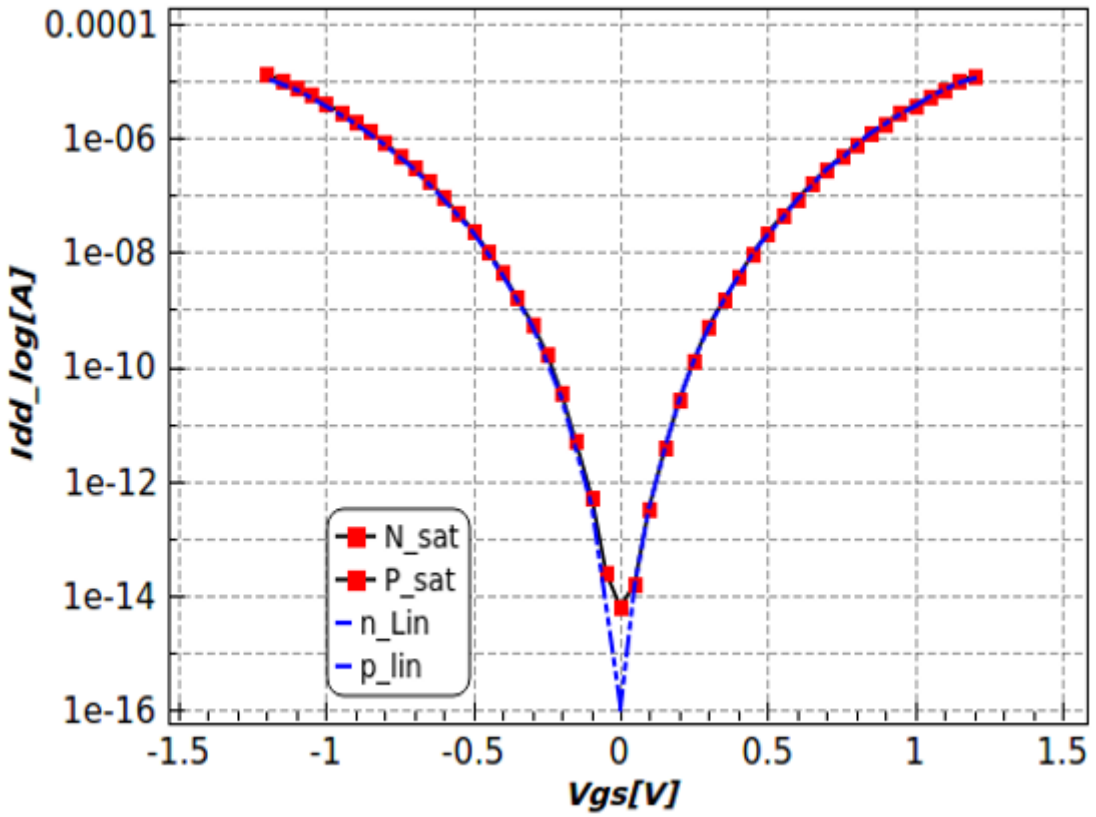


Figure 8

Transfer characteristics plot of p-NS-TFET device.