

# Design And Implementation of An Ultra-Low Power Bose Chaudhuri Hocquenghem Encoding Based Body Channel Communication For Medical Applications

Vijayalakshmi Sankaran (✉ [sankarviji7@gmail.com](mailto:sankarviji7@gmail.com))

Veltech: Vel Tech Rangarajan Dr Sagunthala R&D Institute of Science and Technology

<https://orcid.org/0000-0003-2146-5838>

Paramasivam Alagumariappan

B S Abdur Rahman Crescent Institute of Science & Technology

Nagarajan V

Adhiparasakthi Engineering College

Sankaran E

GRT Institute of Engineering and Technology

---

## Research Article

**Keywords:** Analog Front-end Printed Circuit Board, Bit Error Rate, Body Channel Communication, Bose-Chaudhuri-Hocquenghem, Consecutive Identical Digit and Field-Programmable Gate Array

**Posted Date:** April 22nd, 2021

**DOI:** <https://doi.org/10.21203/rs.3.rs-438733/v1>

**License:** © ⓘ This work is licensed under a Creative Commons Attribution 4.0 International License.

[Read Full License](#)

---

# Abstract

This paper proposes the Bose–Chaudhuri–Hocquenghem (BCH) encoding based Body Channel Communication (BCC) for medical applications by ultra-low power consumption. The transmitter uses channel of 1-100 MHz frequency to enhance the transmitter frequency and time domain properties. The BCH based BCC transmitter uses two stage low power analog processing circuit and digital information restoration circuit. The analog processing circuit consists of capacitor coupled adjustable preamplifier. In addition to that a body channel communication (BCC) transceiver with BCH codes modulation is proposed. In the BCC transceiver side, sensed data are encoded into BCH code format, and then the chosen BCH codes restrict the maximum consecutive identical digit (CID) to rise the data transmission rate. In the BCC receiver side, we use an analog front-end (AFE) circuit board to amplify the attenuated signal from the transmitter and restore the signal to the digital waveform. After the 8x oversampling sampler and vote integrator recovery the clock and data, the BCH code demodulator demodulates the original data. The proposed BCC transceiver has higher data reliability because of the orthogonal characteristic of BCH codes. Moreover, the proposed BCH code concatenated method strengthens the jitter tolerance and improve the code rate. The proposed BCC transceiver was verified on a field-programmable gate array (FPGA) board. The Proposed Data transceiver achieves data rate of 100 Mbps, Also, the BER value is  $< 10^{-6}$  and  $< 10^{-5}$  at 60 Mbps and 100 Mbps, respectively.

## Introduction

Contemporary communication techniques sum up to simple and competent means of interaction between humans [1]. They include smartphones, entertainment through satellite communication, astronomical exploration, etc [2, 3]. Modern communication systems have been gradually heading in the direction of body-centric techniques for various applications including health care systems, consumer electronics, human-machine interface, diet management, security, memory aid and defense purposes [4]. The market for wearable devices is encouraging and it is anticipated to leap from millions to billions in the near future. The effective and novel efforts on the hardware miniaturization of devices and sensors have made communications on the human body more expedient using wearable wireless nodes [1, 5–7]. Modern advances in pervasive and mobile computing have seen a vivid progress in interest for wearable technology. Wireless Body Area Network (WBAN) constituting wearable sensors and systems have progressed to the extent, they can be considered equipped for clinical applications. This has been possible due to the combined effect of increase in research dedicated to this area in the past few years and also due to the huge number of enterprises that have in recent times started financing bountifully in the improvement of wearable products and systems [1, 8–10]

Rapid advancement in miniaturization of unit computing has led to widespread availability of low-cost, tiny form-factor computing units. This has propelled the growth of wearable devices like smart watches, fitness trackers, smart ear phones etc [11–14]. This growth is expected to continue in the future and soon the average human will have multiple interconnected wearables on his/her body [15]. With everyone carrying a significant amount of information on-body, people will seek to exchange them in a secure

manner creating a human body area network (BAN) [16, 17]. Such BANs will require energy-efficient and secure ways for these wearable devices to communicate. Human Body Communication (HBC) is potentially a strong alternative to Wireless Body Area Network (WBAN) for wearables as it meets both these requirements. Energy efficiency comes due to the human body showing significantly low loss compared to air for radio frequencies. Also, it is easier for an attacker to snoop radio signals from air than from a human body making HBC more secure than WBAN [18].

The idea of HBC for Personal Area Network (PAN) was introduced by Zimmerman in [2]. In this work both the transmitter and receiver have a pair of electrodes and communication takes place via the transmitter capacitively coupling a displacement current into the human body, that is picked up by the receiver. In [3] the authors introduce Galvanic coupling for HBC. Two electrodes are used to induce current into the human body and two others to measure the potential difference. The primary bottleneck of HBC is due to the human body acting as an antenna in the FM frequency band leading to significant interference. Adaptive Frequency Hopping [4] and fixed narrowband signaling [5] techniques have been used to solve the interference problem. But they suffer from energy inefficiency due to the use of high carrier-frequencies, narrowband-signaling with agility requirements.

Recently, healthcare products and gadgets are increasingly more well-known, and wireless body region network (WBAN) is generally utilized to apply above applications. In wireless conversation, Bluetooth, ZigBee, and Radio Frequency Identification (RFID) are well-known techniques. The reduced data rate, huge power usage are complications on wireless conversation. Furthermore, the RF transmitting offers many interferences in the surroundings. Body channel conversation (BCC) utilizes body as a conversation moderate to transmit data. It provides characterizations of a higher data rate and fairly low power usage [1–5]. The BCC technology can conquer complications of wireless conversation. In [1, 4], a wide-band signaling (WBS) scheme is usually adopted in the look of the BCC transceiver. Jitter accumulation and duty-routine distortion happen when the transmission transmits through a body. This situation escalates the problems in recovering data in the receiver component. In [2], a frequency-change keying (FSK) modulation scheme is used. The frequencies of the FSK ought to be chosen carefully in order to avoid the popular rate of recurrence bands. The additional drawback may be the active band pass filters needed in the dual-band receiver used a large chip area. In [3], an orthogonal frequency-division multiplexing (OFDM) BCC transceiver offers been proposed. Although the OFDM based transceiver can boost the info rate, additionally there is high power intake and occupies huge chip area. In this paper, an FPGA-centered BCC transceiver is definitely offered. In the transceiver, the followed BCH code modulation strategy can enhance the info reliability. Furthermore, the concatenated technique can boost peak to peak jitter tolerance to 25ns at 12.5Mcps with four 4-bit BCH codes concatenated.

The paper structured as follows. Section II describes about the proposed architecture. Automatic gain enhancement described in the section III. section described about the simulations results. Section V describes about the conclusion.

## Methodology

## ***2.1 Study of Characteristics of Human Body Channel***

For implementation of Body channel communication system-based BCH encoding scheme analysis of human body channel properties is important for design and optimization of BCC transmitter with better performance. The main key factor for calculation of operation frequency and architecture of BCC transceiver is characteristics of human body channel. In modern BCC transceivers the return path is constructed using coupling between the BCC transmitter and BCC receiver electrodes. Previous researches reported that human body channel having variation depends on environmental conditions. Also, the previous researches results show that the channel response was inconsistent when the operating frequency falls below 10 KHz in BCC receiver end.

Human body channel matching nearly same property like wired channel properties, we can use human body as broadband communication applications. Though designing of wireless bcc transceiver overall power consumption is a important factor, the primary requirement for designing BCC transceivers is lowest operating frequency and minimum latency requirements. But the human body channel produces more loss in low frequency operations, so that it is necessary to design a BCC transceiver with high sensitivity ratio with low operating frequency's below 30 kHz.

## ***2.2 Measurement Proposed of Human Body Channel Transmitter***

In our Proposed RF based BCC transmission scheme the transmitter and receivers are connected with the human body using the electrodes independently. They have used air as a medium to send and receive signals. The Fig. 1 represents the architecture of BCC transmission scheme. BCC transceiver offers a high data rate and very low power usage than other wireless transceivers like Bluetooth. Already many researches currently going on Human Body Channel Communication [2, 3]. The transmission data rate and power usage directly depend on the distance between and operating frequency. Previously the BCC transmitters are designed using the different modulation schemes and architectures. frequency-shift keying (FSK) modulation-based body channel communication transmitters are proposed in previous research. A 100 MHz source voltage sent to transmitter to sensor placed on the human body periodically to calibrate the operating frequency. We have proposed BCH error correction code-based BCC transmitter reduce the overall operating power and cost reduced. The proposed BCC transmitter uses a 60 MHz transmission channel to achieve a better data rate. The proposed BCC transceiver utilizes two independent channels of 60MHz, one fixed at 60MHz (L-band) and the another one at 100 MHz (H-band) to achieve a high data rate. Though, the active bandpass filters essential in the dual band BCC receiver engaged a large chip area.

## ***2.3 Design Model for Human Body Channel***

From the resultant of the BCH based BCC transmitter measured results, the basic wireless channel model is implemented for proposed transceiver implementation. Proposed BCC transmitter uses Ideal bandpass filter for circuit model based on the measured results of 1-100 MHz operating frequency. Also, the bandpass filter is a combination of Both low pass filter and high pass filter as a 1st order and 2nd order

function illustrated in Fig. 2. We can achieve a desired frequency and characteristic by varying the resistors and capacitors present in the circuit model.

### ***2.4 Proposed Architecture***

The overall architecture of proposed BCH based BCC transmitter shown in the Fig. 3. The overall architecture of the proposed transceiver includes the transmitter and receiver separately with analog frontend. First, the analog sensor place on the body transmits the sensed data to the block memory space of the TX FPGA through the digital user interface. Following the data kept ready and so are modulated with BCH codes, the information will go through the body channel to an AFE table to amplify the attenuated transmission. After that, the BCC receiver with an 8x oversampling clock and data recovery (CDR) circuit to revive the clock and data. Subsequently, the BCH code demodulator demodulates data to the initial data. Finally. The BCC receiver transmits the received data to the system to show the mass media data.

In this paper BCH Code based low power reliable BCC transmitter is proposed. In the proposed BCC transceiver BCH error correction scheme is proposed to reduce the overall bit error rate (BER). Additionally, we proposed automatic gain enhancement method which can adjust the desired gain level for operation based on the temperature and voltage variations.

### ***2.5 Receiver Architecture***

Based on the wireless channel characteristic two stage analog signal processing and data encoding circuit was proposed in BCC transceiver side as displayed in Fig. 3. Capacitive coupling preamplifier proposed in first stage of the transmitter topology. This circuit will minimize the current leakage and enhance the analog signal for better processing. Also, the high pass filter offers the random interference elimination.

To handle the changes in the signal amplitude due to the variation in the path loss and different channel length, an automatic gain enhancement circuit is proposed in the second stage to maintain a desired gain depends upon the power and temperature variations. To reduce the further current dissipation Schmitt trigger-based comparator is proposed. We introduced self-gain enhancing circuit in maintain a gain level according to the amplitude of received signal strength. Also, it increases the overall stability of the input signal belongs to data recovery circuit. Proceeded by analog signal processing circuit and data recovery circuit we proposed BCH encoding based data recovering methodology to reduce the bit error rate in BCC transmitter. This system is capable of automatic correction of its data during random data fault.

### ***2.6 Wideband Pre-Amplifier***

The signal sensed by the analog sensor using proposed BCC transceiver belongs to no DC offset and narrow width weak signal. To process these signals sensed by the sensors it should be amplified with appropriate preamplifier to satisfy the desired Wide Bandwidth. Also, the sensed narrow band signals have random common data interference due to human body current conducting property. To handle these wideband sensed signals previously the BCC transceivers uses a Coupling capacitor to eliminate these

random data interferences, then the signal surpasses the necessary bias circuit to produce proper common mode voltage. Finally, the operational amplifier used to amplify the received signal.

Also, another conventional BCC receiver uses a dual differential op-amp based circuit as preamplifier with high common mode rejection ratio (CMRR). This conventional preamplifier capable of high interference elimination ratio and convert all the sensed differential signals into accurate differential common mode voltage. The main drawbacks of bot conventional amplifiers present in the previous BCC receivers are overall power consumption. The reported preamplifier uses a monetary bias circuit to achieve a suitable common mode voltage. This bias circuit dissipates the nearly 1.9 mA current, which is 40% of overall BCC transmitter power consumption. Meanwhile another differential dual op-amp structure also dissipates high power, this is not suitable for minimum power WBAN uses. Finally, to decrease to overall power dissipation in analog signal processing circuit we have proposed capacitor coupled preamplifier with wideband signals. This proposed preamplifier is independent of extra bias circuit and uses the bandpass filtering properties. The overall circuit of proposed preamplifier shown in Fig. 4.

The conventional preamplifiers are based on resistor feedback networks and the bias circuit is monitory to get proper DC signal offset. But the proposed capacitor coupled wideband preamplifier shown in Fig. 5 (a) is capable of sensing very weak narrow band signals against the interference of human body potential. Getting into working of proposed preamplifier the sensed pulse signals coupled directly through the  $C_{in}$  negative op-amp, same time the remaining circuits are properly biased by the positive op-amp which is leads to the reduction of extra biasing circuit it results the less power consumption. The self-bias circuit based preamplifier is shown in Fig. 5 (b)

## ***2.7 One Bit Digitizer***

After passing the data through the preamplifier of BCC transmitter the sensed data should be converted into positive and negative pulse series depends upon the sensed analog signal. Once amplification process is over the comparator uses to sampling signal into "1" or "0" with respect to the sample. The frequency range of 1-100 MHz should be allowed through the band pass filter to the proposed BCC transmitter.

The inconsistency in the bandwidth due to the different channel conditions leads to variations in the  $V_{pp}$  after the gain amplification. To deal with the variations in the  $V_{pp}$  we uses threshold adjustable hysteresis comparator. However, the conventional hysteresis comparators affected by unpredictable threshold voltage due to the Power and temperature variations. This will results the variations in the digitization duty cycle randomly. Therefore, to improve the digitization stability of comparator we have proposed completely adjustable power a temperature independent Schmitt trigger-based hysteresis comparator, as displayed in Fig. 6.

We have proposed the Schmitt trigger based on inverter and comparator combination, in which is results the low power consumption and low static current usage. To maintain a desired hysteresis threshold, we use two stage upper and lower voltage tuning branches in inverter (MP11) and comparator (MN11)

model. Depends upon the lower threshold voltage (VTL) and upper threshold voltage (VTH) the inverter and comparator will be operates. Two sets of controlling signals are used to control the corresponding voltage tuning branches separately.

### ***2.8 BCH based Data Encoding Circuit***

In the 8x oversampling sampler and vote integrator is used to recover the clock and data. The 8x oversampling sampler samples eight data at one symbol period. The vote integrator uses these data to determine the recovery data and produces the recovery clock. The BCH code demodulator demodulates 16-bit BCH codes to 5-bit original data after Hamming distance calculation. In the LFSR checker, the same random data sequence as TX is generated by the LFSR circuit. Thus, the LFSR checker can determine whether there have bit errors in random data mode. If the image mode is set, the RX\_DATA will be stored in the block memory. Subsequently, the data are transmitted through the UART interface to the PC #2.

The BCH code modulation in the BCC transceiver increases data reliability, but it also reduces the data rate (or code rate). In standard 16-bit BCH code [5], to avoid too long CID, the selected code words match the rule that the maximum CID is equal to two, and then the code rate is 1/8. Therefore, the concatenated methods of BCH codes are proposed to solve the problem of increasing data reliability with relatively high code rate. The chosen code words from 4-bit BCH codes are concatenated by four 4-bit BCH codes to form the 16-bit modulated codes. The Hamming distance between each code word ranges from 2 to 8, but the code rate is improved as 5/16. As compared to the standard 16-bit BCH codes [5] with code rate 1/8, the data rate of the proposed BCC transceiver with concatenated BCH codes can have 2.5 times speed up.

The architecture of the proposed FPGA-based transceiver is shown in Fig. 3. The transceiver consists of a transmitter (TX), a receiver (RX), and an analog frontend (AFE) circuit. First, the transmitter sends the sensor data to the block memory of the TX FPGA through the interface. After the digital data stored ready and are modulated and encoding using with BCH codes, the data will pass through the human body channel to an AFE board to amplify the attenuated signal.

Then, the receiver system with an 16x oversampling clock and data recovery (CDR) circuit to restore the clock and data. Subsequently, the BCH code demodulator demodulates data to the original data. And corrects the error present in the channel. Finally, the Receiver sends the received data to the memory. The BCC transmitter shown in Fig. 7 has two modes.

In random data mode, the LFSR circuit produces the random data for the transmitter. In random data mode, digital data from transmitter are stored in the Transmitter FPGA and then sent to the human body channel. The chosen sets of BCH code limit the maximum continuous identical digits (CID).

In the proposed BCC receiver shown in Fig. 8, the 16x oversampling sampler and vote integrator is used to recover the clock and data. The 16x oversampling sampler samples eight data at one symbol period. The vote integrator uses these data to determine the recovery data and produces the recovery clock. The BCH code demodulator demodulates 15-bit BCH codes to 7-bit original data after Polynomial distance

calculation. In the LFSR checker, the same random data sequence as TX is generated by the LFSR circuit. Thus, the LFSR checker can determine whether there have bit errors in random data mode. If the data mode is set, the RX\_DATA will be stored in the block memory. Subsequently, the data are transmitted through the receiver.

The BCH code modulation in the BCC transceiver increases data reliability, but it also reduces the data rate (or code rate). In standard 15-bit BCH code, to avoid too long CID, the selected code words match the rule that the maximum CID is equal to two, and then the code rate is 1/8. Therefore, the concatenated methods of BCH codes are proposed to solve the problem of increasing data reliability with relatively high code rate.

The chosen code words from 15-bit BCH codes are concatenated by 15-bit BCH codes to form the 7-bit modulated codes. The Polynomial distance between each code word ranges from 2 to 8, but the code rate is improved as 5/16. As compared to the standard 7-bit Hamming codes with code rate 1/8, the data rate of the proposed BCC transceiver with concatenated BCH codes can have 2.5 times speed up.

## Results And Discussion

Fig. 9 shows an overall jitter tolerance of BCH based BCC transmitter circuit at 100 Mbps. Fig. 10 shows the overall BER results of the proposed transceiver at 100 Mbps. From the Fig. 10 we get that proposed BCC transceiver results the  $10^{-7}$  BER ratio which is best when compares to the other transceivers.

Table I shows the overall comparison of proposed BCC transceivers with conventional designs. The Table I results that proposed BCC transceivers uses low area when compare to others. Also, the data rate and BER performance ratio also better when compare to conventional receivers. Overall power consumption of proposed BCC transceiver comparatively low than other transceivers.

### Table I Performance Summary

Parameters	[13]	[16]	[14]	[11]	[18]	[12]	Proposed Work
CMOS	180nm	130nm	180nm	90nm	65nm	65nm	90nm
Supply Voltage	1V	1.2V	1V	1V	1.V	1.1V	1V
Modulation Scheme	AFH FSK	Frequency Correlation	Double FSK	QPSK	FSK	Hamming FSK	FSK
Frequency	30–120 MHz	1–30 MHz	4–120 MHz	4–120 MHz	20–120 MHz	4–80 MHz	10–100 MHz
SIR	-65 dB	-60 dB	-62 dB	-60 dB	-60 dB	-56 dB	-55 dB
Data Rate	10 Mbps	8.5 Mbps	10 Mbps	10 Mbps	10 Mbps	60 Mbps	80 Mbps
Power usage	2.4 mW	0.6 mW	2 mW	2.2 mW	1.07 mW	1.00 mW	0.87 mW

Therefore, the proposed BCH based BCC receiver is usually certified for low-power transceiver ideal for energy-constrained essential data sensing program in WBAN.

Figure 11 displays the first-bit mistake simulation of the proposed BCC transceiver with data jitter to model the random sound in body channel conversation. The collection “CID = 2” means the overall performance of the BCC transceiver without needing BCH codes. The range “16-bit BCH-code” means the efficiency of the BCC transceiver with 16-bit regular BCH codes [5]. At 25 ns peak-to-peak data jitter, the BCC transceiver with 16-bit regular BCH codes [5] can perform BER  $< 10^{-8}$ . Nevertheless, the BCC transceiver with CID = 2 can only just achieve BER  $< 10^{-5}$ . The series “16-bit, four 4-bit BCH code concatenated” means the proposed concatenated technique, the BER functionality of the four 4-bit BCH code concatenated technique is preferable to 16-bit regular BCH codes when peak to peak data jitter significantly less than 25 ns. The simulation result demonstrates the four 4-bit BCH code concatenated technique offers better data dependability compared to the others even this technique has smaller sized Hamming range between code terms.

## Conclusion

A novel BCH encoding based BCC receiver proposed in this paper. From the analysis of both time and frequency domain implementation the proposed BCC transceiver with 1-100 MHz bandpass filtration system achieves an ultra-low power usage and high data rate. In transmitter side the data is encoded using the BCH encoder to reduce the bit error rate. In the receiver side the random data error can be corrected using the corresponding decoder. In addition, that automatic gain enhancement scheme is proposed to solve the power and temperature variations in the receiver side. This will result the reliable transmitter and receiver for BCC applications. The proposed BCC transceiver achieved 80 Mbps data rate and overall power dissipation of 0.87 mW and overall area occupied by the transceiver was 0.26 mm<sup>2</sup>.

Overall ECG signal system implemented and examined using the proposed BCC receiver circuit and results suggest that the proposed receiver achieves ultra-low power and suitable for Wireless Body Area Network.

## Declarations

**Funding** The author(s) received no financial support for the research, authorship, and/or publication of this article.

### Compliance with Ethical Standards

**Conflict of Interest** The author(s) declares no conflict of interest.

**Availability of Data and Materials** Not applicable.

**Code availability** Software application.

## References

- [1] Seyedi, M., Kibret, B., Lai, D.T.H., Faulkner, M (2013) A survey on intrabody communications for body area network applications. *IEEE Trans. Biomed. Eng.*, 60 (8), 2067–2079
- [2] Joonsung Bae et al, "A 0.24-nJ/b Wireless Body- Area-Network Transceiver With Scalable Double- FSK Modulation," *Solid-State Circuits, IEEE Journal of*, Vol.47, No.1, pp.310-322, Jan. 2012
- [3] X. Zhang, Z. Wang, "A Low-Complexity Three- Error-Correcting BCH Decoder for Optical Transport Network," *IEEE Trans. on Circuits and Systems*, vol. 59, no. 10, pp. 663-667, Oct. 2012.
- [4] Joonsung Bae et al, "A Low-Energy Crystal-Less Double-FSK Sensor Node Transceiver for Wireless Body-Area Network," *Solid-State Circuits, IEEE Journal of*, Vol.47, No.11, pp.2678-2692, Nov. 2012
- [5] C.-L. Chr, S.-L. Su, and S.-W. Wu, "A Low- Complexity Step-By-Step Decoding Algorithm for Binary BCH Codes," *IEICE Trans. Fundamentals*, vol. E88-A, no.1, pp. 359-365, Jan. 2005.
- [6] X. Liu, C. Lu, T. H. Cheng, and S. N. Koh, "A Simplified Step-by-Step Decoding Algorithm for Parallel Decoding of Reed-Solomon Codes," *IEEE Tran. on Communications*, vol. 55, no. 6, pp. 1103- 1109, Jun. 2007.
- [7] Hyunwoo Cho et al, "A 5.2mW IEEE 802.15.6 HBC standard compatible transceiver with power efficient delay-locked-loop based BPSK demodulator," *Solid-State Circuits Conference (A-SSCC), 2014 IEEE Asian*, pp.297-300, 10-12 Nov. 2014
- [8] Joonsung Bae et al, "The Signal Transmission Mechanism on the Surface of Human Body for Body Channel Communication," *Microwave Theory and Techniques, IEEE Transactions on*, Vol.60, No.3, pp.582-

- [9] J. Justesen, K. J. Larsen, and L. A. Pederson, "Error correcting correction for 100G transport networks," *IEEE Commun. Mag.*, vol. 48, no. 3, pp. S48-S55, Mar. 2010.
- [10] Kiseok Song et al, "A 20  $\mu$ W contact impedance sensor for wireless body-area-network transceiver," *Custom Integrated Circuits Conference (CICC)*, 2011 IEEE, pp.1-4, 19-21 Sept. 2011
- [11] S. Vijayalakshmi, V. Nagarajan, "Design and Implementation of Low Power High-Efficient Transceiver for Body Channel Communications," *Journal of Medical Systems*, 43–81. Feb 2019.
- [12] Namjun Cho., Jeabin Lee., Long Yan (2008) A 60kb/s-to-10Mb/s 0.37nJ/b Adaptive-Frequency-Hopping Transceiver for Body-Area Network. *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 801–816.
- [13] Wala Saadeh., Muhammad Awais Bin Altaf (2017) A 1.1-mW Ground Effect-Resilient Body-Coupled Communication Transceiver with Pseudo OFDM for Head and Body Area Network. *IEEE Journal of Solid-State Circuits*, pp. 2690 – 2702.
- [14] Shovan Maity., Baibhab Chatterjee., Gregory Chang (2018) A 6.3pJ/b 30Mbps –30dB SIR-tolerant broadband interference-robust human body communication transceiver using time domain signal-interference separation. *IEEE Custom Integrated Circuits Conference*, 230–242.
- [15] Wala Saadeh, Muhammad Awais Bin Altaf, Haneen Alsuradi, and Jerald Yoo, "A pseudo OFDM with miniaturized FSK demodulation body coupled communication transceiver for binaural hearing aids in 65nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 757-768, Sep. 2017.
- [16] W. Liu, J. Rho, and W. Sung, "Low-Power High- Throughput BCH Error Correction VLSI Design for Multi-Level Cell NAND Flash Memories," *IEEE Workshop on Signal Processing Systems Design and Implementation (SIPS)*, pp. 303-308, Oct. 2006.
- [17] S. Yoon, H. Lee, K. Lee, "High-Speed Two- Parallel Concatenated BCH-based Super-FEC Architecture for Optical Communications," *IEICE Trans. on Fundamentals of Electronics, Communications, and Computer Sciences, Systems*, vol. E92-A, no. 4, pp.769-777, Apr. 2010.
- [18] Vijayalakshmi, S., & Nagarajan, V. (2019). Energy efficient low density parity check scheme for body channel communication using FPGA. *Microprocessors and Microsystems*, 68, 84-91.

## Figures

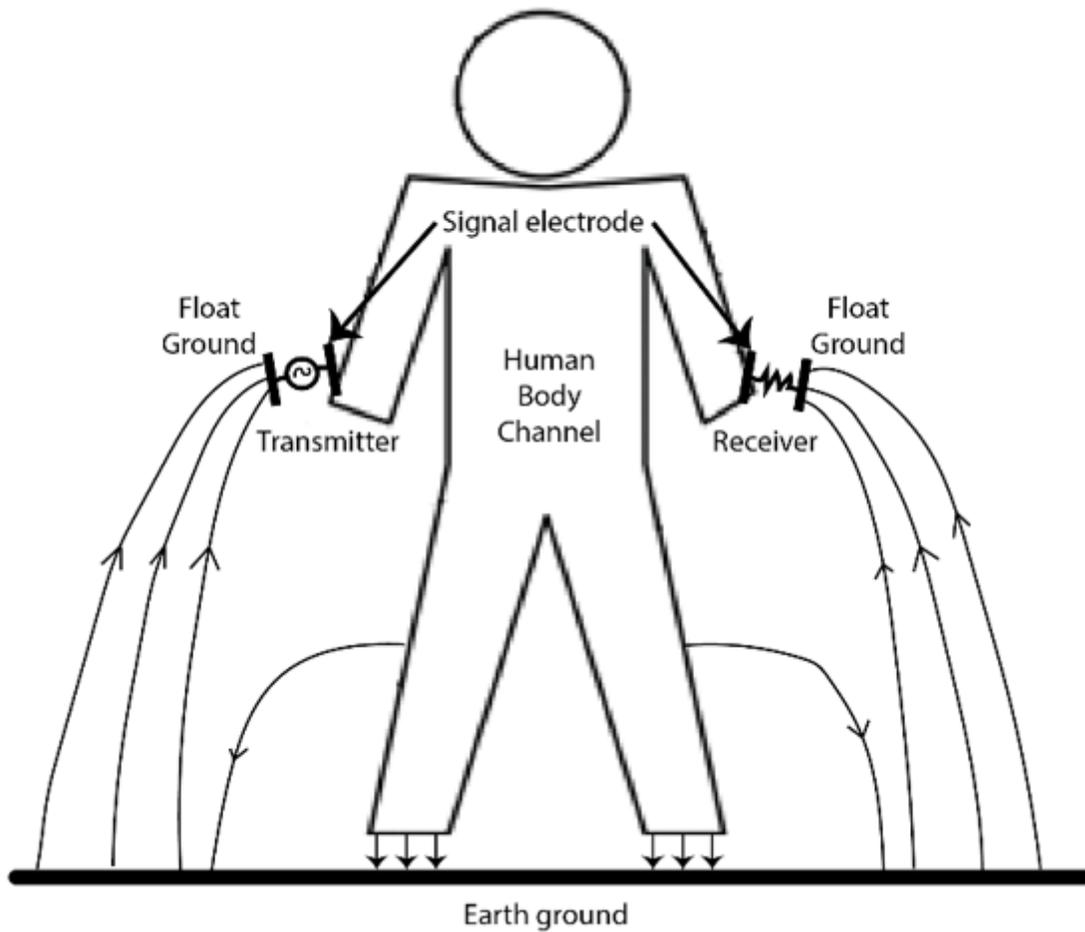


Figure 1

Architecture of capacitive coupling scheme of BCC communication

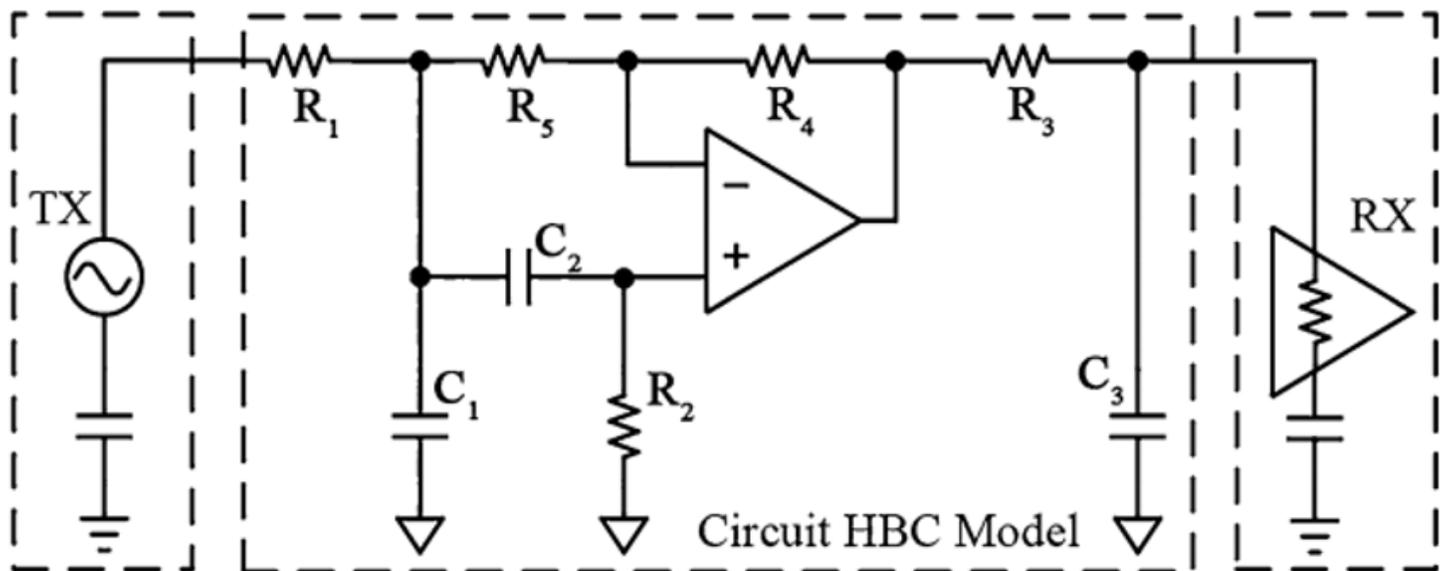


Figure 2

Circuit diagram for BCC transceiver for 100 MHz using Band Pass Filter

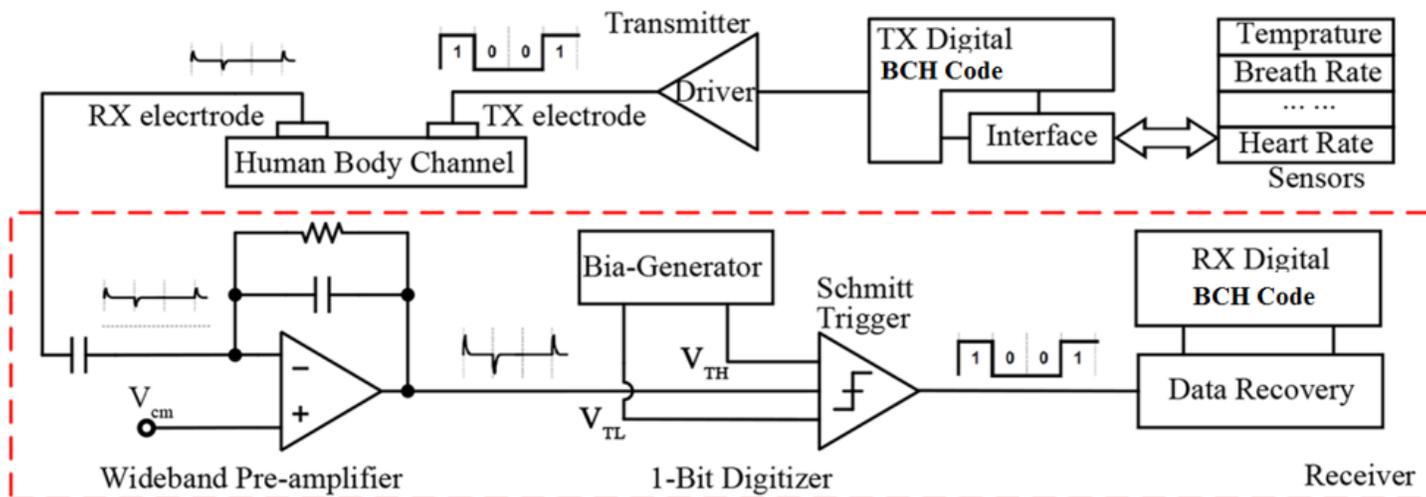


Figure 3

Architecture Proposed of the BCH based BCC receiver

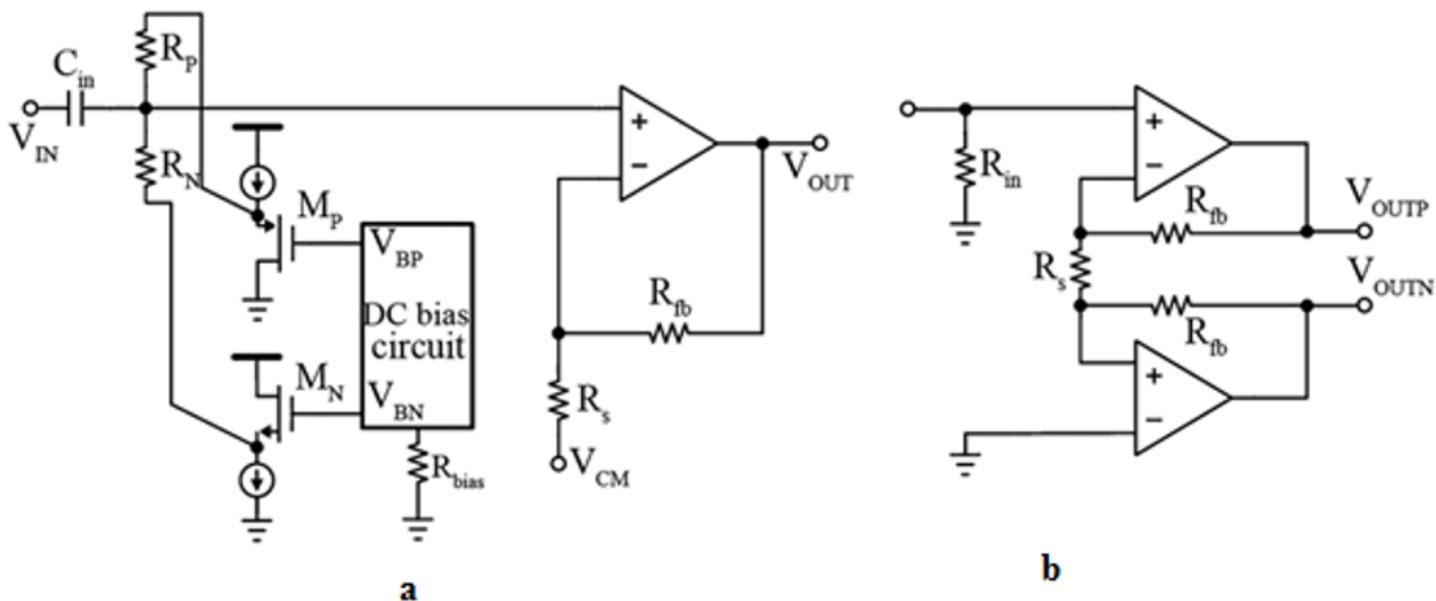


Figure 4

(a) DC bias circuit-based Pre-amplifier (b) Dual op-amp structured preamplifier

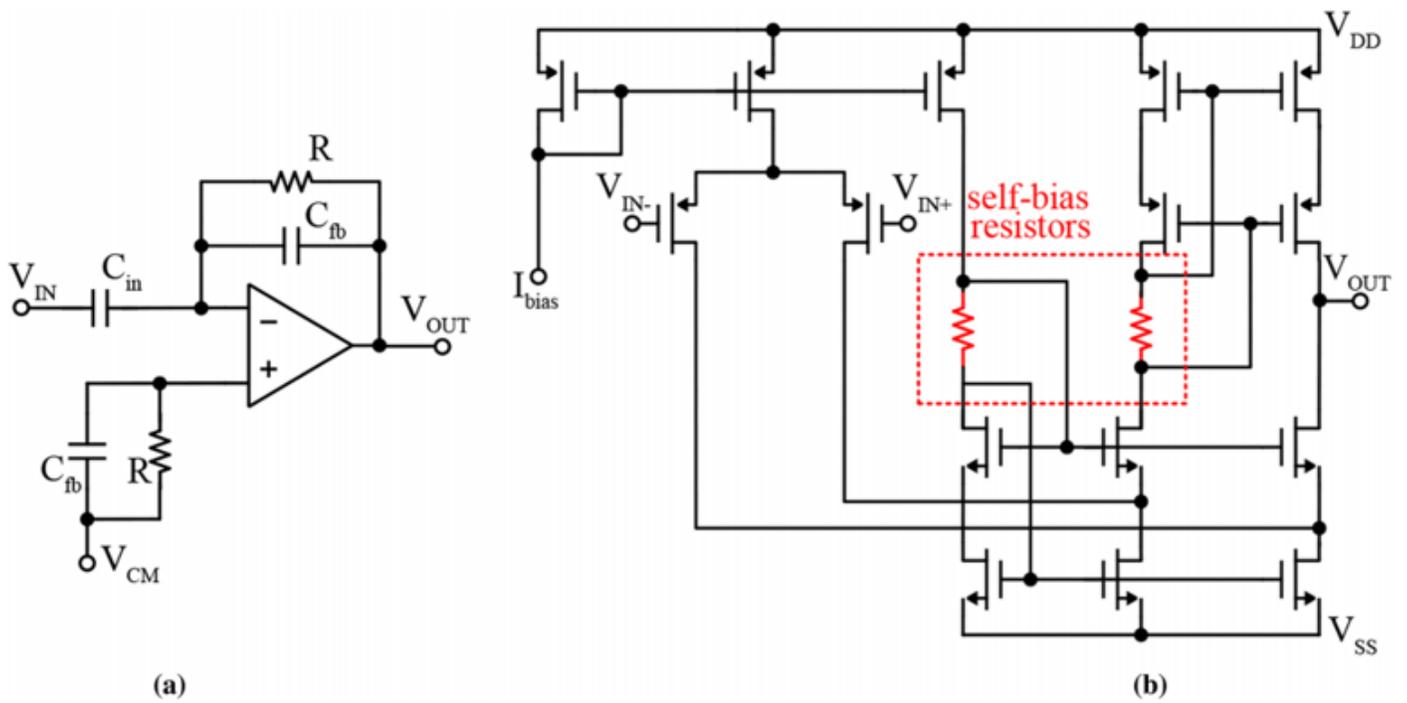


Figure 5

(a) Proposed capacitor-coupling pre-amplifier (b) Self-bias Circuit based preamplifier

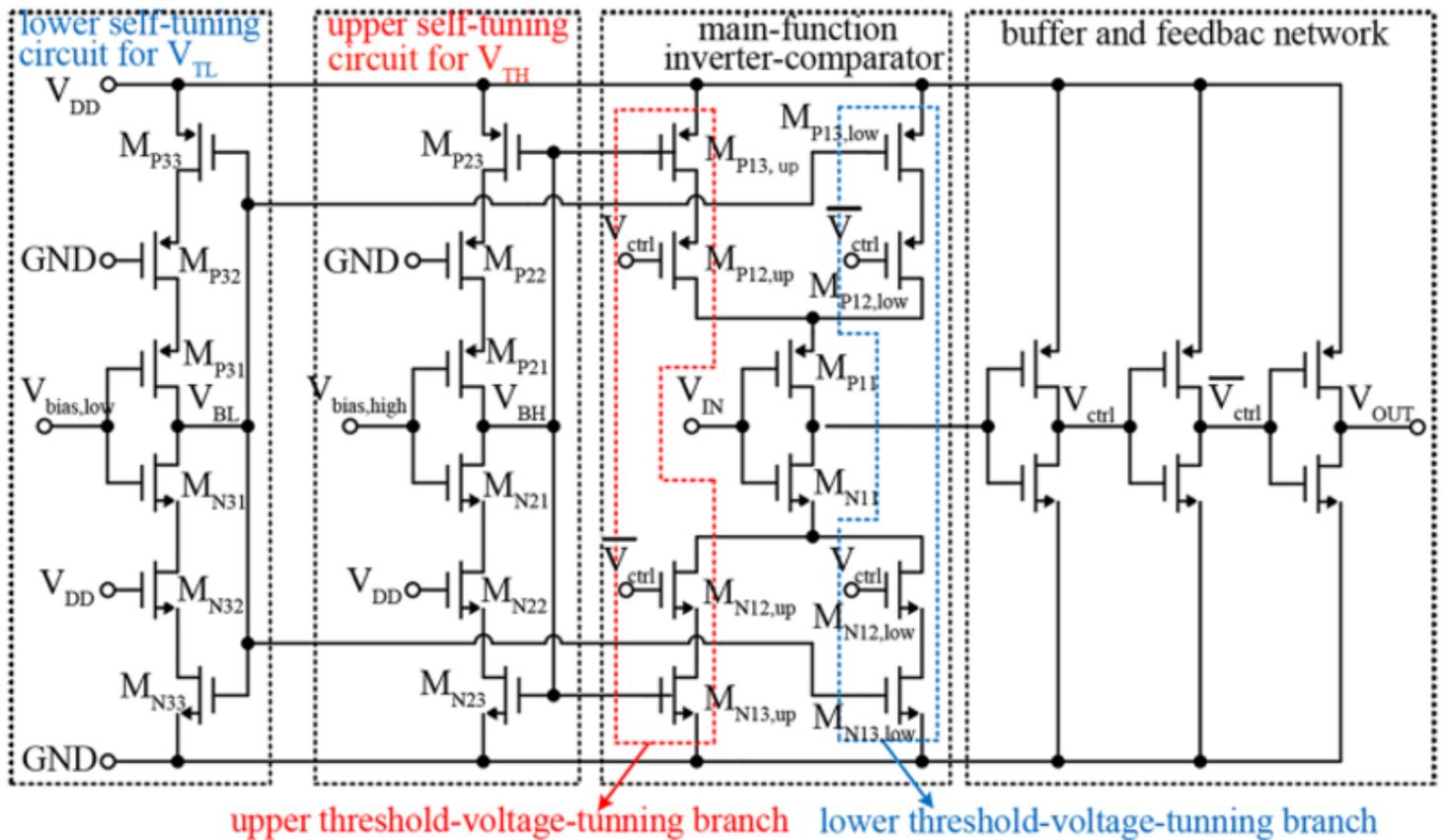


Figure 6

Schematic of proposed fully adjustable Schmitt trigger

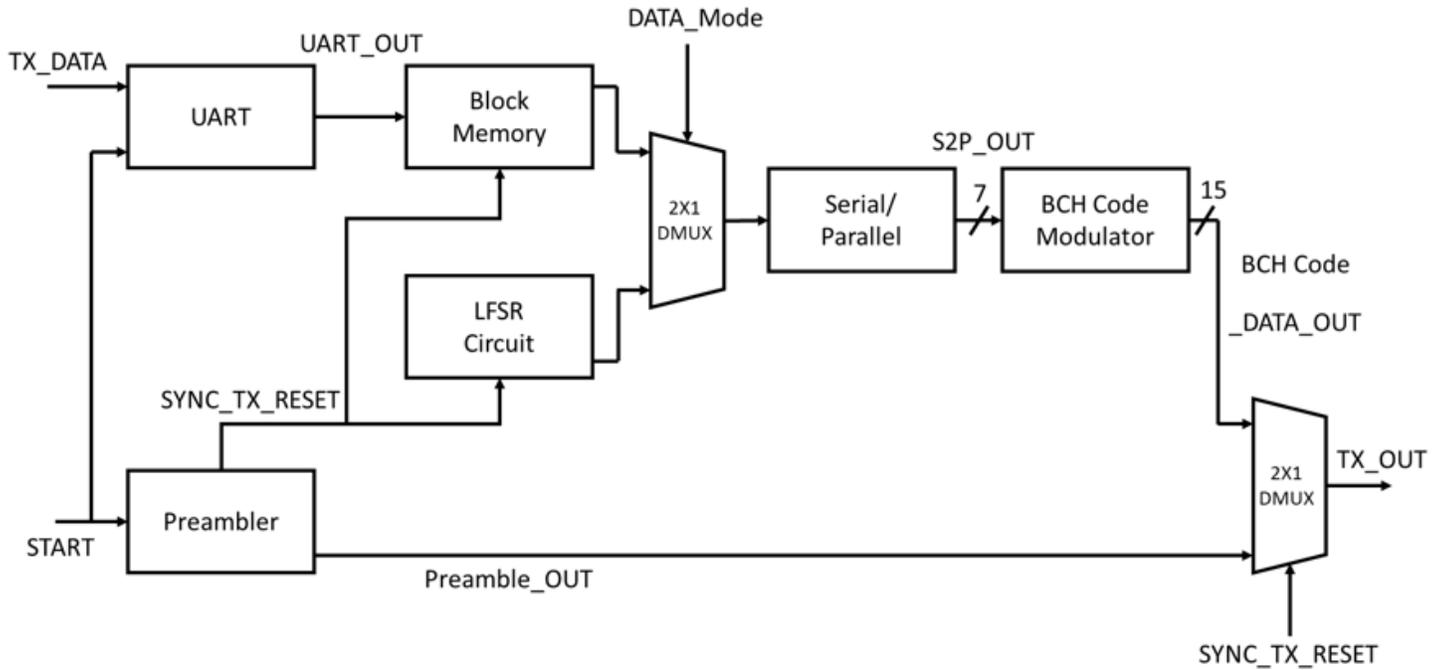


Figure 7

Proposed BCH Based BCC transmitter Design

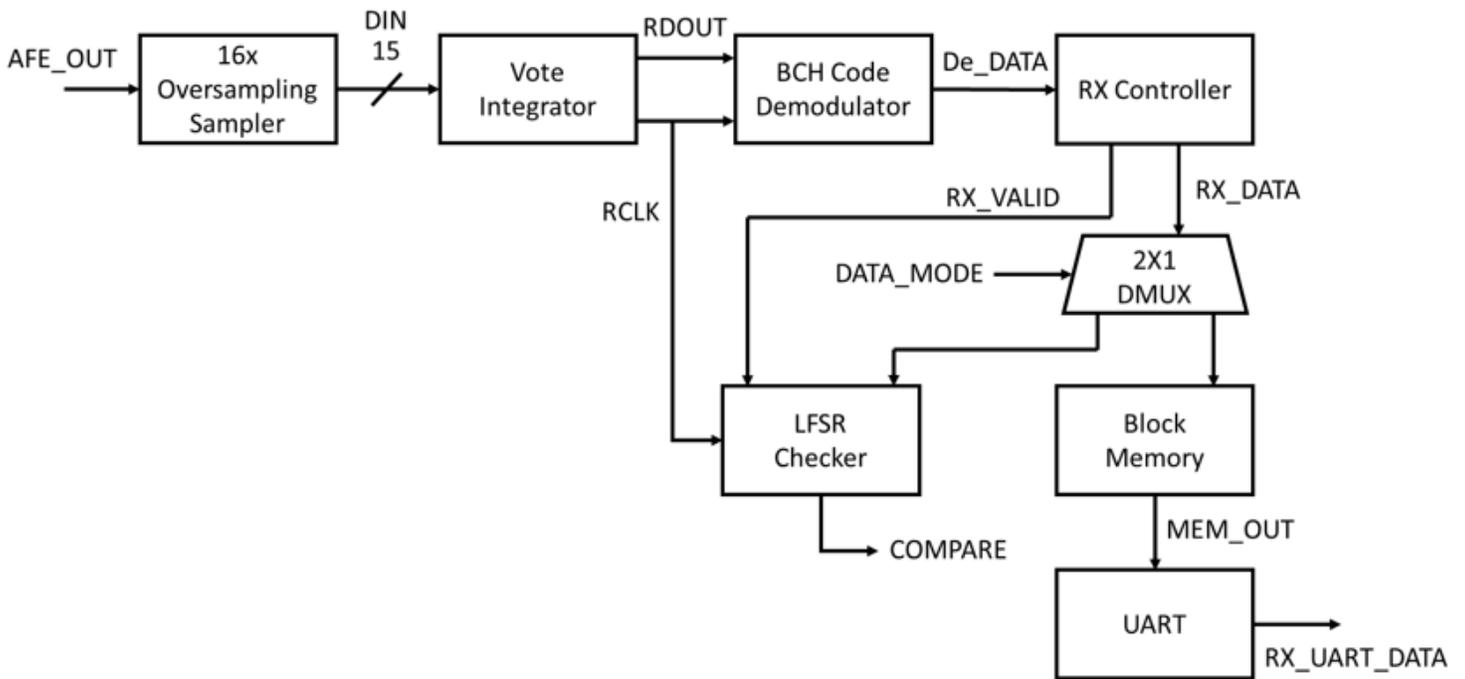


Figure 8

Proposed BCH based BCC receiver design

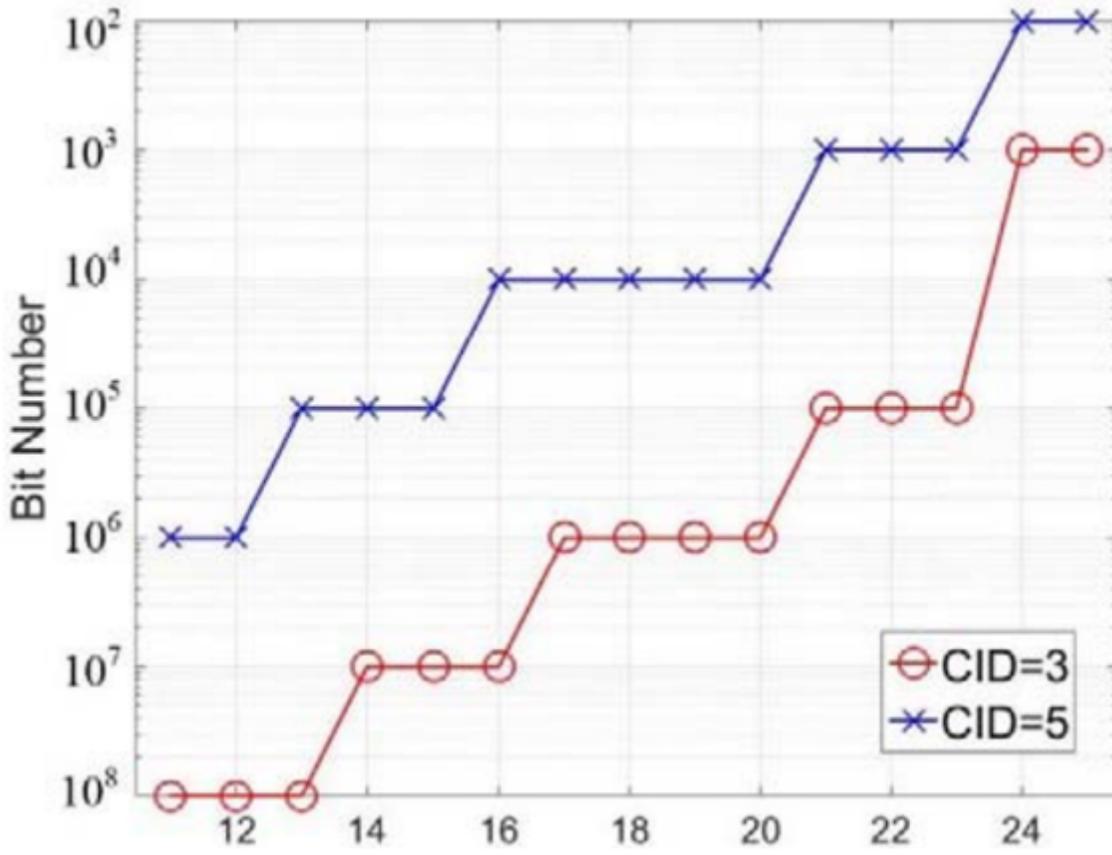


Figure 9

Overall jitter tolerance of BCH based BCC transmitter at 100Mbps

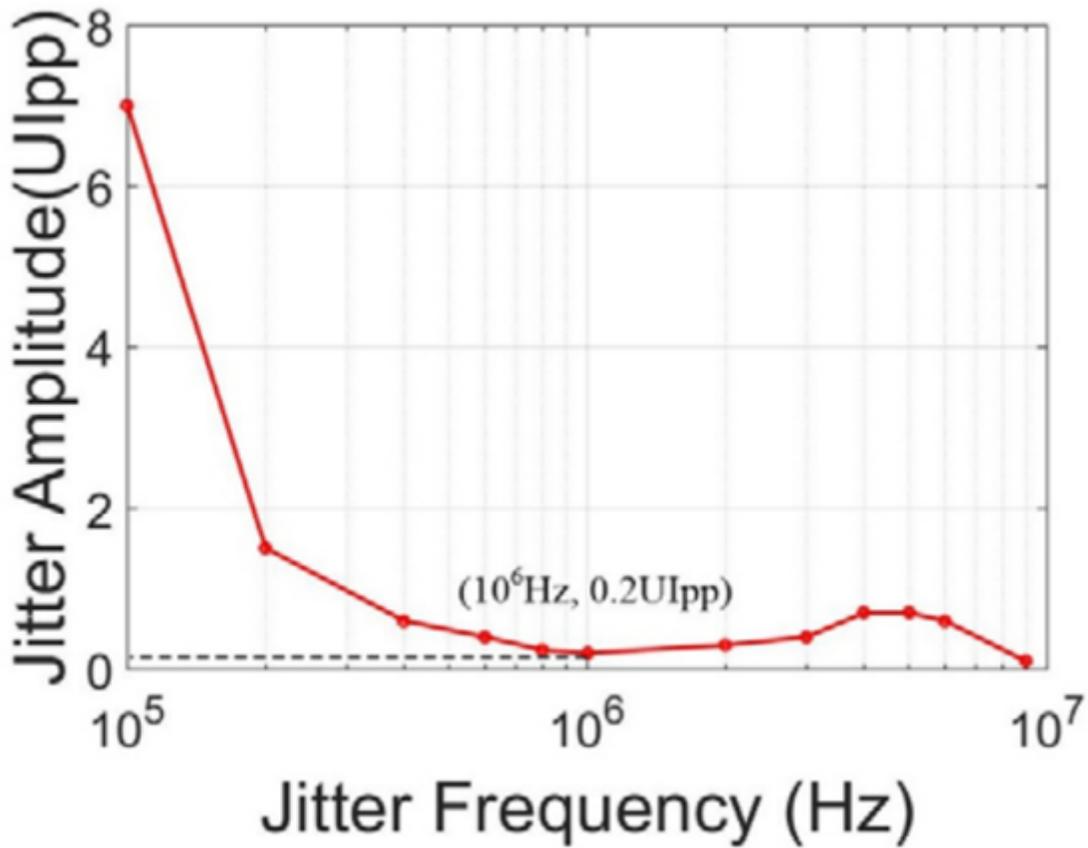


Figure 10

displays the overall BER results of the proposed transceiver at 100 Mbps

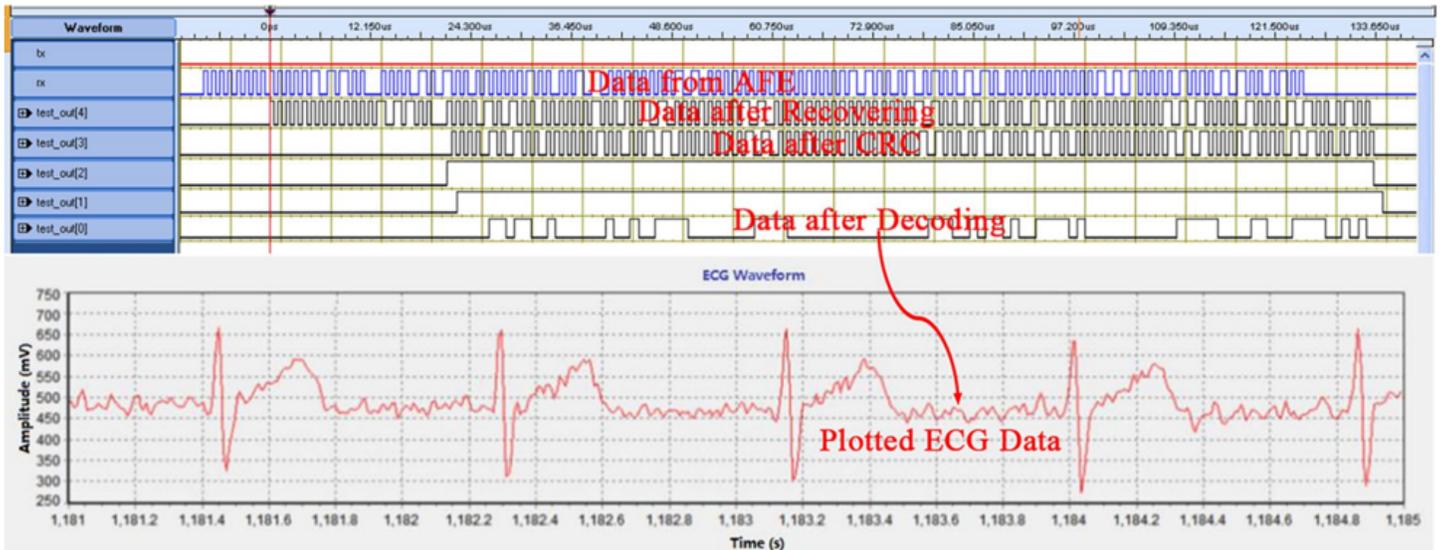


Figure 11

Proposed BCH BCC receiver for ECG sensing usage measured result