New 4H-SiC Metal Semiconductor Field Effect Transistors with Double Symmetric Step Buried Oxide Layer for High Energy Efficiency Applications

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New 4H-SiC Metal Semiconductor Field Effect Transistors with Double Symmetric Step Buried Oxide Layer for High Energy Efficiency Applications

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Abstract

A novel 4H-SiC metal semiconductor field effect transistor (MESFET) device with double symmetric step buried oxide layer is proposed and the mechanism is studied through TCAD simulation. The step buried oxide layer is mainly to reduce the current leakage to the substrate and improve drain current. At the same time, the presence of the oxide layer changes the electric field distribution, reduces the electric field concentration phenomenon, and the breakdown voltage is improved. Due to the presence of the step buried oxide layer, the charge distribution of the device is changed, and the frequency characteristics are improved. When the step buried oxide channel is under the optimized parameter condition, compared with the traditional double-recessed structure 4H-SiC MESFET (DR 4H-SiC MESFET), the direct current (DC) characteristics of the new structure are improved, and the breakdown voltage is increased by 14% to reach 183 V. In radio frequency (RF) characteristics, cut-off frequency is 24.4 GHz, an increase of 11.9 %; maximum operating frequency is 63.9 GHz, an increase of 20.3%; the maximum power added efficiency (PAE) in the L-band and S-band reaches 63.5 %, PAE is 23.7 % higher than the DR structure. At the end of this paper, the new structure is verified for high-energy-efficiency, and the results show that the new structure has great potential in high-frequency applications.

Keywords: **4H-SiC, Metal-Semiconductor Field Effect Transistor (MESFET), Symmetric Step Buried Oxide Layer, Drain current, Power-added-efficiency(PAE)**

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1. Introduction

Wide band gap semiconductor silicon carbide (SiC), because of its excellent electrical properties such as wide band gap width, high critical electric field, high saturation drift velocity and high thermal conductivity, determines its ability to operate at higher frequencies and wider bandwidths, and can still have a higher output power. These excellent characteristics are unmatched by traditional silicon-based semiconductors. SiC power semiconductor devices have attracted people's attention and has become one of the third-generation semiconductor materials [1-2]. SiC devices, especially 4H-SiC metal semiconductor field effect transistors (MESFETs), occupy a major position in applications, and have become one of the research hotspots in the field of microwave power devices in recent years. Compared with traditional Si-MOSFET, 4H-SiC MESFET has larger saturation drain output current, breakdown voltage, cut-off frequency, maximum operating frequency and output efficiency. The MESFETs have a wide range of applications in microwave circuits, in civil communications, petroleum exploration, aviation, aerospace, radar systems and other related fields have very broad application prospects [3-4].

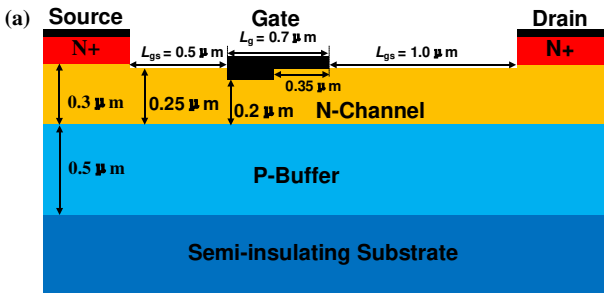
In recent years, the main research point of 4H-SiC MESFET microwave power devices is to improve the DC and RF characteristics and has made great progress [5-8]. Many researchers have proposed many new structures. Optimized the device structure and obtained many structures with excellent characteristics, such as double-recessed structure[9], Field-Plated Buried-Gate structure[10], Dual-channel layer structure[11], L-type gate structure[12],new structure with ion implantation to form channel layer[13], MRD structure[14], serpentine channel structure[15], symmetrical lightly doping gate structure[16], etc., where the maximum breakdown voltage can reach 159 V, the cut-off frequency reaches 23.85 GHz, the maximum operating frequency can reach 59.8 GHz, and the power added efficiency reaches 41.56%[17]. With the increasing demand for energy saving and emission reduction, and a green planet, efficiency will also become one of the research hotspots, the method for improving the efficiency of the microwave circuit is mainly to improve the peripheral circuit, and there is no optimization adjustment from the inside of the device, and there is very little research on designing high efficiency from the perspective of device level. Therefore, how to balance the relationship between DC, RF and efficiency is a difficult problem.

In order to balance the relationship between DC, RF and efficiency from a device-level perspective, this paper proposes a novel 4H-SiC MESFET device with double symmetric step buried oxide layer. By optimizing device parameters, the power added efficiency of the device reaches the optimal value and has better DC and RF characteristics. Compared with the DR 4H-SiC MESFET [9], the new structure has symmetrical step oxide layers on the left and right sides of the channel layer. The presence of the step oxide layer reduces the current leakage to the substrate, thereby increasing the maximum drain Saturation current. At the same time, it also disperses the electric field distribution, so that the breakdown voltage is improved. Another

function of the oxide layer is to improve the frequency characteristics of the device. In this paper, a new device with a large PAE is obtained by optimizing the structural parameters of the stepped oxide layer, and the feasibility of the device in high-efficiency RF applications is analyzed.

2. Device structure and parameters

As shown in Fig. 1 (a) and (b), they are the structural diagrams of the DR 4H-SiC MESFET and the new 4H-SiC MESFET, respectively. The DR 4H-SiC MESFET and the new 4H-SiC MESFET have a gate-source distance L_{gs} = 0.5 μm, a gate-drain distance L_{gd} = 1.0 μm, a gate length L_{g1} = 0.7 μm, and a non-recessed gate length L_{g2}= 0.35 μm, the thickness of the channel layer H_{ch1} = 0.3 μm, H_{ch2} = 0.25 μm, H_{ch3} = 0.2 μm, the thickness of the P buffer layer H_b = 0.5 μm, the thickness of the source cap layer and the drain cap layer is 0.2 μm, and the doping concentration is 2×10^{19} cm^{-3}, the doping concentration of the channel layer is 3×10^{17} cm^{-3}, the doping concentration of the P buffer layer is 1.4×10^{15} cm^{-3}. The work function of Schottky contact between the metal nickel and the gate is 5.1 eV. Under the buffer layer is a semi-insulating substrate. The new structure forms two symmetrical SiO_2 stepped oxide layers under the channel layer, which are located between the source gate and the drain gate. The interface state density of SiC/SiO_2 is set to 3.4×10^{12} cm^{-2} eV^{-1}. By simulating the structural parameters of the stepped oxide layer, we found that each structural parameter of the stepped oxide layer has a small effect on the performance of the device (such as I_{dsat}, BV, f_t, f_{max}, etc.). It can be approximated that the influence of structural parameters on device performance is independent. By analyzing the internal working mechanism of the device, changing the position and size of the stepped oxide layer, an optimized stepped oxide layer is finally obtained. The structural parameters of the new symmetrical oxide layer are shown in Table I. The stepped oxide layer can be injected with oxygen through a step, and then anneal at high temperature to produce a symmetrical stepped oxide layer in the new structure. To reduce the interface charge between SiC/SiO_2, oxygen nitridation is used in the device manufacturing process, which can greatly reduce the interface state density [18].



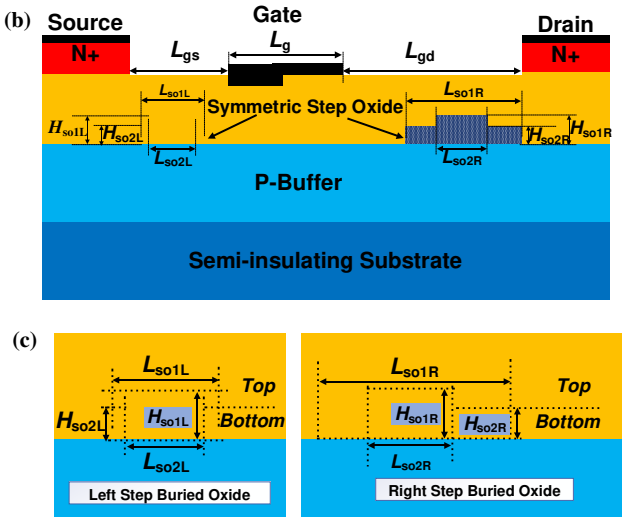


Fig. 1. Schematic diagram of DR MESFET (a), new structure MESFET (b), enlarged view of symmetrical oxide layer structure(c).

TABLE I

THE MAIN DEVICE STRUCTURE PARAMETERS FOR THE 4H-SIC MESFET

Symbol	Device parameters	Value
N_{cap}	Doping concentration of cap layer (N++)	2.0×10^{19} cm^{-3}
$N_{channel}$	Doping concentration of channel layer (N+)	3.0×10^{17} cm^{-3}
N_{buffer}	Doping concentration of buffer layer (P+)	1.4×10^{15} cm^{-3}
W_{mg}	The work function of Schottky contact between the metal nickel and the gate	5.1 eV
H_{so1L}	Thickness of the left oxide layer	0.10 μm
H_{so2L}	Thickness of bottom oxide layer on the left	0.05 μm
L_{so1L}	Width of top oxide layer on the left	0.30 μm
L_{so2L}	Width of bottom oxide layer on the left	0.20 μm
H_{so1R}	Thickness of the right oxide layer	0.10 μm
H_{so2R}	Thickness of bottom oxide layer on the right	0.05 μm
L_{so1R}	Width of top oxide layer on the right	0.80 μm
L_{so2R}	Width of bottom oxide layer on the right	0.40 μm

This paper uses Sentaurus TCAD, a software that can be applied to device simulation and process simulation. TCAD simulation is widely used in the research of semiconductor devices. For 4H-SiC, the simulation and experimental results are in good agreement [19-22]. The main models used in this article include: (1) Carrier transport model. It is mainly the drift-diffusion model, Poisson equation, hole continuity equation and electron continuity equation. When simulating 4H-SiC MESFET, the self-heating effect of the lattice must be considered, and the model used is a thermodynamic model. (2) Band narrowing model. The energy band of 4H-SiC material is related to the doping concentration. Considering the doping band narrowing effect caused by the shrinkage of the bottom of the conduction band and the top of the

valence band by heavy doping, the band narrowing effect is described using the OldSlotboom model. (3) Effective state density model. This model gives the expressions of the effective state density of the conduction band and the effective state density of the valence band, combined with the width of the forbidden band, the carrier concentration of this channel can be obtained. (4) Mobility model. The actual carrier is affected by many factors, which will cause a decrease in mobility. The phenomena that cause mobility degradation include lattice scattering mainly related to temperature, scattering of ionized impurities mainly related to doping concentration, inter-carrier scattering mainly related to carrier concentration and high field saturation mainly related to electric field. (5) Compound model. In the thermal equilibrium state, the recombination process of carrier generation cannot be ignored. The composite models mainly include Schckley-Read-Hall, SRH model and Auger recombination model. SRH recombination describes the recombination of impurities and defects in the forbidden band to form deep-level centers; Auger recombination describes the process in which electrons and holes directly recombine while giving energy to another free carrier. (6) Impact ionization model. The simulation software sets the breakdown type of the 4H-SiC MESFET device to avalanche breakdown, and the impact ionization model describes the avalanche multiplication effect. (7) Impurity incomplete ionization model. At room temperature, 4H-SiC materials have large ionization energy due to the forbidden bandwidth, and the ionization rate of impurities is low. The ambient temperature in this paper is set to 300 K, doped with 3×10^{17} cm^{-3} N ions, and the ionization of N conversion rate is about 70%.

3. Results and discussion

3.1. DC characteristics

As shown in Fig. 2, the drain output current I_d of the new 4H-SiC MESFET and the DR 4H-SiC MESFET at different gate voltages (V_{gs} = -1 V, V_{gs} = -3 V, V_{gs} = -5 V) varies with V_{gs} schematic diagram of the relationship curve. It can be clearly seen in Fig. 2 that the drain output current of the new 4H-SiC MESFET is greater than that of the DR 4H-SiC MESFET. When V_{gs} = -1 V, the drain saturation current Ids of the new 4H-SiC MESFET is 397 mA /mm, which is 5.0 % higher than the 378 mA/mm of the DR 4H-SiC MESFET.

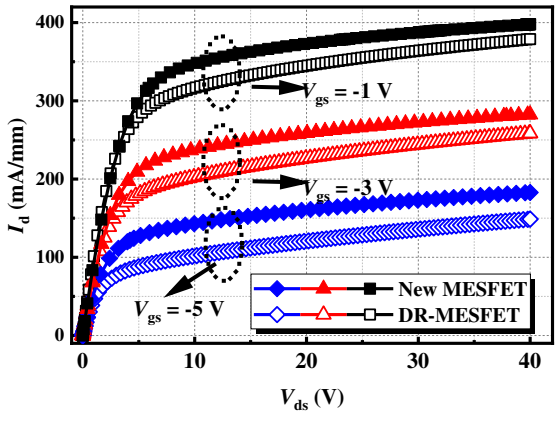


Fig. 2. I_d-V_{ds} characteristics at different gate voltages (V_{gs} = -1 V, -3 V, -5 V).

Fig. 3 is the current distribution of the DR 4H-SiC MESFET and the new 4H-SiC MESFET. It can be clearly seen from the figure that the conventional DR 4H-SiC MESFET has a relatively obvious leakage current, that is, part of the current leaks from the channel region to the substrate, which eventually causes the drain current to decay. The main reason for the increase in the drain saturation current of the new 4H-SiC MESFET is that the channel uses two stepped oxide layers. Due to the barrier of the oxide layer, the leakage current from the channel region to the substrate is slowed, so it can effectively Increasing the drain saturation current. [23-24].

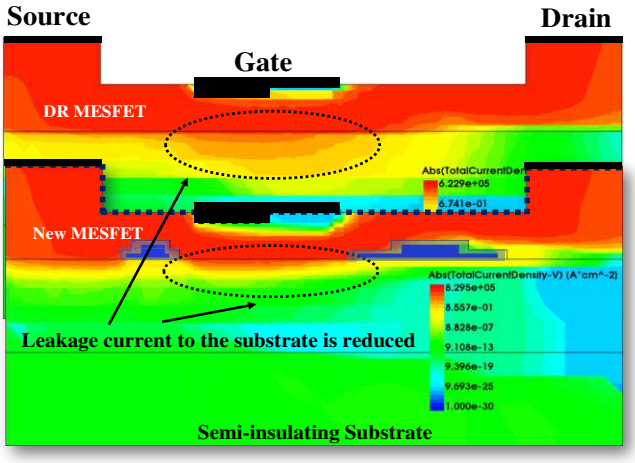


Fig. 3. Simulation diagram of the total current density of the two structures.

Fig. 4 shows the transfer characteristics of the DR 4H-SiC MESFET and the new 4H-SiC MESFET (left y-axis) and the variation curve of transconductance gm with V_{gs} (right y-axis). It can be seen from the figure that the new 4H-SiC MESFET has a larger current output capability than the DR 4H-SiC under the same gate voltage. The threshold voltage V_t is the gate voltage when the device is in critical conduction. The threshold voltages of the new 4H-SiC MESFET and DR 4H-SiC MESFET are -6.9 V and -5.8 V, respectively. This means that the new device can be turned on at a smaller gate voltage Vt. The main reason for the threshold voltage shift of the new device is also mainly caused by the decrease of the current leakage from the channel region to the substrate. The transconductance gm is the rate of change of the drain current with the gate voltage. It can reflect the control ability of the gate voltage to the drain current. As can be seen from Fig. 4, when V_{gs} is about -11 V to -5 V, the current control capability of the new 4H-SiC MESFET is stronger than that of the DR 4H-SiC MESFET. When V_{gs} is about -5 V to 0 V, the current control capabilities of the two devices are not much different. Looking at the transconductance as a whole, the new structure extends the control range of the gate voltage to the leakage current from the original -9.5 V ~ 0 V to -11 V ~ 0 V.

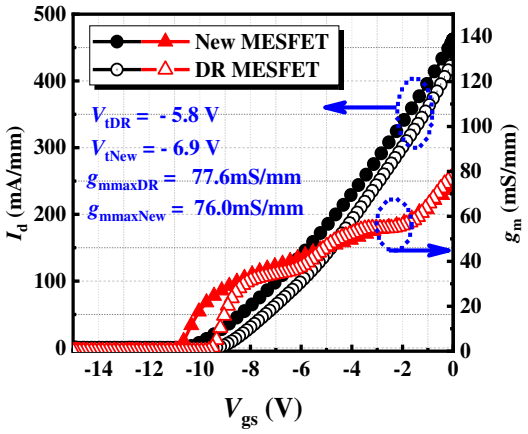


Fig. 4. Transfer characteristics and transconductance of the two structures.

As shown in Fig. 5, the breakdown characteristics of the two devices are as follows. The bias condition is that the gate voltage $V_g = V_t$, the drain voltage increases from 0 V, and the breakdown condition is $I_g = 0.001$ mA. Simulation results show that the breakdown voltage V_b of the new 4H-SiC MESFET device and the DR 4H-SiC MESFET are 183V and 160V, respectively, and the breakdown voltage of the new structure is 14% higher than the original DR structure. The maximum theoretical output power [25] of 4H-SiC MESFET is

$$P_{max} = \frac{I_{dsat}(V_b - V_{knee})}{8} \tag{1}$$

where I_{dsat} is its saturated drain voltage, and V_{knee} is knee voltage. From the above formula, the maximum output power of the new 4H-SiC MESFET is 8.34 mW/mm, which is an increase of 21.8% compared to the 6.85 mW/mm of the DR 4H-SiC MESFET. This shows that the new 4H-SiC MEFET has greater potential in high-power applications. The main reason for the increase in breakdown voltage has been clarified in Fig. 6. It can be clearly seen from the comparison that during the breakdown of the DR 4H-SiC MESFET, the electric field is mainly concentrated on the drain and the gate side close to the drain . Once the electric field density reaches a certain level, the device will break down. In the new 4H-SiC MESFET, due to the presence of a symmetrical stepped oxide layer, the concentration of the electric field is somewhat relieved.

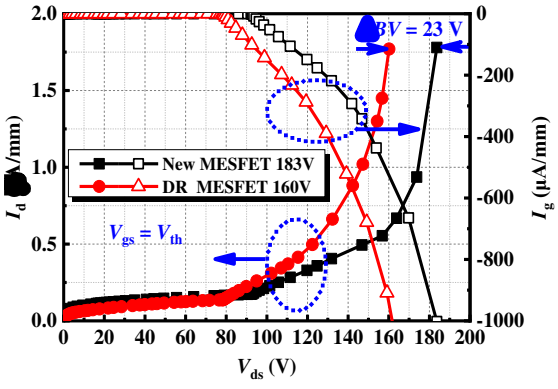


Fig. 5. Breakdown characteristics of two devices.

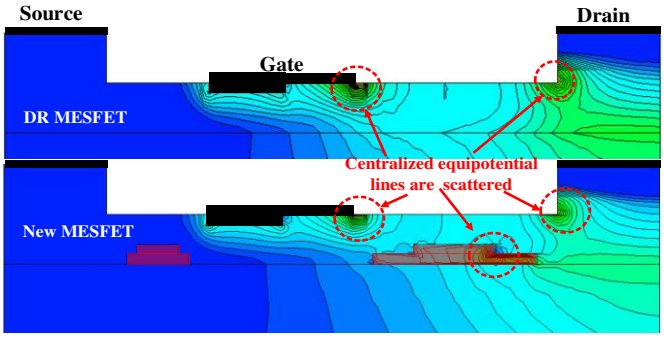


Fig. 6. Electric field distribution curve, DR 4H-SiC MESFET (top), new 4H-SiC MESFET.

3.2. RF characteristics

Fig. 7 is a bias circuit diagram for measuring the RF characteristics of two devices. The gate is used as the input terminal, there are DC input and RF input, and the test frequency range is 100 MHz ~ 100 GHz. Fig. 8 shows the variation of transconductance gm, gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} with frequency. The DC bias conditions are V_{ds} = 20 V and V_{gs} = 0 V. As can be seen from the figure, compared with the DR 4H-SiC MESFET, the maximum AC transconductance of the new 4H-SiC MESFET is 79 mS/mm, and the DR structure is 74 mS/mm. The new structure is slightly better than the DR structure. Under AC conditions, the working state of the device changes and the radio frequency signal on the gate also changes periodically with the frequency, so the drain current in the channel is also subject to the periodic change generated by the gate. When the input frequency at the V_{g2} terminal increases, the signal change period is greater than the time constant, resulting in the channel current being able to change in time. Therefore, when the frequency increases to a certain extent, the AC transconductance will decrease with increasing frequency. The C_{gs} and C_{gd} of the DR 4H-SiC MESFET are 98 pF/mm and 76 pF/mm, respectively, and those of the new 4H-SiC MESFET are 89 pF/mm and 72 pF/mm, respectively. The new structure has a 10.1% and 5.5% reduction in C_{gs} and C_{gd} compared to the DR structure, respectively. It can be seen from Fig. 3 that the presence of a stepped oxide layer reduces the cross-sectional area of the electron flow through the channel. At the same time, since the dielectric constant of the oxide layer is less than 4H-SiC, according to equation (2), the electric constant and the area of the parallel plate are directly proportional to the capacitance value, the gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} of the new structure will be smaller than the DR structure.

$$C = \frac{\varepsilon S}{4\pi k d} \tag{2}$$

Where k is the electrostatic force constant, d is the parallel plate spacing, ε is the dielectric constant, and S is the area directly facing the parallel plate.

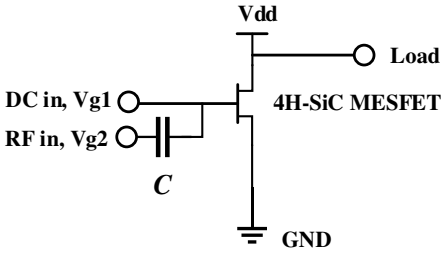


Fig. 7 One tone Load pull schematic for 4H-SiC MESFET measurement.

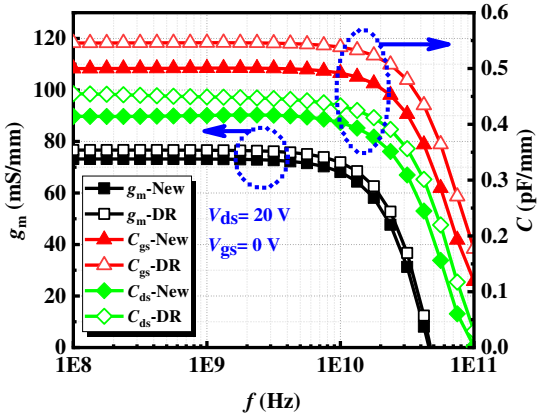


Fig. 8. Changes of AC transconductance gm, C_{gs} and C_{gd} in two periods at different frequencies (V_{ds} = 20 V, V_{gs} = 0 V).

The cut-off frequency f_t and the maximum oscillation frequency fmax determine the radio frequency performance of the device. The cut-off frequency f_t refers to the frequency when the short-circuit small-signal current gain $|h_{21}|$ drops to 0 dB, the maximum oscillation frequency refers to the frequency when the maximum available gain (MAG) drops to 0 dB, and MUG refers to the unilateral power gain of the device. This paper uses a two-port network to perform small-signal S-parameter simulations on the device. The bias conditions are V_{gs} = 0 V and V_{ds} = 20 V. It can be seen from Fig. 9 that when the short-circuit small-signal current gain $|h_{21}|$ drops to 0 dB, the cut-off frequencies f_t of the DR 4H-SiC MESFET and the new 4H-SiC MESFET are 21.8 GHz and 24.4 GHz, respectively, the new structure is 11.9 % higher than the DR structure. When the MAG drops to 0 dB, the maximum oscillation frequencies fmax of the DR 4H-SiC MESFET and the new 4H-SiC MESFET are 53.1 GHz and 63.9 GHz, respectively, and the new structure is 20.3 % higher than the DR structure; Equation (3) and (4) are the expressions of f_t and f_{max}[26],

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{3}$$

$$f_{max} = \frac{f_t}{2}\sqrt{\frac{R_{ds}}{R_g}} \tag{4}$$

among them, R_{ds} and R_g are source-drain resistance and gate resistance, respectively. According to (3) and (4), the new 4H-SiC MESFET has smaller gate-source capacitance

C_{gs} and gate-drain capacitance C_{gd}, and the maximum transconductance gm of the two is not much different. Therefore, the cut-off frequency of the new structure is greater than the DR structure. Since the f_t of the new structure is greater than the DR structure, and the maximum oscillation frequency is greater than and greater than the DR structure, it can be seen from 3.1 that the drain-source resistance R_{ds} of the new structure is greater than the DR structure, Therefore, the reason for the increase of the maximum oscillation frequency of the new structure comes from the reduction of the gate resistance.

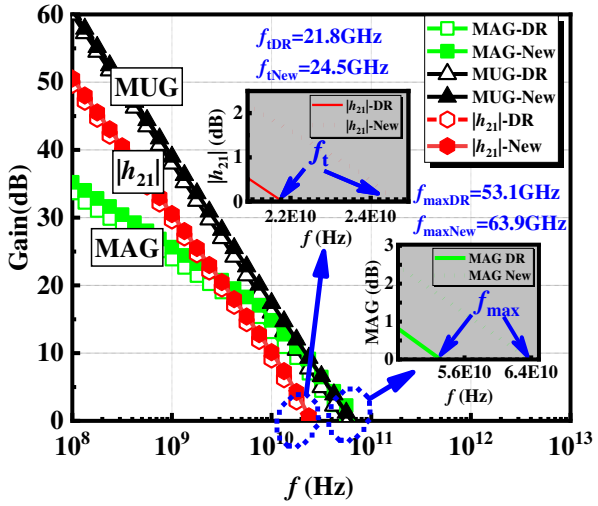


Fig. 9. Variation curve of small signal gain with frequency and f_{max}, f_t.

3.3. High energy efficiency verification

Fig. 10 (a) - (d) is the variation curve of Pout (left y-axis)/PAE (right y-axis) of new 4H-SiC MESFET and DR 4H-SiC MESFET with Pin at different frequencies, The bias conditions are V_{gs} = -4 V and V_{ds}= 20 V. The definition of power added efficiency PAE is

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}(1 - \frac{P_{in}}{P_{out}}) = \eta_d(1 - \frac{1}{G_p}) \qquad (5)$$

where PDC is the power consumption of its DC power supply, η_d=P_{out}/P_{DC} is its drain efficiency, G_p = P_{out}/P_{in} is the power gain. PAE measures the ability of DC power to be converted into AC output power and is an important power performance parameter.

Fig. 10 (a) - (d) shows that as the frequency increases, the advantages of the new 4H-SiC MESFET gradually begin to manifest. In Fig. 10 (a) - (d), P_{out}/P_{in} is the power gain G_p, when the frequency increases, the difference between the Pout of the new structure and the Pout of the DR structure becomes larger and larger, Therefore, the power gain of the new structure is also greater than that of the DR structure. The high energy efficiency advantage over the DR structure is gradually reflected. Simulation of PAE shows that from the L-band and S-band of 600 MHz to 4.8 GHz, the difference between the PAE of the new 4H-SiC MESFET and the DR 4H-SiC MESFET increases from 8.22 % to 10.46 %, and the PAE can reach a maximum of 63.5 %. In general, the new

structure not only maintains excellent DC characteristics, but also has excellent radio frequency characteristics, and has great advantages in high power and high energy efficiency applications.

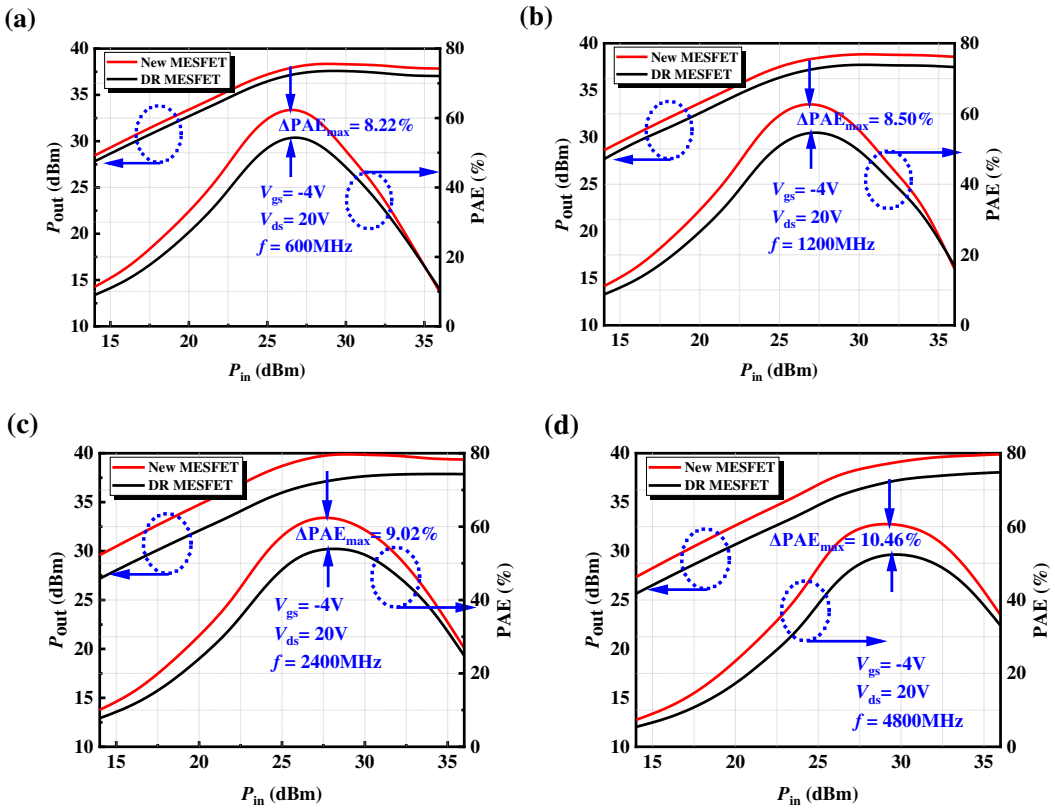


Fig. 10. Variation curve of output power and PAE with input at different frequencies.

4. Conclusion

In summary, a novel 4H-SiC MESFET with double symmetric step buried oxide layer is proposed and the mechanism is studied through TCAD simulation. The step buried oxide layer is mainly to reduce the current leakage to the substrate and improve Drain current. At the same time, the presence of the oxide layer changes the electric field distribution, reduces the electric field concentration phenomenon, and the breakdown voltage is improved. Due to the presence of the step buried oxide layer, the charge distribution of the device is changed, and the frequency characteristics are improved. When the step buried oxide channel is under the optimized parameter condition, compared with the DR 4H-SiC MESFET, the DC characteristics of the new structure are improved, and the breakdown voltage is increased by 14% to reach 183 V. In characteristics, cut-off frequency is 24.4 GHz, an increase of 11.9%; maximum operating frequency is 63.9 GHz, an increase of 20.3%; the maximum power added efficiency in the L-band and S-band reaches 63.5%, PAE is 23.7% higher than the DR structure. At the end of this paper, the new structure is verified for high-energy-efficiency, and the results show that the new structure has great potential in high-frequency applications. Overall, the new MESFET has improved DC and AC characteristics, and provides a new idea for efficiency design.

5 Declarations

Author Contributions: Conceptualization, Shunwei Zhu.; formal analysis, Hujun Jia.; investigation, Mengyu Dong, Xiaowei Wang.; resources, Shunwei Zhu.; data curation, Shunwei Zhu, Yintang Yang; writing—original draft preparation, Shunwei Zhu.; writing—review and editing, Hujun Jia.; visualization, Shunwei Zhu.; project administration, Hujun Jia.; funding acquisition, Yintang Yang. All authors have read and agreed to the published version of the manuscript.

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Data Availability: The data that support the findings of this study are available from the corresponding author, upon reasonable request.

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Competing interests: The authors have declared that no competing interests exist.

Research involving Human Participants and/or Animals: This article does not contain any studies with human participants performed by any of the authors.

Ethics approval and consent to participate: not applicable.

Informed Consent: Informed consent was obtained from all individual participants included in the study.

Consent for publication: not applicable.

References

[1] R. R. Lamichhane et al., "A wide bandgap silicon carbide (SiC) gate driver for high-temperature and high-voltage applications," 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Waikoloa, HI, 2014, pp. 414-417, doi: 10.1109/ISPSD.2014.6856064.

[2] Keffous, A. , et al. "Investigation of porous silicon carbide as a new material for environmental and optoelectronic applications." Applied Surface ence 256.18(2010): P.5629-5639, doi: 10.1016/j.apsusc.2010.03.029.

[3] S. P. Marsh, J. C. Clifton, K. C. Vanner, J. R. Cockrill and I. Davies, "5.4 Watt GaAs MESFET MMIC for phased array radar systems," IEEE MTT/ED/AP/LEO Societies Joint Chapter United Kingdom and Republic of Ireland Section. 1997 Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications. EDMO (Cat., London, UK, 1997, pp. 169-174, doi: 10.1109/EDMO.1997.668593.

[4] V. Banu, P. Godignon and J. Millán, "Design of voltage comparator integrated circuit with normally-on MESFETs on 4H-SiC semiconductor," 2015 International Semiconductor Conference (CAS), Sinaia, 2015, pp. 171-174, doi: 10.1109/SMICND.2015.7355198.

[5] Roustaie, Zohreh , and A. A. Orouji . "A novel 4H-SiC MESFET by lateral insulator region to improve the DC and RF characteristics." International journal of electronics 105.4-6(2018): 614-628, doi: 10.1080/00207217.2017.1382005.

[6] Bai, Yun , et al. "Design and Simulation of 4H-SiC MESFET Ultraviolet Photodetector with Gain." Materials Science Forum 897(2017):610-613, doi:10.4028/www.scientific.net/MSF.897.610.

[7] Naderi, Ali , and F. Heirani . "Improvement in the performanceof SOI-MESFETs by T-shaped oxide part at channel region: DC and RF characteristics." Superlattices & Microstructures 111.nov.(2017):1022-1033,doi: 10.1016/j.spmi.2017.07.058.

[8] T. Phulpin et al., "Contribution to Silicon-Carbide-MESFET ESD Robustness Analysis," in IEEE Transactions on Device and Materials Reliability, vol. 18, no. 2, pp. 214-223, June 2018, doi: 10.1109/TDMR.2018.2817255.

[9] Zhu, C. L. , et al. "Improved performance of SiC MESFETs using double-recessed structure." Microelectronic Engineering 83.1(2006):p.92-95,doi: 10.1016/j.mee.2005.10.054.

[10] K. Andersson et al., "Fabrication and characterization of field-plated buried-gate SiC MESFETs," in IEEE Electron Device Letters, vol. 27, no. 7, pp. 573-575, July 2006, doi: 10.1109/LED.2006.877285.

[11] Zhu, C. L. , Rusli, and P. Zhao . "Dual-channel 4H-SiC metal semiconductor field effect transistors." Solid State Electronics 51.3(2007):p.343-346,doi: 10.1016/j.sse.2006.12.002.

[12] Jia, Hujun , H. Zhang , and Y. Yang . "A novel 4H-SiC MESFET with a L-gate and a partial p-type spacer." Materials Science in Semiconductor Processing 15.1(2012):2-5,doi:10.1016/j.mssp.2011.09.008.

[13] S. Sriram et al., "High-Performance Implanted-Channel SiC MESFETs," in IEEE Electron Device Letters, vol. 32, no. 3, pp. 243-245, March 2011, doi: 10.1109/LED.2010.2095824.

[14] Jia, Hujun , et al. "Improved performance of 4H-silicon carbide metal semiconductor field effect transistors with multi-recessed source/drain drift regions." Materials Science in Semiconductor Processing 31(2015):240-244, doi: 10.1016/j.mssp.2014.11.046.

[15] Jia, Hujun, et al. "A novel 4H-SiC MESFET with serpentine channel for high power and high frequency applications." Superlattices & Microstructures 101.JAN. (2017):315-322,doi: 10.1016/j.spmi.2016.11.055.

[16] Jia, H. J., Li, T., Tong, Y. B., Zhu, S. W., Liang, Y., Wang, X. Y., Yang, Y. T. (2020). A novel 4H-SiC MESFET with symmetrical lightly doped drain for high voltage and high power applications. Materials Science in Semiconductor Processing, 105. doi:10.1016/j.mssp.2019.104707.

[17] Jia, Hujun , et al. "An improved DRBL AlGaN/GaN HEMT with high power added efficiency." Materials Science in Semiconductor Processing 89(2019):212-215,doi: 10.1016/j.mssp.2018.09.013.
[18] Chung, G. Y. , et al. "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide." Applied Physics Letters 76.13(2000):1713.
[19] T. Hiyoshi, T. Hori, J. Suda and T. Kimoto, "Simulation and Experimental Study on the Junction Termination Structure for High-Voltage 4H-SiC PiN Diodes," in IEEE Transactions on Electron Devices, vol. 55, no. 8, pp. 1841-1846, Aug. 2008, doi: 10.1109/TED.2008.926643.
[20] C. -Y. Cheng and D. Vasileska, "Static and Transient Simulation of 4H-SiC VDMOS Using Full-Band Monte Carlo Simulation That Includes Real-Space Treatment of the Coulomb Interactions," in IEEE Transactions on Electron Devices, vol. 67, no. 9, pp. 3705-3710, Sept. 2020, doi: 10.1109/TED.2020.3007368.
[21] J. Zhang, B. Zhang and Z. Li, "Simulation of high-power 4H-SiC MESFETs with 3D tri-gate structure," in Electronics Letters, vol. 43, no. 12, pp. 692-694, 7 June 2007, doi: 10.1049/el:20070777.
[22] S. Onoda, T. Makino, S. Ono, S. Katakami, M. Arai and T. Ohshima, "Spatial, LET and Range Dependence of Enhanced Charge Collection by Single Ion Strike in 4H-SiC MESFETs," in IEEE Transactions on Nuclear Science, vol. 59, no. 4, pp. 742-748, Aug. 2012, doi: 10.1109/TNS.2012.2195199.
[23] Ali, Naderi , and M. Hamed . "High breakdown voltage and high driving current in a novel silicon-on-insulator MESFET with high- and low-resistance boxes in the drift region." The European Physical Journal Plus 133.6(2018):221-, doi: 10.1140/epjp/i2018-12047-5.
[24] A. Aminbeidokhti, A. A. Orouji, S. Rahmaninezhad and M. Ghasemian, "A Novel High-Breakdown-Voltage SOI MESFET by Modified Charge Distribution," in IEEE Transactions on Electron Devices, vol. 59, no. 5, pp. 1255-1262, May 2012, doi: 10.1109/TED.2012.2186580.
[25] C. E. Weitzel et al., "Silicon carbide high-power devices," in IEEE Transactions on Electron Devices, vol. 43, no. 10, pp. 1732-1741, Oct. 1996, doi: 10.1109/16.536819.
[26] R. J. Trew, "High-frequency solid-state electronic devices," in IEEE Transactions on Electron Devices, vol. 52, no. 5, pp. 638-649, May 2005, doi: 10.1109/TED.2005.845862.

Figures

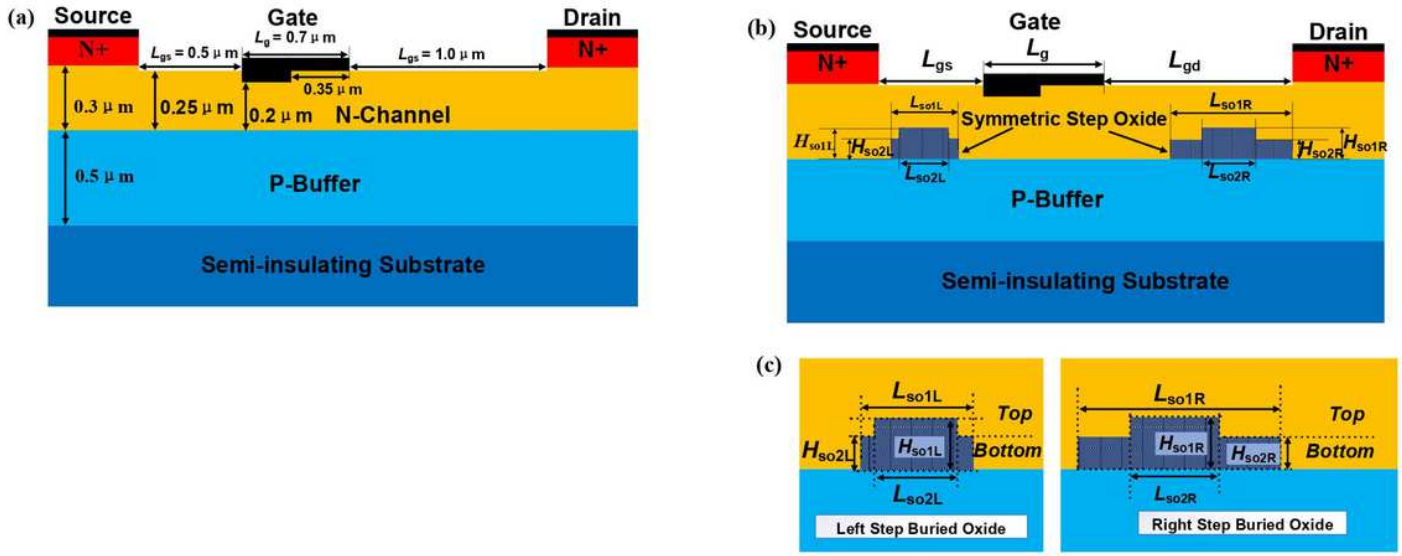

Figure 1

Schematic diagram of DR MESFET (a), new structure MESFET (b), enlarged view of symmetrical oxide layer structure(c).

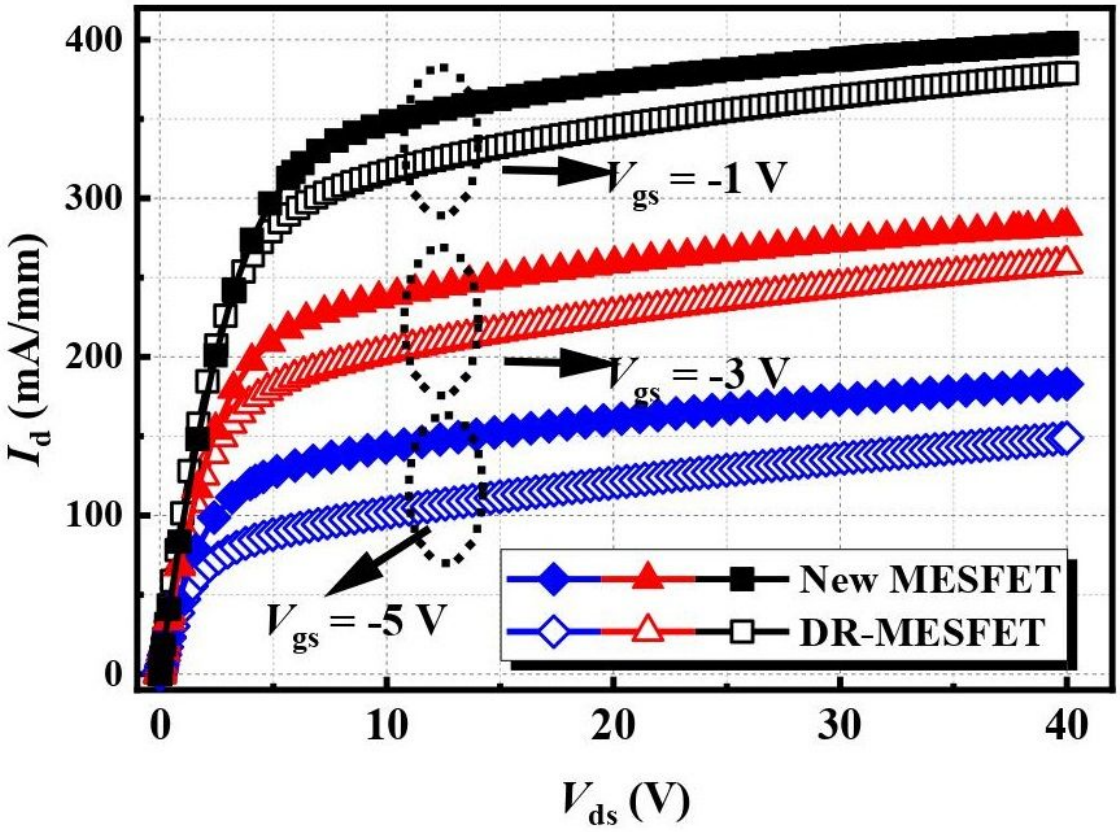

Figure 2

Id-Vds characteristics at different gate voltages (Vgs = -1 V, -3 V, -5 V).

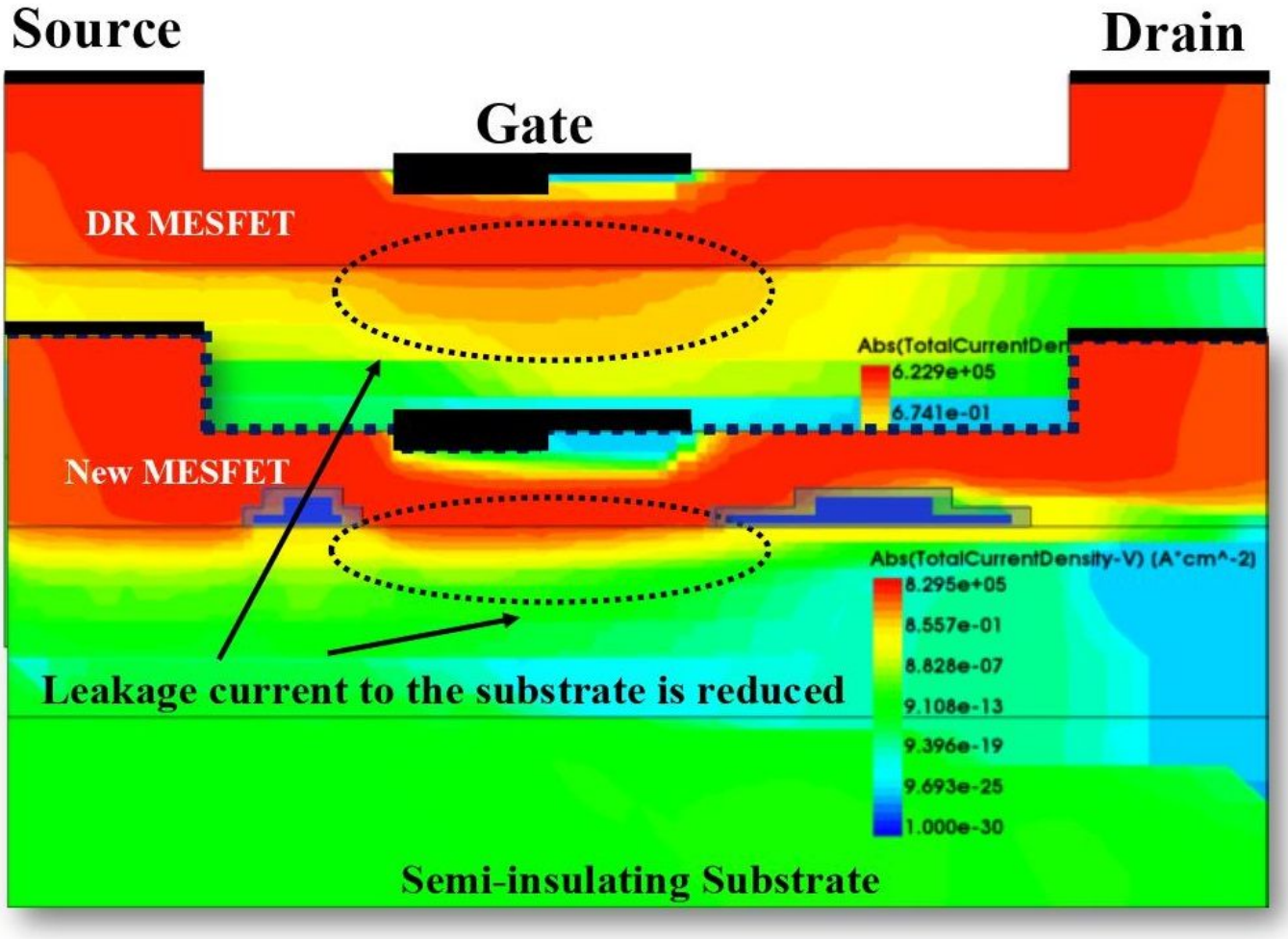

Figure 3

Simulation diagram of the total current density of the two structures.

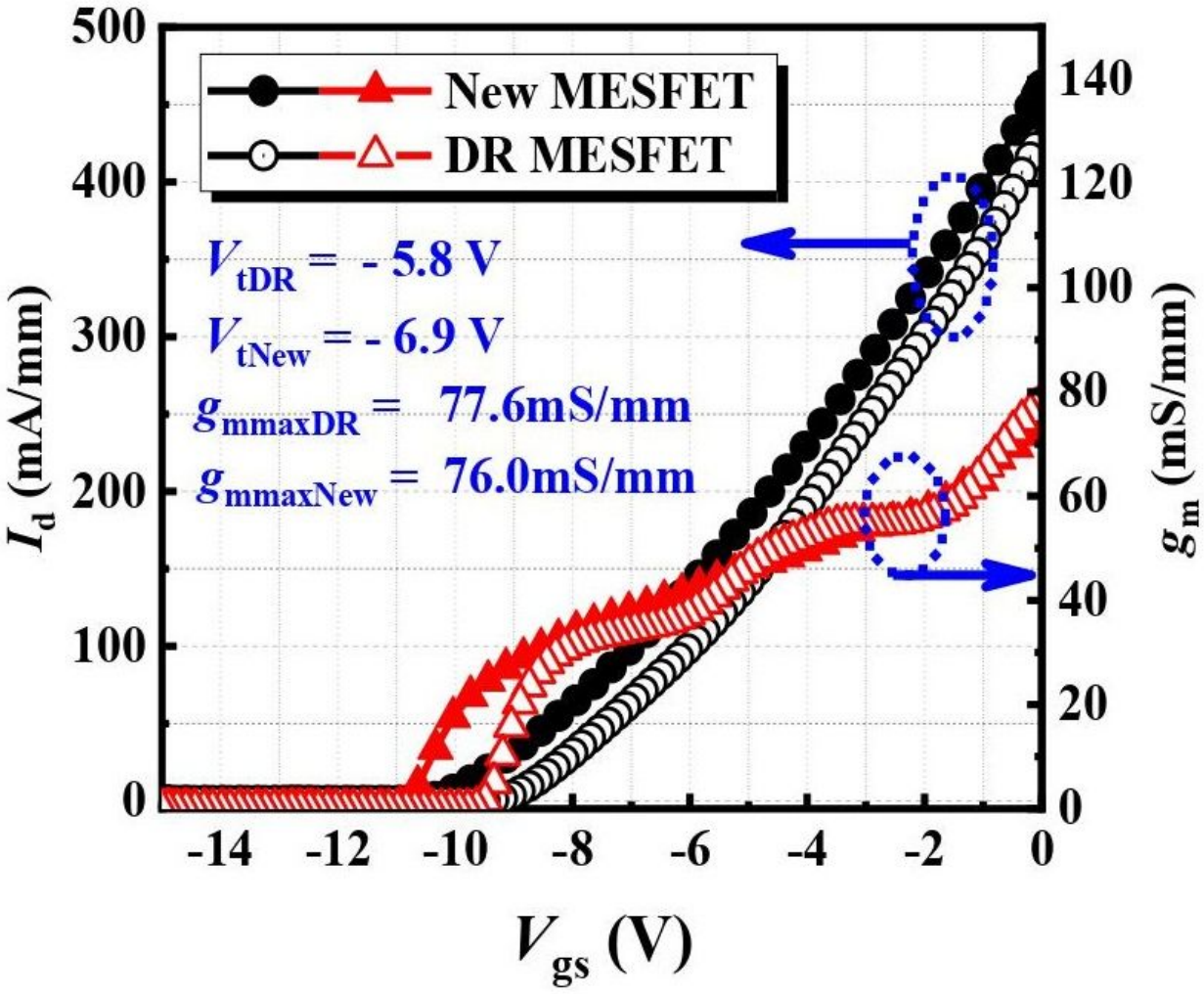

Figure 4

Transfer characteristics and transconductance of the two structures.

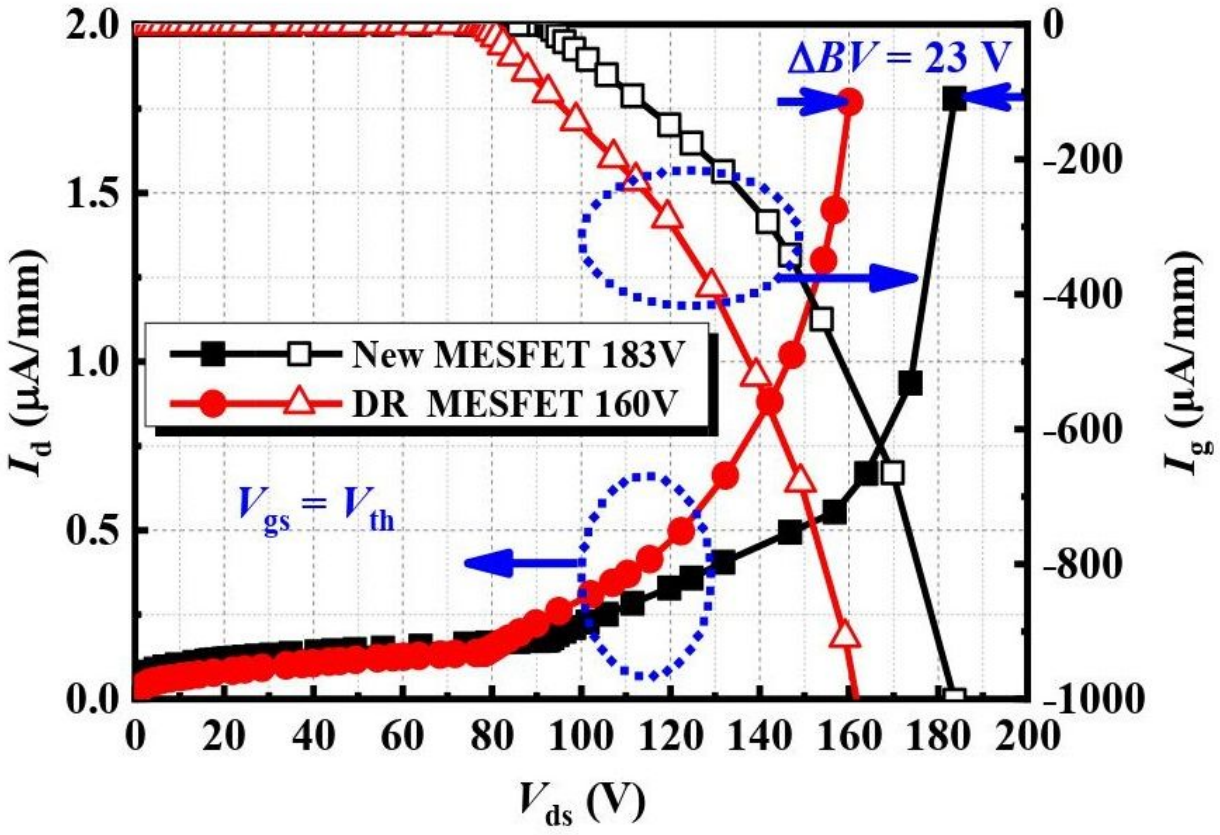

Figure 5

Breakdown characteristics of two devices.

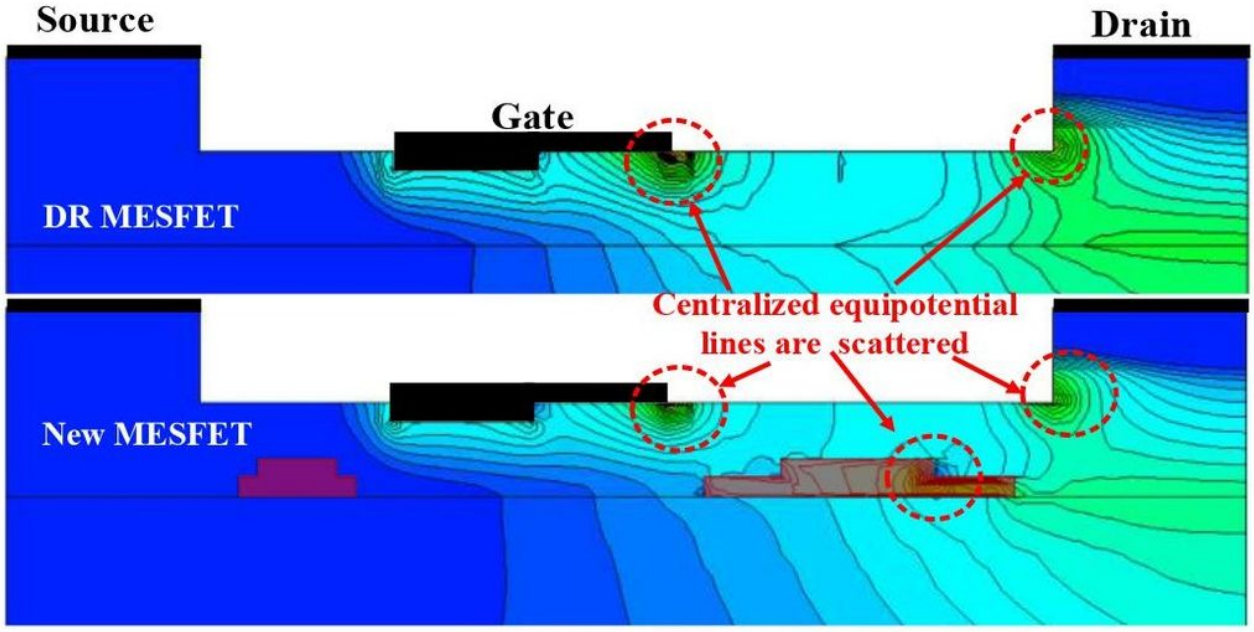

Figure 6

Electric field distribution curve, DR 4H-SiC MESFET (top), new 4H-SiC MESFET.

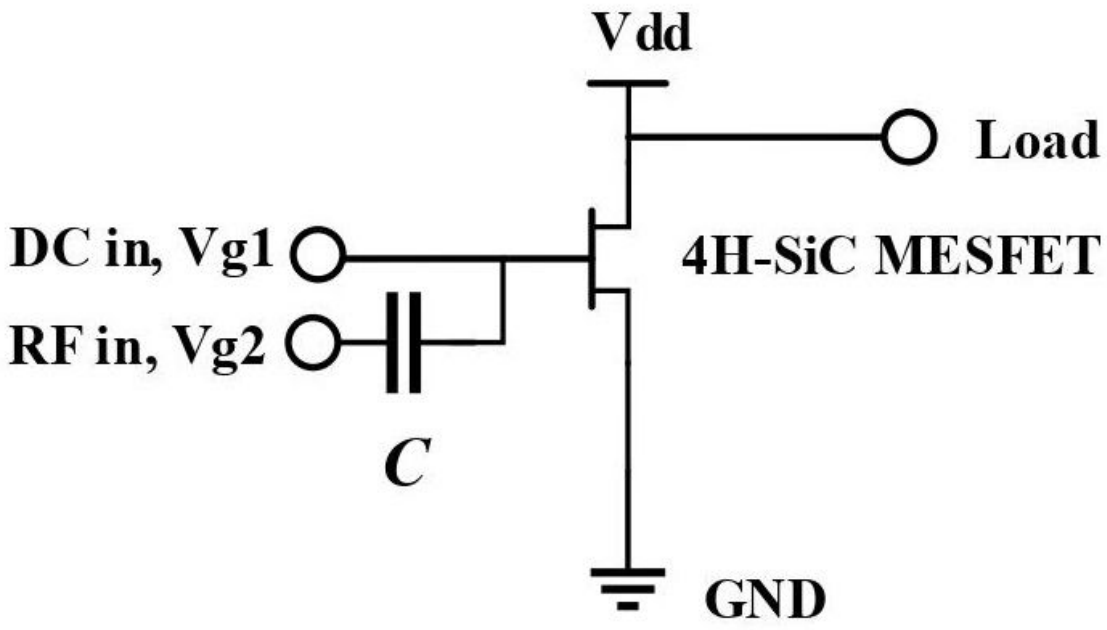

Figure 7

One tone Load pull schematic for 4H-SiC MESFET measurement.

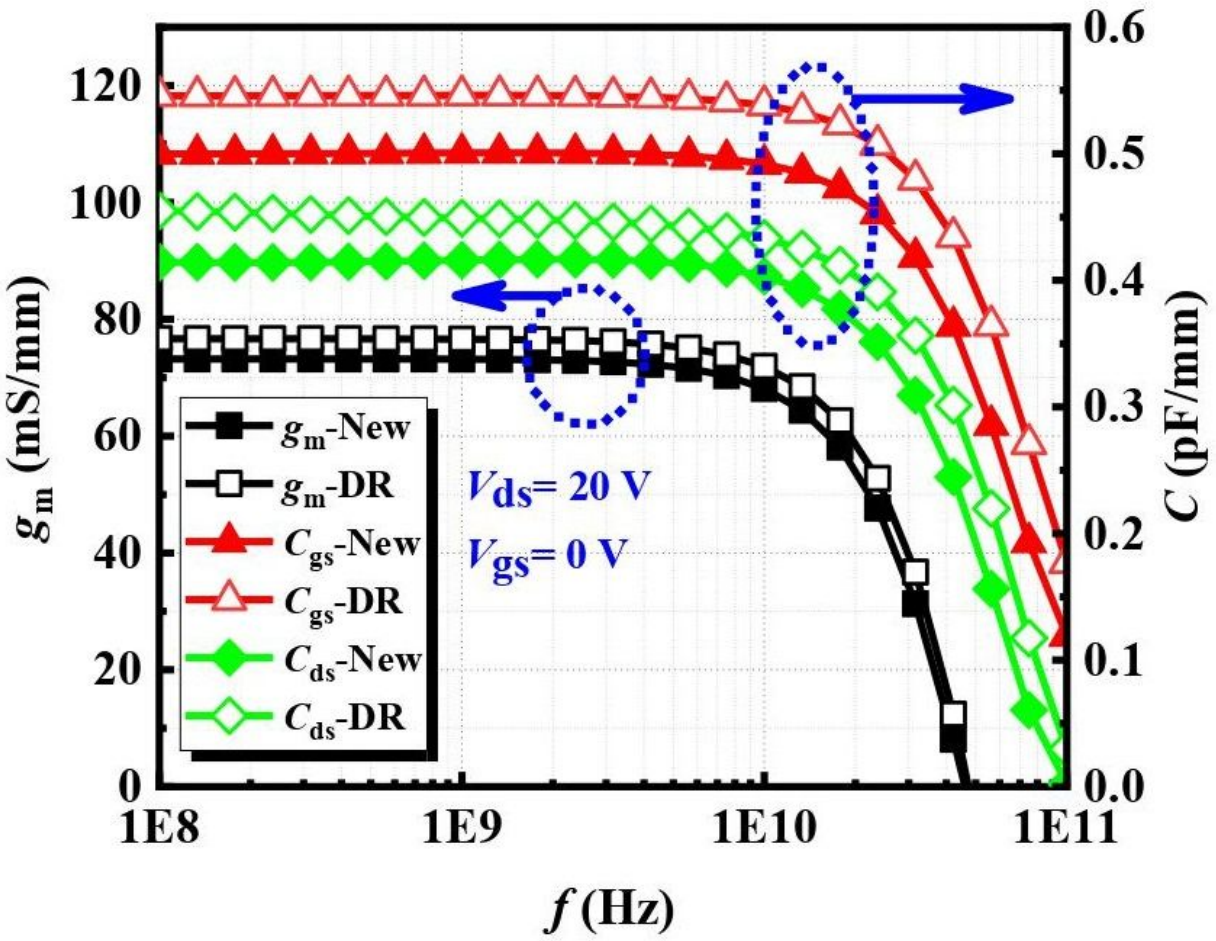

Figure 8

Changes of AC transconductance gm, Cgs and Cgd in two periods at different frequencies (Vds = 20 V, Vgs = 0 V).

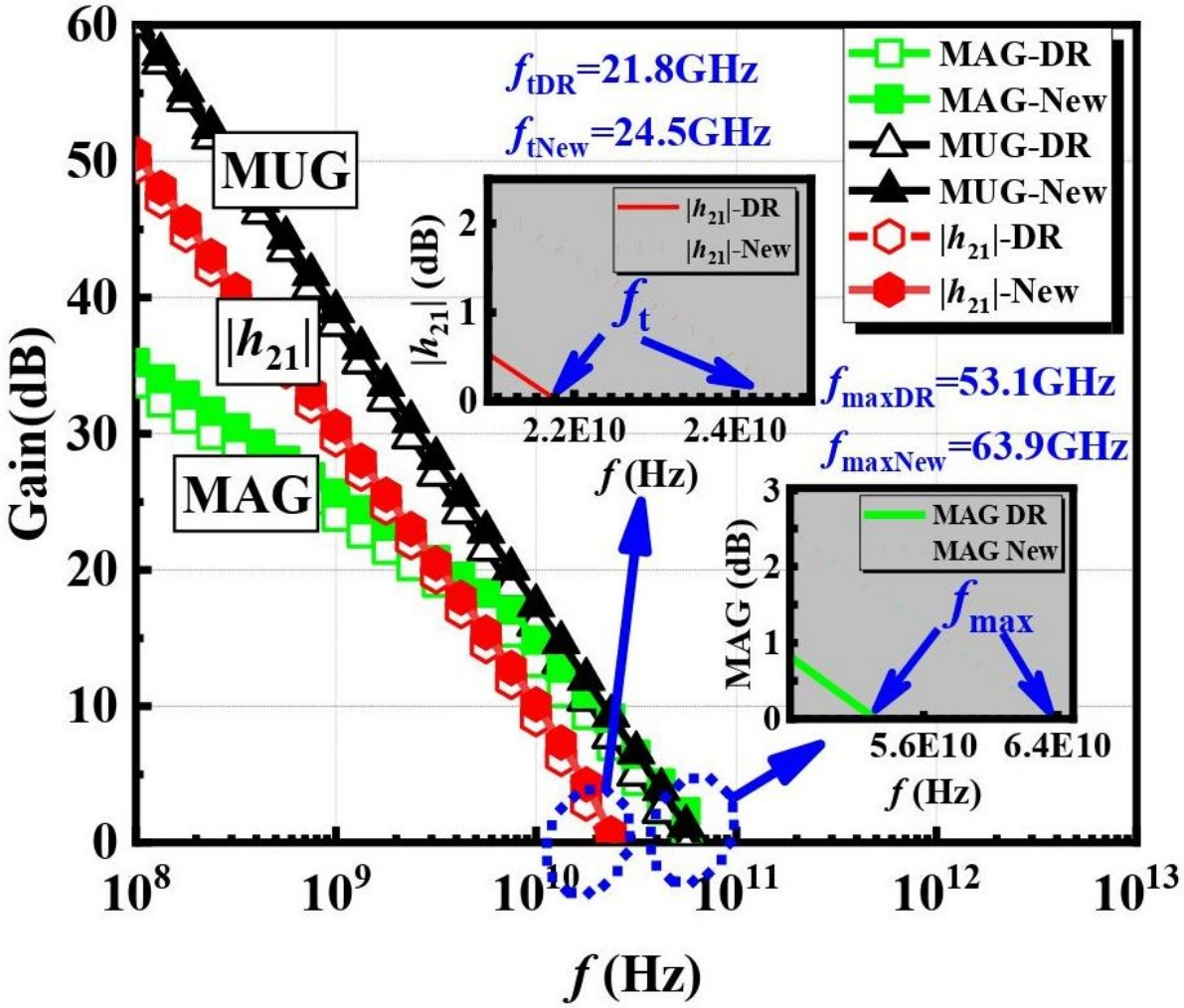

Figure 9

Variation curve of small signal gain with frequency and fmax, ft.

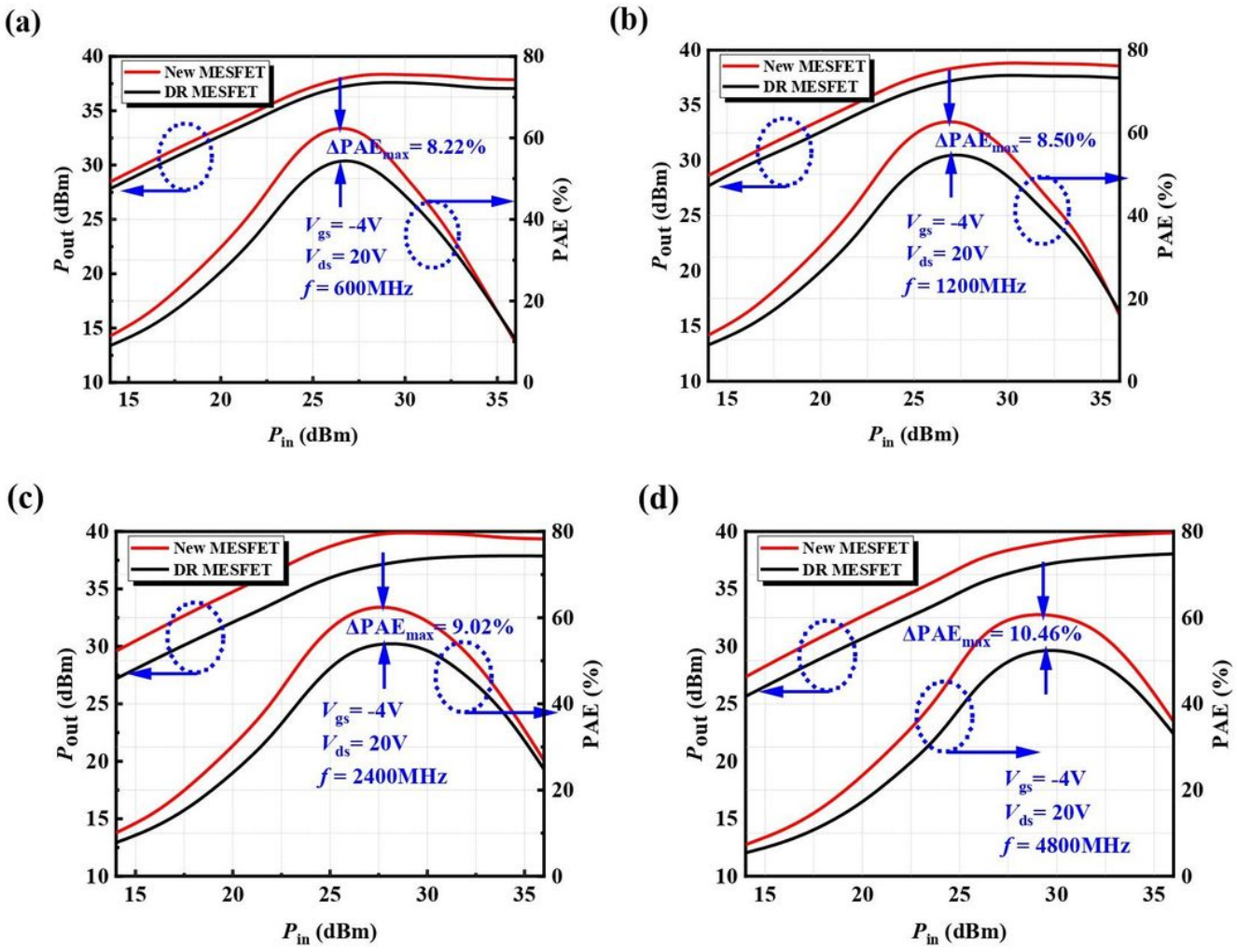

Figure 10

Variation curve of output power and PAE with input at different frequencies.