The Power Analysis of 1T-DRAM Cell with Different FET technologies

Durgesh Addala (✉ addaladurgesh@gmail.com)

Lovely Professional University <https://orcid.org/0000-0001-9148-8600>

Sanjeet Kumar Sinha

Lovely Professional University

Gadiparthi Mohan Chandu

Lovely Professional University

Research Article

Keywords: Semiconductor memories, DRAM, CNTFET, Read, Write, Refresh

Posted Date: July 12th, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-477489/v1>

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Abstract

DRAM's are essential for memory-based electronics devices and the usage of RAM is increasing day by day to reach the user's expectation the products are get designed based on low power and portable. Power dissipation is a major issue to solve this issue researchers are focusing on low power circuits and trying to design the circuits with less number of the transistor so that it will consume less amount of power. In this paper, three structures are presently based on MOSFET technology and CNTFET technology. MOSFET model structures are divided into two they are 1.DRAM circuit with Tri-state buffers and 2. DRAM circuit without Tri-state buffers. CNTFET based structure is built with the help of 'CarbonNanoTube-FET's and the structure is the same as DRAM without Tri-state buffers. Power analysis, voltage, delay are evaluated with the help of cadence virtuoso and LTspice Tools.

1 Introduction

Semiconductor Memories are derived into Random Access Memories and Read Only Memories. The name of these memories itself defines the work and functionality of memories and again these memories are classified based on volatile nature. As we know that volatile memories require power to store the data similarly non-volatile memories can stores data in absence of power. The current trend is focusing on lightweight and portable memory devices if the size and weight of the device decrease everyone is willing to buy such devices [1]. RAM is divided into SRAM and DRAM and these are volatile memories that require power to store. This paper focus on DRAM structure and implementation in cadence tool. Three structure models are described and they are MOSFET based DRAM with Tri-state buffers, MOSFET based DRAM without Tri-state and CNTFET based DRAM.

In the first model '13' no of transistors are used if the transistor count is reduced the amount of power consumption will decrease. So, in the second model, no of transistors is decreased and the transistor count is '4'. The first model structure is almost three times greater than the second model. Similarly, the third model is built simply by replacing MOSFETs with CNTFETs from the second model.

2 Dram Circuitry

Dynamic Random Access Memories requires periodic refresh because the circuitry is built in such format as the capacitor and the output is in contact due to this contact the memory present in the capacitor will lose for this drawback Dynamic Random Access Memories requires periodic refresh [2]. The schematic of 1T and 1C DRAM is shown below in Fig. 1 [3].

[Fig. 1 about here.]

The entire circuit of DRAM requires three inputs and one output. 'Datain', 'R_W', 'WL', and 'refresh' are termed as input terminals and 'Dataout' is termed as an output terminal. Here three buffers are used one high enabled buffer and two low enabled buffers and these are fixed in such a manner to get DRAM output. Coming to buffers the internal structure of high enabled buffer is shown in Fig. 2 [4–5].

[Fig. 2 about here.]

[Fig. 3 about here.]

Here transmission gates are used as buffers and circuitry requires one NMOS and one PMOS arranged in transmission gate manner and for inverting the enabling input inverter is required based on the connecting enable input and inverting output high and low enable buffers are varied. For high enabled buffer enable input is connected to the controlling terminal of NMOS inverting output is connected to the controlling terminal of PMOS. Input is connected to one end of the transmission gate and output is taken from another end of the transmission gate. The output waveforms are shown in Fig. 3 [6].

Figure 1.3. The output waveform of the high enabled buffer.

[Fig. 4 about here.]

The low enabled buffer circuit is the same as the high enabled buffer only the connections of enabling input and inverting output is varied. The schematic of the low enabled buffer is shown in Fig. 4.

The output waveform of the low enabled buffer is shown in below Fig. 5.

[Fig. 5 about here.]

3 Working Of 1t-dram Cell With Tri-state Buffers

one transistor and one capacitor DRAM is shown in Fig. 1.1 coming to the working of DRAM, DRAM circuitry based on charging and discharging of capacitor Dynamic RAM is build [7]. Datain input terminal is used to send the data as input and suppose to store data in the capacitor. 'R_W' input terminal is used to decide whether to Read or Write operation is done. The circuitry is designed in a particular manner that if the high input signal is applied to 'R_W' input, the high enabled buffer is get activated and whatever the data is coming from Datain input terminal is directly short-circuited with the 'N' type pass transistor is connected to the capacitor and NMOS pass transistor is controlled by 'WL' input terminal whenever the high input signal is applied NMOS pass transistor act as short-circuit and if 'R_W' input terminal is applied with low input signal high enabled buffer to get deactivated and stops taking data from 'Datain' input terminal. In this case, Read is activated whatever data present in the capacitor is shown as output at the 'Dataout' output terminal. At Reading state the capacitor is directly contacted with output terminal after some time the capacitor will discharges then wrong output is displayed at the output to avoid this situation refresh buffer is placed and it is a low enabled buffer. With the help of a refresh buffer, the same data is refreshed in the capacitor. The final output waveforms of the 1T and 1C DRAM circuit is shown in Fig. 6.[8–9].

[Fig. 6 about here.]

Figure 6. The output waveform of 1T and 1C DRAM circuit.

4 Dram Without Tri-state Buffers

For the low power and lightweight devices the size of the device is decreased in the same way instead of using high and low enabled Tri-state buffers 'NMOS' and 'PMOS' are replaced. For 1T and 1C DRAM, it requires a '13' number of transistors but DRAM without Tri-state buffers requires only a '4' number of the transistor to execute the DRAM function. If the number of the transistor decreases the power and area will be reduced it is easy to design portable devices. The DRAM without Tri-state buffers is shown in below Fig. 7.

[Fig. 7 about here.]

[Fig. 8 about here.]

5 1t-dram Cell With Cntfet

The entire structure of DRAM is replaced with 'N' and 'P' type CNTFET's. Comparing to bulk CMOS technology CNTFET 5nm technology has many advantages. The circuit diagram of 1T and 1C DRAM based on CNTFET technology is shown in below Fig. 9. [10–13].

[Fig. 9 about here.]

The output waveform 1T and 1C DRAM using CNTFET technology is shown in the below Fig. 10.

[Fig. 10 about here.]

Digital memories are supposed to store in the binary format the capacitor helps to store the data if high input signal digital

'1' is stored by charging the capacitor in the same way for storing digital '0' the capacitor gets discharged [13–15].

6 Dram Circuit With Dg-finfet Technology

DG-FINFET technology files are used to simulate the DRAM circuit and the circuit is the same as DRAM without buffers. And the transient analysis is done with help of the LTspice tool. The schematic of the DRAM circuit with DG-FINFET Technology is shown in below Fig. 11. [16, 17].

[Fig. 11 about here.]

The output waveforms of DRAM circuit-base DG-FINFET is shown below Fig. 12.

[Fig. 12 about here.]

7 Results

Here the comparative analysis of power, voltage and delay are calculated. With the help of this information, a better DRAM circuit is identified for low power application. Table I gives the average power values of DRAM with and without buffers. Table II gives the Average Voltages values of 'WL', 'refresh', 'R_W', 'Datain' & 'Dataout' with different types of DRAM structures. Table III calculates the delay values of different parameters present in the DRAM circuit. And the response of three different structured DRAM cell is represented graphically and in tabular form are shown in below figures and tables.

[Fig. 13 about here.]

of 'WL', 'refresh', 'R_W', 'Datain' & 'Dataout' with different types of DRAM structures. DRAM circuit. the response of three different structured DRAM cell is represented graphically and in tabular form are shown in below figures and tables.

[Fig. 14 about here.]

The output graphs of a DRAM with buffers are shown in the below figures.

[Fig. 15 about here.]

[Fig. 16 about here.]

[Fig. 17 about here.]

[Fig. 18 about here.]

[Fig. 19 about here.]

[Fig. 20 about here.]

[Fig. 21 about here.]

[Fig. 22 about here.]

[Fig. 23 about here.]

[Fig. 24 about here.]

[Fig. 25 about here.]

[Fig. 26 about here.]

[Fig. 27 about here.]

[Fig. 28 about here.]

[Fig. 29 about here.]

[Fig. 30 about here.]

TABLE I

COMPARATIVE POWER ANALYSIS OF DRAM STRUCTURES

[Table 1 about here.]

TABLE II

COMPARATIVE VOLTAGE ANALYSIS OF FOUR STRUCTURES OF DRAM

[Table 2 about here.]

TABLE III

DELAY COMPARISON OF DRAM WITH AND WITHOUT BUFFERS.

[Table 3 about here.]

8 Conclusion

This paper explains the working of 1T DRAM using various technology model files and helps to find better results related to DRAM for low power consumption. Reducing of transistor number will reduce the consumption of power. Compare to DRAM with buffers (no of transistors = 13) DRAM without buffers (no of transistors = 4) having less number of transistors. For DRAM power consumption is very precious, compared to the SRAM circuit the DRAM circuit consumes more because it requires a periodic refresh. For the low power DRAM low power consumed MOSFET's are different types of FET's are required. While comparing with three different structures of DRAM, CNTFET (5nm technology node) based consumes less amount power and it is suitable for producing low power consumption DRAM. For low power dissipation, FDSOI FET is best if DRAM built with FDSOI Technology gives better result compare to other technology.

Declarations

Funding : Not Applicable

Conflict of interest/Competing interests : Not Applicable

Availability of data and material : all simulation results are available in cadence virtuoso Lab of VLSI Domain under School of Electronics and Electrical Engineering , lovely Professional University, Punjab, India

Code availability : Not Applicable

Author's contributions : All the authors did their contribution in the manuscript for the possible publication.

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- ## Figures

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Figure 2

High enabled buffer

Figure 3

The Output waveform of High enabled buffer.

Figure 6

The Output Waveform of 1T and 1C DRAM.

Figure 7

DRAM circuit without Tri-state buffers.

Figure 8

The output waveform of DRAM circuit without Tri-state buffers.

Figure 9

Structure of 1T and 1C DRAM using CNTFET.

Figure 10

The Output Waveform 1T and 1C of DRAM using CNTFET.

Figure 11

The DRAM circuit-based DG-FINFET

Figure 12

The Output Waveform of DG-FINFET based DRAM.

Figure 13

Power Analysis for DRAM with buffers.

Figure 14

Power Analysis for DRAM without buffers.

Figure 15

Power (w) vs Time (sec) graph.

Figure 16

DataoutVoltage (VDO) vs time (Sec) graph.

Figure 17

DatainVoltage (VDI) vs time (Sec) graph

Figure 18

R_W Voltage (VR_W) vs time (sec) graph

Figure 19

Refresh Voltage (VR) vs time (Sec) graph.

Figure 20

WL Voltage (VW L) vs time (Sec) graph.

Figure 21

Power (W) vs time (sec) (130nm).

Figure 22

Dataout Voltage (VDO) vs time (sec).

Figure 23

Datain Voltage (VDI) vs time (sec).

Figure 24

R_W Voltage (VR_W) vs time (sec).

Figure 25

Refresh Voltage (VR) vs time (sec).

Figure 26

WL Voltage (VW L) vs time (Sec) graph.

Figure 27

R_W Voltage (VR_W) vs time (sec).

Figure 28

WL Voltage (VW L) vs time (sec).

Figure 29

Datain Voltage (VDI) vs time (sec).

Figure 30

Dataout Voltage (VDO) vs time (sec).

Figure 31

Refresh Voltage (VR) vs time (sec).