Design and Performance Enhancement of Gate-on-Source PNPN Doping–Less Vertical Nanowire TFET

Kritika Lal
Amity University

Anushka Verma
Amity University

Pradeep Kumar
Amity University

Naveen Kumar
University of Glasgow

S. Intekhab Amin
Jamia Millia Islamia Central University: Jamia Millia Islamia

SUNNY ANAND (✉ sunnyanand.42@gmail.com)
Amity University   https://orcid.org/0000-0002-0188-5790

Research Article

Abstract

This paper outlines the study of a Doping-Less Vertical Nanowire Tunnel Field Effect Transistor (DLVNWTFET) with a p-i-n structure, aiming to enhance the performance of this device. The proposed device, which is a p-n-p-n configured DLVNWTFET, switches with a steeper sub-threshold slope while keeping the Off-state current (I_{OFF}) and threshold-voltage (V_{TH}) low and also improves the On-state current (I_{ON}) of the device; which is one of the crucial problems in TFETs. The nanowire TFET structure is vertically grown on an intrinsic silicon wafer. This vertical structure eases the fabrication process and also helps in the implementation of Charge-Plasma (CP) Technique. It is a process by which electrodes of specific work functions are used to induce charges in the Source (P) and Drain (N) regions. To realize the p-n-p-n configured structure, pocketing technique is used where the N+ heavily doped pocket is introduced between the Source and the Channel through CP concept. Upon calculation and comparison of various analog and device parameters, the proposed p-n-p-n structure shows better performance in contrast to the p-i-n DLVNWTFET. Analysis of the performance of the two configurations has been done, comparing various parameters like transconductance (G_m), output conductance (G_D), transfer characteristics ($I_D - V_{GS}$), output characteristics ($I_D - V_{DS}$), cut-off frequency (fT), total gate capacitance (C_{GG}) and intrinsic gain.

1. Introduction

The electronics industry has been greatly influenced since the remarkable technological invention of Integrated Circuits. In 1965, Moore predicted the pace of upcoming revolution in modern digital era, which became the golden rule for electronics industry. To keep up with the Moore's law, the electronics industry has been working to make faster, affordable and smaller transistors that would drive our modern digital gadgets. The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) which was first invented in 1959 at Bell Labs, has been attempted to scale down for the past 50 years in order to attain high density, performance and cost-effectiveness [1]. However, Short channel effects (SCE) are introduced due to scaling down of MOSFET [2] which adds to the already existing limitation of threshold voltage (V_{TH}), high Off-state Current (I_{OFF}) and Sub-Threshold Swing (SS) (60 mV/dec) [3]. MOSFET-based nano-devices are more susceptible to SCE and it is difficult to attain Saturation of drain current due to the ballistic effect of charge carriers [4]. TFETs have shown potential to be considered as a capable alternative as they outperform MOSFET in terms of SS, V_{TH} and I_{OFF} [5]. This is made possible due to the mechanism of TFET i.e., Band to Band Tunnelling, which increases the On to Off State Current ratio (ION/IOFF) as compared to Thermionic emission in MOSFET. This also breaks the limitation of MOSFET by achieving a SS lower than 60 mv/dec. However, TFETs offer low ON-state current due to the tunneling inefficiency [6]. Abrupt junctions are effective in tunneling but a high-temperature process is required to create these. [7]. To resolve these issues, Charge Plasma (CP) technique can be used.

The objective is to achieve high Ion, low V_T, reduce cost and overcome the shortcomings of Conventional TFETs. Therefore, in this paper, a Doping-Less Vertical Nanowire Tunnel Field Effect Transistor is being

introduced which has a p-n-p-n configuration. Doping-less structure are more economical and defect-free [3]. There are two ways to induce doping in the intrinsic substrate which are Electrostatic and Charge Plasma (CP)Technique. The proposed device is based on CP technique as it also resolves the problem of the Abrupt Doping Profile. CP technique utilizes Electrodes having suitable work- function to induce p-doped Source and n-doped Drain regions [8]. Vertical Nanowire eases the device fabrication process compared to axial nanowires [3]. The cylindrical-shaped GAA structure offers stronger electrostatic control of the charge carriers due to greater surface inversion which in turn increases the drain current. The p-n-p-n configured structure is similar to the p-i-n TFETS with a variation by introducing a n-pocket from the CP technique.

2. Device Architecture And Simulation Parameters

The 2D structures of the two devices, DL-V-NW-TFET with p-i-n and p-n-p-n configuration, are presented in Figure 1(a) and (b) respectively. Similarly, the 3D structures for the same is represented in Figure 1(c) and (d) respectively. Drain (D), Source (S), Gate(G), Channel, electrodes and oxide regions are indicated in the diagrams.

The proposed nanowire device is grown vertically on the SOI (Silicon on Insulator) wafer [3]. In this device, intrinsic Si with 7nm thickness, is used for Drain (D), Source (S), Channel regions. This is a Doping-less device, thus for fabricating the source and drain regions, Charge Plasma (CP) technique is adopted [6]. In this technique, metals with relevant work function are used as the drain/source electrode, as a result of which, generation of e^- and h^+ is facilitated [9].

Table1 illustrates the designing parameters used in the process. To create the Source (p^+) region, Platinum (work-function = 5.93eV) is used as a source-metal. Similarly, Aluminium (work-function = 4.2eV) is used as drain-metal to form drain (n^+) region. The aim of choosing Platinum and Aluminium for source and drain electrodes, respectively, is that for p-type doping in the source region, work-function electrode used for Source metal must be higher than that of intrinsic Si substrate. Similarly, in drain region, electrode work function of the drain-metal must be less than that of intrinsic Silicon, for n-doping [8]. Figure 1 clearly shows the placement of the aforementioned metal electrodes. Tungsten (work function = 4.5 eV) is used for the Gate metal electrode. The gate oxide thickness for both structures is 2 nm. SiO_2 makes up the oxide region surrounding the intrinsic silicon body in both devices. This use of SiO_2 facilitates the effortless process of deposition and feasibility of ultra-thin consistency settled above the surface of intrinsic silicon [3]. Channel length (L_G), Source length (L_{DS}) and Drain Length (L_{SD}) for the structure is 20 nm each. The doping concentration is 3×10^{19} cm^{-3} for the source (p) region, 2×10^{19} cm^{-3} for the drain (n) region and 10^{19} cm^{-3} for the channel region, for both the device configurations. Radius (R) of the nanowire is 7.5 nm.

The p-n-p-n configuration of the device structure is similar to a TFET of pin structure. The only difference is that an N^+ pocket is induced between the Source (S) and channel region in the p-n-p-n configured

device. For actualizing this, we use CP technique in which an electrode of suitable work-function is used to introduce n^+ doping near the interface of the source (S)-channel. By doing so, the tunneling field is increased, which therefore increases I_{ON}, and thus the device performance is improved when weighed up against p-i-n TFET [10]. The proposed device predominates the formation of the abrupt-junction [3]. For efficient tunneling in the TFETs, an abrupt junction is required. However, this process is difficult and requires a high-temperature process which often diffuses dopant atoms into the channel from S/D regions. For this reason, we use CP technique in our work.

Table 1 Parameters for designing the DLVNWTFET

PARAMETERS	DLVNWTFET
Channel Length (L_G)	20 nm
Radius (R)	7.5 nm
Oxide Thickness (t_{ox})	2 nm
Source Doping (p)	3×10^{19}
Drain Doping (n)	2×10^{19}
Channel Doping	1×10^{19}
Insulator Permittivity (SiO_2)	25
Source and Drain Length (L_{DS} and L_{SD})	20 nm
Source Material	Silicon
Channel Material	Silicon
Drain Material	Silicon
Gate Oxide	SiO_2
Source Metal Electrode (p) work function	5.93 eV
Drain Metal Electrode (n) work function	4.2 eV
Gate Metal Electrode (p) work function	4.5 eV
p Doping Concentration (Si)	1×10^{15}

Models mentioned below are used to define the characteristics of the device and are used in the simulation. For the tunneling of charge carriers through the device, BTBT (Band-to-Band Tunnelling) model is used. SRH (Shockley-Read-Hall) and AUGER models used help in calculating the generation and recombination rate of charge carriers. Various models like FLDMOB (Field Dependent Mobility), CONMOB

(Concentration Dependent Mobility) and CVT (Lombardi Model) are used to calculate mobility dependence on electric field and charge concentration. Models like FERMI & NI.FERMI adhere to Fermi Dirac Statistics as charge carrier concentration may exceed the available density of states due to CP technique. BGN model is effective in taking into account the variation in energy bandgap that can occur due to heavy induced doping of S/D region. QUANTUM correction models help in analyzing the feasible quantum effects in the device [3].

3. Ac And Dc Performance Analysis

In our work, we have analysed the performance of our proposed device, p-n-p-n DLVNWTFET with the p-i-n structure and compared them for the two operating states, i.e., ON and OFF. We have performed both the DC and AC analyses.

Figure 2a and 2b respectively compare the simulated Energy Band diagrams of DLVNWTFET of p-i-n and p-n-p-n configuration. This comparison is made for both the OFF-state where (V_{GS} = 0 V, V_{DS} = 1.0 V) and ON-state where (V_{GS} = 1.5 V, V_{DS} = 1.0 V). In the OFF-state, the p-n-p-n configuration DLVNWTFET shows a reduced bandgap in the source region. When the device is working in on-state, the reduced bandgap at Source (S) side reduces the tunneling width as seen in Fig. 2b. Introducing a pocket(N+) near the Source(S)-Channel interface helps in reducing the tunneling width. The band is bent further at source junction because of pocketing in p-n-p-n configuration DLVNWTFET resulting in lowering of tunnel width, resulting in an increase in tunneling probability at the interface of Source(S) and Channel, hence improving the device performance [11].

The Electric field plot of the DLVNWTFET of p-i-n and p-n-p-n configuration along x-coordinate in I_{OFF} and I_{ON} are studied in Figure 3a, 3b correspondingly. Electric field intensity can be seen to rise at the interface of Source & Channel and decrease towards the Drain-Channel interface. In p- n-p-n configuration, e⁻ field intensity rises near the source − channel interface in contrast to that of p-i-n configuration, this happens because of the N-pocket induced by using CP technique. Since there is more bending of the band at source-channel interface (shown in Fig 2a), this leads to a high electric field and probability of tunneling at the source-channel interface hence the p-n-p-n is configured DLVNWTFET offers improved performance.

The electron concentration profiles of DLVNWTFET of p-i-n and p-n-p-n configuration along x-coordinates in I_{OFF} and I_{ON} are represented in Figure 4a, 4b, respectively. Required electron concentration is achieved with the use of suitable S/D metal work function by using the charge plasma technique. In p-n-p-n configuration, e⁻ conc is higher at the interface of source and channel as compared to that of p-i-n configuration, this indicates the introduction of N pocket by the usage of CP technique.

Figure 5 shows the $I_D - V_{GS}$ characteristics of the DLVNWTFET of p-i-n and p-n-p-n configuration. From the graph, we can conclude that p-n-p-n configuration DLVNWTFET offers a higher I_D and has a lower threshold voltage and steeper curve in contrast to p-i-n configured DLVNWTFET. It is observed that the I_{ON}

is improved, keeping the I_{OFF} unaffected in the p-n-p-n configured TFET. The rise in I_D is observed because of the use of CP technique near the source-channel region, which introduces a N-type pocket that improves the electron concentration, bends the bandgap more near the Source-channel junction lowering the tunneling width and increasing the tunneling probability which therefore increases drain current for lower gate voltages and enhances the I_{ON} of the device, as represented in Figure 5. With this, we conclude that p-n-p-n structure offers a higher I_{ON} (i.e., I_{ON}= 8.86653 x 10^{-6}) and is switched on at a lower gate voltage (i.e., Vt=0.372621).

Transconductance (G_m) showcases the ability to amplify and hence is a crucial factor in the designing of analog circuits (like amplifiers). It is illustrated as the slope of I_D-V_{GS} curve and is calculated by the formula given below:

$$Gm = Id/VGS \qquad\qquad ...(1)$$

The comparison of Transconductance for the DLVNWTFET of p-n-p-n configuration and p-i-n configuration is shown in Fig. 6. These results conclude that the proposed p-n-p-n TFET is desirable as it shows a steeper Gm slope in relation to p-i-n configured DLVNWTFET. Higher Gm corresponds to higher drain current at lower V_{GS} making the device energy efficient at a lower value of V_G, which is a crucial factor in analog applications using low power.

Total Gate capacitance (C_{GG}) is the addition of gate-to-source capacitance (C_{GS}) and its gate-to-drain capacitance (C_{GD}). The charges which are present in the channel region of the device, responsible for generating these capacitances. This is useful in predicting the switching speed and determines the power depletion of the TFET. C_{GS} depends on the concentration of the electrons present in the source region, while C_{GD} depends on the concentration of the electrons present in the drain region. Figure 7 shows the comparison of C_{GG} for both p-n-p-n and p-i-n TFETs. Lower C_{GG} corresponds to higher cutoff frequency (fT) as they are inversely proportional to each other (shown in equation 2). Therefore p-n-p-n configured TFET having lower C_{GG} showcases improvised performance in contrast with p-i-n TFET.

The highest frequency which can be achieved by a device is referred to as Cut-off frequency(fT). It can be calculated using the formula given below:

$$fT = gm/2\pi C_{GG} \qquad\qquad ...(2)$$

Higher fT is used in RF applications. Figure 8 shows that fT is higher for the p-n-p-n configured TFET as compared with the p-i-n configuration, due to the higher transconductance (fT is directly proportional to Gm) as shown in Figure 6.

In p-n-p-n DLVNWTFET in Figure 6 and 7, there is a surge in Gm while a contraction in C_{GG}, and this is significantly due to the inducing of N pocket, by CP technique in contrast to p-i-n DLVNWTFET. Because of this, there is an increase in the cutoff frequency p-n-p-n TFETs which can be observed from Figure 8.

Figure 9(a) depicts the output characteristics I_D–V_{DS} of both DLVNWTFETs at V_{GS}=1.0V. These results clearly help in understanding that p-n-p-n configured TFET saturates at a higher drain current at (~ 9 x 10^{-6} A/ µm) whereas drain current is about (~ 3 x 10^{-6} µm) for p-i-n).

Representation of Output conductance (G_d) is done in Fig. 9(b). Gd is extracted from I_D–V_{DS} curve (Fig. 9(a)). Gd is dependent on the operating state of the device. In the linear region, its value is high but as the V_{DS} increases, Gd starts decreasing. In the saturation region, Gd lowers down to the lowest value. The p-i-n DLVNWTFET exhibits low G_d in comparison to the proposed device.

G_d is an essential factor because the intrinsic gain of a device is dependent on it. Lower G_d and higher G_m are needed for high intrinsic gain.

Figure 10 shows the plot of the intrinsic gain as a function of gate bias at V_{DS} = 1.0 V. The values in the above plot were calculated by using the following formula:

$$Intrinsic\ gain = \frac{Gm}{Gd} \qquad\qquad ...(3)$$

From the above results, we can infer that p-n-p-n DLVNWTFET is better for analog applications, as it gives high value of gain in contrast to the p-i-n DLVNWTFET.

Table 2: Extracted DC performance parameter of DLVNWTFET and other TFETs.

Reference	Device	I_{ON} (A/µm)	I_{OFF} (A/µm)	Ion/Ioff	Threshold Voltage (mV)	G_m (S)	Cutoff Freq, fT (Hz)	Gain (dB)
This Work	DL-V-NW-TFET (p-i-n)	3.72311 x 10^{-6}	5.68951 x 10^{-20}	6.54381 x 10^{13}	0.590558	1.88 x 10^{-5}	4.0022 x 10^{10}	58.56
This Work	DL-V-NW-TFET (p-n-p-n)	8.86653 x 10^{-6}	5.88177 x 10^{-20}	1.50746 x 10^{14}	0.372621	3.29 x 10^{-5}	5.6511 x 10^{10}	96.69
Ref [9]	Silicon DLTFET	1.54 × 10^{-6}	7.29857 x 10^{-18}	2.11 × 10^{11}	0.83	~1.0 x 10^{-5}	~1.5 x 10^{7}	64.86
Ref [6]	Si-CS-DL-NT-TFET	3.92 x 10^{-8}	1.22884 x 10^{-19}	3.19 x 10^{11}	-	~1.0 x 10^{-7}	~1.5 x 10^{6}	-
Ref [12]	Si/Ge vertical NT	1.8 x 10^{-7}	-	>10^{6}	-	-	-	-

Conclusion

In this paper, p-n-p-n Doping-less Vertical Nano-wire Tunnel Field Effect Transistor has been proposed and compared with the p-i-n configuration of the same device. Charge Plasma technique has been used throughout in the formation of this device. In the p-n-p-n configuration, the N pocket has been induced without the need of separate implantation through CP technique. Upon the completion of DC and AC analysis, we can conclude that the proposed DLVNWTFET in p-n-p-n configuration offers the highest ON-State current, I_{ON}-I_{OFF} ratio, G_m, cutoff frequency and intrinsic gain amongst all the TFETS considered in Table 3. The p-n-p-n configured DLVNTFET device has reduced Vth and SS_{avg} which is the least value in comparison to all the devices considered in table. In the analog performance analysis, we have seen the p-n-p-n shows better performance in contrast to the p-i-n structure DLVNWTFET like steeper I_D-V_{GS} curve and higher I_{ON} due to better electron concentration, increased intensity of electric field and reduced bandgap near the Source-Channel interface. So, on the basis of AC and DC analysis of this device proposed in this work, we can conclude that the performance of DLVNWTFET is better than other devices we have referred.

Declarations

o **Ethics approval and consent to participate:** Not Applicable.
o **Consent for publication:** Not Applicable.
o **Availability of data and materials:** Not Applicable.
o **Competing interests:** Not Applicable.
o **Funding:** The author(s) received no financial support for the research, authorship, and/or publication of this article.

o **Authors' contributions**

Kritika Lal: Simulation, TCAD Software, Writing- Original draft preparation.

Anushka Verma: TCAD Software, Writing- Original draft preparation.

Pradeep Kumar: Revision and Supervision.

Naveen Kumar: Simulation, TCAD Software, Logical-Methodology, Data curation, conceptualization.

S. I. Amin: Revision and Supervision, Validation.

Sunny Anand: Simulation, TCAD Software, Writing and Editing, computations.

o **Acknowledgements:** Not applicable.

Compliance with Ethical Standards section

o **Disclosure of potential conflicts of interest:** No conflicts to report.

o **Research involving Human Participants and/or Animals:** Not applicable.

o **Informed consent:** Not applicable.

References

1. LEE2020 INTRO- Takayasu, S. Perspectives of low-power VLSI's. IEICE Trans. Electron. 2004, 87, 429–436. 3. Jo, J.; Shin, C. Study of Temperature Effects on Negative Capacitance Field-Effect Transistor. IEEK 2014, 37, 70–72

2. Schaller, Robert R. "Moore's law: past, present and future." IEEE spectrum 34.6 (1997): 52-59.

3. Kumar, Naveen, and Ashish Raman. "Novel design approach of extended gate-on-source based charge-plasma vertical-nanowire TFET: proposal and extensive analysis." IEEE Transactions on Nanotechnology 19 (2020): 421-428.

4. Kumar, Naveen, and Ashish Raman. "Novel Asymmetric Recessed-Gate/Source Architecture Advancement of Dual-Metal-Gate SiGe/Si Dopingless Nanowire-TFET for Low-Voltage Performance Optimization." Silicon (2020): 1-11

5. Turkane, Satish M., and A. K. Kureshi. "Review of tunnel field effect transistor (TFET)." International Journal of Applied Engineering Research 11.7 (2016): 4922-4929.

6. Kumar, Naveen, S. Intekhab Amin, and Sunny Anand. "Design and performance optimization of novel Core−Shell Dopingless GAA-nanotube TFET with Si 0.5 Ge 0.5-based source." IEEE Transactions on Electron Devices 67.3 (2020): 789-795.

7. Kumar, M. Jagadesh, and Sindhu Janardhanan. "Doping-less tunnel field effect transistor: Design and investigation." IEEE transactions on Electron Devices 60.10 (2013): 3285-3290.

8. Kumar, Naveen, and Ashish Raman. "Performance assessment of the charge-plasma-based cylindrical GAA vertical nanowire TFET with impact of interface trap charges." IEEE Transactions on Electron Devices 66.10 (2019): 4453-4460.

9. Sunny Anand, R. K. Sarin, "Analog and RF performance of doping-less tunnel FETs with Si0.55Ge0.45 source", Journal of Computational Electronics, 15 (2016): 850–856.

10. Abdi, Dawit Burusie, and Mamidala Jagadesh Kumar. "In-built N+ pocket pnpn tunnel field-effect transistor." IEEE Electron Device Letters 35.12 (2014): 1170-1172.

11. Narang, Rakhi, et al. "Device and circuit level performance comparison of tunnel FET architectures and impact of heterogeneous gate dielectric." JSTS: Journal of Semiconductor Technology and Science 13.3 (2013): 224-236.

12. Hanna, A. N., and Muhammad Mustafa Hussain. "Si/Ge hetero-structure nanotube tunnel field effect transistor." Journal of Applied Physics 117.1 (2015): 014310.
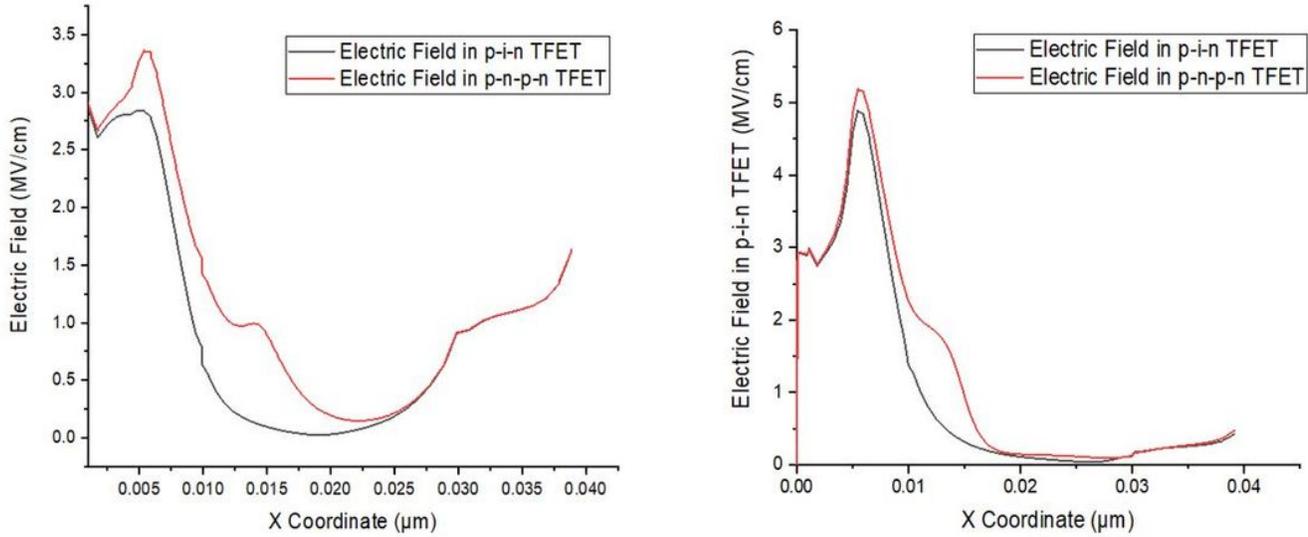
Figures
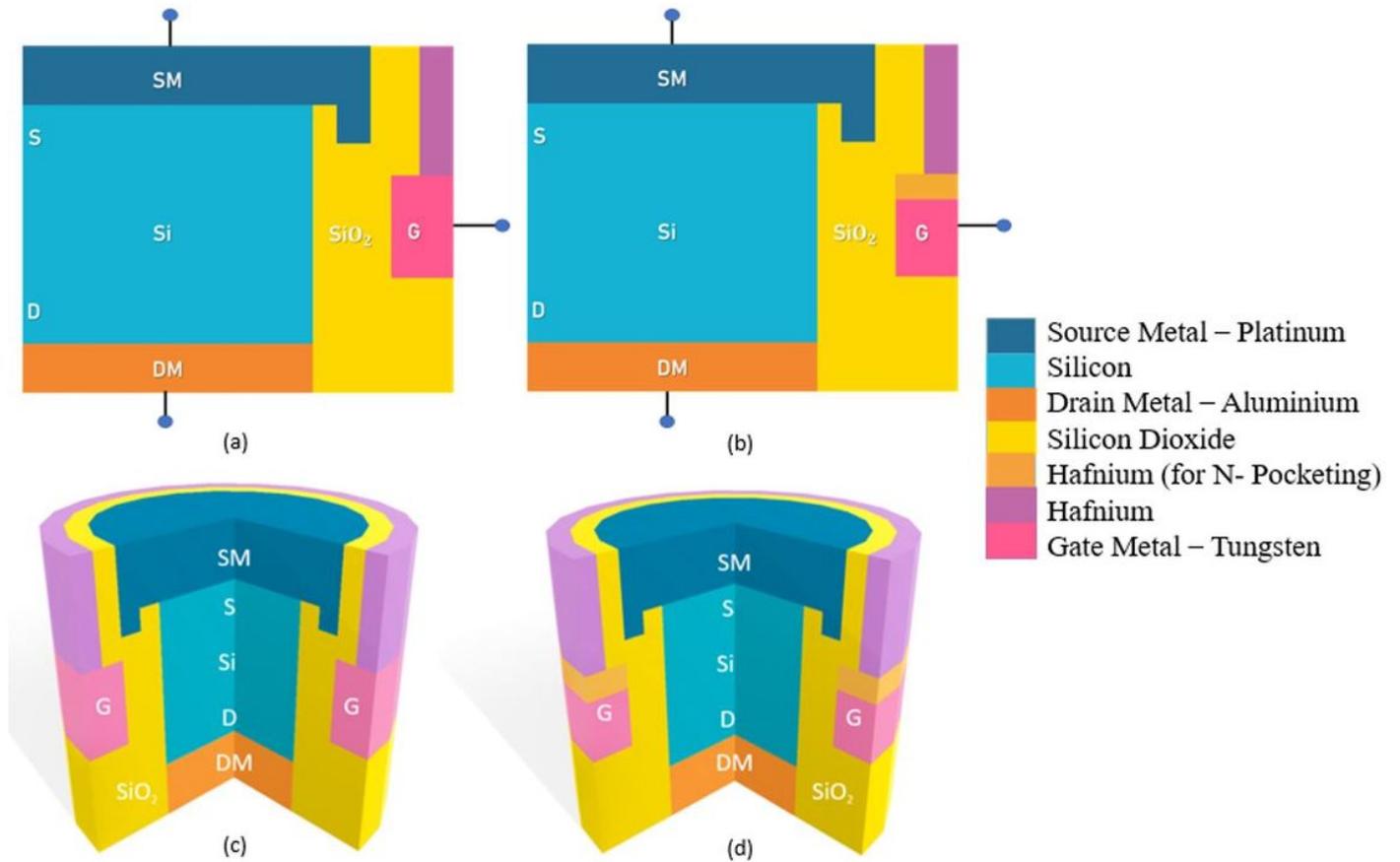
Figure 1

(a) 2D Structure of DLVNWTFET of p-i-n (b) 2D Structure of DLVNWTFET of p-n-p-n configuration, (c) 3D Structure of DLVNWTFET of p-i-n (d) 3D Structure of DLVNWTFET of p-n-p-n configuration
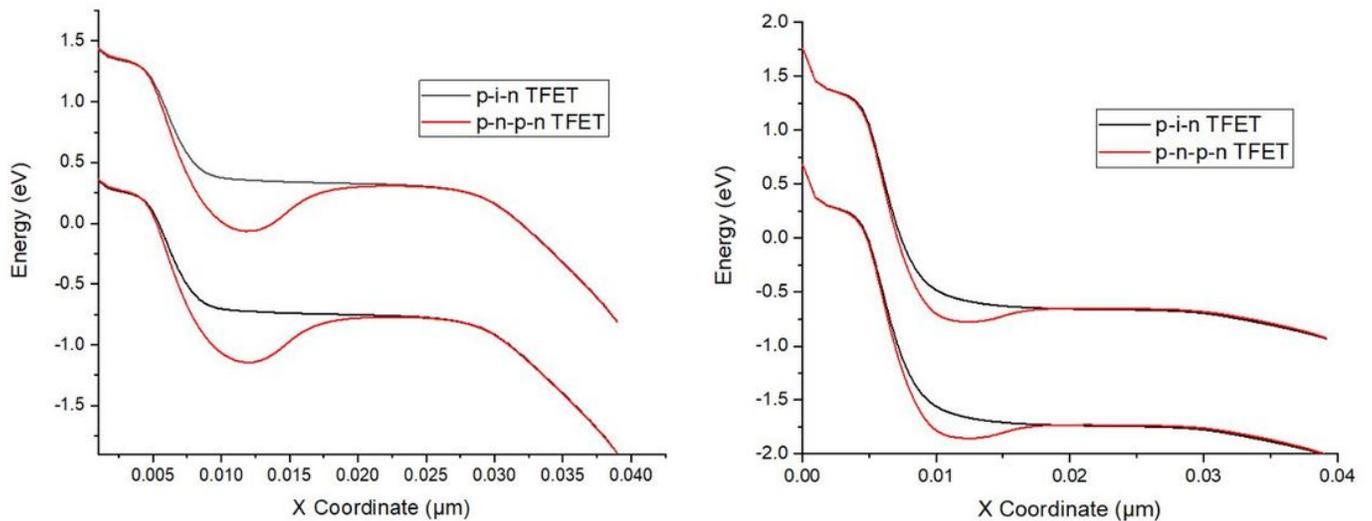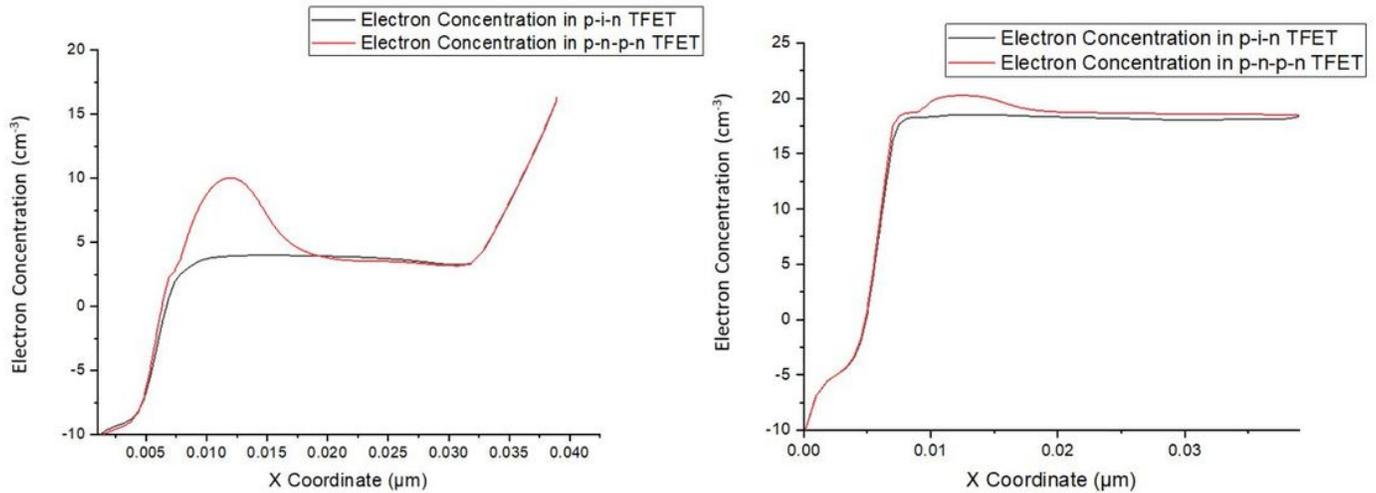

Figure 2

Energy band diagram of p-i-n TFET and p-n-p-n TFET at (a) OFF-state and (b) ON-state (cut-line from the source region to drain region)
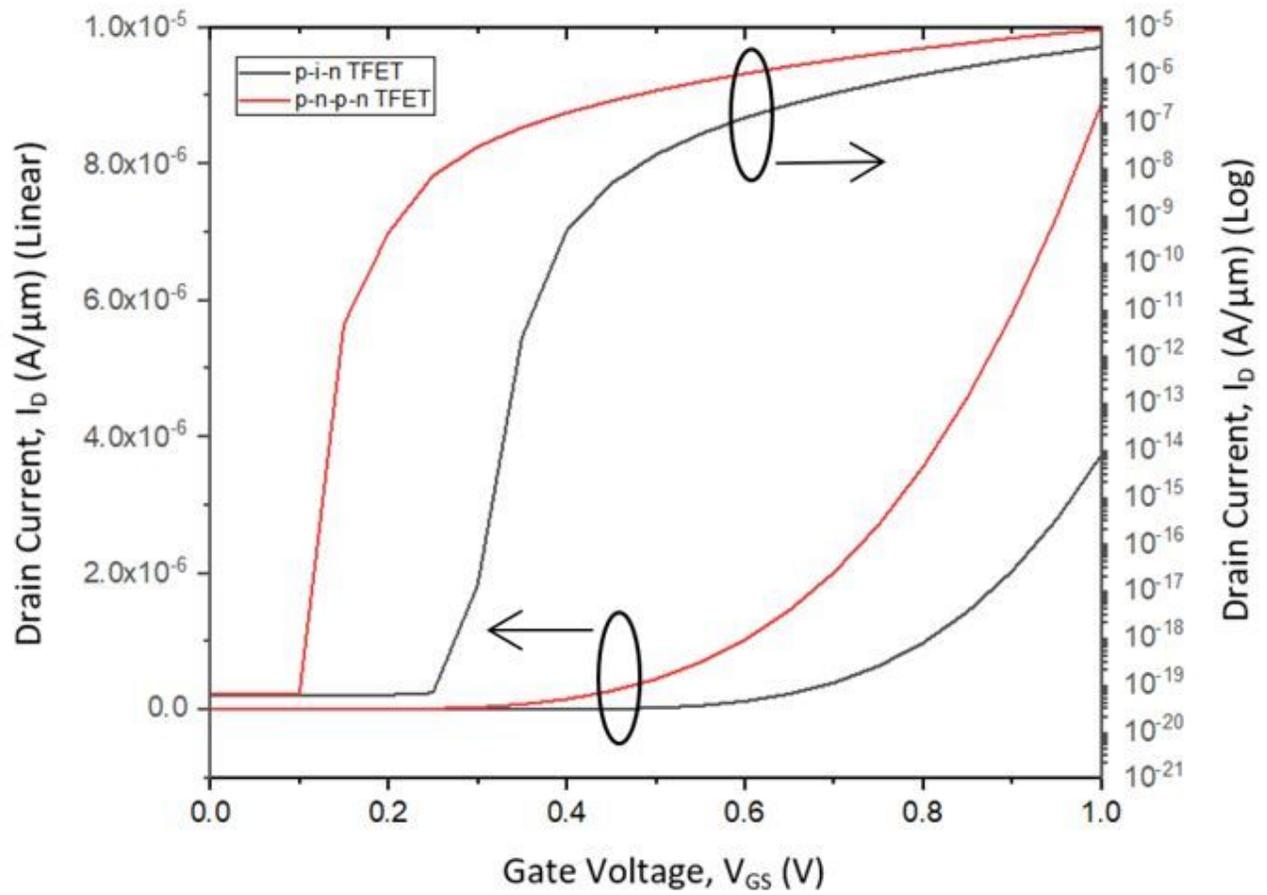

Figure 3

Electric Field of p-i-n TFET and p-n-p-n TFET at (a) at VGS=0 V and VDS=1.0 V (OFF-state) and (b) at VGS=1.5 V and VDS=1.0 V (ON-state)

Figure 4

Electron Concentration of p-i-n TFET and p-n-p-n TFET at (a) OFF state and (b) ON-state

Figure 5

Transfer characteristics curve (ID–VGS) at VDS = 1.0 V (linear scale on the left and log scale on the right y-axis) of p-i-n TFET and p-n-p-n TFET
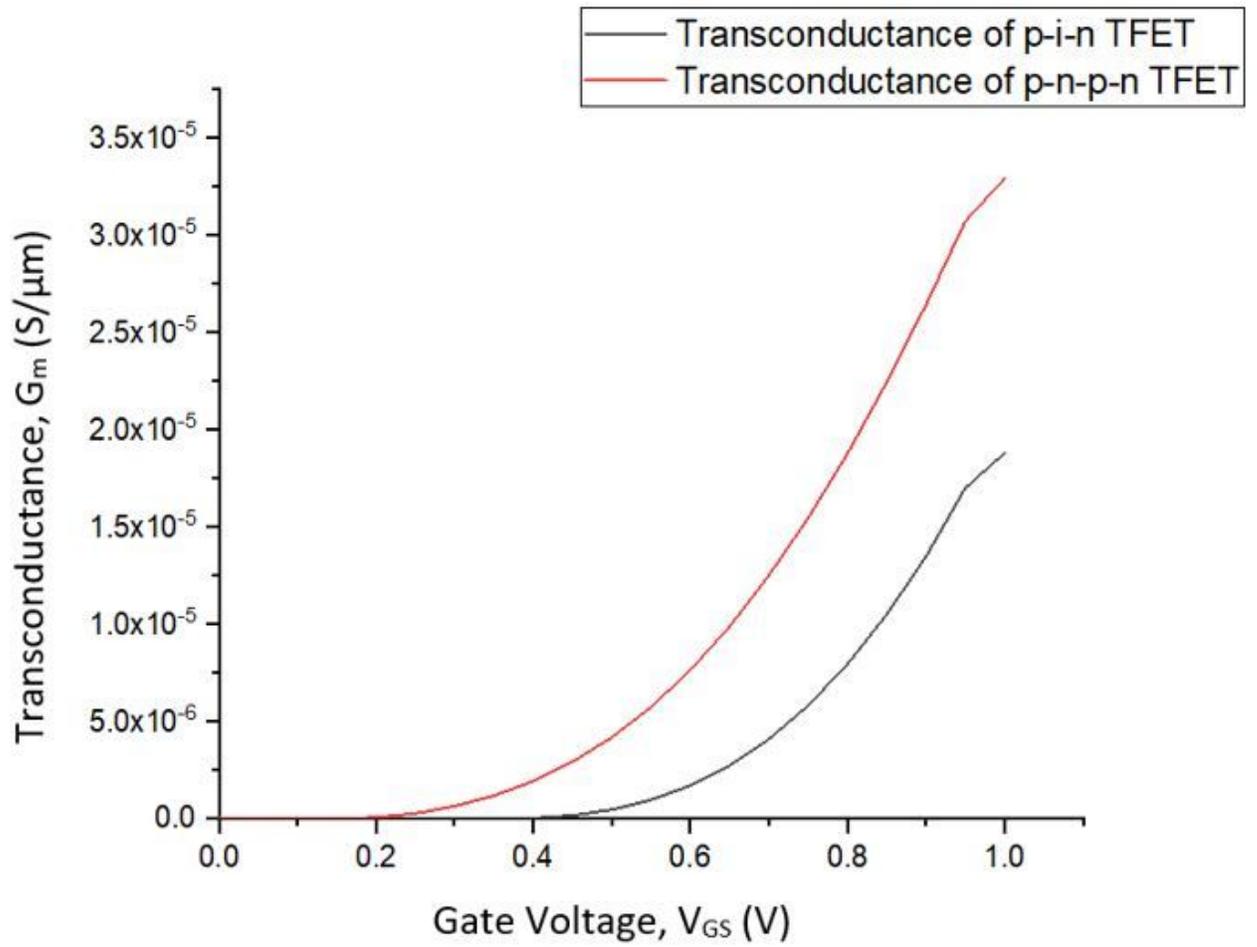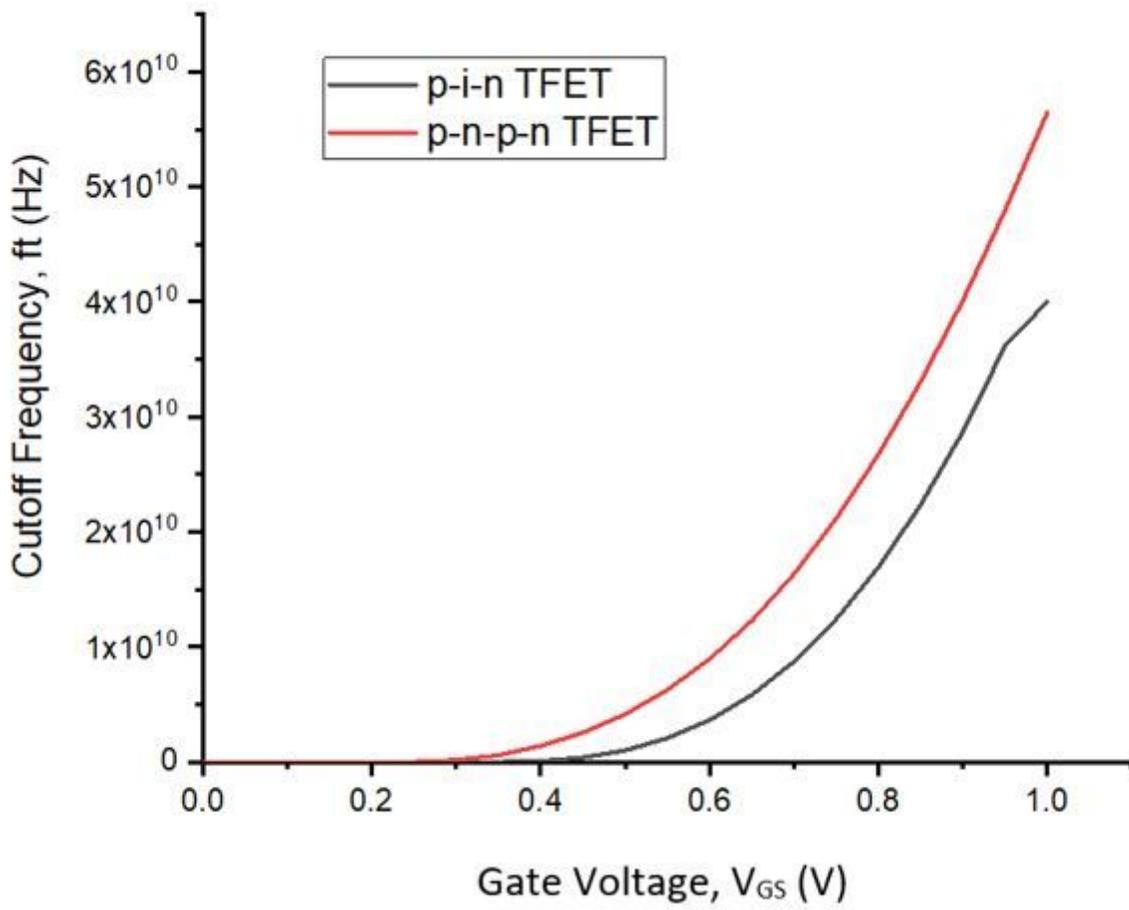
Figure 6

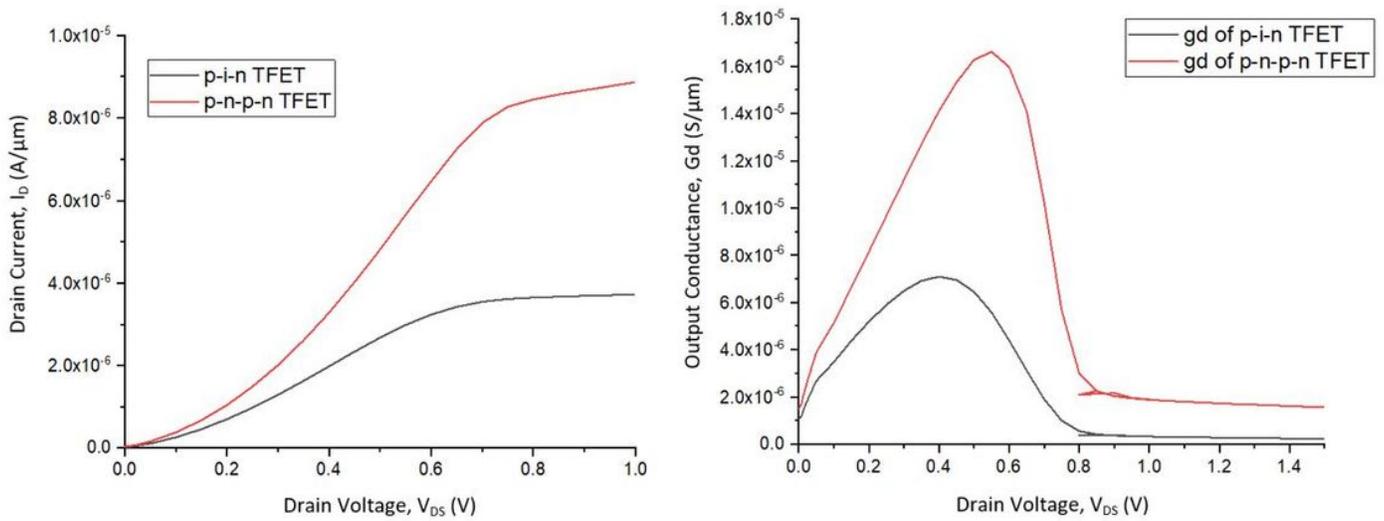Transconductance (Gm) along VGS (at VDS = 1.0V) of p-i-n TFET and p-n-p-n TFET
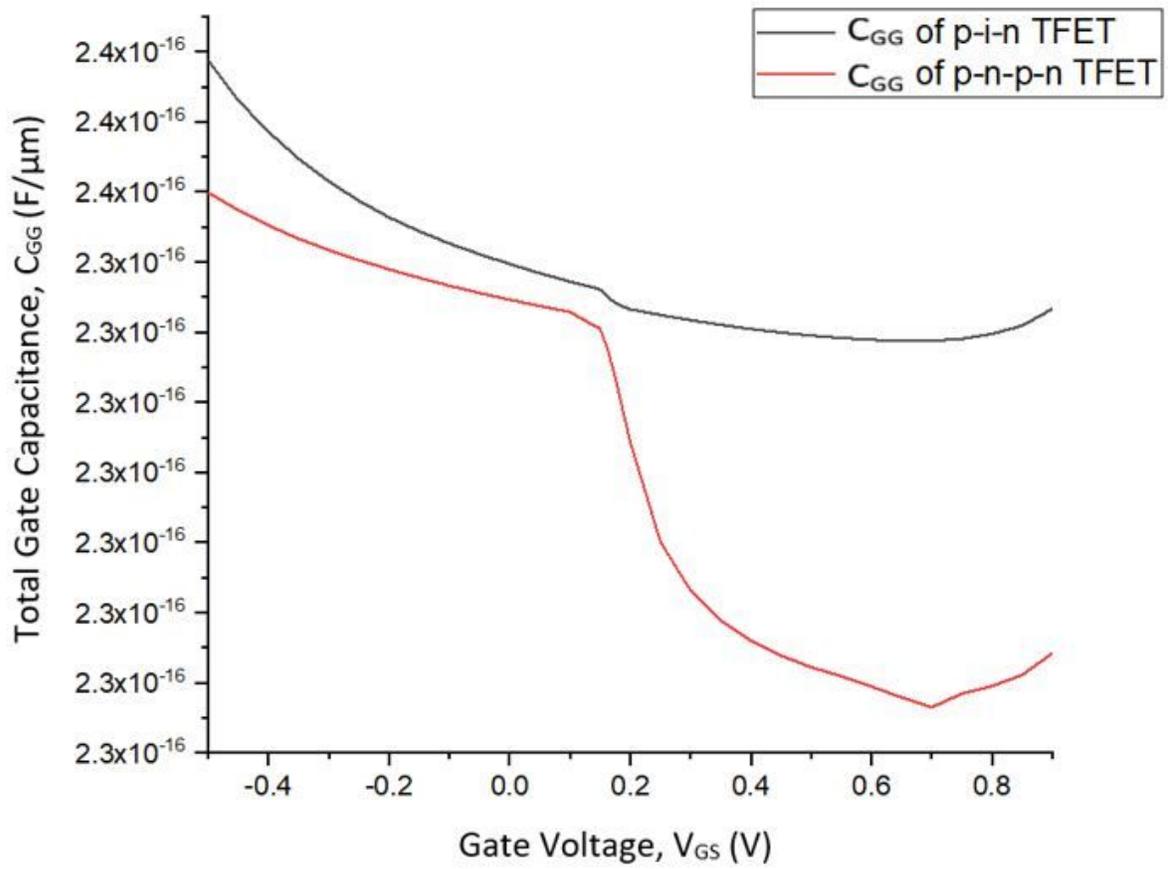
Figure 7

Total Gate Capacitance (CGG) versus VGS (at VDS=1.0 V) of p-i-n TFET and p-n-p-n TFET

Figure 8

Cut-off frequency (fT) variation along VGS (at VDS = 1.0V) of p-i-n TFET and p-n-p-n TFET

Figure 9

a) Output characteristics (ID−VDS) and (b) output conductance (Gd) versus VDS plot at different values of VGS for p-i-n TFET and p-n-p-n TFET
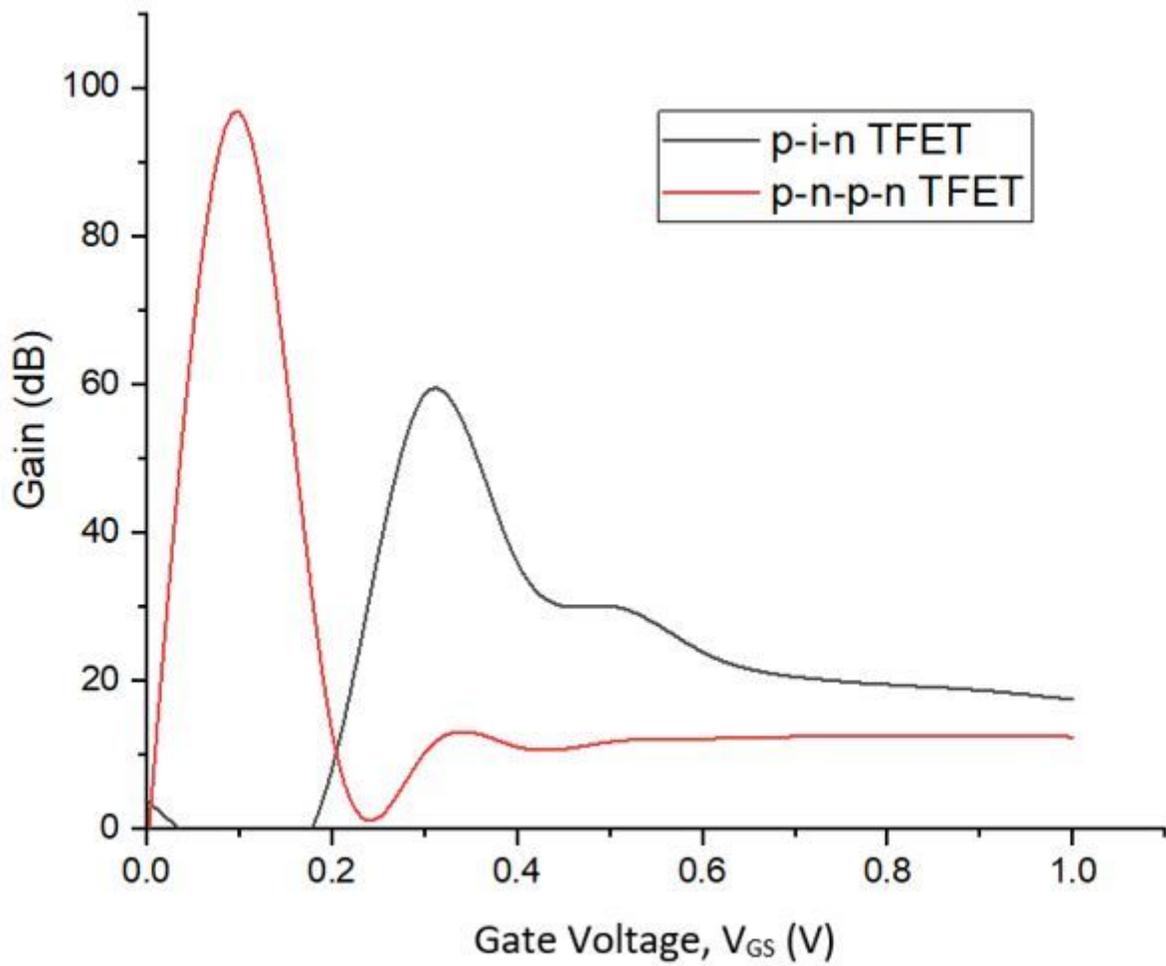
Figure 10

Intrinsic Gain of p-i-n TFET and p-n-p-n TFET at VDS = 1.0 V