A Novel LDMOS with Ultralow Specific on-Resistance and Improved Switching Performance

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Abstract

A stepped split triple-gate SOI LDMOS with P/N strip (P/N SSTG SOI LDMOS) is proposed, which has ultralow specific on-resistance ($R_{on,sp}$) and low switching losses. The proposed device has a triple-gate (TG) and stepped split gates (SSGs). P strip, N-drift and oxide trench are alternately arranged in the Z direction. Meanwhile, the SSGs are located in the oxide trench of the N-drift region and are distributed in steps. Firstly, the TG increases the channel width (W_{ch}) and has the effect of modulating current distribution, resulting in lower $R_{on,sp}$ and higher transconductance (g_m). Secondly, the SSGs serve as the field plate to assist the depletion of the N-drift region, increasing the optimal doping concentration of the N-drift region ($N_{d\text{-}opt}$) and further reducing the $R_{on,sp}$. Moreover, the SSGs also have the effect of modulating the electric field distribution to maintain a high breakdown voltage (BV). Meanwhile, gate-drain charge (Q_{GD}) and switching losses are reduced on account of the introduction of the SSGs. Thirdly, in the off-state, the P strip and SSGs multidimensional assisted depletion of the N-drift region, which greatly increases the $N_{d\text{-}opt}$. The highly doped N-drift region provides a low-resistance path for the current, which also further reduces $R_{on,sp}$. Compared with triple-gate (TG) SOI LDMOS with almost equal breakdown voltage, the $R_{on,sp}$ and Q_{GD} of P/N SSTG SOI LDMOS are reduced by 62% and 63%, respectively.

1. Introduction

Power LDMOS is extensively applied to power integrated circuits because of its advantages of low switching losses, simple driving circuit, and easy integration [1-4]. During these years, high-voltage is one of the main development directions of Power LDMOS, but due to the silicon limitation of Power LDMOS, the development of high power of power LDMOS is limited [5,6]. Therefore, it is necessary to consider a tradeoff between the BV and $R_{on,sp}$. At the same time, low losses are also one of the main development directions of power LDMOS. The static losses are only related to the $R_{on,sp}$, and the switching losses are related to the Q_{GD} [7,8]. At first, the oxide trench is introduced into the drift region to improve the contradictory relationship between $R_{on,sp}$ and BV [9-11]. With the advancement of power device technology, trench gate technology is proposed by combining oxide trench and gate [12]. The trench gate structure has greatly improved the static losses due to the formation of a low-resistance channel. However, the trench gate structure has a relatively large gate area, and the overlap area between the gate and drain is also relatively large, which makes the gate-drain capacitance (C_{GD}) or Q_{GD} larger and the dynamic losses become larger. As the switching frequency continues to increase, the switching losses rise rapidly. In the high-frequency field, dynamic losses account for the main part of the total losses. At this time, it is also particularly important to make a tradeoff between $R_{on,sp}$ and Q_{GD}. The proposed split-gate technology is to improve the contradiction between $R_{on,sp}$ and Q_{GD} [13-17]. The split-gate technology is to connect the second or third gate to the source potential to shield the C_{GD}, which can effectively reduce the C_{GD}, reduce the Q_{GD} and switching losses [18-20].

This paper proposes a P/N SSTG SOI LDMOS, which has low-on-resistance and small switching losses. The SSGs connected to the source potential are located in the oxide trench of the N-drift region and are distributed in steps. P strip, N-drift, and oxide trench are alternately arranged in the Z direction. The SSGs shield part of the overlap area between the gate and drain, so the Q_{GD} and switching losses are significantly reduced. Meanwhile, SSGs are equivalent to field plates that can modulate the electric field and maintain a high *BV*. Moreover, the TG can modulate the current distribution, and the P strip and SSGs multidimensionally assist in depleting the N-drift region to make the $N_{d\text{-}opt}$ relatively high, both of which effectively reduce $R_{on,sp}$. The proposed device achieves low-on-resistance and low switching losses without sacrificing much *BV*, and optimizes the tradeoff relationship between $R_{on,sp}$ and Q_{GD}.

2. Structure And Work Mechanism

Figure (Fig.) 1 presents the 3-D structure of P/N SSTG SOI LDMOS, which features a TG and SSGs. The TG is composed of two planar gates and a trench gate. The SSGs connected to the source potential are located in the oxide trench in the N-drift region and are distributed in steps. And the proposed device has a super-junction structure. The N-drift region is close to the oxide trench, and the P strip is connected to the N-drift region. Therefore, the P strip, the N-drift, and the oxide trench are arranged alternately in the Z direction. In this paper, the simulator Sentaurus is used to study the physical characteristics of P/N SSTG SOI LDMOS. And in Fig. 1 and Table 1, the coordinate system and key parameters used in the simulation of P/N SSTG SOI LDMOS are given.

Table 1: Key parameters in the simulation

Symbol	Parameter	Value
W_p	Width of the P strip	0.4μm
W	Width of oxide trench	0.5μm
W_n	Width of the N-drift region	0.6μm
L_s	Starting position of the split gate	Optimized
L_d	Length of the drift region	4μm
T_b	Thickness of the buried oxide layer	1μm
T_{si}	Thickness of the epitaxial layer	2.5μm
T_1	Gate oxide thickness of the first SSG	Optimized
T_2	Gate oxide thickness of the second SSG	Optimized
N_d	Doping concentration of the N-drift region	Optimized
N_p	Doping concentration of the P strip	Optimized
N_{sub}	Doping concentration of the P-Substrate	$1\times10^{14}cm^{-3}$

Fig. 2 illustrates the mechanism diagram of P/N SSTG SOI LDMOS. In the on-state, the inversion layer is not only formed under the planar gate but also formed on the sidewall of the trench gate, so the TG expands the W_{ch} to obtain a low channel resistance and improve transconductance, as shown in Fig. 2(a). Fig. 2(b) and Fig. 2(c) show that SSGs act as filed plates and assist in depleting the N-drift region in the off-state. Meanwhile, P strip also assists in depleting the N-drift region in the off-state. Therefore, the multidimensional assisted depletion effect can increase the optimal N_d, which reduces the resistance of the N-drift region. Both help to significantly reduce $R_{on,sp}$ and static losses, so the N-drift region acquires a large current density in the on-state. In addition, SSGs connected to the source potential are equivalent to field plates, which has the effect of modulating the electric field and obtains high *BV*.

Fig. 3 shows the mechanism diagram of the P/N SSTG SOI LDMOS along the cutting line CC'. Fig. 3(a) demonstrates that the ionized positive charge of the N-drift region will be shared by the negative charge of the P-well, P strip, and SSGs. Therefore, the SSGs and P strip multidimensionally assist depletion effect on the N-drift region, increasing the optimal N_d and further decreasing the $R_{on,sp}$. In addition, the SSGs connected to the source potential serve as field plates and have the effect of adjusting the electric field distribution. Fig. 3(b) shows the shielding effect of SSGs. The SSGs act as a shielding layer between the gate and drain, and convert part of the C_{GD} into C_{GS} and C_{DS}, degrading gate-drain overlap and gate-drain charge. Thereby reducing switching losses.

3. Simulation Results And Discussion

Fig. 4 and Fig. 5 show the current density distribution of P/N SSTG SOI LDMOS, conventional (Con.) SOI LDMOS and triple-gate (TG) SOI LDMOS in the on-state. Firstly, comparing Fig. 4(b) and Fig. 4(c), the black dotted rectangle in Fig. 4(a) can clearly see that the current density is relatively large, and the current density is 3775-7329 A/cm^2. This is because the P/N SSTG SOI LDMOS introduces vertical channel and has high $N_{d\text{-}opt}$. Secondly, the introduction of P strip and SSGs can assist in depleting the N-drift region, making the $N_{d\text{-}opt}$ higher. Therefore, from the Fig. 4 (a), we can know that the Y-direction current density range of P/N SSTG SOI LDMOS is 5518-7329 A/cm^2. As shown in Fig. 4(b), the surface current density of Con. SOI LDMOS is 990 A/cm^2, and the current density at the bottom of the drift region is 355-538 A/cm^2. So, owing to the lack of vertical channel for Con. SOI LDMOS, the current mainly flows along the surface and decreases sharply at the bottom of the drift region. For TG SOI LDMOS, it has vertical channel but no multidimensional assisted depletion effect of P strip and SSGs. Therefore, the total current density of the N-drift region is in the range of 538-990 A/cm^2, which is much smaller than that of the P/N SSTG SOI LDMOS, as shown in Fig. 4 (c). P/N SSTG SOI LDMOS, TG SOI LDMOS and Con. SOI LDMOS have almost the same current density at Z=0.5μm and Z=0.8μm, respectively, as shown in Fig. 5. Moreover, the $R_{on,sp}$ and the $N_{d\text{-}opt}$ of the three devices are respectively marked in Fig. 4(a)-(c).

Fig. 6 shows the transfer characteristics and output characteristics of the three devices. The inset in Fig. 6 (a) is the electron density distribution diagram of Con. SOI LDMOS and SOI LDMOS with TG structure in the on-state. It can be clearly seen that compared with Con. SOI LDMOS, the channel width (W_{ch}) of P/N SSTG SOI LDMOS and TG SOI LDMOS is increased from 1.5 μm to 2.5 μm. In addition, the multidimensional assistant depletion effect increases the $N_{d\text{-}opt}$ value, expanding the channel width modulates the current distribution. Consequently, P/N SSTG SOI LDMOS has better transfer characteristics than the other two devices. Under the same gate-source voltage (V_{GS}), the drain current of P/N SSTG SOI LDMOS is much larger than that of TG SOI LDMOS and Con. SOI LDMOS. Meanwhile, the g_m of P/N SSTG SOI LDMOS is slightly larger than that of the Con. SOI LDMOS, and has excellent gate control capability. Fig. 6(b) illustrates the output characteristics of the three devices. It is not difficult to see that the output current of P/N SSTG SOI LDMOS is larger than that of the other two devices. The output characteristic at V_{DS}=0.5V, is shown in the inset figure of Fig. 6(b). The output current of TG SOI LDMOS is higher than that of Con. SOI LDMOS, which owing to the formation of a low resistance channel on the side of the trench gate close to the drift region, and decreases the $R_{on,sp}$ from 1.37 mΩ·cm^2 to 0.74 mΩ·cm^2. And the SSGs and P strip of the P/N SSTG SOI LDMOS help to assist in depletion of the N-drift region, thereby further reducing $R_{on,\,sp}$ to only 0.28 mΩ·cm^2.

Fig. 7 shows the distribution of the surface electric field and the equipotential lines for the three devices in the breakdown state. The insets present the equipotential lines distribution diagrams of the three devices at their $N_{d\text{-}opt}$ in breakdown state. The $N_{d\text{-}opt}$ of P/N SSTG SOI LDMOS is significantly higher than that of the other two devices, which is due to SSGs and P strip can assist the depletion of the N-drift region,

resulting in a significant increase in the charge capacity of the N-drift region. Moreover, it can be clearly seen that the equipotential lines of P/N SSTG SOI LDMOS at SSGs are relatively dense. Meanwhile, the SSGs are equivalent to field plates with a modulating electric field effect, and the electric field distribution of P/N SSTG SOI LDMOS is more uniform, which effectively prevents premature breakdown. For Con. SOI LDMOS and TG SOI LDMOS, the *BV* is the same. Consequently, P/N SSTG SOI LDMOS acquires the *BV* of 105V. the *BV* of TG SOI LDMOS and Con. LDMOS are both 110 V.

Fig. 8 illustrates the trend of *BV* and $R_{on,sp}$ with N_d for the three devices. Owing to the introduction of p strip and SSGs lead to high $N_{d\text{-}opt}$, and there are multiple conductive channels in the TG, which reduces the $R_{on,sp}$ of P/N SSTG SOI LDMOS by 80 % and 62 % compared with that of Con. SOI LDMOS and TG SOI LDMOS, respectively. Moreover, Super-junction structures are very sensitive to the change of doping concentration and are greatly affected by charge imbalance, which can significantly affect *BV.* Therefore, the *BV* of P/N SSTG SOI LDMOS is slightly smaller than that of Con. SOI LDMOS and TG SOI LDMOS. Besides, The $R_{on,sp}$ of P/N SSTG SOI LDMOS is weakly depended on N_d because of the extremely large N_d.

Fig. 9 reveals that the influence of P/N strip concentration on the performance of the proposed device. The N_d represents the doping concentration of the N-drift region, and N_p is the doping concentration of the P strip. Owing to the proposed device contains a super-junction structure, the *BV* is more sensitive to the concentration. Therefore, the change of the N_d and N_p greatly affects the *BV*. It can be clearly seen that when N_d is different, the *BV* and $R_{on,sp}$ of P/N SSTG SOI LDMOS have the optimal values. Each optimized *BV* and $R_{on,sp}$ in the figure has a suitable N_p. Besides, as N_d increases, the $R_{on,sp}$ becomes smaller. Consequently, when the *BV* of P/N SSTG SOI LDMOS is 105V and the $R_{on,sp}$ is 0.28mΩ·cm^2, it has the best performance.

Fig. 10 shows the effects of the *BV* and $R_{on,sp}$ on N_d as a function of T_1 (or T_2) for the P/N SSTG SOI LDMOS. When T_1≤0.2μm, the ability of SSGs to assist the depletion of the N-drift region is weakened, so the N-drift region is not completely depleted and the *BV* begins to decrease. Meanwhile, when T_1 (or T_2) is very small (e.g. T_1 (or T_2)=0.1μm), premature breakdown occurs at the end of SSGs. Therefore, P/N SSTG SOI LDMOS has the best performance when T_1=0.2μm, as shown in Fig. 10(a). As shown in Fig. 10(b), because SSGs modulate the electric field distribution, the P/N SSTG SOI LDMOS has the largest *BV* at T_2=0.4μm. Meanwhile, SSG has little effect on $R_{on,sp}$ at different T_2 in the on-state, because N_d is large enough.

Fig. 11 presents the Q_{GD} of P/N SSTG SOI LDMOS, TG SOI LDMOS, and Con. SOI LDMOS. The right inset shows the charge simulation circuit [19-21]. Owing to the SSGs shield part of the overlap area between the gate and drain, Q_{GD} is reduced [18,19]. Therefore, the Q_{GD} of the P/N SSTG SOI LDMOS is significantly degraded, and the switching rate is increased. The Q_{GD} of TG SOI LDMOS is the maximum because the trench gate is used to maximize the overlap between the gate and drain. The Q_{GD} of the P/N SSTG SOI

LDMOS is reduced by 63% compared with that of TG SOI LDMOS. However, owing to the lack of TG, the Con. SOI LDMOS shows the lowest Q_{GD}, but $R_{on,sp}$ is large enough. Consequently, the FOM2 (FOM2=$R_{on,sp}$*Q_{GD}) of TG SOI LDMOS is the maximum value, which is 7 times that of P/N SSTG SOI LDMOS (as shown in Table 2). This means that TG SOI LDMOS has the largest switching losses.

Table 2: Comparison of FOM of four LDMOSFETs

LDMOSFETs	FOM1 = $BV^2/R_{on,sp}$ ($MW\cdot cm^{-2}$)	FOM2 = Q_{GD}*$R_{on,sp}$ ($nC\cdot m\Omega$)
Con. SOI LDMOS	8.83	116.5
TG SOI LDMOS	16.4	218.3
P/N ETG SOI LDMOS	40.5	50.65
P/N SSTG SOI LDMOS	**39.4**	**30.8**

Fig. 12 compares the dynamic performance of the P/N SSTG SOI LDMOS and TG SOI LDMOS. The inset shows the switching circuit used in the simulation [22,23]. It can be seen from the figure that P/N SSTG SOI LDMOS has a faster turn-off speed. Fig. 13 illustrates the effect of L_s on $R_{on,\,sp}$, Q_{GD}, and FOM2. The insets show the P/N SSTG SOI LDMOS with different L_s. L_s represents the position where the gate starts to split on the X coordinate. For P/N SSTG SOI LDMOS, with the increase of L_s, $R_{on,sp}$ decreases, and Q_{GD} increases, which is because the area of the electron accumulation layer of the TG increases, while the shielding effect of SSGs decreases. As shown in Fig. 13, P/N SSTG SOI LDMOS achieves the best tradeoff between $R_{on,sp}$ and Q_{GD} when L_s=1.7μm, and obtains the lowest FOM2 (FOM2=$R_{on,sp}$*Q_{GD}), so the switching losses are the lowest.

The key feasible fabrication processes of P/N SSTG SOI LDMOS are shown in Fig. 14. (a) Phosphorus ion implantation to form an N-type drift region. (b) Boron ions are implanted to form a P-well, and then etched to determine the region of the oxide trench and perform thermal oxidation. Thermal oxidation is helpful to obtain high-quality interface. (c) The oxide is deposited and Chemical Mechanical Planarization (CMP) is carried out to form an oxide trench. (d) Etching and determining the SSGs region. (e) Polysilicon is deposited. (f) Etching and determining the trench gate. (g) Thermal oxidation forms the gate oxide of the planar gate and the trench gate. (h) Polysilicon is deposited and electrodes are formed. And ion implantation to form N+, P+.

4. Conclusion

A P/N SSTG SOI LDMOS is put forward to ameliorate the static state and switching losses. Without sacrificing much *BV*, compared with Con. SOI LDMOS and TG SOI LDMOS, the $R_{on,sp}$ of P/N SSTG SOI

LDMOS is reduced by 80% and 62%, respectively, which significantly reduces conduction losses and improves the static losses. At the same time, compared with TG SOI LDMOS, the Q_{GD} of P/N SSTG SOI LDMOS is reduced by 63%, and the switching losses are significantly reduced. So the proposed device achieves an excellent tradeoff between $R_{on,sp}$ and Q_{GD}. Besides, the proposed device is generally applied to medium and low rated voltages, substantially reducing power losses.

Declarations

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Contributions:

All the works (Methodology, Writing Original Draft, Software, Validation and Investigation, Formal analysis, Resources, Data Curation,Writing Review and Editing) in this paper have done together by Lijuan Wu, Haifeng Wu, Jinsheng Zeng, Xing Chen and Shaolian Su.

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We have no ethical conflict. All authors give their consent to participate in this manuscript.

Consent for Publication:

Consent was obtained from all the authors for the publication of this manuscript.

Conflicts of Interest/Competing Interests:

The authors declare that there is no conflict of interest reported in this paper.

Research Involving Human Participants and/or Animals:

Not applicable.

Informed Consent:

Not applicable.

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Figures

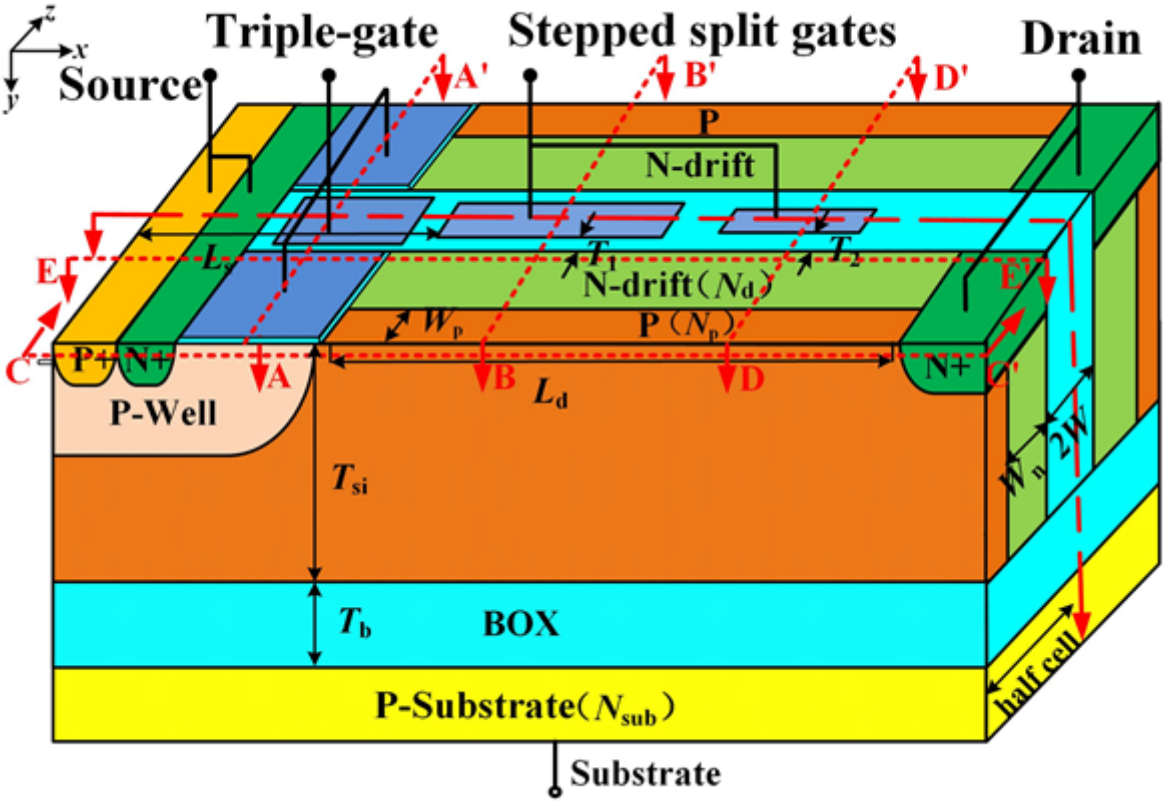

Figure 1

Three dimensions structure of the P/N SSTG SOI LDMOS.

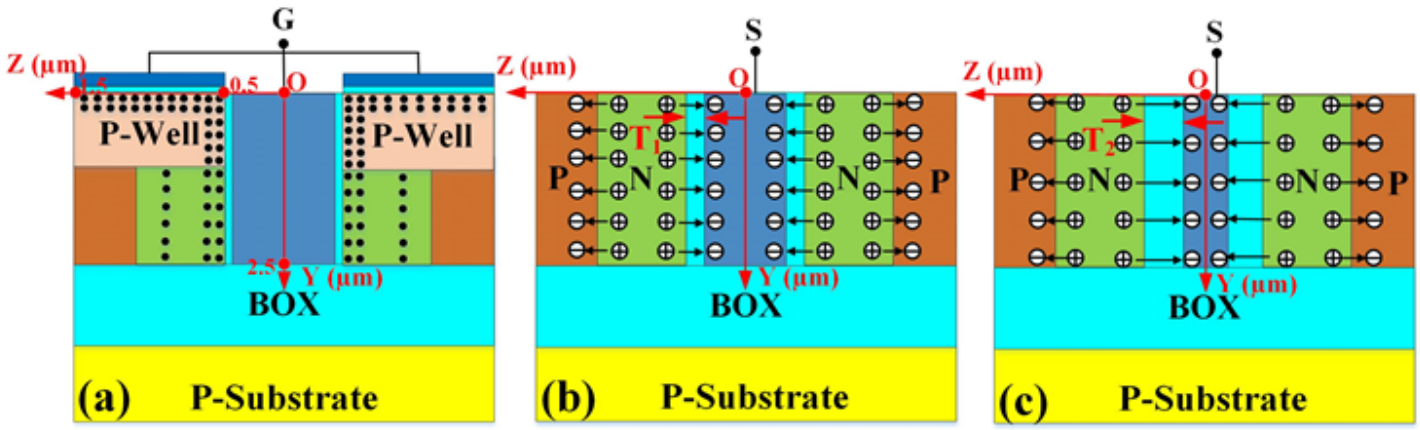

Figure 2

Mechanism diagram of P/N SSTG SOI LDMOS. (a) Distribution of electrons at the channel in the on-state: along the cut line AA'. SSGs have assistant depletion effect in the off-state (b) along the cut line BB' and (c) along the cut line DD'.

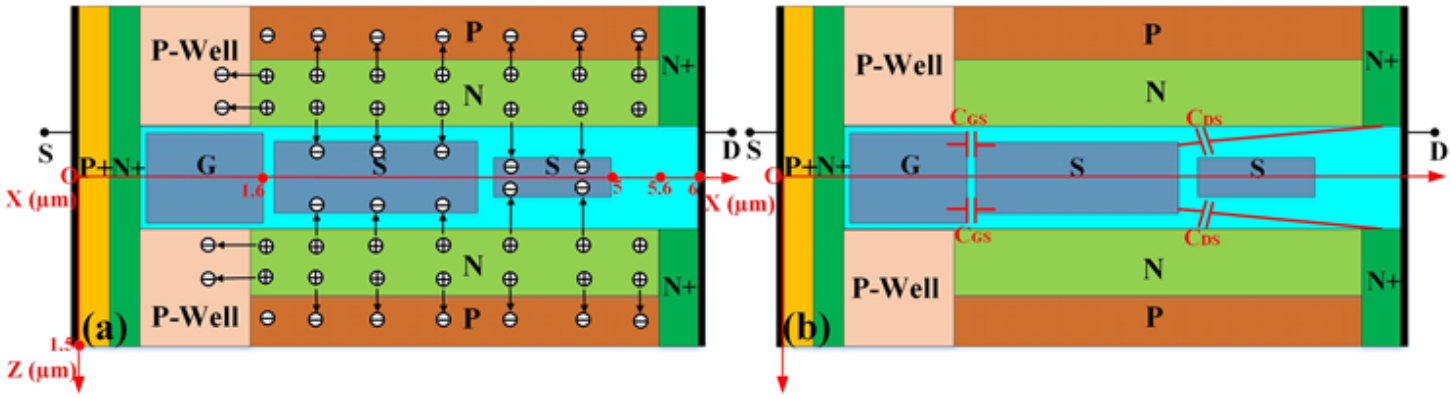

Figure 3

Mechanism diagram of P/N SSTG SOI LDMOS along the cut line CC'. (a) Assistant depletion effect in the off-state. (b) Shielding effect of the SSGs.

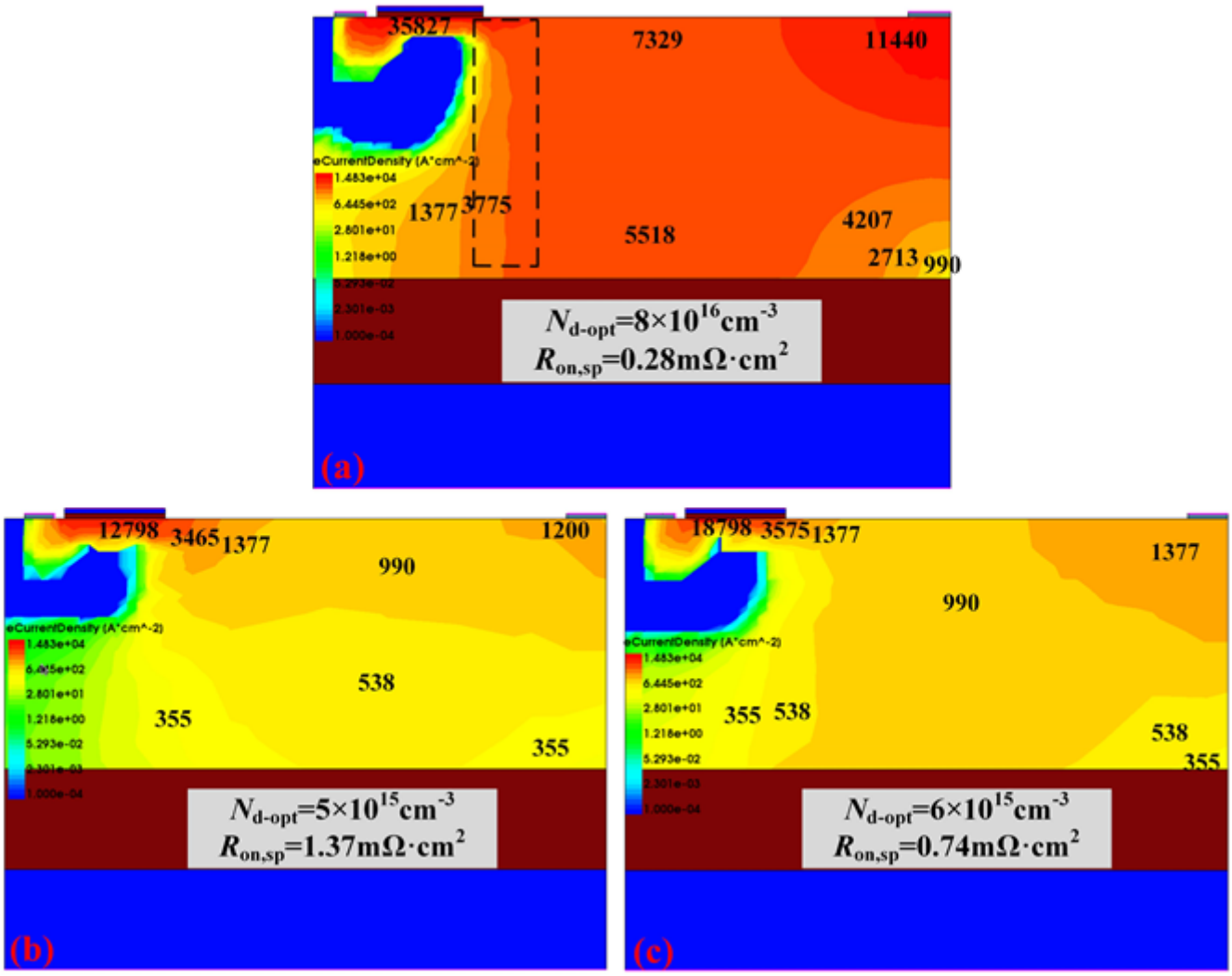

Figure 4

Current density distributions along the cut line EE'. (a) P/N SSTG SOI LDMOS. (b) Con. SOI LDMOS. (c) TG SOI LDMOS.

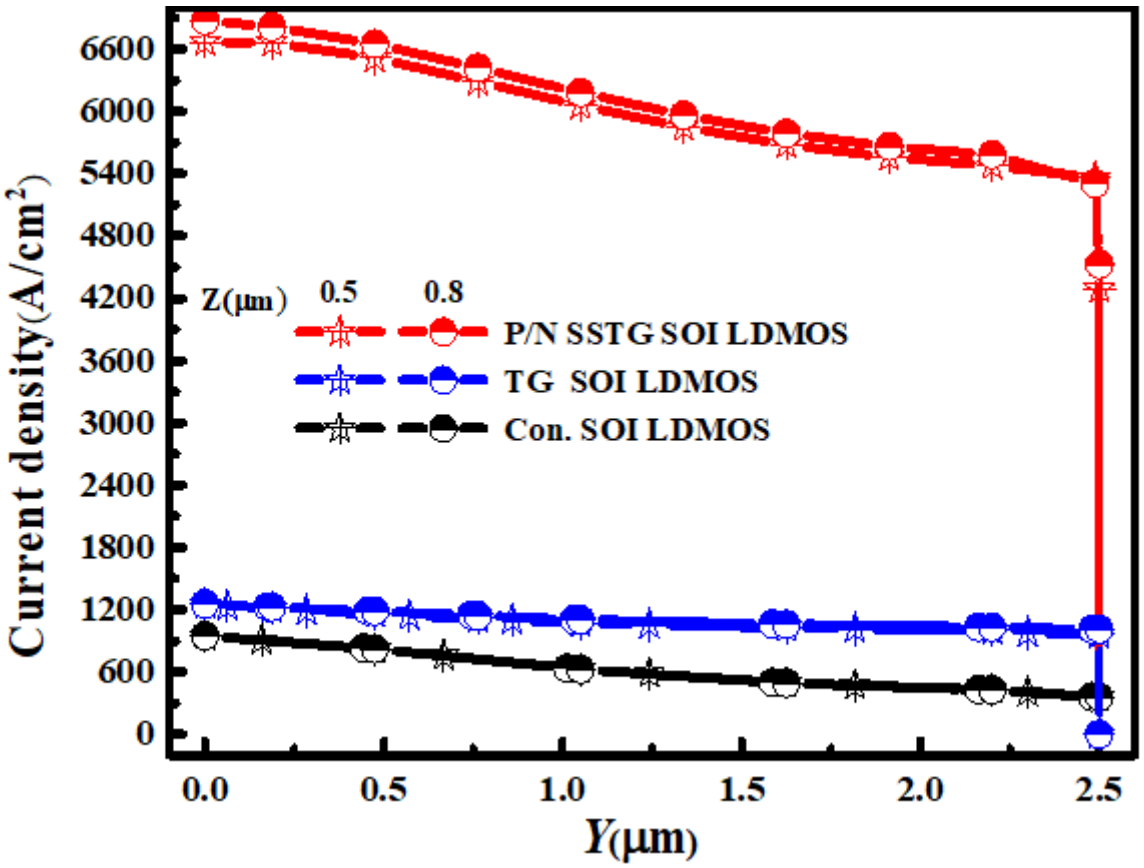

Figure 5

Current density distributions in the Y-direction. (X=3μm).

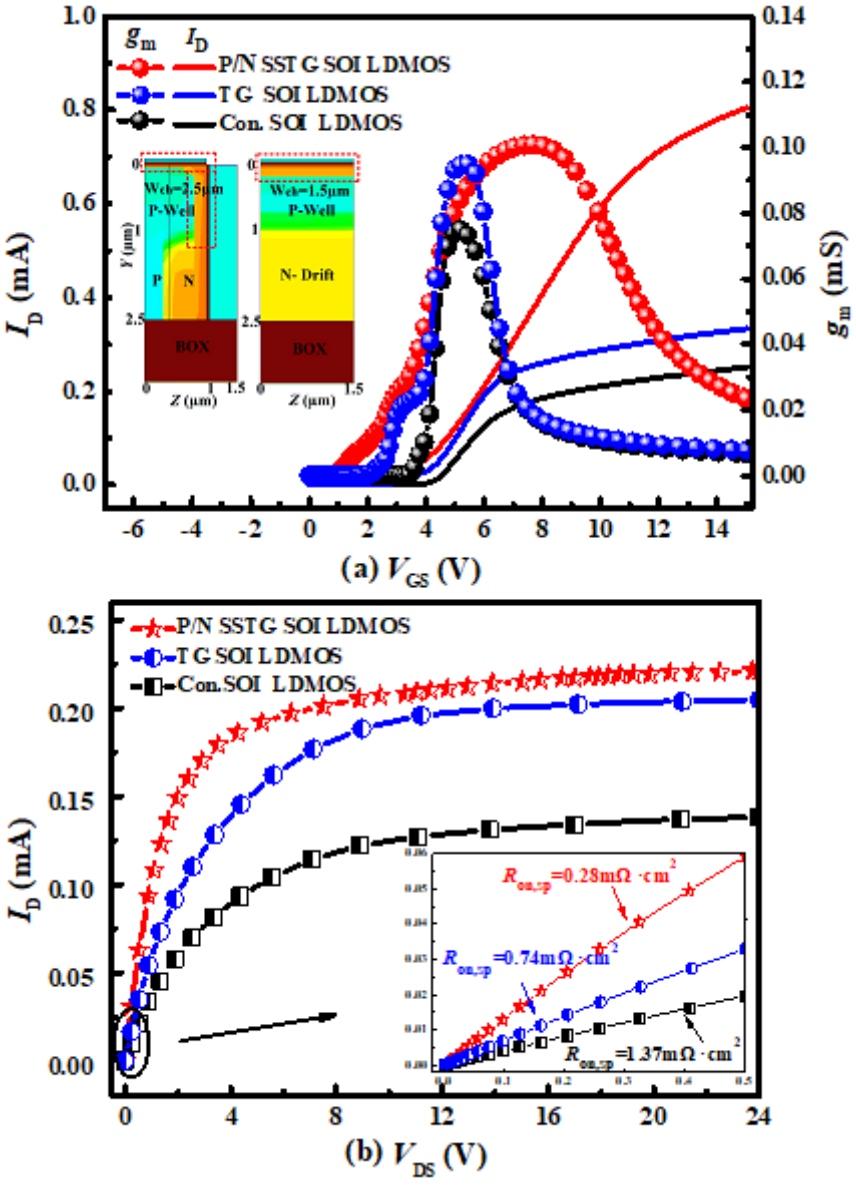

Figure 6

Transfer characteristics and output characteristics for three devices. (a) Transfer characteristics. (b) Output characteristics.

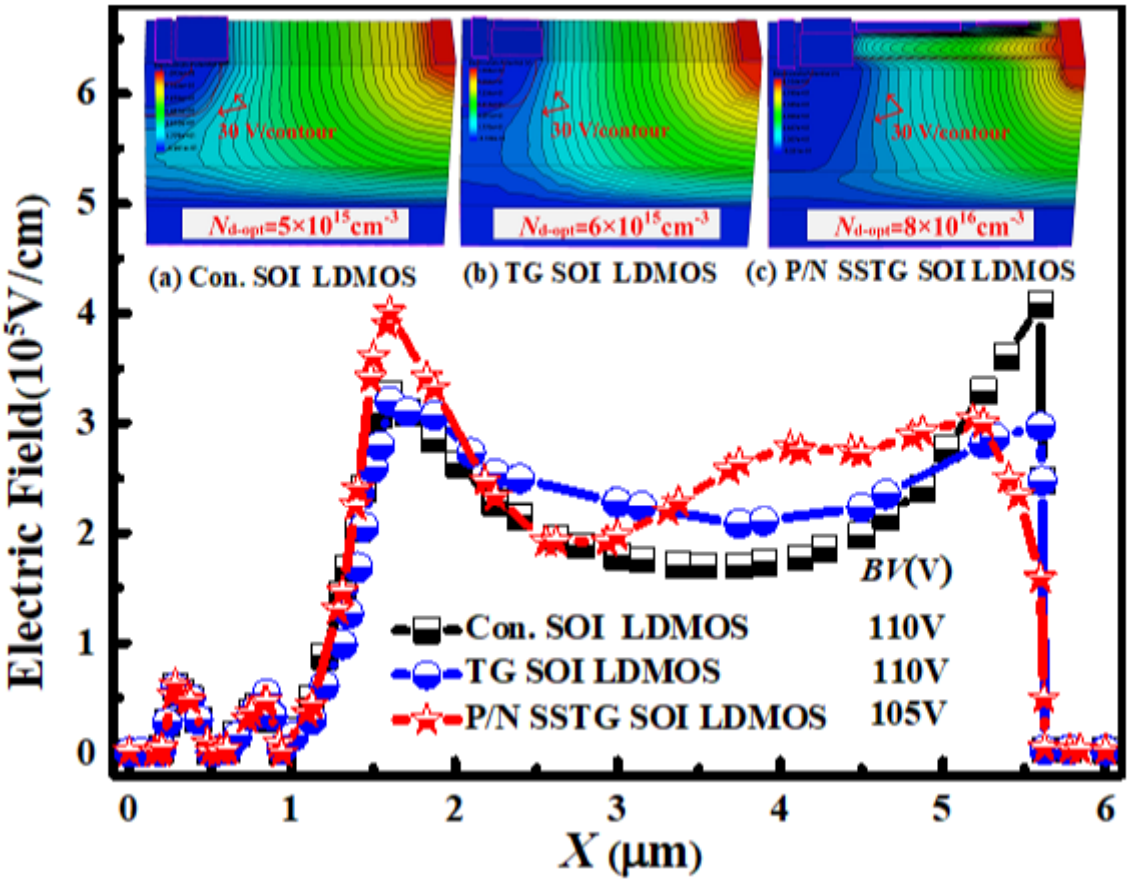

Figure 7

Equipotential lines distribution and surface electric field distribution (Y=0.01μm, Z=0.6μm) for the three devices in breakdown state.

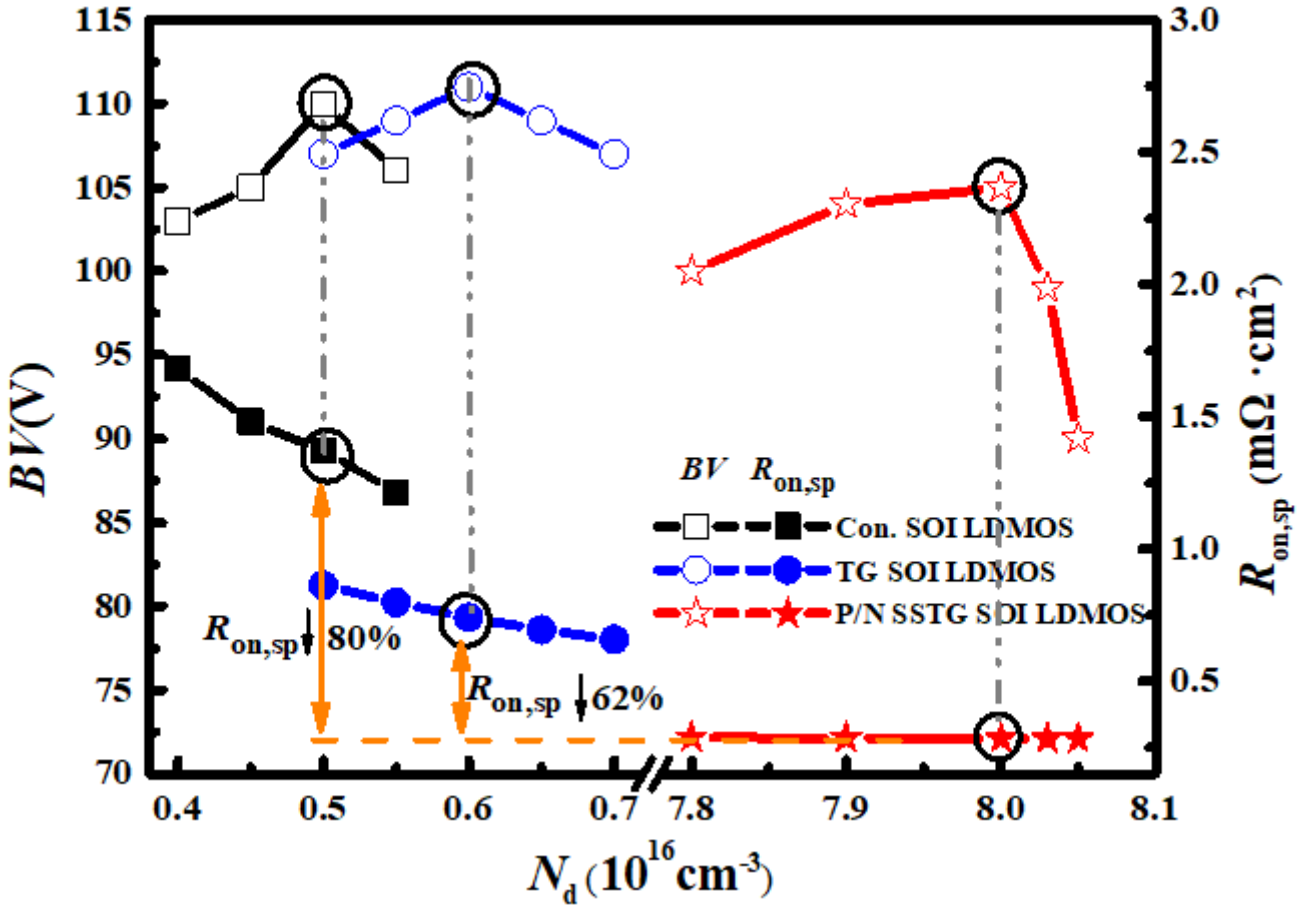

Figure 8

Trend of BV and Ron,sp with Nd for the three devices.

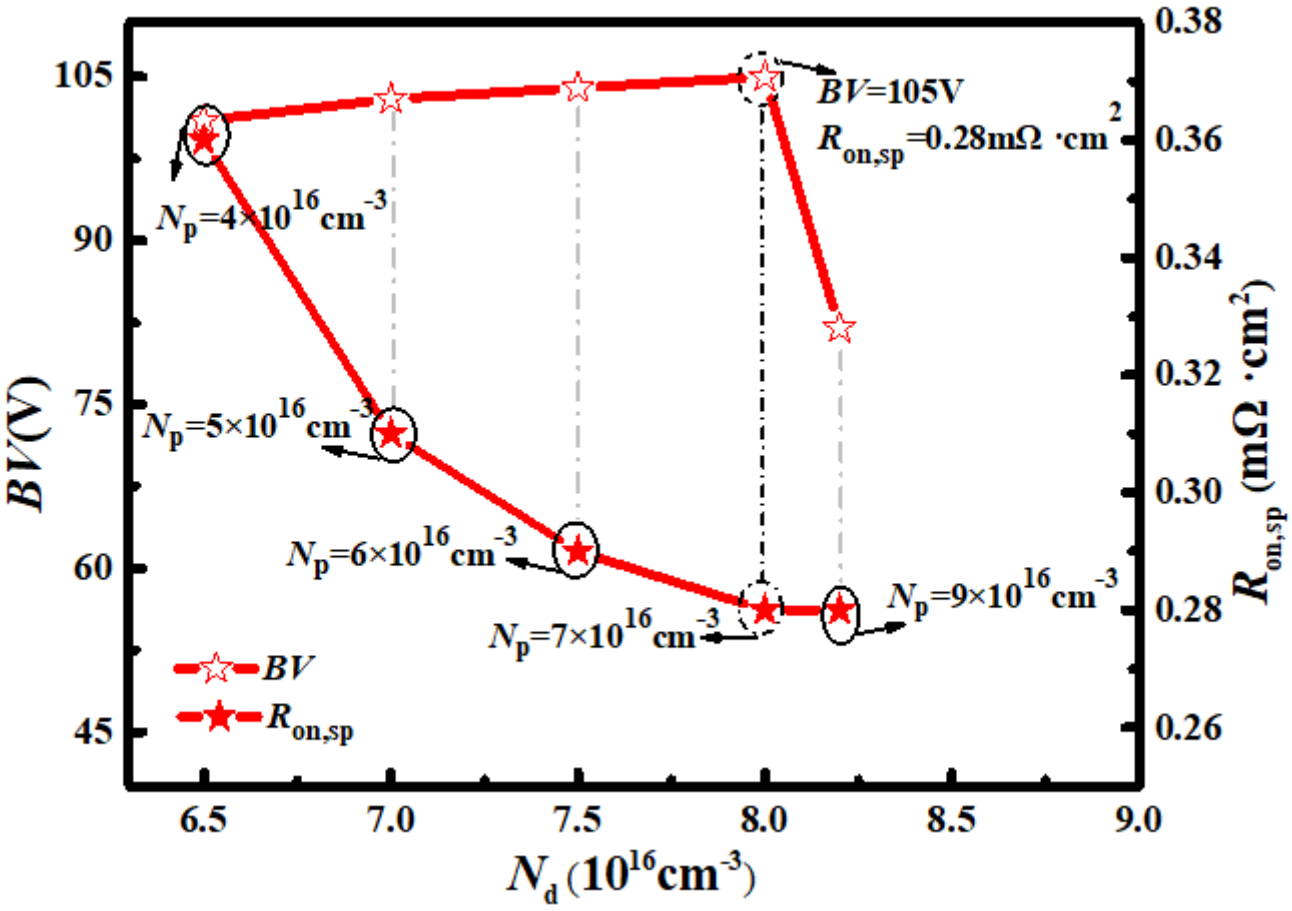

Figure 9

Effect of P/N strip concentration on performance.

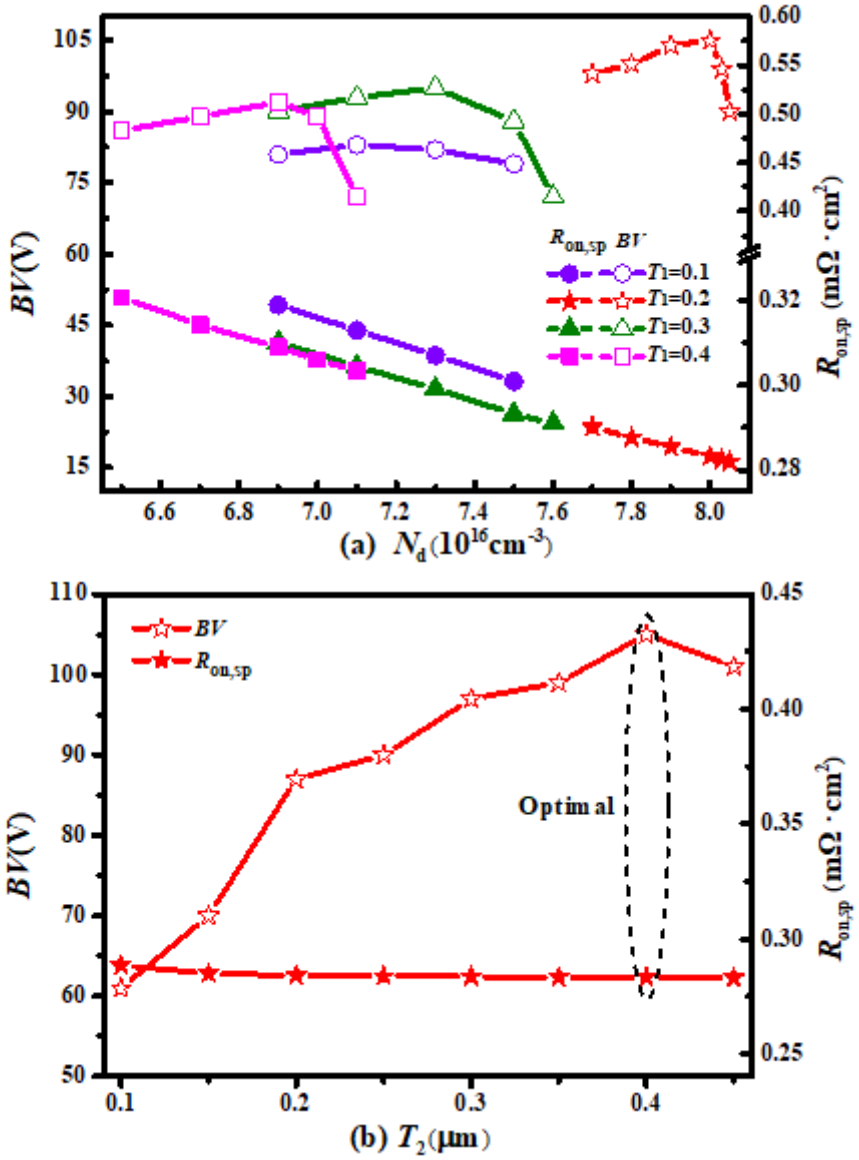

Figure 10

Effect of T1 and T2 on BV and Ron,sp . (a) Effect of T1 on BV and Ron,sp. (b) Effect of T2 on BV and Ron,sp.

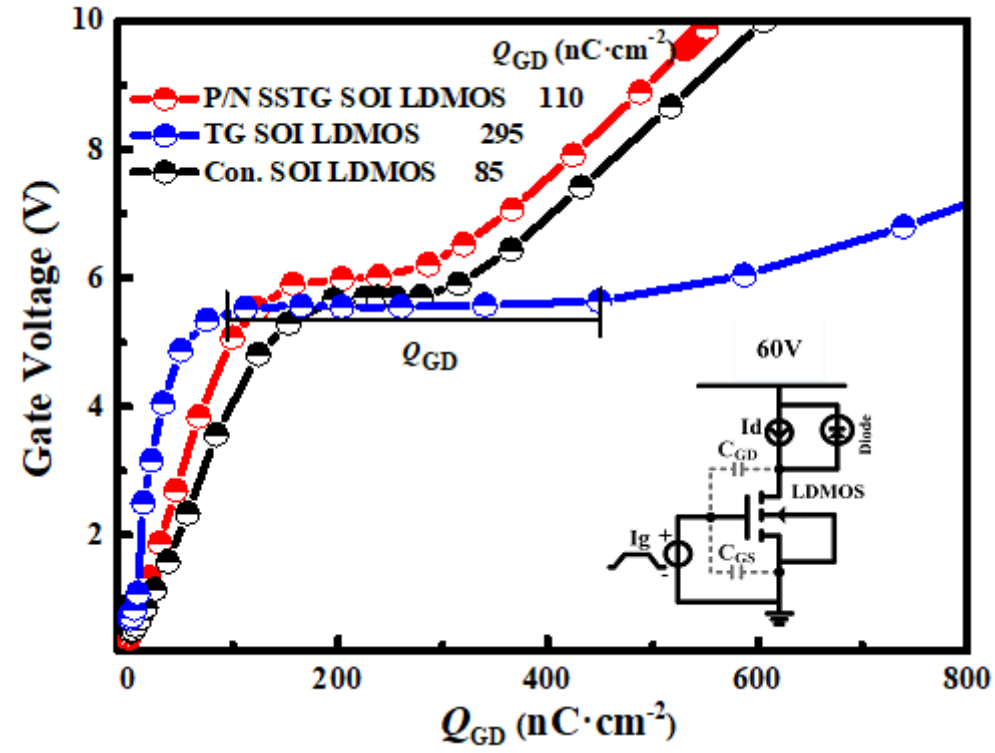

Figure 11

Comparison of the QGD of the P/N SSTG SOI LDMOS, TG SOI LDMOS and Con. SOI LDMOS.

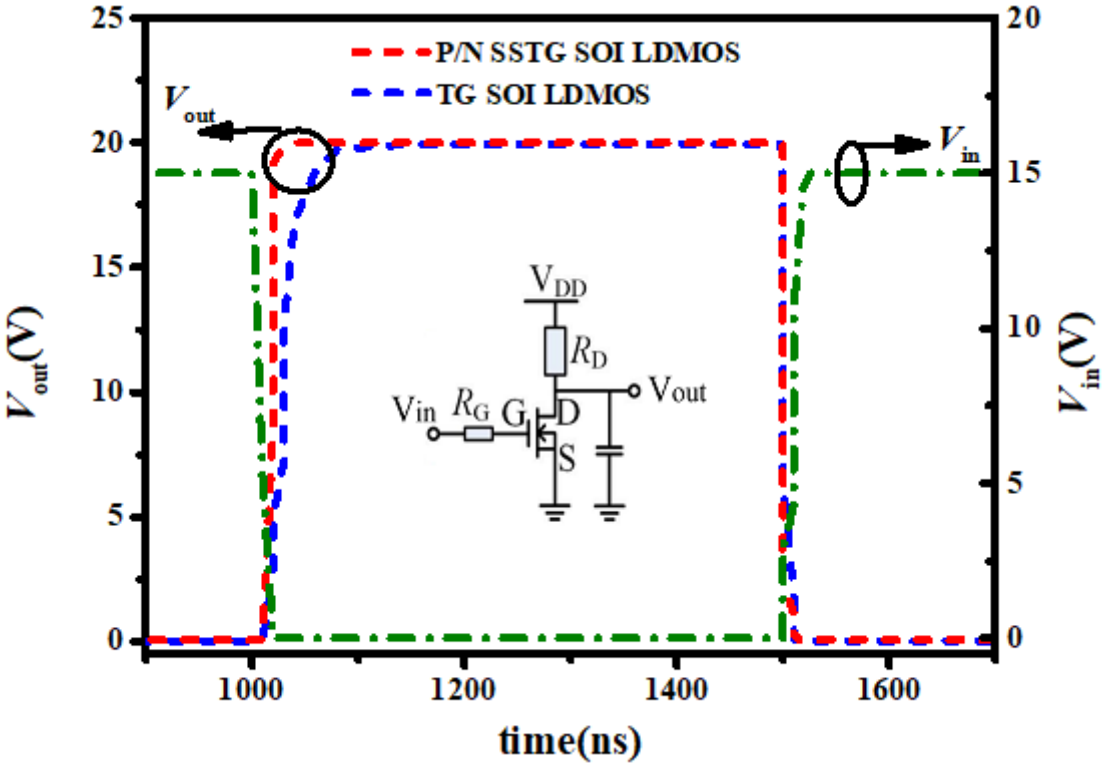

Figure 12

Switching waves of the P/N SSTG SOI LDMOS and TG SOI LDMOS at the same VDD=20V.

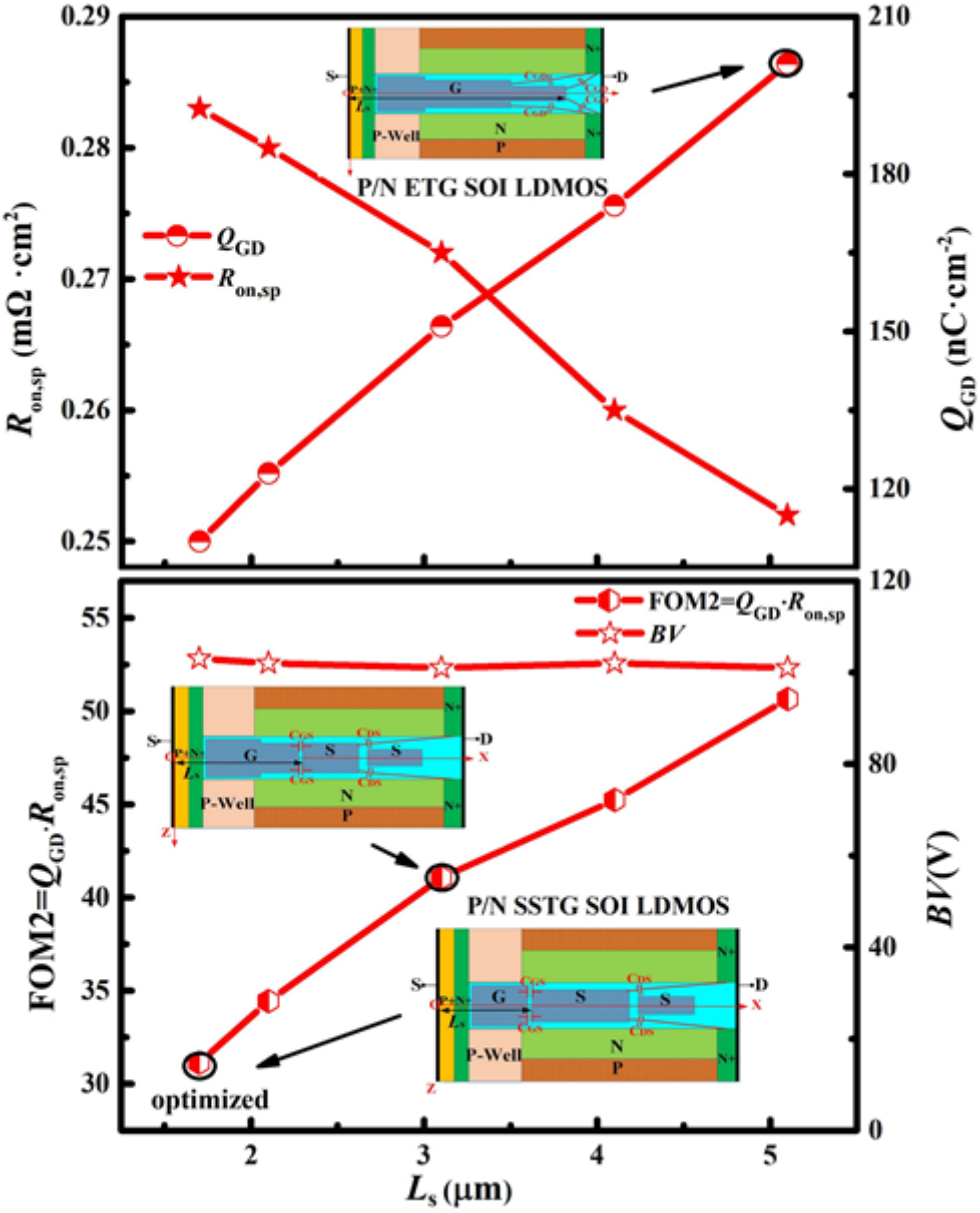

Figure 13

Effect of Ls on the Ron,sp, QGD, FOM2 and BV.

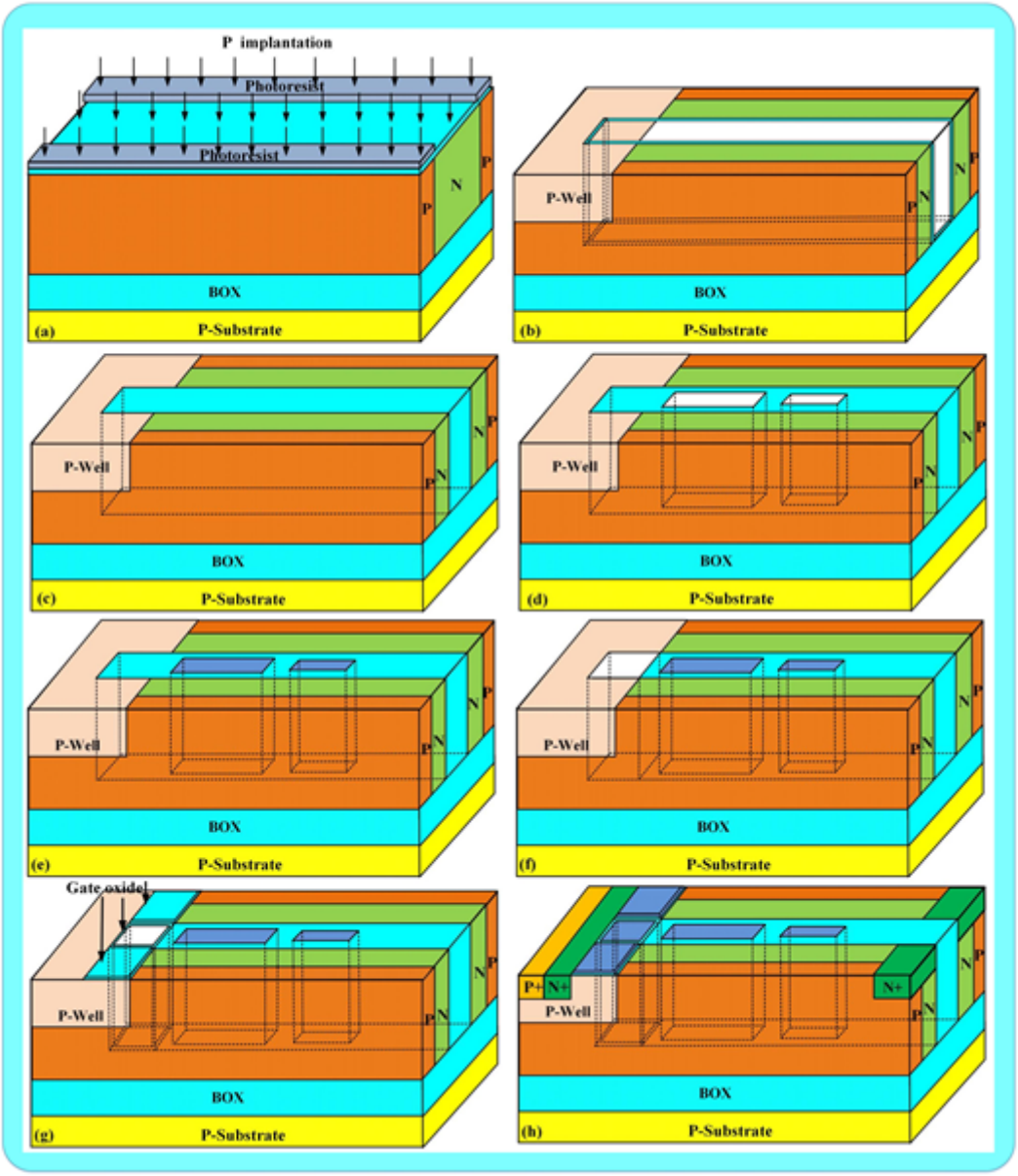

Figure 14

Fabrication process of the proposed P/N SSTG SOI LDMOS.