Comparative Performance and Reliability Analysis of Doping and Junction Free Devices with High-κ/Vacuum Gate Dielectric

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Research Article

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Abstract

A comparative evaluation of channel hot carrier (CHC) reliability and pursuance of dopingless FET (DL JLFET) and junctionless FET (JLFET) are studied for various dielectrics and compared with conventional dielectric (SiO_2) JLFET. The use of dielectrics such as vacuum near the drain and the high-κ (HfO_2) near the source in DL JLFET (VacuHDL JLFET) allows better pursuance and reliability against channel hot carrier (CHC) effects. A simulation study has shown that the pursuance of VacuHDL in terms of I_{on}/I_{off} ratio is improved by 4.5, 19.38 and 39.58 times, respectively, in comparison with vacuum based DL, HJL and JL. Similarly, the intrinsic delay of VacuHDL is improved by 9.5%, 56.8 % and 58.7 %, respectively, in comparison with VacuDL, VacuHJL and VacuJL. Hence, VacuHDL is a potential candidate for digital circuit applications. Further, we have found that vacuum-based HDL and HJL are more immunes against CHC stress and shown that the drain current of vacuHDL and vacuHJL is reduced by 6.9 % and 17.5 %, respectively, in comparison with conventional dialectic (SiO_2) based DL and JL which is 10.4 % and 20.5 %. Hence, the incorporation of vacuum dielectric towards drain terminal is helpful in reducing CHC induced effect in comparison with conventional dielectric.

I. Introduction

Charge plasma (CP) based dopingless field effect transistor (DL-JLFET) has captivated profound attention in future CMOS technology due to its high fabrication feasibility and enhance current-driving capability [1], [2]. Due to the use of the intrinsic channel, it reduces the thermal budget requirements and demonstrates refinement in process variation such as random dopant fluctuations inside the silicon [3]-[7]. Aside from this, the investigation against reliability performance suggests that DLJLFETs are more immune to channel hot carrier (CHC) effect than conventional JLFET [8], [9]. Although, the DJLFETs can be preferred or suitable for replacing the conventional JLFET, but the CHC induced deterioration still in existence as a severe reliability concern. This deterioration in nano-scaled devices is mainly pronounced as the

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inoculation of aggressive hot carriers deep into the gate dielectric near drain side. These energetic hot-carriers damage the dielectric property of the material [10]–[12]. Hence, the performance investigation against CHC effect and suitable replacement of dielectric material (SiO_2) are necessary for reliable digital circuit design. In literature, the different dielectrics (vacuum and high-κ) have been used to improve the pursuance and reliability of JLFETs [13]. Incorporation of vacuum as a dielectric below the gate however enhances the amnesty towards the hot carrier effects (HCEs) but on the flip side decrease the pursuance of the devices. For this, Ghosh et al. [26] incorporated the high-k dielectrics which results in minimum

surface potential and help to boost the carrier efficiency with better current driving capabilities. It became possible due to the inclusion of this dielectric just beneath the gate electrode. Although, the use of both dielectrics (Al_2O_3, HfO_2) has been studied in the past for RF and reliability performance of vacuum JLFET [14], [15]. But the comparative investigation of CP based high-κ/vacuum dielectric DL-JLFET (VacuHDL-JLFET) with conventional DL and JLFETs has not been performed yet. Hence proposed work focused on analyzing the pursuance and reliability of proposed vacuum and CP based HDL-JLFET and compared with conventional dielectric DL and JLFETs. The incorporation of high-κ dielectric towards the source terminal increases carrier transport efficiency, while vacuum dielectric towards drain terminal reduces electric field. Hence, the proposed device offers better performance and reliability against CHC effect. Due to its superior performance when we talk about Ion/Ioff ratio and intrinsic delay, the vacuum HDL-JLFET is also a potential candidate for digital circuit applications.

Ii. Device Structure And Simulation

Figure 1 (a-b-c-d) demonstrate a two dimensional cross sectional view of vacuJL, VacuHJL, VacuDL and VacuHDL. Here, we have considered the same dimensions and parameters as reported in [1] such as: Silicon layer thickness (T_{si}) = 10 nm, gate length (L_g) = 15 nm, oxide thickness = 1 nm, drain and source extension (L_{ext}) = 15 nm. The work function of gate electrode for JLFET devices is taken as 5.5 eV with same doping throughout silicon layer ($10^{19}cm^{-3}$). However, for DL devices, the gate electrode work function is taken as 4.73 eV with undoped Si layer ($10^{15}cm^{-3}$). To create N^+ source and drain regions in DL devices, hafnium metal contact with workfunction of 3.9 eV are used as source and drain contacts. From Fig. 1 (a) and (c), it can be seen that the conventional gate dielectric (SiO2) has been completely replaced by vacuum in JL and DL devices. Whereas, in Fig. 1 (b) and (d), the length of the gate dielectric material is divided into two parts, one part with high-κ dielectric (length = 10 nm) towards the source end and the other part with vacuum (length = 5 nm) towards the drain end. Hence, this asymmetric arrangement of gate dielectrics improve the reliability and performance of VacuHDL and VacuHJL.

Device simulations are performed through Silvaco ATLAS 2D TCAD software by considering default parameters of silicon [16]. Models of device physics i.e. Lombardi mobility model

(CVT), band-gap narrowing (BGN) and Shockley Read Hall (SRH) were enabled during simulations. To analyze the reliability against CHC effect, the hot carrier injection model (HEI) and energy balance transport (EBT) are incorporated. CHC effect is evaluated by applying gate and drain voltage of VD = VG = 1.9 V for 2000s, while, source was grounded. Forthis, we have used measure-stress-measure (MSM) technique [17]. The transfer characteristics of both fresh and stressed devices are observed before and after CHC stress. During measurement, the drain current variation is monitored by changing the gate voltage at fixed value of drain voltage. Here, the drain current variation is observed at room temperature under CHC stress of 2000s.

Iii. Simulation Results And Discussion

The comparison between the drain current characteristics of conventional DL and JL and high-k/vacuum dielectric based DL and JLFETs is shown in Fig. 2 (a-b-c). It is observed, the drain current (I_{on}) of vacuum DL and JLFETs are degraded by 25 % and 30% in comparison with conventional DL and JLFET. Whereas the drain current of vacuum HDL-JLFET and HJLFET is degraded by 20.05% and 2%, respectively. Hence, the improvement in drain current of vacuum HDL-JLFET is higher than vacuum based HJLFET, DL-JLFET and JLFET. This improvementin drain current of vacuum HDL-HLFET is obtained due to combination of high-k dielectric near the source side **Fig. 2 - Drain current characteristics of (a) conventional DL and JL, (b) VacuDL and VacuJL, and (c) VacuHDL and VacuHJL at VDS = 1 V and VGS = 1 V.**

and hafnium metal electrodes at S/D contact which enhances the transport efficiency and electron plasma. In addition, the lightly doped channel in HDL-JLFET reduces leakage current (I_{off}). Hence, the overall performance of HDL-JLFET in terms of I on/Ioff is improved by 4.5, 19.38 and 39.58 times, respectively, in comparison with vacuum based DL-JLFET, HJLFET and JLFET, as summarized in Table-I and table-II.

Parameters	JL	VacuJL	VacuHJL
I_{on}/I_{off}	7.6×10^{6}	2.4×10^{6}	4.9×10^{6}
C_{gg}(fF)	0.79	0.53	0.55
τ(pS)	0.96	0.92	0.88
CHC Degradation	20.05 %	14 %	17.5 %

TABLE I. COMPARISON OF PURSURANCE METRICS AND CHC DEGRADATION OF CONVENTIONAL JLFET, VACUUM JLFET, AND VACUUM HJLFET.

Parameters	DL	VacuDL	VacuHDL
I_{on}/I_{off}	1.82×10^{8}	0.21×10^{8}	0.95×10^{8}
C_{gg}(fF)	0.51	0.31	0.39
τ(pS)	0.49	0.42	0.38
CHC Degradation	10.4 %	6.0 %	6.9 %

TABLE II. COMPARISON OF PURSURANCE METRICS AND CHC DEGRADATION OF CONVENTIONAL DL-JLFET, VACUUM DL-JLFET, AND

VACUUM HDL-JLFET.

From Table I and II, it is summarized that the total gate capacitance (C_{gg}) decreases with the incorporation of vacuum dielectric in DL and JLFETs as compared to conventional dielectric DL and JLFETs. However, the C_{gg} of vacuum DLJLFET is lower than the vacuum HDL-JLFET, in spite of that the

intrinsic delay of HDL-JLFET is improved by 9.5% in comparison with vacuum DL-JLFET. Because, the intrinsic delay of FET is approximated as $C_{gg}V_{ds}/I_d$ and here, in case of vacuum HDL-JLFET, the rate of increase in capacitance is compensated by amount of increase in drain current, hence, the intrinsic delay of vacuum HDL-JLFET is lower than vacuum DL-JLFET. On the other hand, the gate capacitance of other vacuum dielectric based JLFETs is higher than HDL-JLFET. Hence, the intrinsic delay of HDL-JLFET is improved by 56.8 % and 58.7 %, respectively, in comparison with vacuum based HJLFET and JLFET, as summarized in Table I and II. Thus, the lower intrinsic delay and higher I_{on}/I_{off} ratio of vacuum HDL-JLFET will show better switching performance and make it the most suitable candidate for high speed digital circuit applications.

The degradation in drain current of conventional and vacuum/ high-κ dielectric DL and JLFETs under CHC stress of 2000s. It can be observed from Table I that the conventional dielectric DL and JLFETs experience higher drain current degradation (10.4 % and 20.5 %) as compared to vacuum HDL-JLFET and HJLFET (6.9 % and 17.5 %). Whereas, the drain current of only vacuum dielectric DL and JLFETs are degraded by 6 % and 14 %. The lower drain current degradation is observed with vacuum DL and JLFETs due to lower electric field at the drain side **Fig. 3 - Electric field profile of (a) conventional DL-JLFET, vacuum DLJLFET, and vacuum HDL-JLFET, (b) conventional JLFET, vacuum JLFET, and vacuum HJLFET under CHC stress for 2000 seconds at $V_D = V_G = 1.9$ V.**

Figure 4 - Threshold voltage variation of (a) conventional DL-JLFET, vacuum DL-JLFET, and vacuum HDL-JLFET, (b) conventional JLFET, vacuum JLFET, and vacuum HJLFET under CHC stress for different time spans at $V_D = V_G = 1.9$ V.

and hence the fewer probability to occur the impact ionization process driven by electrical bias, as shown in Fig. 3 (a) and (b). Thus, the vacuum DL and JLFETs are more immune from short channel effects (SCEs) in contrast with conventional DL and JLFETs. Moreover, fabrication of high-k dielectric on top of silicon directly may cause defects in the interface of these two layers and adversely can affect the channel formation inside the silicon [18]. Due to this defect, influence occurs in drain current of both the device (vacuum DL and JLFETs). But, here, we have considered the most damaging CHC stress condition near the drain side in both devices and this effect in short channel devices is mainly caused by the SCE not by the presence of high-k layer [11]. Hence, the CHC induced degradation is less pronounced in vacuum HDL-JLFET and HJLFET as compared to conventional DL and JLFETs. Similarly, the lower degradation was obtained with vacuum DL and JLFETs due to much lower electric field near drain side. It can be seen from Fig. 3 (a) and (b), the lower electric fields are observed near the drain side in the channel in high-k/vacuum dielectric based DL and JLFETs as compared to conventional DL and JLFETs. Hence, the short channel effect (SCE) is insignificant with vacuum dielectric based DL and JLFET and it is more immune from CHC stress. It is also summarized in Table I and II.

From the Fig. 4 (a-b), variation in threshold voltage is observed and lead to enhancement in it under CHC stress at $V_D = V_G = 1.9$ V and it is less pronounced in high-κ/vacuum dielectric DL and JLFETs in comparison with conventional dielectric DL and JLFETs. Hence introduced vacuum dielectric near the

drain side reducing electric field as a reuslt minimizing the effect of impact ionization. Moreover, the possibilities of damaging the dielectric are now reduced since hot carriers are now dealing directly with gate electrode. It is just due to decrement in traping inside the dielectric. One can also observe from Fig. 4 (a) that the DL structures show less V_{th} variability due to CHC stress in comparison to JLFET based structures. In addition, drain current degradation results in an increment in density of states and hence the threshold volage. Drain current of DL-JLFET is comparatively very low than the drain current of JLFET, it may be as a result of the reduction in doping concentration, electric field and density of interface states. Hence, the combination of CP with vacuum dielectric based HDL-JLFET and DL-JLFET show more immunity against CHC induced stress.

Iv. Conclusion

A comparison of the pursuance and reliability of conventional dielectric DL and JLFETs with high-κ/vacuum dielectric DL and JLFETs is made and successfully elaborated. The use of only vacuum dielectric in DL and JLFET enhances reliability against CHC stress and observed lower pursuance. Whereas, the combination of high-κ/vacuum dielectric CP based HDL-JLFET exhibits superior performance in terms of higher I_{on}/I_{off} (~ 1×10^{8}) and least intrinsic delay as compared to other vacuum-based devices. Intrusion of high-k (HfO_2) dielectric towards the source side increases transport efficiency, while, vacuum dielectric near the drain reduces electric field, and thereby diminishing the ionization and CHC effects. However, from the simulation, CHC stress impact on drain current and degradation is less pronounced in HDL-JLFET than conventional JL and DLFETs. Further, the CHC stress was analyzed for different time spans and it was found that Vth variation is more significant in JL devices than CP based DL devices. Hence, vacuum HDLJLFET is a potential candidate for digital circuit applications and shows better immunity against CHC stress.

Declarations

A. Funding Statement

Authors declare that for this work, we have not got any funding from anywhere.

B. Conflict of Interest

There is no competing or conflict of interests in the presented preposed work.

C. Author contributions

Rakesh Kumar have analyzed and interpreted the problem statement and suggested a solution. Along with Lokesh Bramhane and Meena, we have simulated the different results and calibrated with the literatures. After evaluation, we all have equal contribution in preparing the manuscript. Hence authors gauranteed about the proposed work.

D. Availability of data and material

Data sharing is not applicable to this article.

E. Compliance with ethical standards

Not Applicable

F. Consent to participate

Not Applicable

G. Consent for Publication

Not Applicable

H. Compliance with Ethical Standards

This article does not contain any studies with human participants or animals performed by any of the authors.

I. Author Declarations

We authors of the above titled paper hereby declare that the work included in the above paper is original and is an outcome of the research carried out by the authors indicated in it.

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Figures

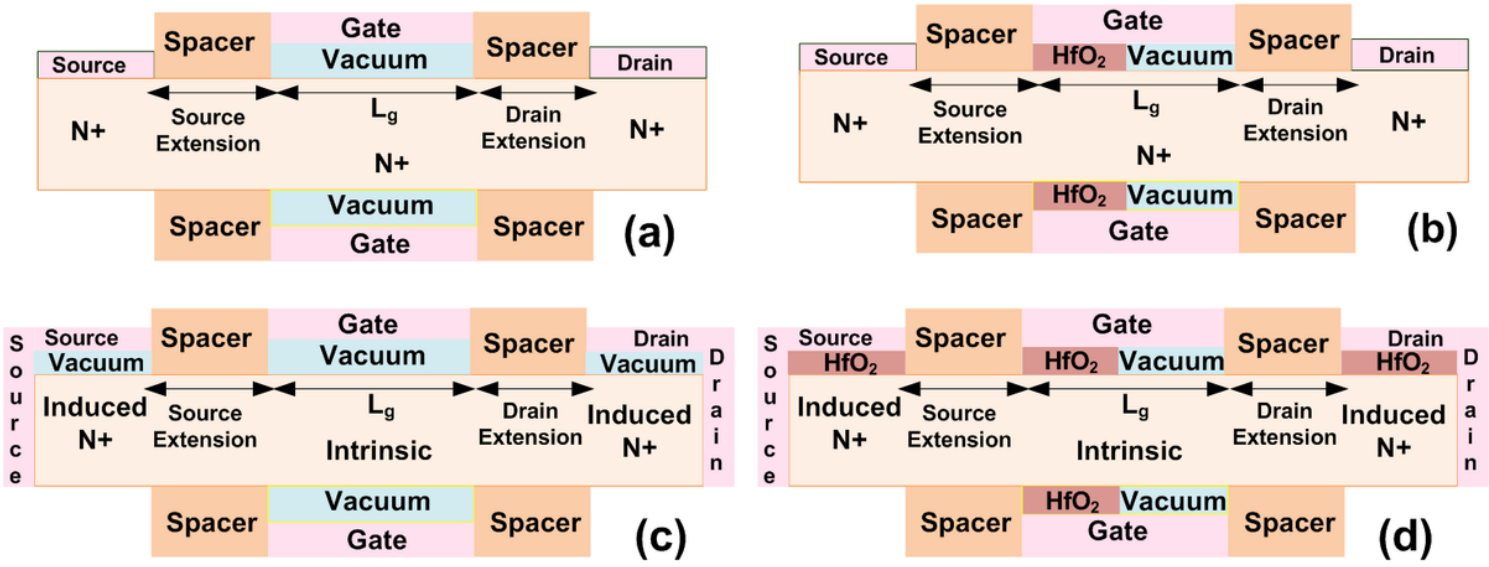

Figure 1

Cross-sectional views of (a) VacuJL, (b) VacuHJL, (c) VacuDL, and (d) VacuHDL.

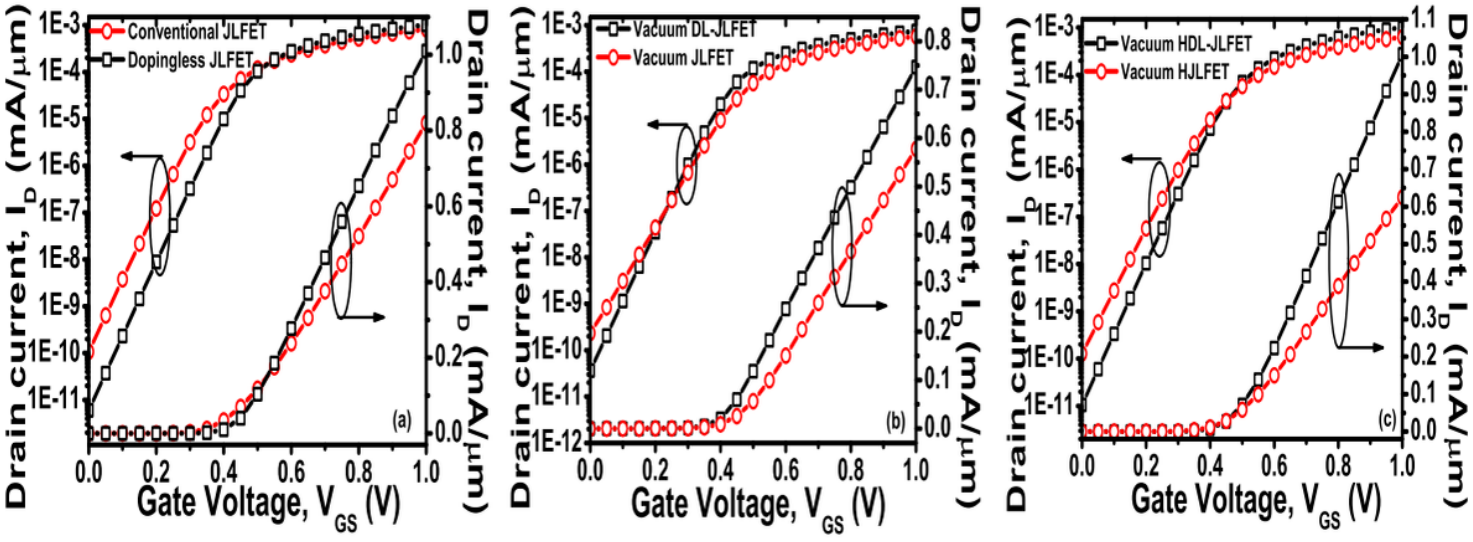

Figure 2

Drain current characteristics of (a) conventional DL and JL, (b) VacuDL and VacuJL, and (c) VacuHDL and VacuHJL at VDS = 1 V and VGS = 1 V.

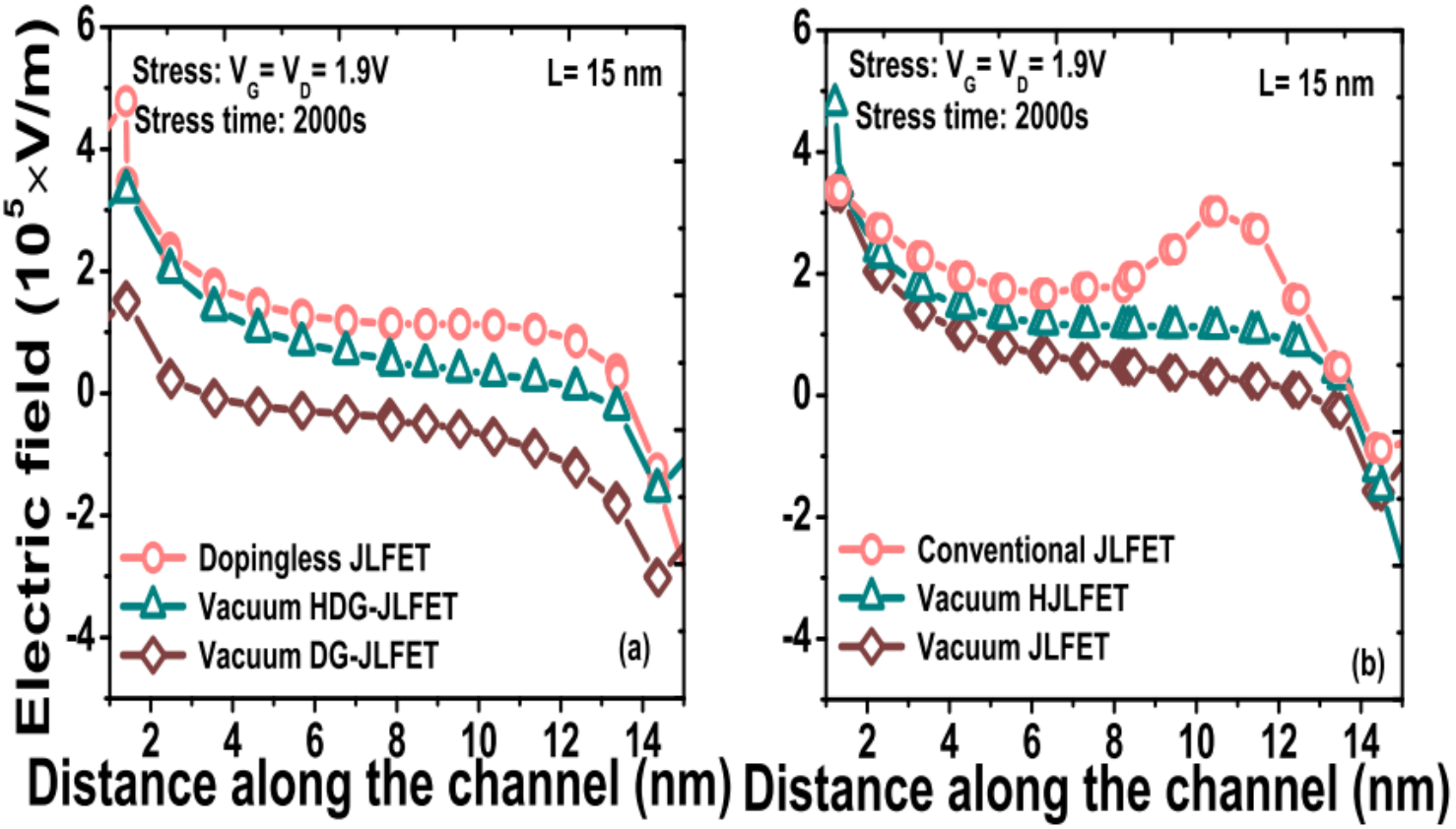

Figure 3

Electric field profile of (a) conventional DL-JLFET, vacuum DLJLFET, and vacuum HDL-JLFET, (b) conventional JLFET, vacuum JLFET, and vacuum HJLFET under CHC stress for 2000 seconds at VD = VG = 1.9 V.

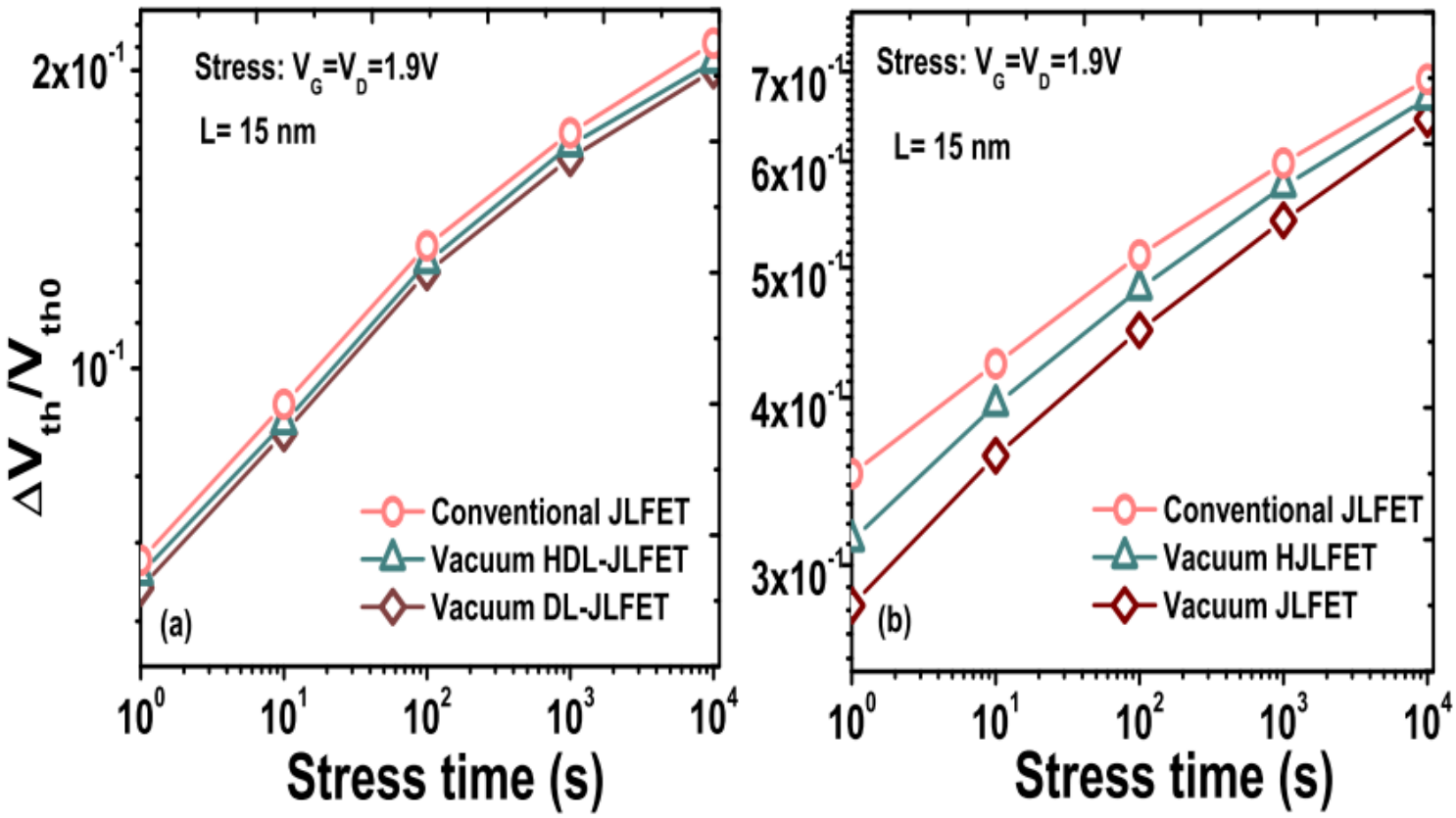

Figure 4

Threshold voltage variation of (a) conventional DL-JLFET, vacuum DL-JLFET, and vacuum HDL-JLFET, (b) conventional JLFET, vacuum JLFET, and vacuum HJLFET under CHC stress for different time spans at VD = VG = 1.9 V.