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Fermi-level pinning-free WSe_2 transistors via 2D van der Waals metal contacts and their complementary logic gate circuits

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Precise control over the polarity of transistors is a key necessity for the construction of complementary metal–oxide–semiconductor circuits. However, the polarity control of two-dimensional (2D) transistors remains a challenge because of Fermi-level pinning resulting from disorders at metal–semiconductor interfaces. Here, we propose a strategy for clean van der Waals contacts, wherein a highly degenerate (metallic) 2D material, chlorine-doped $SnSe_2$ (Cl–$SnSe_2$), is used as the contact to provide an interface that is free of defects and Fermi-level pinning. Such clean contacts created via van der Waals integration of a 2D metal possess nearly ideal Schottky barrier heights, thus permitting polarity-controllable transistors. With the integration of 2D metallic Cl–$SnSe_2$ as contacts, WSe_2 transistors exhibit pronounced p-type characteristics, which are distinctly different from those of the devices with evaporated metal contacts, where n-type transport is observed. Finally, this ability to control the polarity enables the fabrication of functional logic gates and circuits, including inverter, NAND, and NOR.

Precise control over the polarities (n- or p-type) of transistors is a key necessity for the fabrication of modern complementary metal–oxide–semiconductor (CMOS) circuits. Although ion implantation is a common doping process for modifying the polarities of silicon transistors,[1] this procedure is limited in 2D materials because of their atomic-scale thicknesses.[2] Thus, the majority carrier type of 2D transistors relies mainly on carrier injections through the Schottky barriers at metal–semiconductor junctions, which are intrinsically bipolar[3,4]—that is, the simultaneous injection of both electrons and holes is possible and can be tuned via Schottky barrier engineering. Multiple n-type transistors with high electron motilities and on/off ratios, such as MoS_2, $MoSe_2$, and ReS_2,[5] have been demonstrated; however, their p-type counterparts have been scarce despite years of effort. The fundamental issue in controlling device polarity is the presence of strong Fermi-level pinning at the metal–2D semiconductor interface.[2] This pinning is attributed to the difficulty in creating an atomically clean metal–2D semiconductor interface; conventional metallization process could damage the 2D semiconductors and create associated defect-induced gap states that eventually pin the Fermi level at the charge neutrality level.[2,6] Therefore, the Schottky barrier is fixed once pinning, setting the transistors into a particular polarity (i.e., mostly n-type).

One approach to address such a challenge is to create 1D edge electrical contacts for MoS_2 field-effect transistors (FETs).[7] Fermi-level depinning was realized with this approach, following Schottky–Mott rule. However, an aggressive plasma etching process is required to create strong coupling between the edges of 2D materials and metals, which necessitates careful investigation into side effects, such as chemical impurities and contamination. Alternatively, the creation of van der Waals (vdW) contact via metal transfer has been explored, allowing for a highly tunable Schottky barrier depending on the work function of the metal

used.[2] However, difficulties in performing a reliable transfer process and preventing interface contamination pose challenges to their practical application. On the other hand, recently, the use of vdW 2D metals as contacts has been shown to provide atomically clean interfaces at metal–semiconductor junctions;[8-11] these clean interfaces from vdW 2D metals could potentially prevent Fermi-level pinning, thus promising excellent control over the Schottky barrier and the resulting device polarity. Several attempts have been made to use vdW 2D metals as contacts on WSe_2 or MoS_2, such as highly p-doped WSe_2,[8] $NbSe_2$,[9] highly p-doped MoS_2,[10] and 1T-TaS_2.[11] Although all of these studies have shown improvement in contact properties (e.g., contact resistance, FET mobility) through the use of vdW 2D metals, the underlying mechanisms need to be clarified; these improvements could have resulted from Fermi-level depinning, doping effects, interface dipoles, or interactions within the contact interface, yet such aspects have not been investigated, which limits further development. Furthermore, functional applications that rely on control over the device polarity, such as CMOS logic gates, are yet to be achieved using vdW 2D metal contacts.

Here, we propose a strategy for clean van der Waals contacts, in which metallic Cl–$SnSe_2$ is used as contact, resulting in Fermi-level depinning at the metal–semiconductor interface. Such atomically clean interfaces lead to near-ideal Schottky barrier heights (SBHs), thus allowing tunability over the carrier polarity. We demonstrate a complementary logic inverter with the ability to control the polarity of WSe_2 transistors, achieving a high voltage gain of 40 (at a bias voltage of 5 V). This allows us to design and fabricate more complex logic functions, such as NAND and NOR gates.

Electrical characterization of Cl–$SnSe_2$

Fig. 1a shows the energy band alignments of multilayer WSe_2,[12] MoS_2,[13] and metal contacts used in this study. Ideally, the majority carriers for both multilayer WSe_2 and MoS_2 should be holes for palladium (Pd), because the Fermi level of Pd lies closer to the valence band edge than to the conduction band edge.[14] However, most reported Pd-contacted multilayer WSe_2 and MoS_2 FETs exhibit n-type characteristics because of Fermi-level pinning.[15] Theoretical studies have suggested that the use of vdW 2D metals is an effective, doping-free approach to solving this pinning issue.[16,17] Inspired by this, we explore Cl–$SnSe_2$ as a promising 2D metal for hole injection into 2D semiconductors. Recently, we synthesized metallic $SnSe_2$ via substitutional doping of Cl atoms;[18,19] in contrast to pristine $SnSe_2$, Cl–$SnSe_2$ exhibits metallic behaviour with high conductivity comparable to that of few-layer graphene.[20] Furthermore, because of its high work function (~4.7 eV) and pinning-free surface, Cl–$SnSe_2$ is expected to provide efficient hole injection and thus p-type transport as designed.

Single crystals of Cl-doped $SnSe_2$ were synthesized via melt-solidification process (see Methods). Figure 1b illustrates the atomic lattice structure of Cl–$SnSe_2$, where Cl atoms replace Se atoms in the parent $SnSe_2$. The X-ray diffraction (XRD) patterns (Supplementary Fig. 1a) for Cl–$SnSe_2$ and pristine $SnSe_2$ are nearly identical, indicating that the structural integrity of $SnSe_2$ is maintained. Such a high crystallinity was also confirmed from Raman spectra (Supplementary Fig. 1b), where no noticeable change in peak-to-peak distance or full width at half-maximum (FWHM) of the E_g peak was observed in Cl–$SnSe_2$. Moreover, a slight redshift (~1.0 cm^{-1}) of A_{1g} peak, which is an indication of a n-type doping in other substitutionally doped materials,[21,22] was observed in Cl–$SnSe_2$.

Ultraviolet photoelectron spectroscopy (UPS) measurements were performed to elucidate the

band structure of the Cl–$SnSe_2$ (Fig. 1c). The energetic difference between the valence band maximum and Fermi level is ~1.30 eV. The inset in Fig. 1c shows clear and sharp peak around the Fermi level, which corresponds to a partly filled conduction band originating from hybridized orbitals of Sn and Se atoms.[18] These hybridized states around the Fermi level would lead to degenerate semiconductor and therefore a metal-like behaviour, in contrast to intrinsically semiconducting $SnSe_2$. The estimated work function of Cl–$SnSe_2$ is 4.71 eV (left panel of Fig. 1c), which is close to the valence band of multilayer WSe_2 (5.11 eV), indicating that p-type behaviour could be obtained for FET devices constructed using Cl–$SnSe_2$, as will be shown in the following sections.

Metallic Cl–$SnSe_2$ must also exhibit ohmic contact with low resistance between Cl–$SnSe_2$ and 3D metal to ensure optimized charge injection within the 3D metal/2D metal contact system. The FET performance of 13-nm-thick Cl–$SnSe_2$ was investigated using a transfer line method (TLM) device with varying channel lengths (Fig. 1d). The device structure consisted of a Ti/Au local bottom gate, a 16-nm h-BN gate dielectric, and Pd as source/drain metal electrodes. The transfer characteristic of a device with a channel length of 1 μm (Fig. 1e) exhibited negligible current modulation by the gate voltage, and metallic behaviour with excellent conductivity that resulted from degenerate states, consistent with our UPS results. The sheet carrier density of Cl–$SnSe_2$, derived from the transfer curves, is ~10^{14} cm^{-2} at V_{GS} = 0 V (Supplementary Fig. 2), which is higher than those of pristine transition metal chalcogenides (on the order of 10^{13} cm^{-2} or even less). Figure 1f presents the total resistance normalized by width (R_T) as a function of channel length (L) for the same device. Through TLM analysis, the contact resistance (R_c) and the sheet resistance of the channel (R_{sh}) were obtained from the y-axis intercept and slope, respectively, of the linear fit to the data (Fig. 1f).

The Pd/Cl–$SnSe_2$ junction exhibits a low contact resistance of ~0.164 kΩ μm at V_{GS} = 0 V, which guarantees highly efficient carrier injection at the 3D metal/2D metal junction. Notably, this contact resistance value is lower than values obtained using a phase-engineered (0.2–0.3 kΩ μm),[23] 3D metal/graphene (2–10^2 kΩ μm),[24,25] and 3D metal/2D 1T′-WTe_2 contacts (0.4–1.03 kΩ μm),[26,27] which shows the great potential of our Cl–$SnSe_2$ as a 2D metal contact. The inset in Fig. 1f shows the linear output characteristics of corresponding devices, suggesting well-defined ohmic contacts (i.e., low-resistance contacts) between Cl–$SnSe_2$ and Pd. The metallicity of Cl–$SnSe_2$ is further supported by the sheet resistance–temperature (R_{sh}–T) plot (Fig. 1g), where the obtained sheet resistance of Cl–$SnSe_2$ is almost independent of temperature. Together, the data in Fig. 1. demonstrate that we have produced a high-quality, degenerately doped semiconductor Cl–$SnSe_2$, which can serve as a 2D metal electrode for pinning-free high-performance 2D devices. Below, by fabricating WSe_2 devices as the main example, we reveal unique potential and excellent pinning-free nature of this 2D metal.

Device fabrication

Figure 2a–c shows the fabrication steps for WSe_2 FETs with Cl–$SnSe_2$ contacts: (a) multilayer WSe_2 onto an h-BN-capped local bottom Au gate, (b) alignment and transfer of Cl–$SnSe_2$, (c) removal of polycarbonate film from Cl–$SnSe_2$/WSe_2, and deposition of Pd metal pads for electrical characterization (see Methods). Such an integration of a 2D metal electrode can create atomically clean interfaces at metal–semiconductor junctions because this process prevents damage caused by direct metallization, as illustrated in Fig. 2d. Moreover, Cl–$SnSe_2$ acts as a physical buffer layer protecting the underlying WSe_2 from possible contaminations (e.g., chemicals, polymers, and mechanical strain) that can occur in subsequent fabrication. By

contrast, the conventional processes for metal integration typically result in substantial damage to 2D semiconductors and introduce interface disorder such as defect, metal diffusion, and chemical bonds (Fig. 2f).[2,6,28]

Characterizations of WSe_2 FETs with Cl–$SnSe_2$ contacts

We explored this picture experimentally by first comparing the physical properties of differently constructed contact interfaces. Cross-sectional transmission electron microscopy (TEM) images of Pd/WSe_2 (upper panel of Fig. 3a) show apparent damage to the topmost WSe_2 layers, which we believe is the main reason for Fermi-level pinning, as reported in previous studies.[2,28] By contrast, the Cl–$SnSe_2$/WSe_2 interface remained intact and free of defects, featuring an atomically clean interface (lower-magnification images are also included in Supplementary Fig. 3). The image further shows that the spacing between two dissimilar materials is nearly indistinguishable from that in the natural van der Waals structure of WSe_2, suggesting that the Cl–$SnSe_2$/WSe_2 interface becomes a van der Waals contact. X-ray photoelectron spectroscopy (XPS) was also conducted to investigate the chemical states of the Cl–$SnSe_2$/WSe_2 interface. The spectra obtained from Cl–$SnSe_2$/WSe_2 (Fig. 3b) show features almost identical to those of pristine WSe_2, suggesting that Cl–$SnSe_2$ in contact with WSe_2 does not introduce any chemical reactions, defects, or strains at the interface or within the WSe_2. The Raman spectrum of the WSe_2/Cl–$SnSe_2$ heterojunction (Fig. 3c) shows no peaks associated with nonstoichiometric W_xSe_y, further confirming a clean interface and agreeing well with our TEM and XPS results. These results show the advantage of using Cl–$SnSe_2$ as a contact electrode with which a clean contact interface can be readily achieved. Such a clean interface of 2D/2D contacts could offer a nearly ideal Schottky barrier height dictated by the metal work

function, which is crucial for the rational design and fabrication of 2D devices and circuits.[29]

To this end, the effect of Cl–$SnSe_2$ contacts on the electrical properties of WSe_2 transistors was investigated using charge-transport measurements. Figure 3d shows a schematic (upper) and optical (lower) image of the fabricated device; two different contacts of both evaporated Pd (denoted by a black box) and Cl–$SnSe_2$ (red box) are formed on a single WSe_2 flake for comparison. For the Cl–$SnSe_2$ contact, the device exhibited predominantly p-type characteristic (Fig. 3e), as expected from the energy band offset between the Fermi level of Cl-$SnSe_2$ and the valence-band energy level of multilayer WSe_2 (Fig. 3e). By contrast, for the evaporated Pd contacts, with a higher work function (5.3 eV) than that of Cl–$SnSe_2$, the device consistently exhibited n-type behaviour (Fig. 3f). This is similar to that in previously reported multilayered WSe_2 transistors, where direct metallization was employed to form the contacts.[12,15] This observation indicates that the Fermi level is pinned closer to the conduction band edge of WSe_2, and thus a low electron barrier is formed at the interface between Pd and WSe_2. For a clear estimation, we tested 20 devices to obtain the statistical variation in carrier polarity (Fig. 3g). Here, the carrier polarity was characterized by the current ratio of I_{3V} (I_{DS} at V_{GS} = 3 V) to I_{-3V} (I_{DS} at V_{GS} = −3 V), which represents the majority carrier type. There is a clear and distinguishable trend showing that only the Cl–$SnSe_2$-contacted devices exhibited p-type transport, with I_{3V}/I_{-3V} ratios exceeding values of 10^{-2}. The observed distinction could be explained by the presence (or absence) of a pinning effect, which normally originates from the interface morphology of contacts, as discussed later in the text.

The FET mobility was extracted from the linear region of transfer curves,[12] and their hole and electron mobility are 15.7 and 33.0 $cm^2\ V^{-1}\ s^{-1}$, respectively. The contact resistances (R_c) of the devices are also estimated using the *Y*-function method (Supplementary Fig. 4), where R_c

is measured to be 7.3 kΩ μm (at $n = 1.9 \times 10^{12}$ cm^{-2}) for Cl–$SnSe_2$ contact, and 114.1 kΩ μm (at $n = 2.0 \times 10^{12}$ cm^{-2}) for the evaporated Pd contact. Compared to that of evaporated contacts, the higher contact resistance of the Cl–$SnSe_2$ contact is attributed to its larger Schottky barrier height.[30] Moreover, air stability was demonstrated by WSe_2 transistor with Cl–$SnSe_2$ contacts (Supplementary Fig. 5). The device retained its original polarity (p-type) under ambient conditions for a three-month period, except for a slight threshold voltage shift that may be caused by ambient water, which clearly suggests the stability of our Cl–$SnSe_2$ contacts.

Characterization of Schottky barrier height

To gain insight into the distinctly opposite polarities that result from different contact types, we investigated a range of different metals (Ti, Au, Pd and Cl–$SnSe_2$) with varying work functions within the framework of the Schottky–Mott model, which allows us to distinguish between the effect of Fermi-level pinning and the doping effect as a mechanism. Figure 4a–d shows the I_{DS}–V_{GS} transfer curves of multilayer WSe_2 FETs with contacts composed of a series of metals. As shown in Fig. 4a–c, all devices with evaporated metals exhibited similar n-type characteristics, regardless of the metal work function, indicating that the effect is not specific to a particular metal. By contrast, for the device with Cl–$SnSe_2$ contact (Fig. 3d), the majority charge carrier switched, and well-behaved p-type characteristic was observed with clear metal–insulator transistor behaviour,[31] suggesting an optimized metal–semiconductor contact with a low hole barrier.

To quantitatively estimate the Schottky barrier height (SBH), we performed temperature-dependent I–V measurements on the aforementioned devices. The effective barrier height (Φ_B) can be calculated from the slope of the linear fit to $\ln(I_{DS}/T^2)$ versus $1/T$ using thermionic

emission:[32]

$$I_{\mathrm{DS}} = AA^{*}T^{2}\exp\left[-\frac{\Phi_{\mathrm{B}}}{k_{B}T}\right] \quad (1)$$

where A is the area of the Schottky junction, A^{*} is the Richardson constant, I_{DS} is the total current, k_{B} is the Boltzmann constant, and T is the absolute temperature. Plots of Φ_{B} versus V_{GS} for the different contacts are presented in Fig. 4e. The SBH (Φ_{SB}) of each WSe_2 device was determined under the flat-band condition ($V_{\mathrm{GS}} = V_{\mathrm{FB}}$), which corresponds to the deviation from linear dependence of V_{GS} of the thermionic emission model.

Figure 4f shows the measured SBH values for different contact metals as functions of their work functions. Here, the pinning factor S ($S = |\mathrm{d}\Phi_{\mathrm{SB}}/\mathrm{d}W|$) is the slope of the fitted line, indicated by the dashed black line, of the experimentally obtained values. For devices with evaporated metals, the SBH is nearly independent of the work function of the metal, with a small electron barrier ranging from 190 to 250 meV. Furthermore, the S parameter was determined to be 0.001, indicating that the Fermi level is strongly pinned at the metal–semiconductor interface.[33] By contrast, for the device with Cl–$SnSe_2$, the Schottky barrier type is tuned from electrons to holes, and the energy barrier for hole injection was measured to be ~350 ± 26 meV, which is consistent with the value expected for the WSe_2/Cl–$SnSe_2$ junction (Fig. 1a). This result indicates that Cl–$SnSe_2$ forms a nearly ideal interface with WSe_2 without pinning and thus largely follows the Schottky–Mott rule ($S = 1$), indicated by the dashed red line. The clean interface was further verified by the enhancement of the subthreshold swing (SS) value, which is related to the trap densities at or near the contact (Supplementary Fig. 6).[34,35] The schematics of the band diagrams are shown in Fig. 4h,i and Supplementary Fig. 7, depicting the cases of evaporated metal and Cl–$SnSe_2$ contacts, respectively.

The observed opposite behaviours between the different types of contacts could be explained by the presence (or absence) of Fermi-level pinning effect, which originates mainly from interface disorders due to aggressive fabrication processes or chemical reaction at the metal–2D semiconductor interface.[2,6,28] Previously, scanning transmission electron microscopy experiments[2,6,28] demonstrated that direct metallization can induce damages that significantly modify the original levels, leading to Fermi-level pinning and thus large deviations from the Schottky–Mott limit. This principle is consistent with the observations on our devices, which predominantly show a particular polarity (i.e., the n-type) irrespective of the work functions of the evaporated metals. By contrast, 2D metal Cl–$SnSe_2$ does not interact with adjacent WSe_2, thus forming a vdW interface, which is thought to be a near-ideal interface, and preventing the creation of defects that otherwise lead to Fermi-level pinning. Consequently, the SBH can possess an intrinsic value, thereby contributing to p-type characteristics in the WSe_2 devices.

In addition to WSe_2, we also confirmed the formation of a clean contact interface on MoS_2. Using the same methodology, multilayer MoS_2 devices were fabricated with different metal contacts, after which variable-temperature *I–V* measurements were performed. For MoS_2 devices using evaporated metals, we consistently observed n-type behaviours, with low electron barriers of 90–141 meV and a slope $S = 0.05$, suggesting strong Fermi-level pinning (Fig. 4g and Supplementary Fig. 8a–c). By contrast, for the device with the Cl–$SnSe_2$ contact, we observed ambipolar characteristics, with the electron current being higher than the hole current (Supplementary Fig. 9). Our measurement further revealed that the SBH for electrons was ~420 ± 37 meV and the SBH for hole injection was ~780 ± 26 meV (Supplementary Fig. 8d), consistent with the Schottky−Mott theory and our FET characteristics. These results also confirm the high interfacial quality of vdW 2D metal on 2D semiconductors.

Logic gates and circuits based on WSe_2 FETs

The ability to precisely control the carrier type of an individual device enables the implementation of CMOS logic gate circuits on a single material; this strategy can generate homogeneous CMOS structures within a single compatible process, in contrast to heterogeneous types prepared from two materials (n- and p-type),[36,37] which necessitates distinct synthesis and processing. Given the two discrete polarities (p- and n-type) with high on/off ratios, multilayer WSe_2 transistors were selected as the building blocks. First, we fabricated a complementary inverter, the simplest logic gate, as shown in Fig. 5a. The inverter consisted of two WSe_2 FETs placed in series, where one was created using evaporated Pd contacts (n-FET) and the other was fabricated with Cl−$SnSe_2$ contacts (p-FET). Plots of I_{DS} versus V_{GS} for both FETs are shown in Fig. 5b, featuring highly symmetric characteristics centered around V_{GS} = 0 V. Figure 5c shows the voltage transfer characteristics of the inverter under different voltage bias (V_{DD}). The voltage swing of the inverter features clear logic outputs with a sharp voltage transition, achieving a high gain of approximately 40 at V_{DD} = 5 V. Such a high voltage gain is crucial for robust logic operation in integrated circuits.[29] The static peak energy consumption of the corresponding device is also presented in Supplementary Fig. 10. The performance of the inverter is sufficient for the construction of more complex circuits. To this end, we also constructed NAND and NOR logic gates by integrating four WSe_2 transistors, as shown in the circuit diagram in Fig. 5d. Successful operation of both NOR and NAND was observed from logically valid outputs (Fig. 5e, f). Thus, these results prove the practicality of vdW 2D/2D contacts for multifunctional integrated circuitry.

Conclusion

In summary, we have demonstrated the creation of clean vdW 2D/2D contacts, where 2D metal Cl–$SnSe_2$ is in contact with 2D semiconductor WSe_2, to enable control over the polarity of transistors. Through detailed investigations, we found that these vdW contacts can resolve the Fermi-level pinning issue in typical metal contacts, leading to near-ideal Schottky barrier heights and thus p-type characteristics in WSe_2 transistors. Notably, the Schottky barrier heights of these devices also largely obey the Schottky–Mott limit, indicative of defect-free interfaces. We further confirmed that this vdW contact is applicable to MoS_2, yielding ambipolar FET characteristics. Finally, the ability to control the polarities of WSe_2 devices allows us to construct various functional logic gates, such as a complementary inverter, NAND, and NOR. This vdW contact strategy not only allows the device polarity to be tunable, but also provides a pathway for high-performance 2D electronic applications such as CMOS logic devices.

Method

Synthesis of Cl–$SnSe_2$. Cl-$SnSe_2$ ($SnSe_{1.96}Cl_{0.04}$) was synthesized via a solid-state reaction, following a procedure described elsewhere.[19] Briefly, this procedure was as follows: Stoichiometric amounts of Sn, Se, and anhydrous $SnCl_2$ powders were mixed: $(2 - x)Sn + xSnCl_2 + 2(2 - x)Se \rightarrow 2SnSe_{2-x}Cl_x$. The reaction was performed via a two-step process: the mixture was heated to 250 °C for 24 h, followed by annealing at 400 °C for 48 h. Finally, the sample was melted at 750 °C for 24 h, and then slowly cooled to 550 °C at a rate of 2 °C h^{-1} to grow single crystals.

Device fabrication. We first prepared a Ti (1 nm)/Au (10 nm) local bottom gate onto a Si/SiO_2 substrate as the back-gate electrode. Afterward, through the use of a polyvinyl alcohol film, h-BN (15–20 nm) and multilayer WSe_2 flakes (8–13 nm, unless otherwise stated) were transferred on top of the predeposited gate electrodes. The h-BN serves as a gate dielectric that greatly suppresses substrate-induced doping and preserves the intrinsic electronic properties of WSe_2.[2] Using a poly(dimethylsiloxane) (PDMS) stamp covered with a polycarbonate (PC) film,[38] we successively picked up Cl–$SnSe_2$ flakes from the substrate and place them onto WSe_2 at an elevated temperature of 170 °C. The PC film was removed using chloroform, followed by acetone and isopropyl alcohol. Finally, the top electrodes were defined using e-beam lithography followed by electron-beam metal deposition. For comparison, devices with evaporated metal contacts were fabricated on the same flake via the same procedure.

Characterization. XRD (D8 Advance, BRUKER) and Raman spectroscopy (LabRAM HR Evolution, Horiba Jovin-Yvon) with a laser excitation wavelength of 532 nm were used to characterize the crystallinities and qualities of WSe_2, MoS_2, and Cl–$SnSe_2$. Cross-sectional TEM images of the contact interfaces were obtained using an image aberration-corrected TEM

(HF-3300, Hitachi). XPS and UPS measurements were performed to estimate the band alignments of WSe_2 and Cl–$SnSe_2$ using VersaProbe with micro-focused and monochromatic Al Ka (1486.6 eV) and He I (21.22 eV) discharging excitation sources, respectively. All electrical measurements of the devices were conducted using a semiconductor parameter analyzer (4200-SCS, Keithley) in vacuum (~10^{-3} Torr) at 293–353 K.

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Author contributions

D.H. conceived the research. J.J. and H.S.R. designed experiments and fabricated the devices. K.L. synthesized and supplied Cl-$SnSe_2$ single crystal samples. J.A., T.W.K., S.H.S., S.P., T.T., and K.W. contributed in terms of the material/analysis tools used. J.J., H.S.R., and D.H. wrote the draft of the manuscript, and all authors contributed to the scientific interpretations as well as the editing of the manuscript.

Additional information

Supplementary information accompanies this paper at https://www.nature.com/natelectron/

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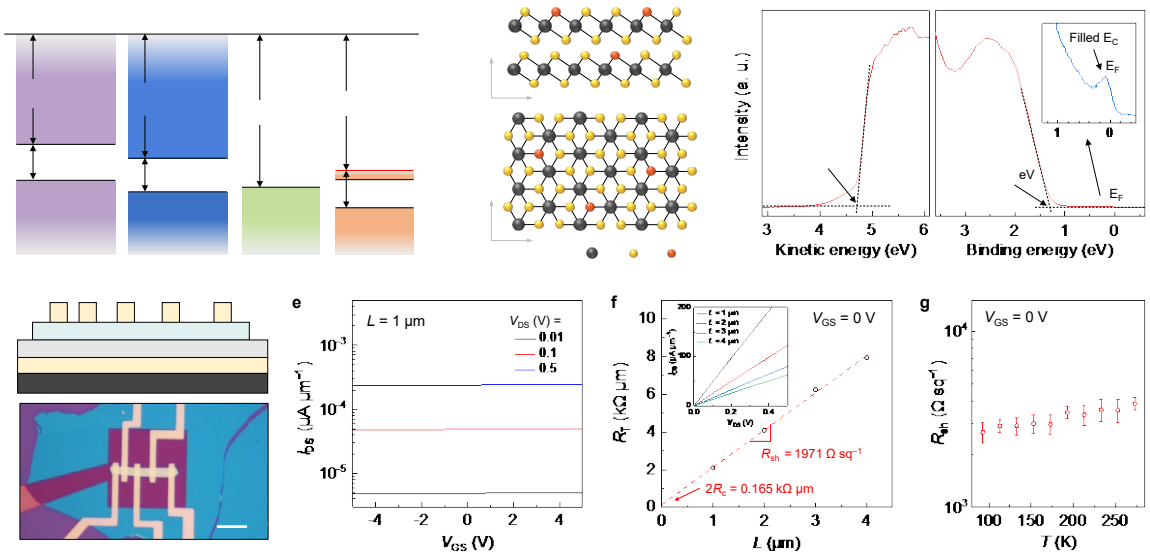

Figure 1| Electrical properties of chlorine-doped $SnSe_2$ (Cl–$SnSe_2$). a, Band alignments of multilayer WSe_2 and MoS_2 and metal contacts (i.e., Pd and Cl–$SnSe_2$). **b,** Crystal structure of Cl–$SnSe_2$. Cl–$SnSe_2$ exhibits degenerate n-type doping by chlorine substitution while retaining structural integrity of pristine $SnSe_2$. **c,** Secondary electron cutoff and valence band spectra of Cl–$SnSe_2$. The inset is a zoom of region near the Fermi level, confirming degenerate states. **d,** Schematic (upper) and optical image (lower) of ~13-nm-thick Cl-$SnSe_2$ TLM device. **e,** I_{DS}–V_{BG} transfer curves of a device with 1-μm channel length. **f,** Total resistance (R_T) versus L at V_{GS} = 0 V. Contact resistance (R_c) and sheet resistance (R_{sh}) are obtained from y-axis intercept and slope of linear fit, respectively. Inset: I_{DS}–V_{DS} curves for different channel lengths (L) at V_{GS} = 0 V. **g,** Extracted values of R_{sh} versus T, where the sheet resistance of Cl–$SnSe_2$ is on the order of 10^3 Ω sq^{-1}. Each error bar represents one standard deviation.

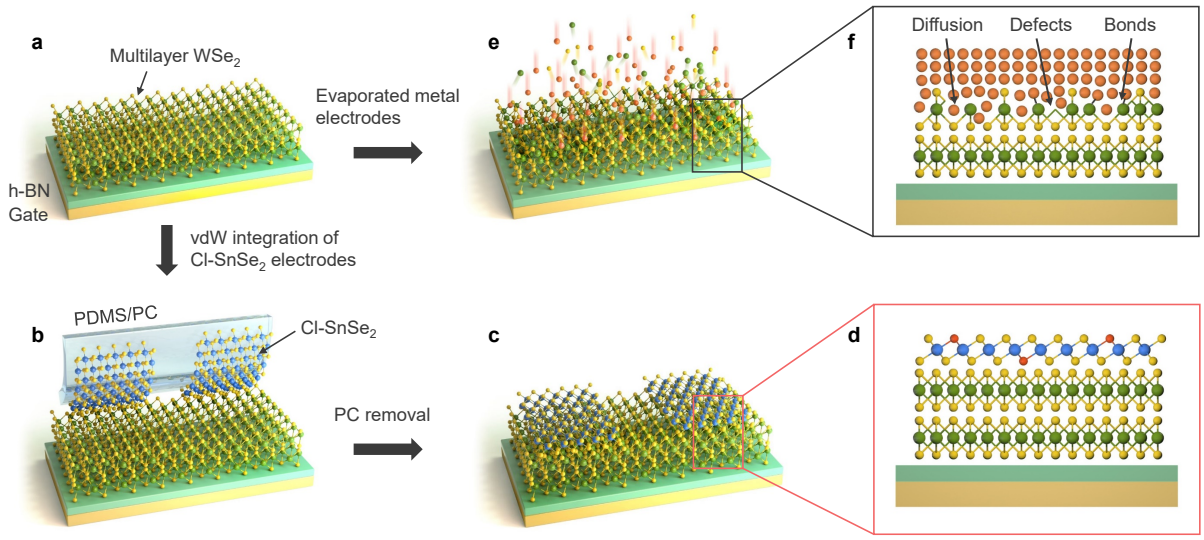

Figure 2| Schematic illustrations of device fabrication steps. a–c, Fabrication steps of vdW Cl–$SnSe_2$ contacts to WSe_2 transistor. Multilayer WSe_2 flake exfoliated on h-BN/Au substrate (**a**); alignment and transfer of Cl–$SnSe_2$ flakes (**b**); removal of PC and metallization (**c**). **d,** Cross-sectional schematic of Cl–$SnSe_2$ contact with WSe_2. **e,** Metal contacts fabricated on WSe_2 using direct metallization. **f,** Cross-sectional schematic of evaporated metal contact with WSe_2.

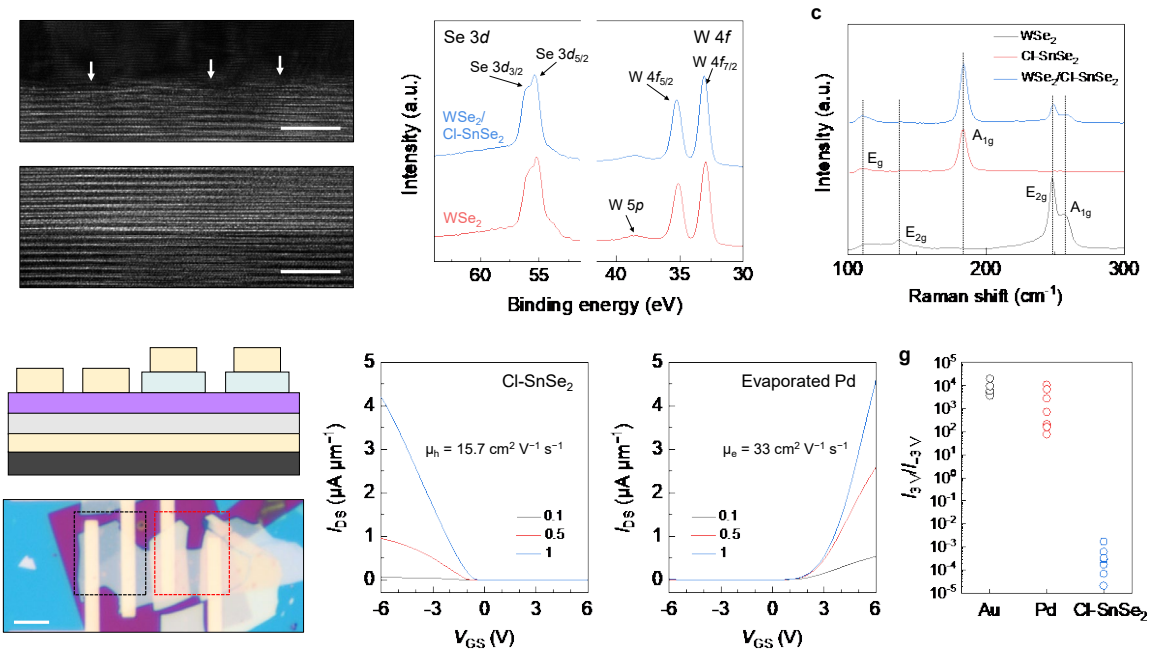

Figure 3| Cl–$SnSe_2$ contacts on multilayer WSe_2. a, Cross-sectional TEM images of contacts to WSe_2 with evaporated Pd (upper) and Cl–$SnSe_2$ (lower). **b,** XPS spectra of WSe_2/Cl–$SnSe_2$ interface showing pristine W and Se peaks. **c,** Raman spectra of WSe_2, Cl–$SnSe_2$, and WSe_2/Cl–$SnSe_2$. **d,** Schematic (upper) and optical image (lower) of a WSe_2 device contacted with both evaporated Pd and Cl–$SnSe_2$ electrodes. **e,f,** I_{DS}–V_{GS} transfer curves of WSe_2 transistors with Cl–$SnSe_2$ (**e**) and evaporated Pd contacts (**f**). **g,** Comparison of the current ratio between I_{3V} (I_{DS} at V_{GS} = 3 V) and I_{-3V} (I_{DS} at V_{GS} = −3 V) for different metal contacts (i.e., Cl–$SnSe_2$, Pd, and Au).

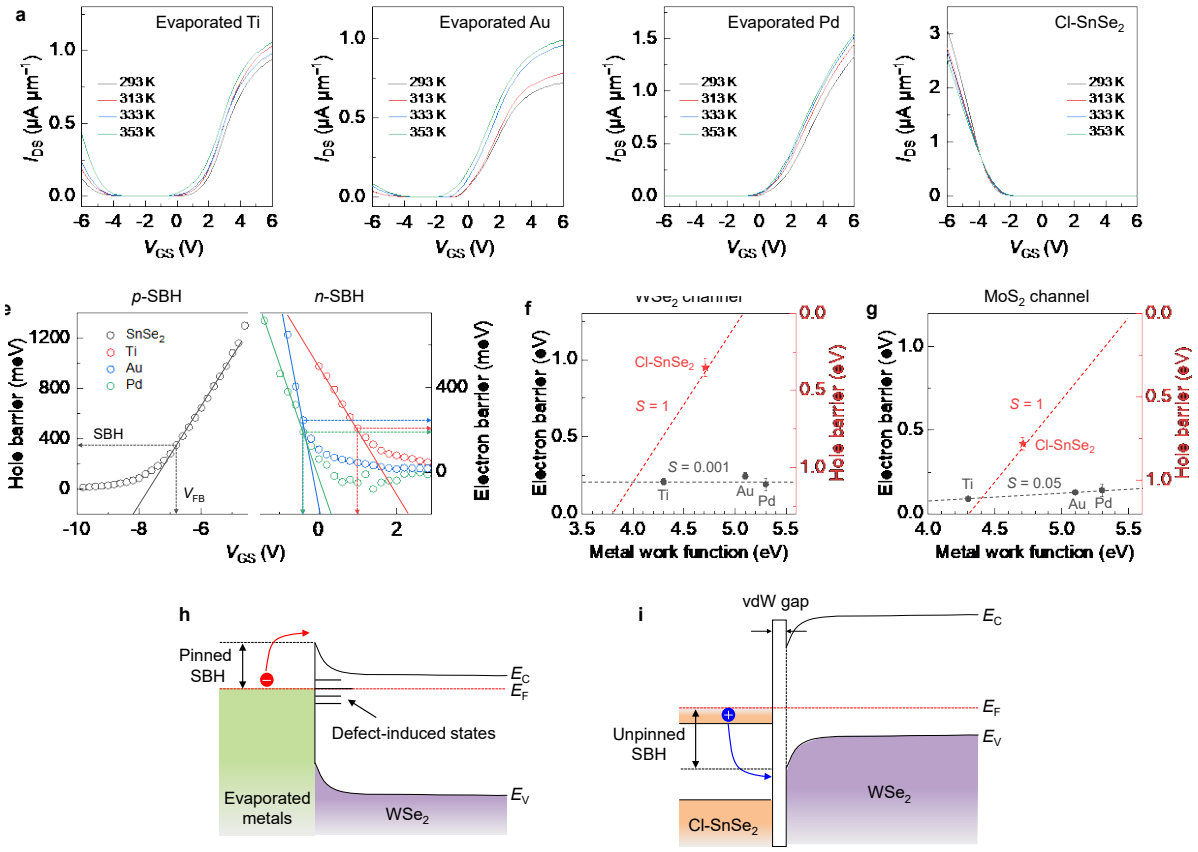

Figure 4| Transfer characteristics and Schottky barrier heights for Cl–$SnSe_2$ and evaporated metal contacts. a–d, Temperature-dependent I_{DS}–V_{GS} transfer curves of multilayer WSe_2 transistors with evaporated Ti (**a**), Au (**b**), Pd (**c**), and Cl–$SnSe_2$ contacts (**d**). **e,** Effective barrier height of each contact as a function of V_{GS}. Schottky barrier height is obtained at flat-band voltage condition (V_{GS} = V_{FB}), which corresponds to onset of deviation from linear behaviour. **f,g,** Estimated Schottky barrier heights for different metal contacts for WSe_2 (**f**) and MoS_2 transistors (**g**), each obtained from three tested devices. Red dashed line indicates ideal Schottky barrier height predicted by Schottky–Mott rule (S = 1). S values of the evaporated metal contacts are calculated from linear fitting, denoted by grey dashed line, of experimental data. **h,i,** Schematic band diagrams of multilayer WSe_2 for the evaporated metals (**h**) and Cl–$SnSe_2$ contact (**i**), respectively.

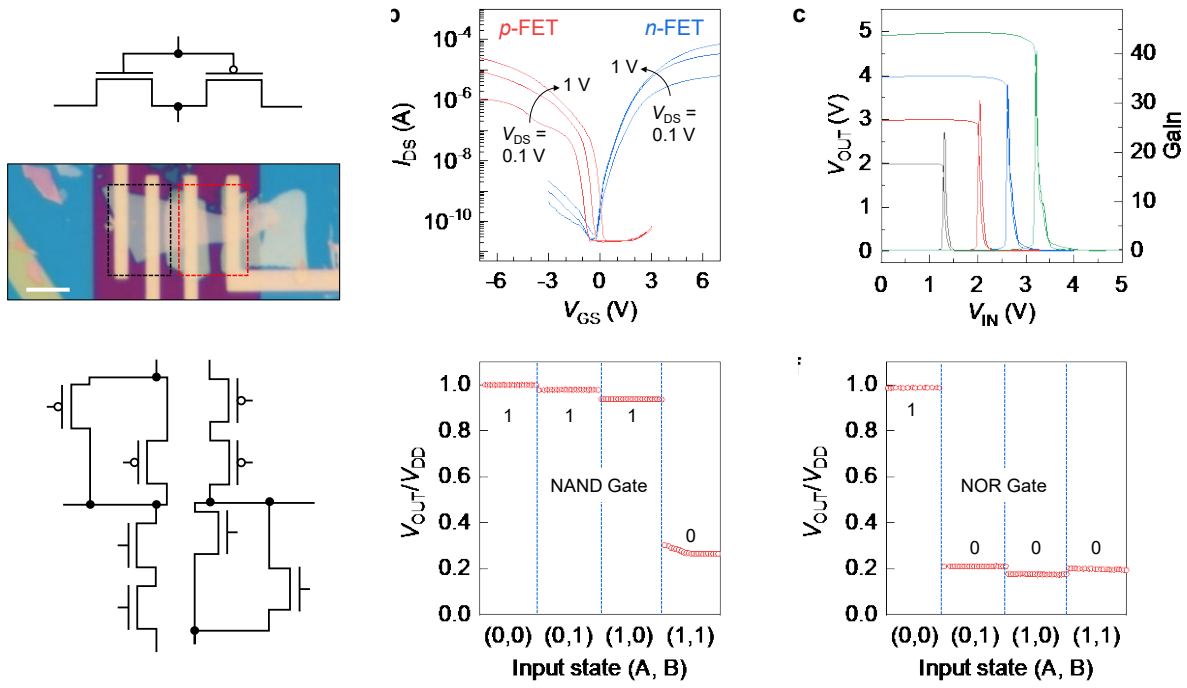

Figure 5| Logic gates based on WSe_2 transistors with different contact approaches. a, Circuit diagram (upper) and optical image (lower) of an inverter fabricated by connecting evaporated Pd-contacted FET (n-type) and Cl–$SnSe_2$-contacted FET (p-type) in series on a single flake. **b,** I_{DS}–V_{GS} transfer curves for evaporated Pd-contacted device (blue line) and Cl–$SnSe_2$-contacted device (red line). **c,** Output voltage (left axis) and voltage gain (right axis) of the logic inverter for a power supply of V_{DD} = 2, 3, 4, and 5 V. The voltage gain is defined as gain = dV_{OUT}/dV_{IN}. **d,** Circuit diagrams of NAND and NOR logic gates. **e,f,** Output voltages of the logic NAND (**e**) and NOR (**f**) gates at four input states ($V_{IN,A}$, $V_{IN,B}$), with a V_{DD} = 3 V. '0', low binary output state; '1', high binary output state. All electrical measurements were conducted at room temperature in vacuum, except **e** and **f**.

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